Contador 0-99

PROF ROBERTO FEDERICO MANDUJANO WILD

CONTADOR 0 A 99

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY CONT99 IS
        PORT(CLK, UD, RST: IN STD_LOGIC;
                ONE: OUT STD_LOGIC;
                CUENTAU,CUENTAD: OUT  STD_LOGIC_VECTOR (3 downto 0));
END ENTITY;

ARCHITECTURE ALGO OF CONT99 IS
        SIGNAL AUXU,AUXD: STD_LOGIC_VECTOR (3 downto 0);
        BEGIN
                PROCESS(CLK, RST,UD)
                BEGIN
                        IF (RST='0') THEN
                                AUXU<="0000";
                                AUXD<="0000";
                        ELSIF FALLING_EDGE (CLK) THEN
                                IF (UD='1') THEN
                                        IF AUXU="1001" THEN
                                        AUXU<= "0000";
                                                IF AUXD="1001" THEN
                                                AUXD<="0000";
                                                ELSE
                                                AUXD<=AUXD+'1';
                                                END IF;
                                        ELSE
                                        AUXU<=AUXU+'1';
                                        END IF;
                                ELSE
                                        IF AUXU="0000" THEN
                                        AUXU<="1001";
                                                IF AUXD="0000" THEN
                                                AUXD<="1001";
                                                ELSE
                                                AUXD<=AUXD-'1';
                                                END IF;
                                        ELSE
                                        AUXU<=AUXU-'1';
                                        END IF;
                                END IF;
                        END IF;
                END PROCESS;
        CUENTAU<= AUXU;
        CUENTAD<=AUXD;
        ONE<='1';
END ARCHITECTURE;
```

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DIVISOR DE FRECUENCIA

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY DIV_F IS
PORT(CLK: IN STD_LOGIC;
        FOUT,F1,F2: OUT STD_LOGIC);
END ENTITY;

ARCHITECTURE ALGO OF DIV_F IS
        SIGNAL AUX: INTEGER RANGE 0 TO 50000000;
        SIGNAL AUX2: STD_LOGIC;
BEGIN
        PROCESS(CLK)
        BEGIN

        IF RISING_EDGE(CLK) THEN
                IF AUX =50000000 THEN
                        AUX<=0;
                        AUX2<= NOT AUX2;
                ELSE
                        AUX<= AUX+1;
                END IF;
        END IF;
END PROCESS;

FOUT<=AUX2;
F1<='1';
F2<='1';
END ALGO;
```

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DISPLAY

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY DISPLAY IS
PORT(           BINARIO: IN  STD_LOGIC_VECTOR (3 downto 0);
                                DISPLAY: OUT STD_LOGIC_VECTOR (6 downto 0));
END ENTITY;

ARCHITECTURE ALGO OF DISPLAY IS
                SIGNAL AUX: STD_LOGIC_VECTOR (6 downto 0);
BEGIN
PROCESS (BINARIO)
BEGIN
                CASE BINARIO is
                when "0000" => AUX <=  "0000001"; --0
                when "0001" => AUX <=  "1001111"; --1
                when "0010" => AUX <=  "0010010"; --2
                when "0011" => AUX <=  "0000110"; --3
                when "0100" => AUX <=  "1001100"; --4
                when "0101" => AUX <=  "0100100"; --5
                when "0110" => AUX <=  "0100000"; --6
                when "0111" => AUX <=  "0001111"; --7
                when "1000" => AUX <=  "0000000"; --8
                when "1001" => AUX <=  "0001100"; --9
                when "1010" => AUX <=  "0000001"; --0
                when "1011" => AUX <=  "0000001"; --0
                when "1100" => AUX <=  "0000001"; --0
                when "1101" => AUX <=  "0000001"; --0
                when "1110" => AUX <=  "0000001"; --0
                when "1111" => AUX <=  "0000001"; --0
                END CASE;
END PROCESS;

                DISPLAY<=AUX;
END ALGO;
```

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MULTIPLEXOR

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY MUX IS
PORT(CLK: IN STD_LOGIC;
                UN, DEC: IN STD_LOGIC_VECTOR (6 downto 0);
                D1,D2: OUT STD_LOGIC;
                DIG: OUT STD_LOGIC_VECTOR (6 downto 0));
END ENTITY;

ARCHITECTURE ALGO OF MUX IS
                SIGNAL AUX2: STD_LOGIC;
BEGIN
                PROCESS(CLK)
                BEGIN
                IF RISING_EDGE(CLK) THEN
                                IF AUX2='1' THEN
                                                D1<='1';
                                                D2<='0';
                                                DIG<=UN;
                                                AUX2<=NOT AUX2;
                                ELSE
                                                D2<='1';
                                                D1<='0';
                                                DIG<=DEC;
                                                AUX2<=NOT AUX2;
                                END IF;
                END IF;
END PROCESS;

END ALGO;
```

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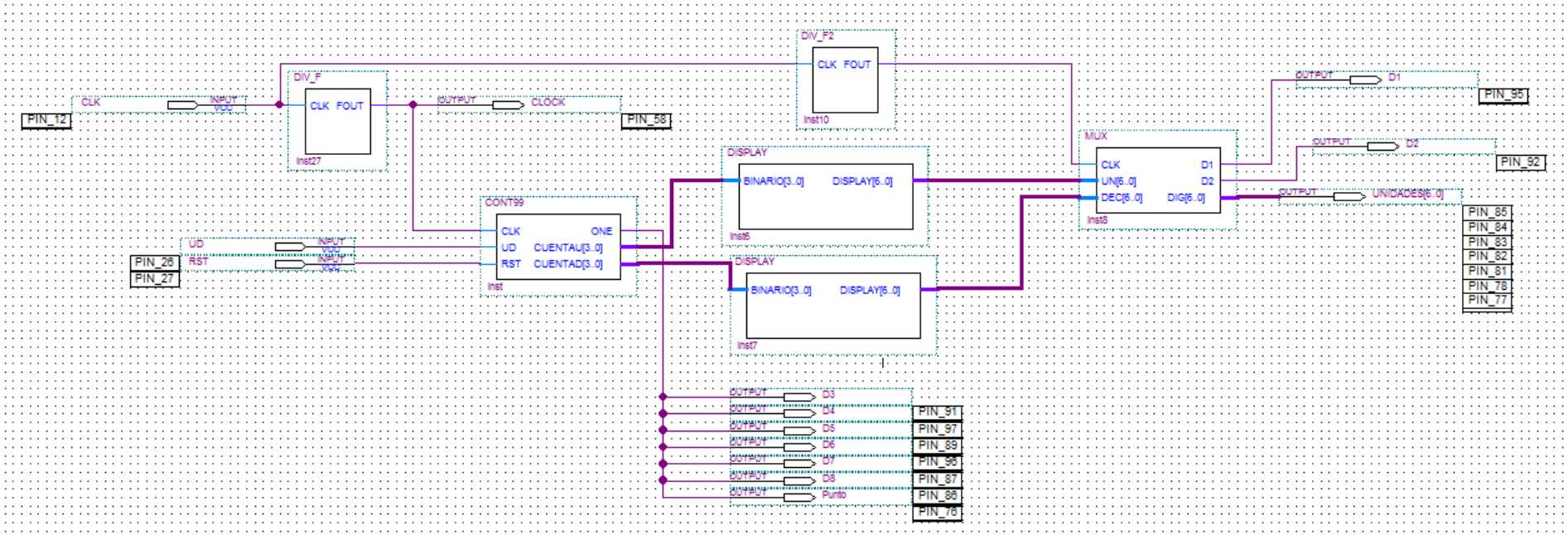
CLK
INPUT
PIN_12
DIV_F
CLK FOUT
Inst27
OUTPUT
CLOCK
PIN_58
DIV_F2
CLK FOUT
Inst10
UD
RST
INPUT
PIN_26
PIN_27
CONT99
CLK ONE
UD CUENTAU[3..0]
RST CUENTAD[3..0]
Inst
DISPLAY
BINARIO[3..0] DISPLAY[6..0]
Inst6
DISPLAY
BINARIO[3..0] DISPLAY[6..0]
Inst7
MUX
CLK D1
UN[6..0] D2
DEC[6..0] DIG[6..0]
Inst8
OUTPUT
D1
PIN_95
OUTPUT
D2
PIN_92
OUTPUT
UNIDADES[6..0]
PIN_85
PIN_84
PIN_83
PIN_82
PIN_81
PIN_78
PIN_77
OUTPUT
D3
D4
D5
D6
D7
D8
Punto
PIN_91
PIN_97
PIN_89
PIN_96
PIN_87
PIN_86
PIN_76