Ezz Addin Kukhun

Computer Engineer
Nablus, Palestine
059-983-6899 ezkukhun2000@gmail.com ezzaddinkukhun EzzAddinKukhun

Profile

Fresh graduate from Computer Engineering with a good background of Digital Circuits, either designing, or testing these circuits. Highly organized, self- motivated, passionate and interested in this field, wishful to join your company to share my skills.

Education

An-Najah National University, Nablus **Aug 2018 – June 2023**
Bachelors of Computer Engineering *GPA: **3.29/4***
Related Courses: Data Structures, OOP, Digital Design Circuits (I, II, III), Digital Design Circuits Lab (I, II), Microprocessors, Microcontrollers.

King Talal Secondary School, Nablus **Aug 2017 – June 2018**
High School Certificate - Scientific Stream ***93.6/100***

Skills

Personal Skills: Work under pressure, Teamwork, Taking responsibility, Quick learner, Self-Motivation, Time management and Problem Solver.
Languages: Arabic, English.
Programming Languages: Verilog, System Verilog, VHDL, C/C++, Java and Python.
Frameworks: UVM.

Experience

An-Najah Company For Consultancy and Technical Studies **Jun 2023 – Present**
Design Verification Internship *Nablus*

- Writing RTL designs for different circuits and communication protocols.
- Testing designs by simple testbench.
- Studying about System Verilog, and testing designs using programming features which they supplied in this language.
- Coverage designs while testing, and show the coverage report.
- Studying about scripting using Python, and how it can help us to write our designs, and then convert python files to Verilog or VHDL.
- We used EDAplayground for simulation, and coverage.
- We used the MobaXterm tool for simulation, coverage, show schematic diagram, and get netlist file.
- We started recently studying the UVM framework.

Projects

I^2C | **Aug 2023**

- **Languages**: Verilog, System Verilog.
- **Description**:The one of the communication protocols between multiple masters to multiple slaves, and this design represents just one master and one slave (memory), we test this design using System verilog features, and we simulated it on MobaXterm tool, we got the coverage report ,schematic diagram, and netlist file.

SPI | **Jul 2023**

- **Languages**: Verilog, System Verilog.
- **Description**:The one of the communication protocols between one master to multiple slaves, and this design represents the master and one slave (memory), we simulated this design and tested it using EDAPlayground.

UART | **Jul 2023**

- **Languages**: Verilog.
- **Description**:The one of the communication protocols between transmitter and receiver, we wrote the RTL design for transmitter, reciever and clock generator. And we test the design using simple testbench.

FIFO Memory | **Jun 2023**

- **Languages**: Verilog.
- **Description**:The one of the communication protocols between transmitter and receiver, we wrote the RTL design for transmitter, reciever and clock generator. And we test the design using simple testbench.

CRC | **Jan 2021**

- **Languages**: Verilog.
- **Description**: This design represents CRC mechanism to insure the data integrity.