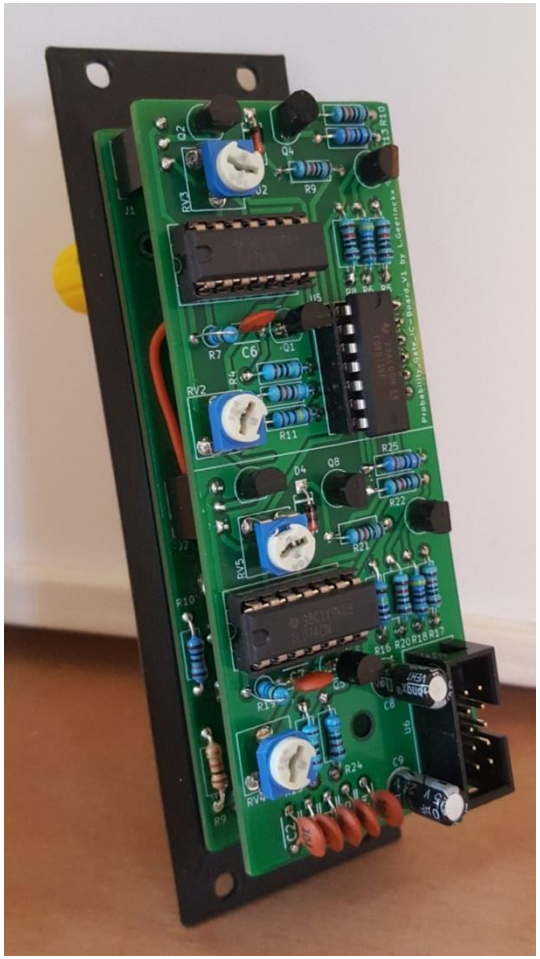
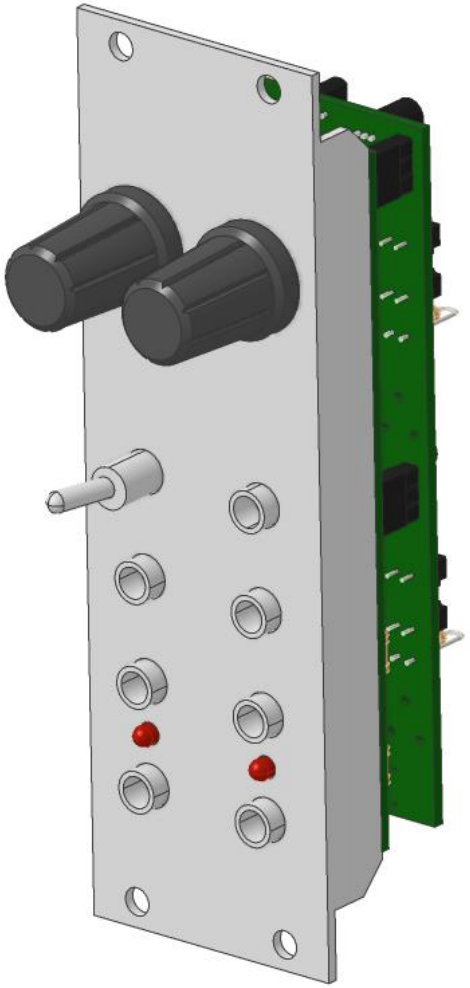
Dual Probability Gate By Luther; Manual v2.2

Please note that the current version of the pcb has few early errors in the design. Future versions will be improved. This document also covers how to fix them.





Content

- Page 3 — BOM
- Page 5 — Feature overview
- Page 6 - 8 — How it works
- Page 9 — A tip before you start building
- Page 10 – 14 — Errorzzzz
- Page 15 – 17 — Calibration
- Page 18 — Tips & Trouble shooting

See also: https://github.com/PierreIsCoding/sdiy/tree/main/Probability_Gate

Dual Probability Gate; BOM

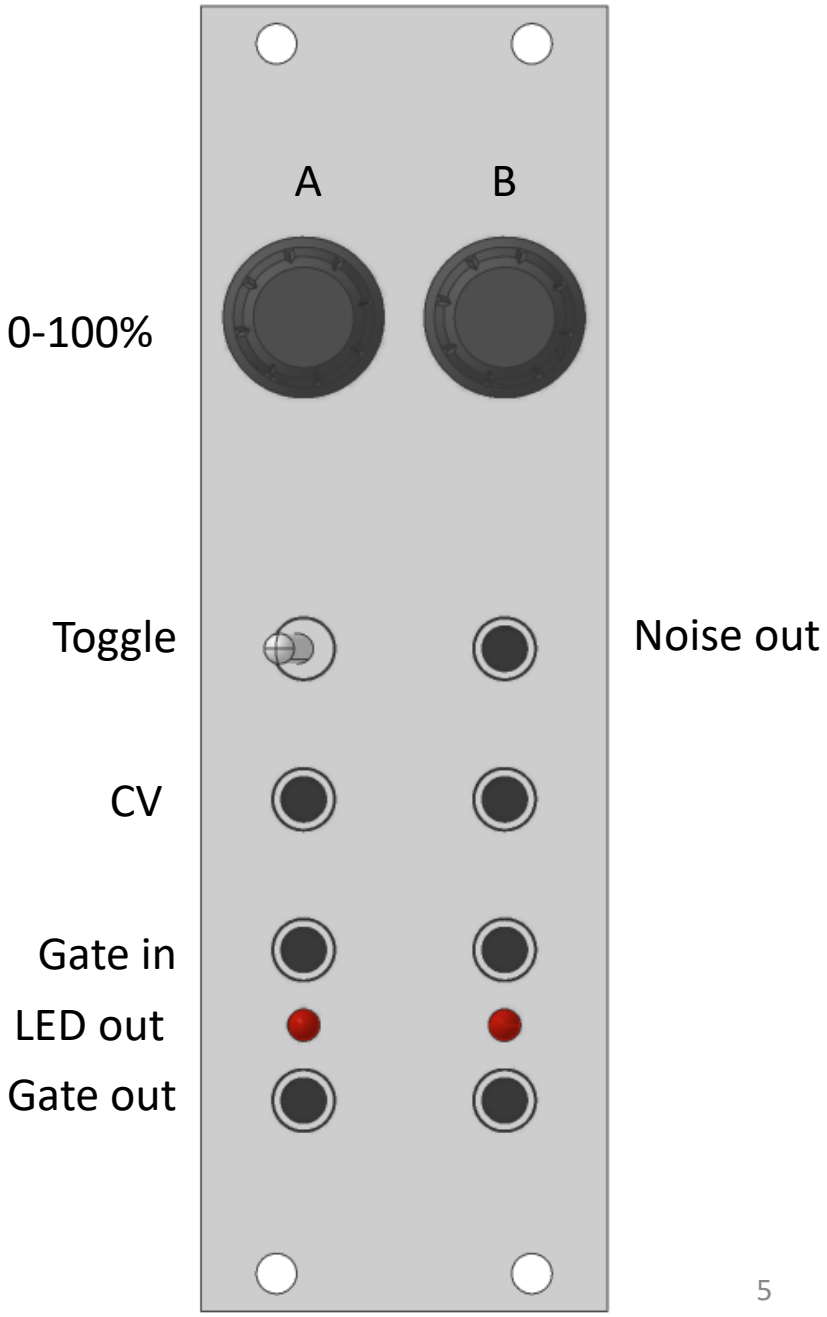
Reference	BOARD	Quantity	Value	Description	Footprint
C6 C7	IC	2	0.01uF	Ceramic Capacitor	SamacSys_Parts:K104K15X7RF53H5
RV1 RV2	IO	2	100K	Potentiometer	SamacSys_Parts:RD901F4015R1B100K00DL1
R13 R25	IC	2	100K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R5 R10	IO	2	100K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
RV2 RV3 RV4 RV5	IC	4	100K	Trimpot	LP_Footprint_Library:Tayda_Trimpot_6mm
C1 C2 C3 C4 C5	IC	5	100nF	Ceramic Capacitor	SamacSys_Parts:K104K15X7RF53H5
R5 R8 R17 R20	IC	4	10K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R9 R10 R21 R22	IC	4	10k	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R3 R8	IO	2	10K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
See manual	IC	2	10nF	Ceramic Capacitor	See manual
C8 C9	IC	2	10uF	Electrolyth Capacitor	Capacitor_THT:CP_Radial_D5.0mm_P2.00mm
R4 R9 R11	IO	3	1K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R4 R11 R16 R23	IC	4	1M	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R7 R19	IC	2	1M	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P2.54mm_Vertical
D2 D4	IC	2	1n4148	Diode	Diode_THT:D_A-405_P7.62mm_Horizontal
D2 D4	IO	2	1N4148	Diode	Diode_THT:D_A-405_P7.62mm_Horizontal
Q4 Q2 Q3 Q8 Q6 Q7	IC	6	2N3904	Transistor	Package_TO_SOT_THT:TO-92_Inline
Q1 Q5	IC	2	2N3904_C	Transistor	Package_TO_SOT_THT:TO-92_Inline
R6 R18	IC	2	4K7	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R12 R24	IC	2	68K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
R1 R2 R6 R7	IO	4	68K	Resistor	Resistor_THT:R_Axial_DIN0207_L6.3mm_D2.5mm_P10.16mm_Horizontal
U5	IO	1	CD4013	IC	Package_DIP:DIP-14_W7.62mm_Socket
J1 J2	IC	2	Conn_01x03	Pin Header	Connector_PinHeader_2.54mm:PinHeader_1x03_P2.54mm_Vertical
J1 J2	IO	2	Conn_01x03	Pin Socket	Connector_PinSocket_2.54mm:PinSocket_1x03_P2.54mm_Vertical
J3	IC	1	Conn_01x06	Pin Header	Connector_PinHeader_2.54mm:PinHeader_1x06_P2.54mm_Vertical
J3	IO	1	Conn_01x06	Pin Socket	Connector_PinSocket_2.54mm:PinSocket_1x06_P2.54mm_Vertical
U1	IO	1	CV_IN_A	Mono Jack	LP_Footprint_Library:Jack_3.5mm
U2	IO	1	CV_IN_B	Mono Jack	LP_Footprint_Library:Jack_3.5mm
U3	IO	1	GATE_IN_A	Mono Jack	LP_Footprint_Library:Jack_3.5mm
U5	IO	1	GATE_IN_B	Mono Jack	LP_Footprint_Library:Jack_3.5mm
U4	IO	1	GATE_OUT_A	Mono Jack	LP_Footprint_Library:Jack_3.5mm
U6	IO	1	GATE_OUT_B	Mono Jack	LP_Footprint_Library:Jack_3.5mm
U6	IC	1	IDC_10	IDC header pins	Connector_IDC:IDC-Header_2x05_P2.54mm_Vertical
D1 D3	IO	2	LED	Red LED	LED_THT:LED_D3.0mm
U7	IO	1	NOISE_OUT	Mono Jack	LP_Footprint_Library:Jack_3.5mm
SW1	IO	1	SW_SPDT	Mono Jack	LP_Footprint_Library:Simple_SPST_Switch
U2 U7	IC	2	TL074	IC	Package_DIP:DIP-14_W7.62mm_Socket
	both	1		PCB standoff	Optional between both PCB's. Length = 10mm, Screwsize =3mm

Dual Probability Gate; BOM - Notes

- Some builders noticed that it is required to change the 10K of R10 and R22 (10K) to 47K / 100K.
- See for IBOM https://github.com/PierreIsCoding/sdiy/tree/main/Probability_Gate
- The IBOM doesn't include some afterthought components. Please check this doc as well.
- I named Q1 and Q5 2n3904C. They are just 2N3904's but be sure they are cheap noise ones for creating white noise. See also page 9.

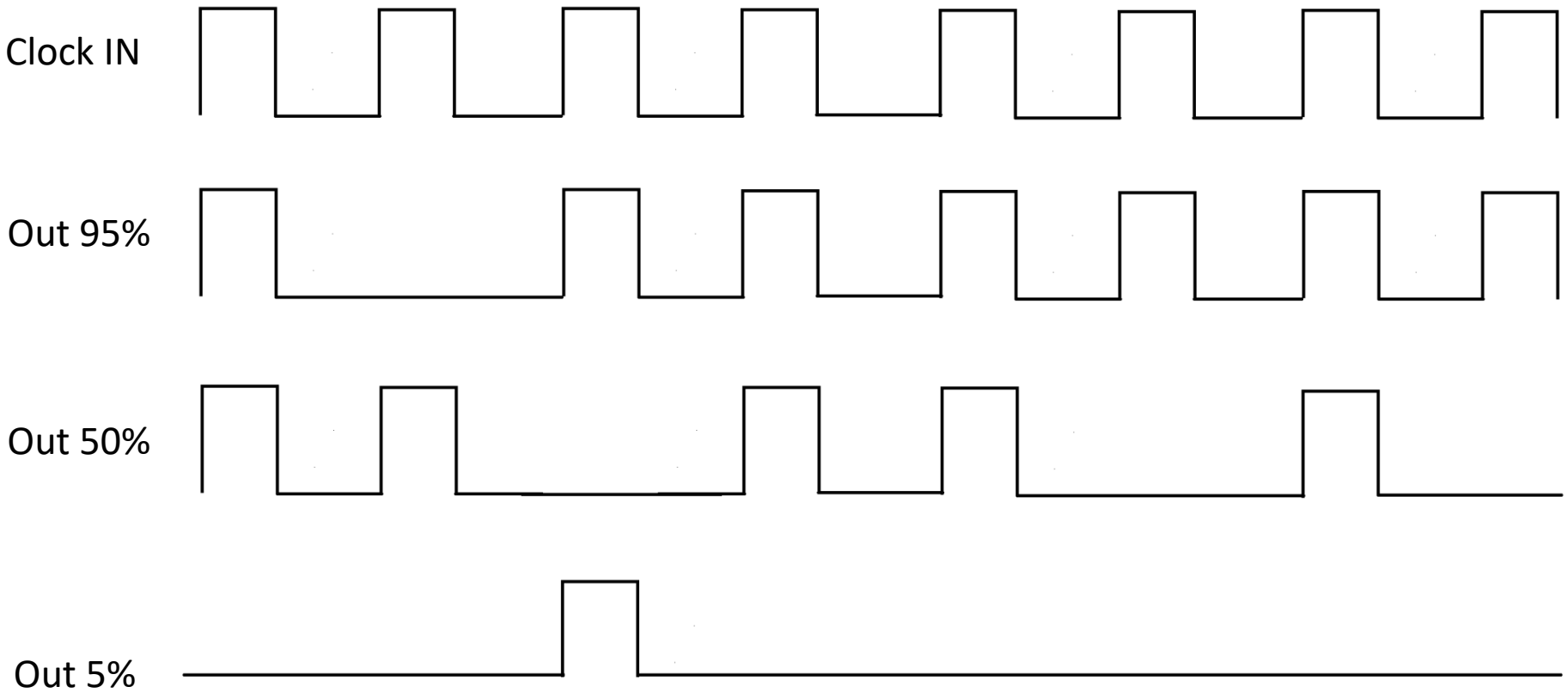
Features

- Adjust the probability of a gate signal begin “copied” to the gate output between 0-100%.
- Change the probability with a potentiometer or with a (bipolar) CV
- A noise output.
- Each channel has its own noise source. The toggle switch lets you decide which noise source is selected for the noise out and the second channel. When both channels have the same noise source random but semi synchronized events happen between the two channels.
- Left position toggle switch
  - Noise out = A
  - Noise source B = A
- Right position toggle switch
  - Noise out = B
  - Noise source B = B
- Furthermore you can also use this module as a cv controllable bit-crusher

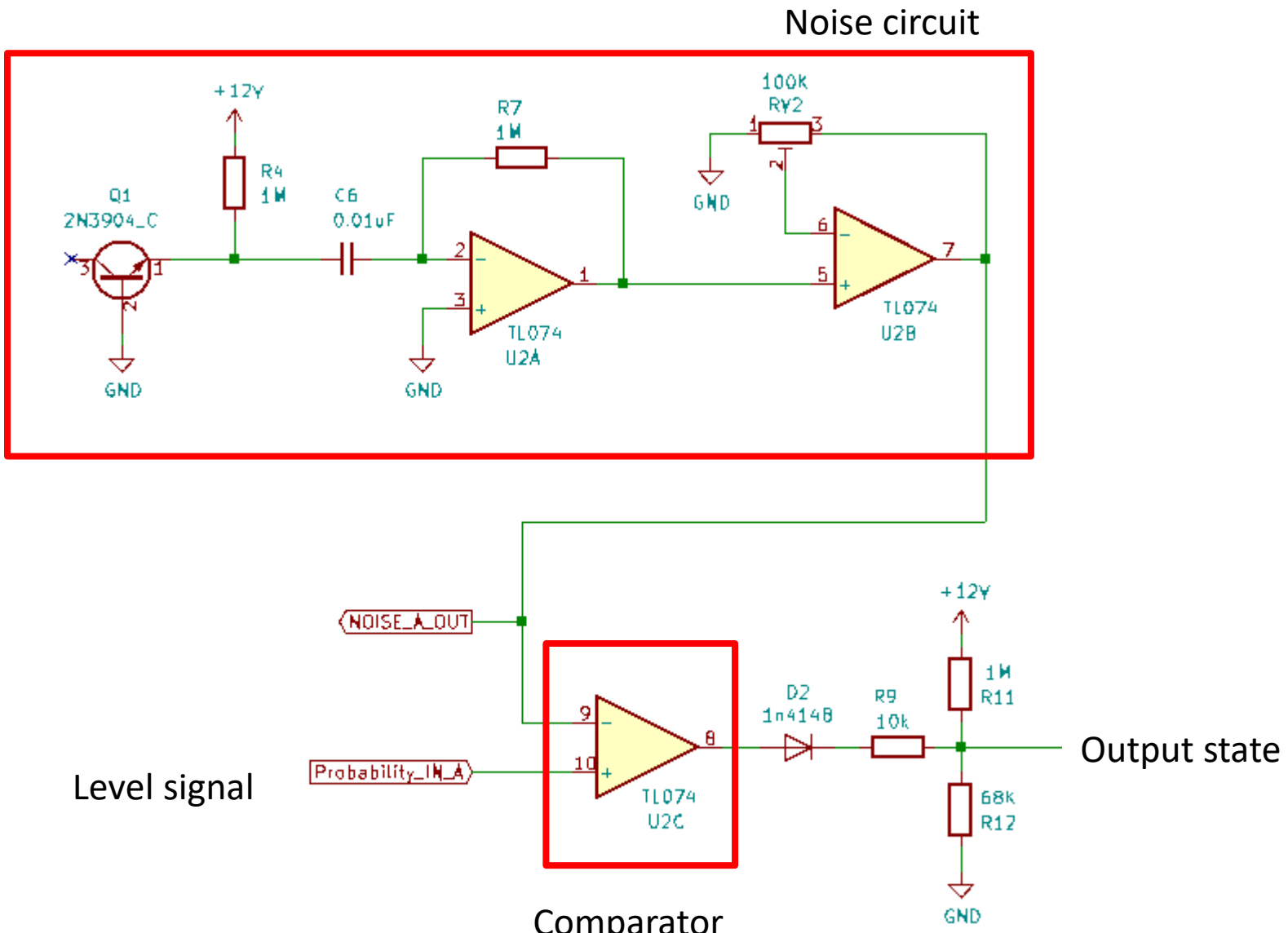


How it works

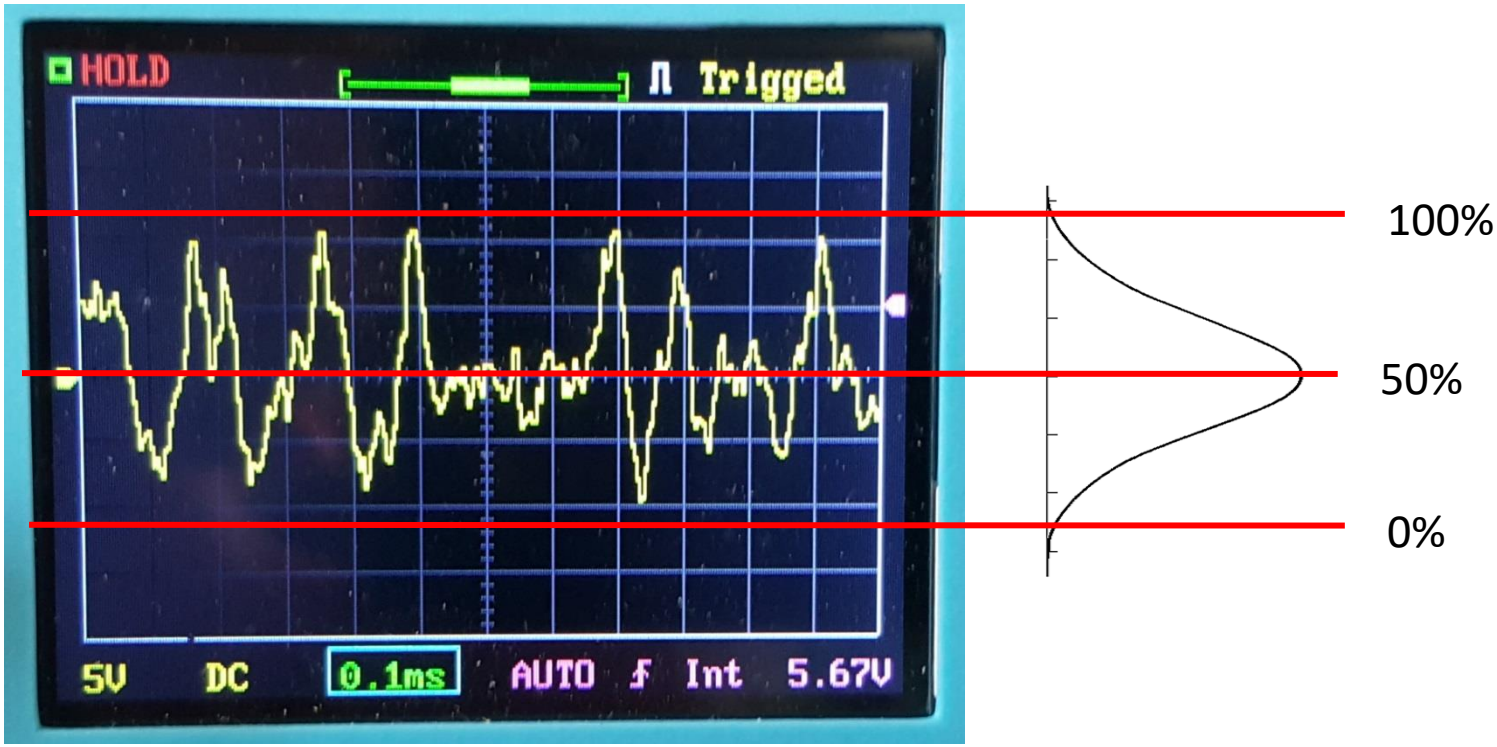
Example of clock outputs depending on “Clock IN” and “Probability”



How it works


Noise circuit
+12V
R4
1M
Q1
2N3904_C
C6
0.01uF
R7
1M
100k
RV2
GND
GND
GND
TL074
U2A
TL074
U2B
NOISE_A_OUT
Probability_IN_A
TL074
U2C
D2
1n4148
R9
10k
+12V
1M
R11
68k
R12
GND
Level signal
Output state
Comparator

How it works



See also page before. A noise signal is compared with a level signal (given by the potentiometer or CV input). Only when that level signal (see red lines) is above that noise signal we get a high output from the comparator and thus the input gate will be perpetuated to the output gate.

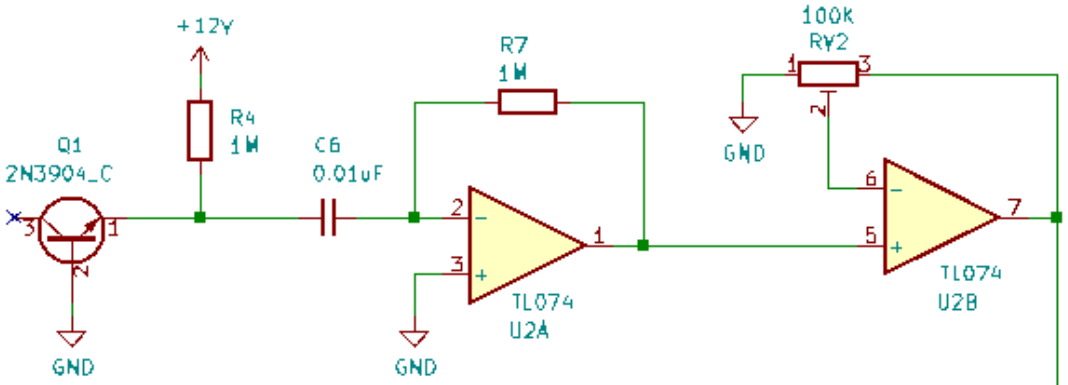
White noise is distributed in such a way that higher and lower voltage spikes are a less likely to happen than centric voltages. By this we get a probability distribution with a bell like shape centered around 0 Volts. The surface area above the 0V will be on average the same as below 0V. Therefore 0V will give us a 50% chance. By changing the potentiometer you basically adjust the chance of the noise signal being higher or lower than the level signal.

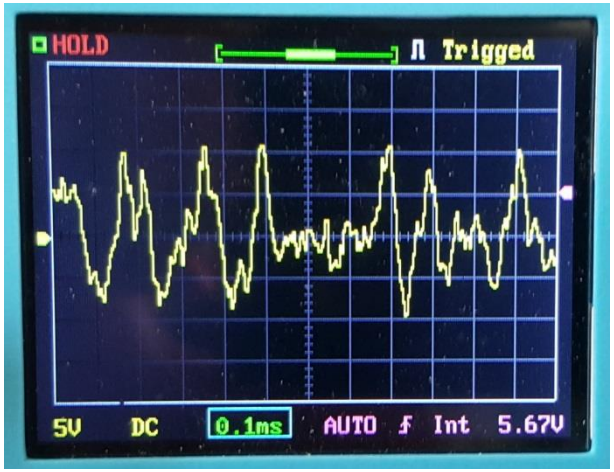
The rest of the module saves this ever fluctuating given state with the next clock pulse. Here a rising edge of a clock input saves/ latches this state in the flipflop. See it as a binary sample and hold. A falling edge of the clock pulse resets that flipflop and thus your gate is copied or not ;)

A tip before you start building

As explained in previous section the module works with a white noise. The white noise is generated by reverse-biasing transistors Q1 for side A and Q5 for side B.

However and unfortunately this effect depends on how those transistors were created. Not all 2N3904's are the same. So before you solder Q1 and Q5 you might want to breadboard the noise part of the circuit and test your 2N3904's from different suppliers and batches. The oscilloscope should display a random signal dancing around 0 Volts.



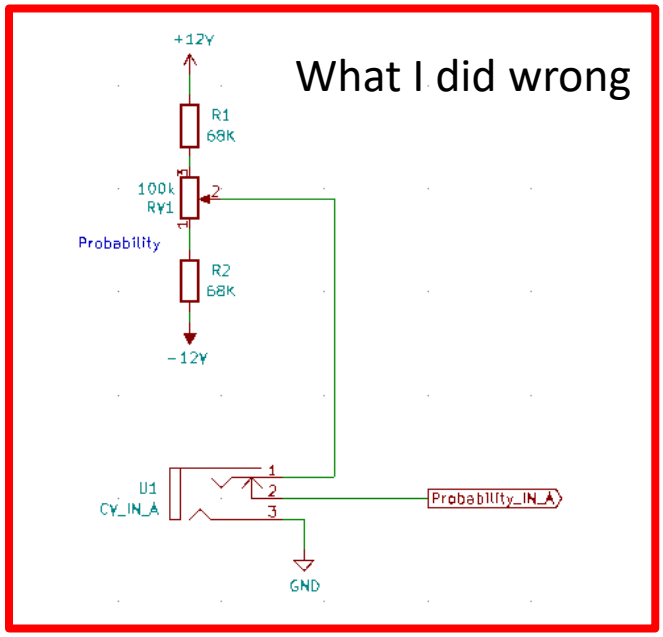


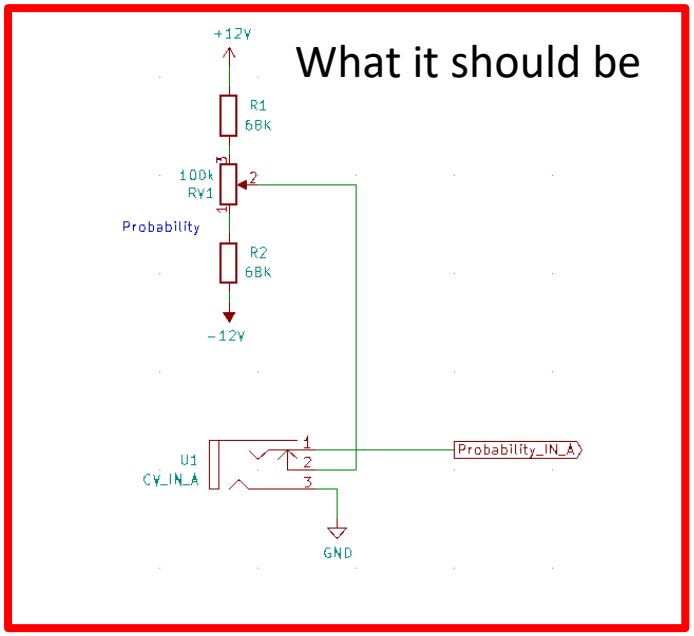
ERRORzzz

Unfortunately I did a few errors with this prototype for the pcb design. I also got a new issue I didn't saw during prototype phase, but you can fix those one too. I hope you can easily fix all of these issues with this guide.

I prepared the bug fixes somewhat on the pcb itself, but please check afterwards for unwanted connections.

ERRORzzz @ IO-BOARD

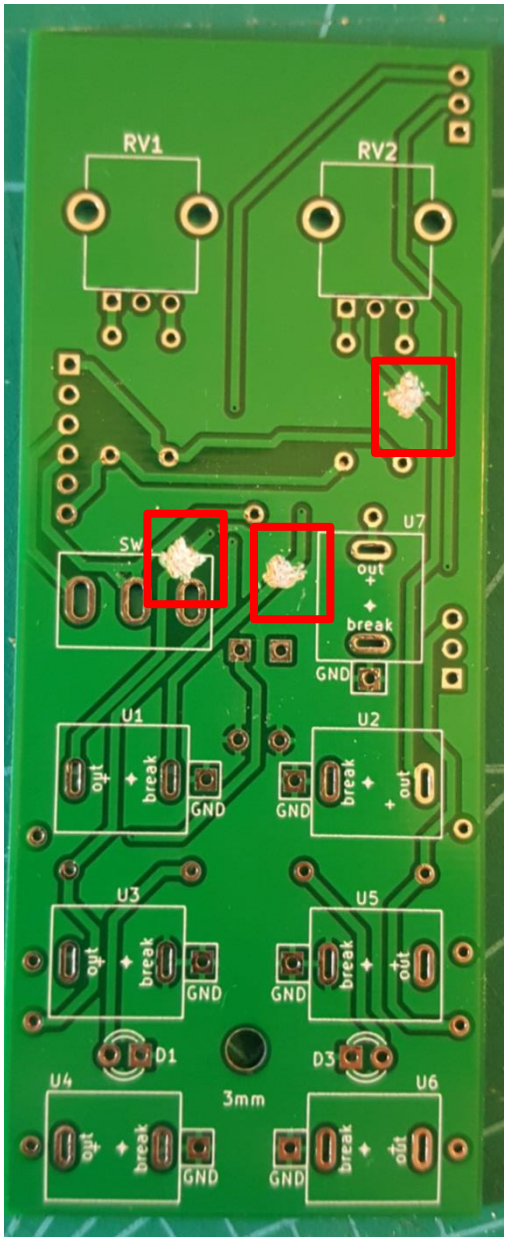


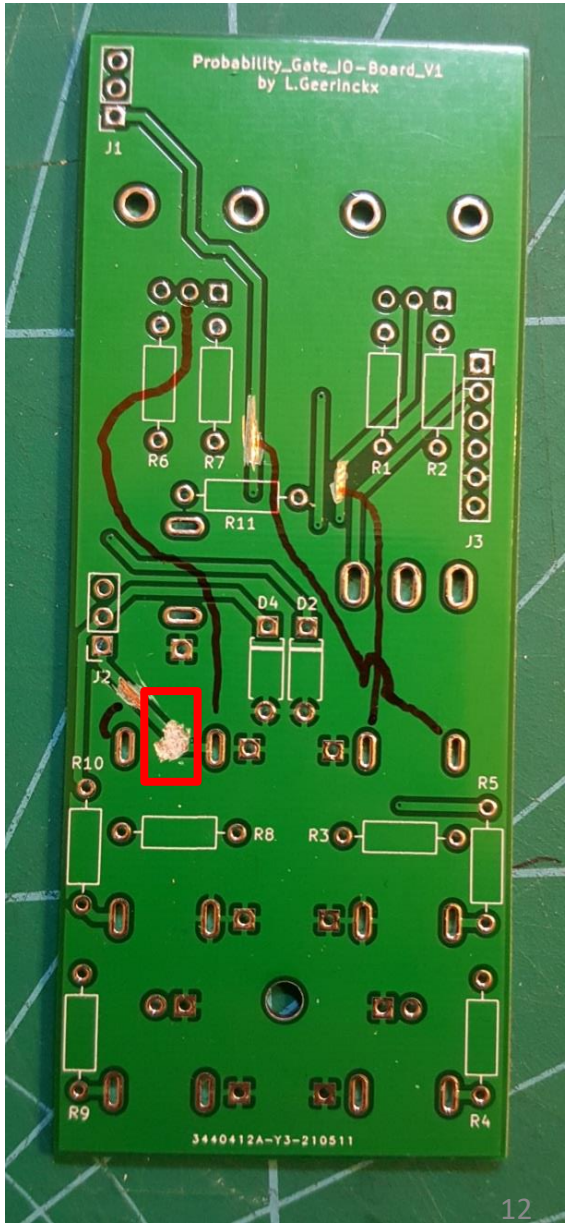


…for both channels … :((

ERRORzzz @ IO-BOARD

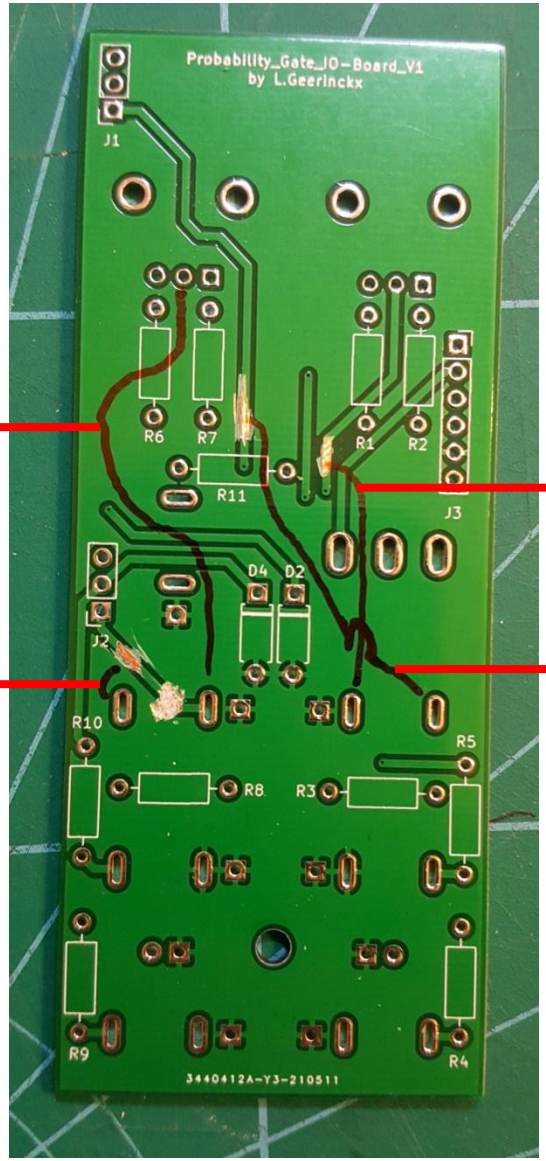
Please check if these connections are properly disconnected





ERRORzzz @ IO-BOARD

Example result

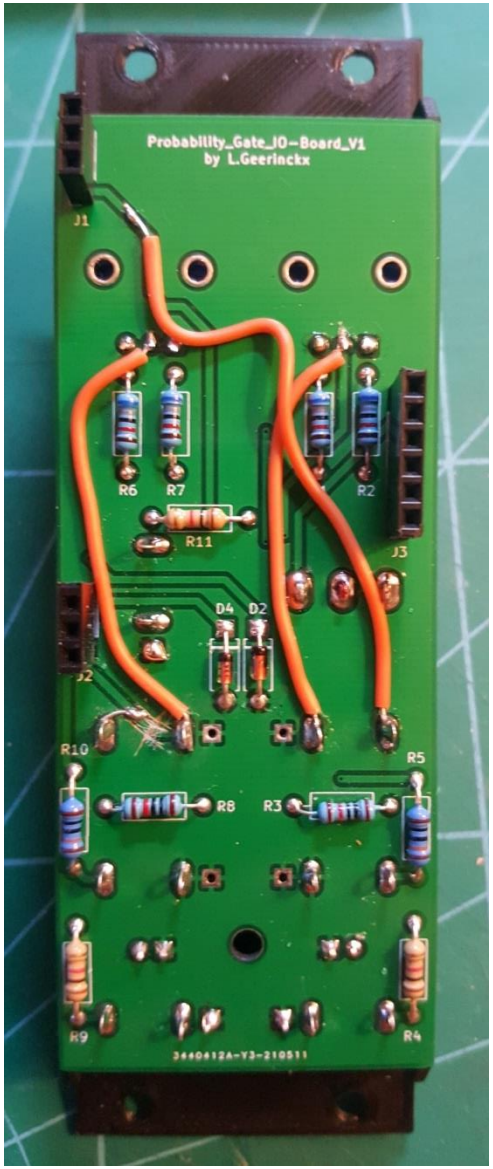


Make connection

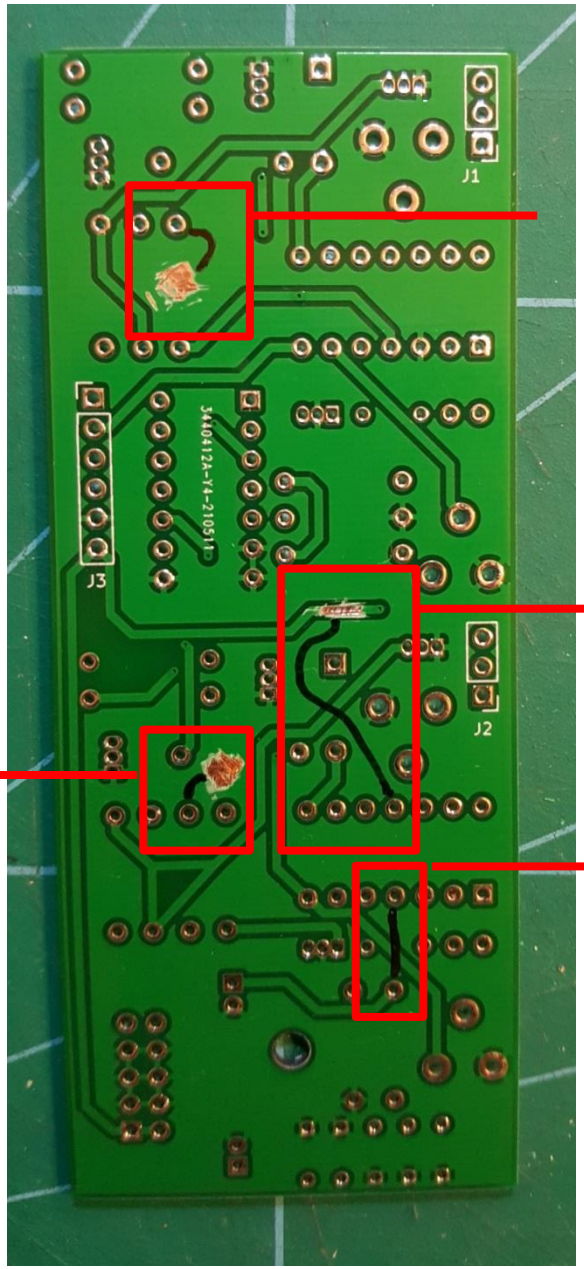
Make connection

Make connection

Make connection



ERRORzzz @ IC-BOARD



Add a ceramic 10nF capacitor between ground and R8. It improves the trigger input.

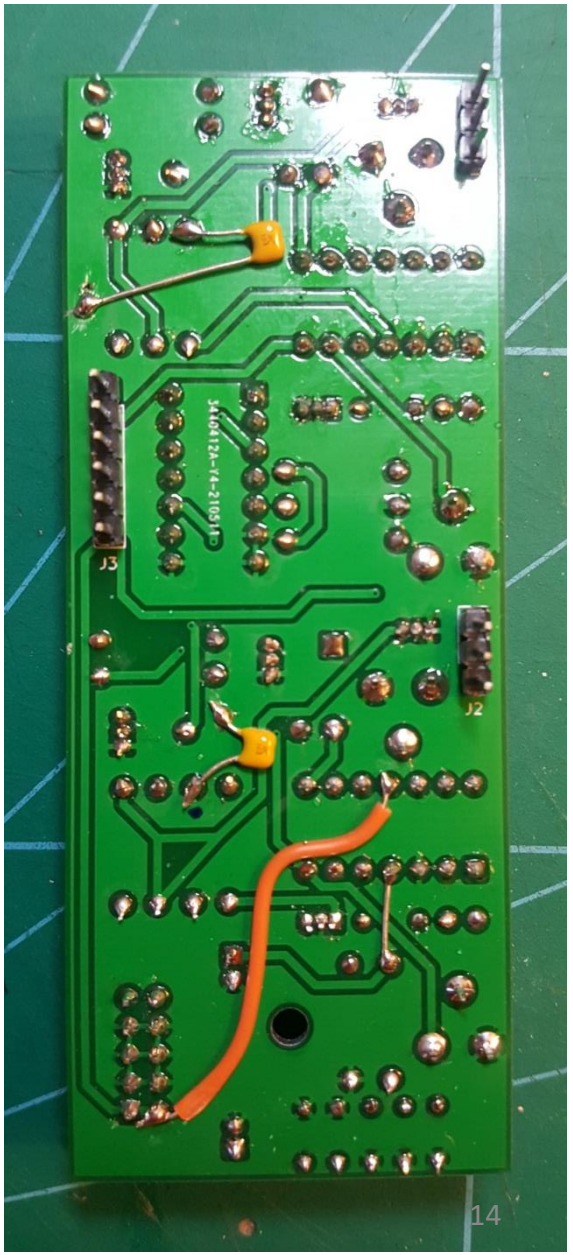
Make connection. Gives U7 -12V

Add a ceramic 10nF capacitor between ground and R20. It improves the trigger input.

Make connection.

Gives U7 +12V

Example result



Calibrating the noise

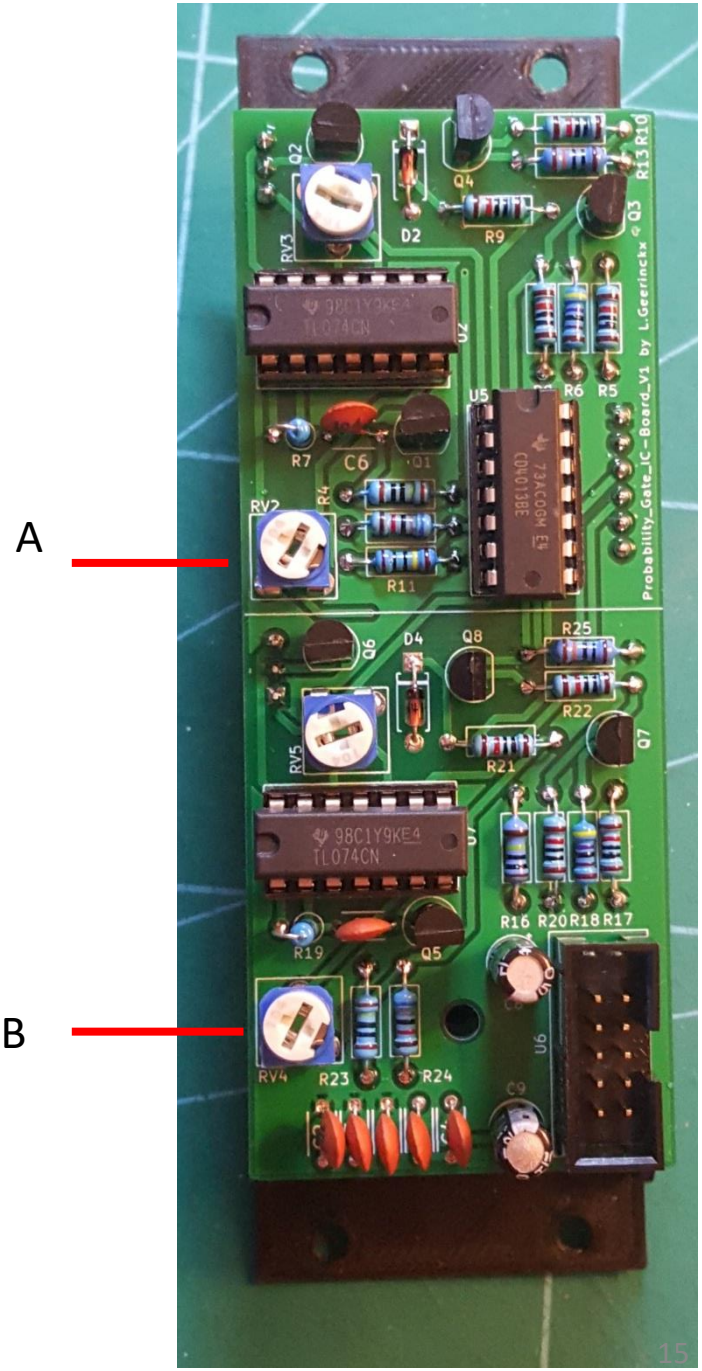
- First. If possible use an oscilloscope and notice that the noise signals will be dancing around 0 Volts.
- The potentiometers will deliver a voltage level between -5V and +5V (approximately). You need to calibrate the gain of the two noise sources so they match this range.

Calibration technique 1:

- Set the toggle switch to the left.
- Connect the noise out to an oscilloscope. Adjust A until the noise lives between -5V and +5V.
- Set the toggle switch to the right.
- Idem. for B.

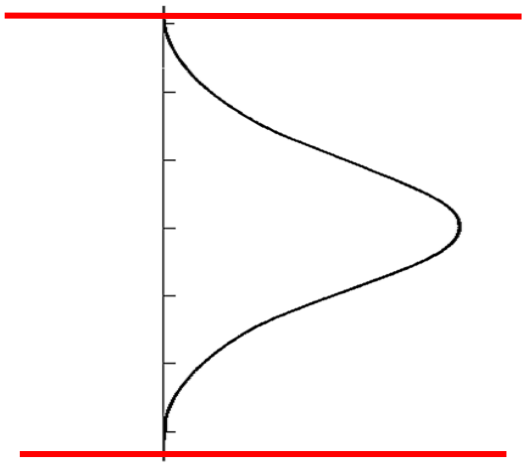
Calibration technique 2:

- Connect the gate-in for A to a fast clock pulse.
- Turn the potentiometer for A to the left
- Adjust until you have no or almost no blinking led for A.
- Idem for B.

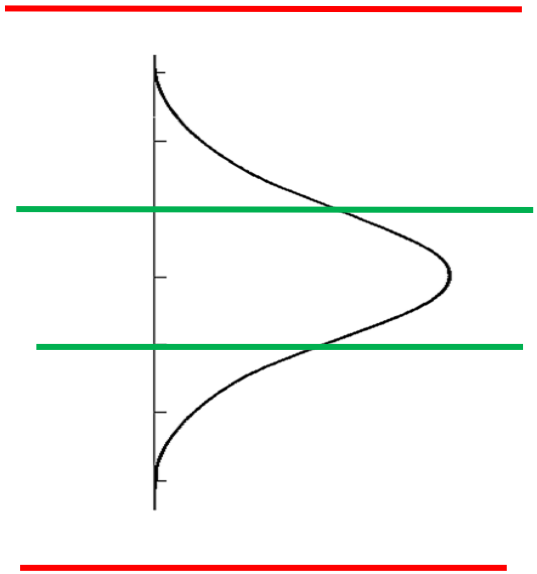


Calibrating the noise

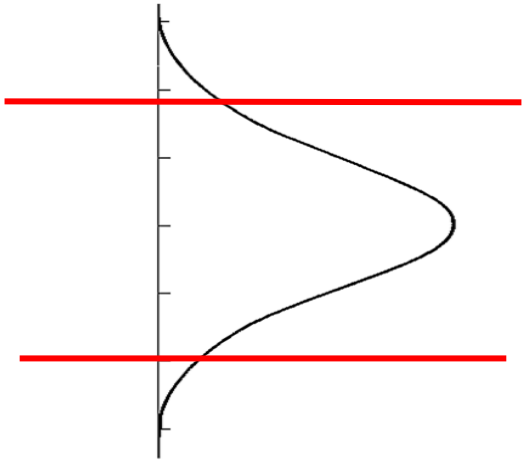
Exact



Undershoot



Overshoot



When you calibrate the noise-gain you can decide how close the most left and most right position of the potentiometer is to the edges of the noise source. You have three options:

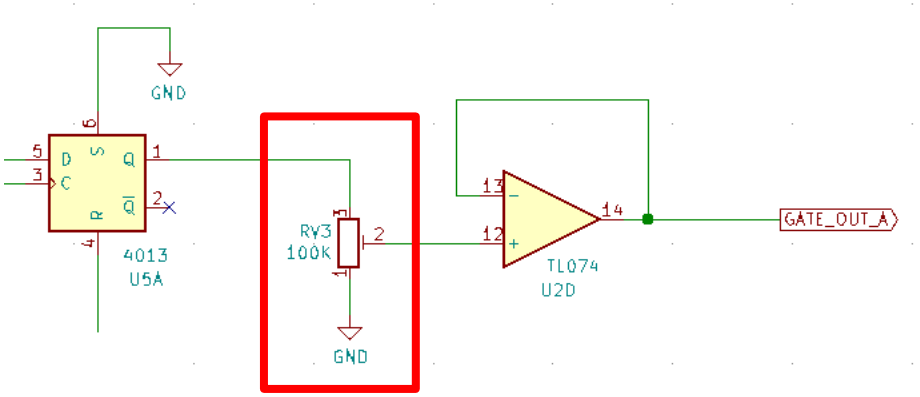
- Exact. This means that when you turn the knob to 0% you will have no triggers, but if you move it just a so slightly triggers will emerge. However the first problem is that your noise source is probably not completely symmetric thus either 0% or 100% will not be perfect. The second issue is that since the probability is really low at the edges you have to wait to see if it is truly 0% or 100%. Maybe after a while longer while you will see a trigger anyways even though you thought it was set at 0%. (a faster input clock helps).
- Undershoot. To make it easier you can undershoot it. Now you will get a true 0% and a true 100% for sure, but with this the probability between 0-34% and 68-100% is a way bigger area than 34% and 68%. Or in other words to change the probability between 0% and 34% you turn the potentiometer a lot, but between 34% and 68% you turn the potentiometer just a little but, so you have basically less control over that area.
- Overshoot. You gain more control over the probabilities around 50% but you will not have a true 0% and a true 100%.

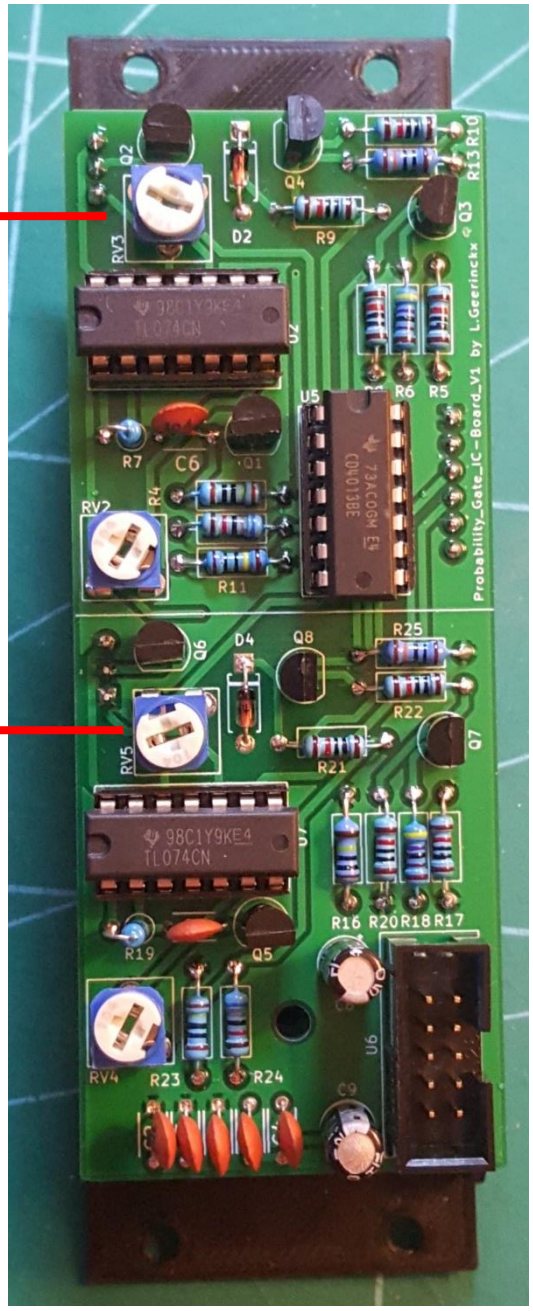
Calibrating the output

I could not really decide what the voltage of the output trigger / gate should be. (What do you think?) So I just used the most easy trick from the book: a voltage divider with a trimpot.

These trimpots lets you set the output voltage of each channel between 12V and 0V.

Normally I would set those between 5 a 10 Volts.





Tips & Troubleshooting

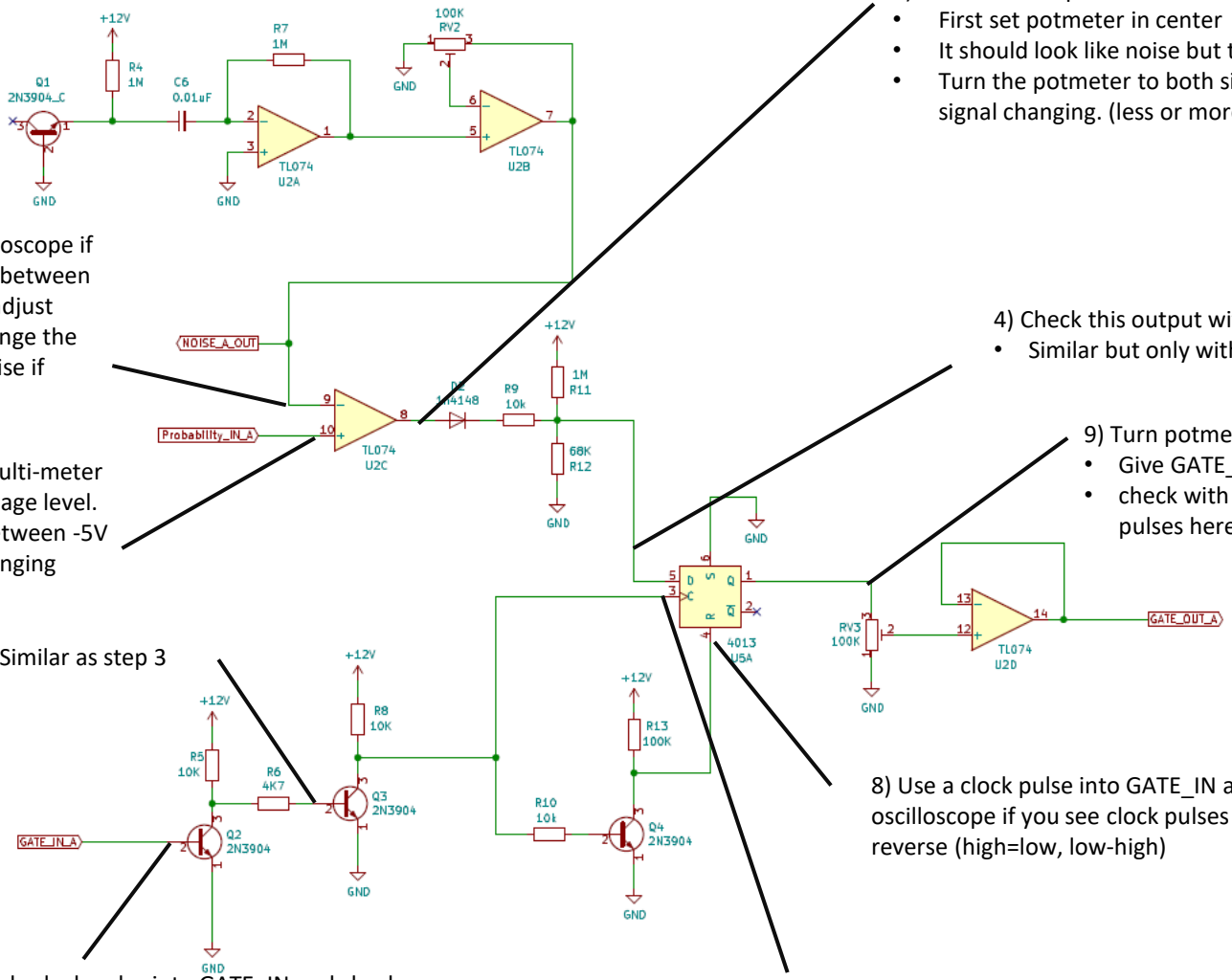
Tips

- Use a spacer between the two boards. See the 3mm mounting holes. This makes the board less fragile, especially when mounting / removing the power connector.

Troubleshooting

- The footprints of the transistors are a bit tight. Check if those pins are not unwantedly connected with a continuity test.
- Check if the IC's have correct power supply.
- Check if the errorzz are resolved correctly.
- Let me know if you have more tips for other future builders.

Trouble shooting Channel A step by step (Channel B is similar actually)



3) Check this output with oscilloscope.
- First set potmeter in center
- It should look like noise but then with square waves.
- Turn the potmeter to both sides and you should see the signal changing. (less or more spikes)

1) Check with oscilloscope if noise is somewhat between -5V and +5V. Also adjust trimpot RV2 to change the amplification of noise if needed

4) Check this output with oscilloscope.
- Similar but only with positive voltages

2) Measure with multi-meter or oscilloscope voltage level. See if it changes between -5V and +5V, when changing potmeter

9) Turn potmeter fully clockwise.
- Give GATE_IN a steady clock pulse.
- check with oscilloscope if you see a clock pulses here as well

6) Similar as step 3

8) Use a clock pulse into GATE_IN and check with oscilloscope if you see clock pulses here as well, but in reverse (high=low, low-high)

5) Use a steady clock pulse into GATE_IN and check with oscilloscope if you see a clock pulses here as well

7) Similar as step 3

Kind regards Louis-Pierre Geerinckx
alias Luther