Quad, Low Power, 12-Bit, 180 MSPS, Digital-to-Analog Converter and Waveform Generator

Data Sheet

AD9106

FEATURES

Highly integrated quad DAC
On-chip 4096 × 12-bit pattern memory
On-chip DDS
Power dissipation at 3.3 V, 4 mA output typical
  315.25 mW at 180 MSPS
Power-down mode: <5 mW at 3.3 V
Supply voltage: 1.8 V to 3.3 V
SFDR to Nyquist: 86 dBc at 10 MHz output
Phase noise at 1 kHz offset, 180 MSPS, 4 mA: −140 dBc/Hz
Differential full-scale current outputs: 8 mA maximum at 3.3 V
Small footprint, 5 mm × 5 mm with 3.5 mm × 3.6 mm exposed paddle, 32-lead LFCSP
RoHS compliant package

APPLICATIONS

Medical instrumentation
  Ultrasound transducer excitation
Portable instrumentation
  Signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The AD9106 TxDAC® and waveform generator is a high performance, quad digital-to-analog converter (DAC) integrating on-chip pattern memory for complex waveform generation with a direct digital synthesizer (DDS). The DDS is a 12-bit output, up to 180 MHz master clock sinewave generator with a 24-bit tuning word allowing 10.8 Hz/LSB frequency resolution. The DDS has a single frequency output for all four DACs and independent programmable phase shift outputs for each of the four DACs.

SRAM data can include directly generated stored waveforms, amplitude modulation patterns applied to DDS outputs, or DDS frequency tuning words.

An internal pattern control state machine allows the user to program the pattern period for all four DACs as well as the start delay within the pattern period for the signal output on each DAC channel.

Registers accessed using the serial peripheral interface (SPI) configure the digital waveform generator and load patterns into the SRAM.

There are gain adjustment factors and offset adjustments applied to the digital signals on their way into the four DACs.

The AD9106 offers exceptional ac and dc performance and supports DAC sampling rates up to 180 MSPS. The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9106 make it well suited for portable and low power applications.

Rev. B **Document Feedback**

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REVISION HISTORY

12/2017—Rev. A to Rev. B

2/2013—Rev. 0 to Rev. A

11/2012—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

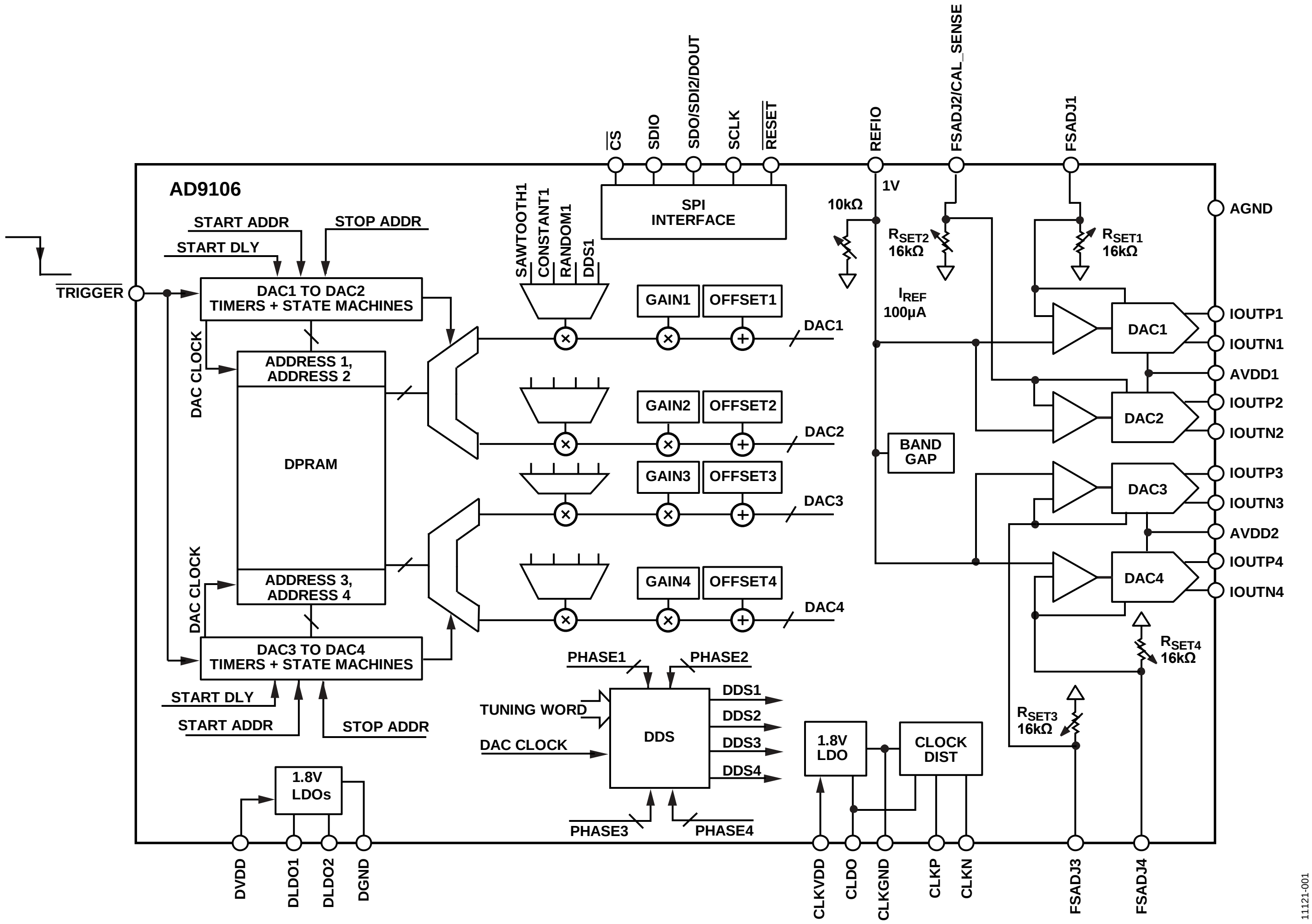


Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDDx = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ACCURACY AT 3.3 V				
Differential Nonlinearity (DNL)		±0.4		LSB
Integral Nonlinearity (INL)		±0.5		LSB
DAC OUTPUTS				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current[1] at 3.3 V	2	4	8	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
Crosstalk, DAC to DAC				
f_{OUT} = 10 MHz		96		dBc
f_{OUT} = 60 MHz		82		dBc
DAC TEMPERATURE DRIFT				
Gain with Internal Reference		±251		ppm/°C
Internal Reference Voltage		±119		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDDx = 3.3 V		1.0		V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External, Reference Mode		1		MΩ
DAC MATCHING				
Gain Matching—No Automatic I_{OUTFS} Calibration		±0.75		% of FSR

[1] Based on use of 8 kΩ external R_{SETx} resistors.

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ACCURACY AT 1.8 V				
Differential Nonlinearity (DNL)		±0.4		LSB
Integral Nonlinearity (INL)		±0.4		LSB
DAC OUTPUTS				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current[1] at 1.8 V	2	4	4	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
Crosstalk, DAC to DAC				
f_{OUT} = 30 MHz		94		dB
f_{OUT} = 60 MHz		78		dB
DAC TEMPERATURE DRIFT				
Gain		±228		ppm/°C
Reference Voltage		±131		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDDx = 1.8 V		1.0		V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External, Reference Mode		1		MΩ
DAC MATCHING				
Gain Matching—No Automatic I_{OUTFS} Calibration		±0.75		% of FSR

[1] Based on use of 8 kΩ external R_{SETx} resistors.

DIGITAL TIMING SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDDx = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKx)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time, SDIO to SCLK	3.5			ns
Hold Time, SDIO to SCLK	1.5			ns
Output Data Valid, SCLK to SDO[1] or SDIO		6.2		ns
Setup Time, $\overline{CS}$ to SCLK	4.0			ns
$\overline{TRIGGER}$ TIMING RELATIVE TO CLKP/CLKN RISING EDGE				
Setup Time (t_{SU}), $\overline{TRIGGER}$ Edge to CLKP/CLKN	1.5			ns
Hold Time, CLKP/CLKN to $\overline{TRIGGER}$ Edge	2.0			ns

[1] Note that throughout this data sheet, multifunction pins, such as SDO/SDI2/DOUT, are referred to either by the entire pin name or by a single function of the pin, for example, SDO, when only that function is relevant.

DIGITAL TIMING SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKx)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time, SDIO to SCLK	3.5			ns
Hold Time, SDIO to SCLK	1.5			ns
Output Data Valid, SCLK to SDO or SDIO		8.8		ns
Setup Time, $\overline{CS}$ to SCLK	4.0			ns
$\overline{TRIGGER}$ TIMING RELATIVE TO CLKP/CLKN RISING EDGE				
Setup Time, $\overline{TRIGGER}$ Edge to CLKP/CLKN	1.5			ns
Hold Time, CLKP/CLKN to $\overline{TRIGGER}$ Edge	2.0			ns

INPUT/OUTPUT SIGNAL SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL (SCLK, $\overline{CS}$, SDIO, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$)					
Input Voltage, V_{IN}					
Logic High	DVDD = 1.8 V	1.53			V
	DVDD = 3.3 V	2.475			V
Logic Low	DVDD = 1.8 V			0.27	V
	DVDD = 3.3 V			0.825	V
CMOS OUTPUT LOGIC LEVEL (SDIO, SDO/SDI2/DOUT)					
Output Voltage, V_{OUT}					
Logic High	DVDD = 1.8 V	1.79			V
	DVDD = 3.3 V	3.28			V
Logic Low	DVDD = 1.8 V			0.25	V
	DVDD = 3.3 V			0.625	V
DAC CLOCK INPUT (CLKP, CLKN)					
Minimum Peak-to-Peak Differential Input Voltage, V_{CLKP}/V_{CLKN}			150		mV
Maximum Voltage at V_{CLKP} or V_{CLKN}			V_{DVDD}		V
Minimum Voltage at V_{CLKP} or V_{CLKN}			V_{DGND}		V
Common-Mode Voltage Generated on Chip			0.9		V

AC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDDx = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
DAC Sample Rate (f_{DAC}) = 180 MSPS, DAC Output Frequency (f_{OUT}) = 10 MHz		86		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		73		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		92		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		77		dBc
NOISE SPECTRAL DENSITY (NSD)				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−167		dBm/Hz
PHASE NOISE AT 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−140		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time, Full-Scale Output Step (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time, Full-Scale Swing[1]		3.25		ns
Fall Time, Full-Scale Swing[1]		3.26		ns

[1] Based on the 85 Ω resistors from DAC output terminals to ground.
[2] Start delay = 0 f_{DAC} clock cycles.

AC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V, I_{OUTFS} = 4 mA, maximum sample rate, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		83		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		74		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		91		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		83		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE AT 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−140		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time[1]		3.25		ns
Fall Time[1]		3.26		ns

[1] Based on the 85 Ω resistors from DAC output terminals to ground.
[2] Start delay = 0 f_{DAC} clock cycles.

POWER SUPPLY VOLTAGE INPUTS AND POWER DISSIPATION

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG SUPPLY VOLTAGES					
AVDD1, AVDD2		1.7		3.6	V
CLKVDD		1.7		3.6	V
CLDO	On-chip low dropout (LDO) regulator not in use	1.7		1.9	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.7		3.6	V
DLDO1, DLDO2	On-chip LDO not in use	1.7		1.9	V
POWER CONSUMPTION, 3.3 V	AVDDx = 3.3 V; DVDD = 3.3 V; CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2				
f_{DAC} = 180 MSPS, Pure Continuous Waveform (CW) Sine Wave	12.5 MHz (DDS only), all four DACs		315.25		mW
I_{AVDDx}			28.51		mA
I_{DVDD}					
DDS Only	CW sine wave output		60.3		mA
RAM Only	50% duty cycle full-scale (FS) pulse output		27.1		mA
DDS and RAM Only	50% duty cycle sine wave output		39.75		mA
I_{CLKVDD}			6.72		mA
Power-Down Mode	REF_PDN = 0, DACs sleep, clock power down, external clock, and supplies on		4.73		mW
POWER CONSUMPTION, 1.8 V	AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		167		mW
I_{AVDDx}			28.14		mA
I_{DVDD}			0.151		mA
I_{DLDO2}					
DDS Only	CW sine wave output		53.75		mA
RAM Only	50% duty cycle FS pulse output		17.78		mA
DDS and RAM Only—50% Duty Cycle Sine Wave Output			35.4		mA
I_{DLDO1}			4.0		mA
I_{CLKVDD}			0.0096		mA
I_{CLDO}			6.6		mA
Power-Down Mode	REF_PDN = 0, DACs sleep, clock power down, external clock, and supplies on		1.49		mW

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
AVDD1, AVDD2, DVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLKVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLDO, DLDO1, DLDO2 to AGND, DGND, CLKGND	−0.3 V to +2.2 V
AGND to DGND, CLKGND	−0.3 V to +0.3V
DGND to AGND, CLKGND	−0.3 V to +0.3 V
CLKGND to AGND, DGND	−0.3 V to +0.3 V
$\overline{\text{CS}}$, SDIO, SCLK, SDO/SDI2/DOUT, $\overline{\text{RESET}}$, $\overline{\text{TRIGGER}}$ to DGND	−0.3 V to DVDD + 0.3 V
CLKP, CLKN to CLKGND	−0.3 V to CLKVDD + 0.3 V
REFIO to AGND	−1.0 V to AVDDx + 0.3 V
IOUTP1, IOUTN1, IOUTP2, IOUTN2, IOUTP3, IOUTN3, IOUTP4, IOUTN4 to AGND	−0.3 V to DVDD + 0.3 V
FSADJ1, FSADJ2/CAL_SENSE, FS4DJ3, FSADJ4 to AGND	−0.3 V to AVDDx + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
CP-32-12[1]	30.18	6.59	3.84[2]	°C/W

[1] Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a JEDEC 4-layer 2S2P board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} and θ_{JB}.
[2] θ_{JC} is junction to case on the exposed pad.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

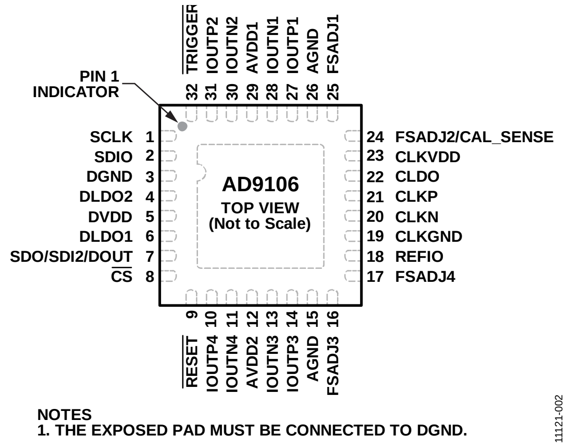


Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	SPI Clock Input.
2	SDIO	SPI Data Input/Output. Primary bidirectional data line for the SPI port.
3	DGND	Digital Ground.
4	DLDO2	1.8 V Internal Digital LDO1 Output. When the internal digital LDO1 is enabled, bypass this pin with a 0.1 µF capacitor.
5	DVDD	3.3 V External Digital Power Supply. DVDD defines the level of the digital interface of the AD9106 (SPI interface).
6	DLDO1	1.8 V Internal Digital LDO2 Outputs. When the internal digital LDO2 is enabled, bypass this pin with a 0.1 µF capacitor.
7	SDO/SDI2/DOUT	Serial Data Output (SDO). In 4-wire SPI mode, this pin outputs the data from the SPI. Second Data Input Line (SDI2). In double SPI mode, this pin is a second data input line, SDI2, for the SPI port used to write to the SRAM. Pulse Output (DOUT). In data output mode, this terminal is a programmable pulse output.
8	$\overline{\text{CS}}$	SPI Port Chip Select, Active Low.
9	$\overline{\text{RESET}}$	Active Low Reset Pin. Resets registers to their default values.
10	IOUTP4	DAC4 Current Output, Positive Side.
11	IOUTN4	DAC4 Current Output, Negative Side.
12	AVDD2	1.8 V to 3.3 V Power Supply Input for DAC3 and DAC4.
13	IOUTN3	DAC3 Current Output, Negative Side.
14	IOUTP3	DAC3 Current Output, Positive Side.
15	AGND	Analog Ground.
16	FSADJ3	External Full-Scale Current Output Adjust for DAC3.
17	FSADJ4	External Full-Scale Current Output Adjust for DAC4.
18	REFIO	DAC Voltage Reference Input/Output.
19	CLKGND	Clock Ground.
20	CLKN	Clock Input, Negative Side.
21	CLKP	Clock Input, Positive Side.
22	CLDO	Clock Power Supply Output (Internal Regulator in Use), Clock Power Supply Input (Internal Regulator Bypassed).
23	CLKVDD	Clock Power Supply Input.
24	FSADJ2/CAL_SENSE	External Full-Scale Current Output Adjust for DAC2 (FSADJ2). Sense Input for Automatic I_{OUTFS} Calibration (CAL_SENSE).
25	FSADJ1	External Full-Scale Current Output Adjust for DAC1 or Full-Scale Current Output Adjust Reference for Automatic I_{OUTFS} Calibration.
26	AGND	Analog Ground.
27	IOUTP1	DAC1 Current Output, Positive Side.

Pin No.	Mnemonic	Description
28	IOUTN1	DAC1 Current Output, Negative Side.
29	AVDD1	1.8 V to 3.3 V Power Supply Input for DAC1 and DAC2.
30	IOUTN2	DAC2 Current Output, Negative Side.
31	IOUTP2	DAC2 Current Output, Positive Side.
32	$\overline{\text{TRIGGER}}$	Pattern Trigger Input, Active Low.
	EPAD	Exposed Pad. The exposed pad must be connected to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDDx = 3.3 V; DVDD = 3.3 V; CLKVDD = 3.3 V; internal CLDO, DLDO1, and DLDO2.

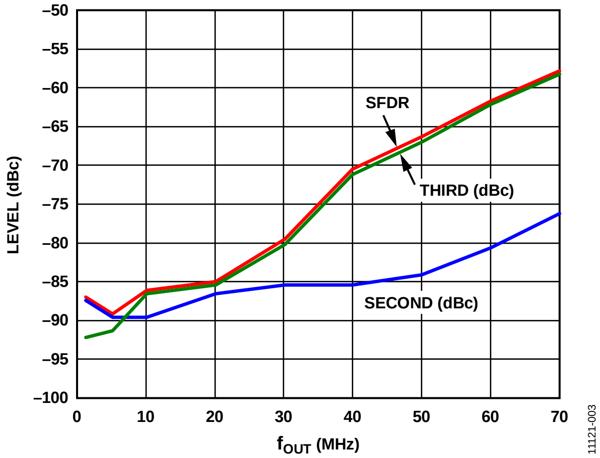


Figure 3. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 8 mA

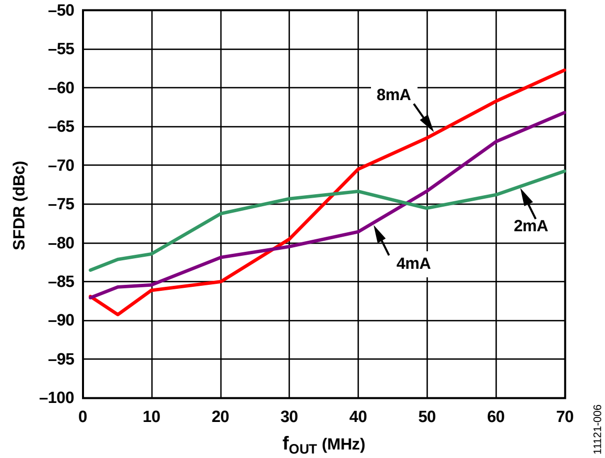


Figure 6. SFDR vs. f_{OUT}, at Three I_{OUTFS} Values

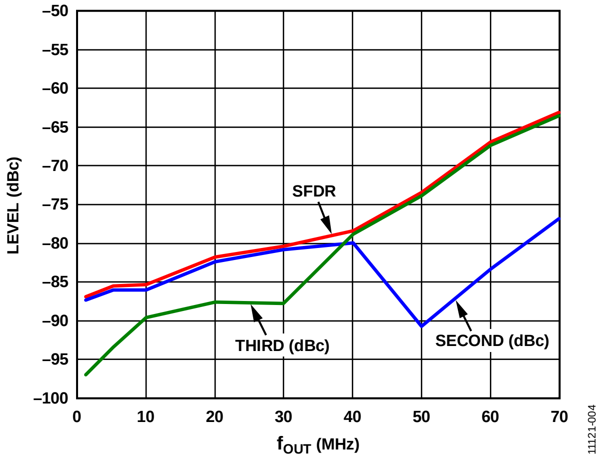


Figure 4. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 4 mA

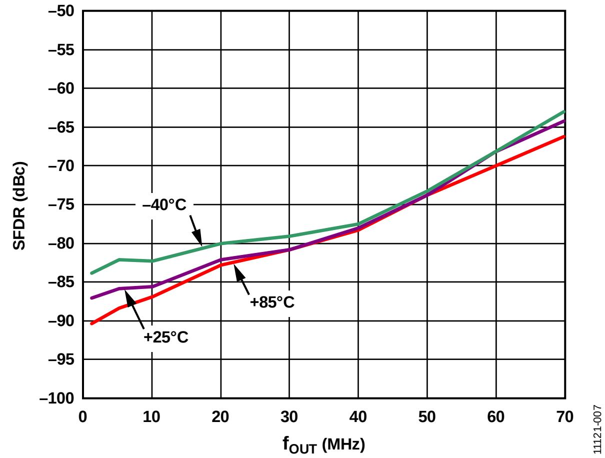


Figure 7. SFDR vs. f_{OUT}, at Three Temperatures

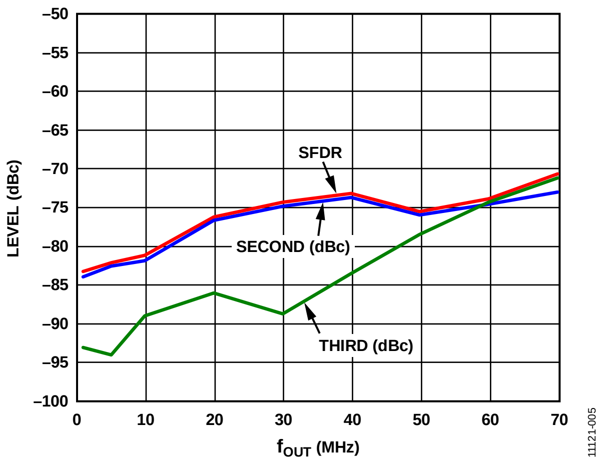


Figure 5. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 2 mA

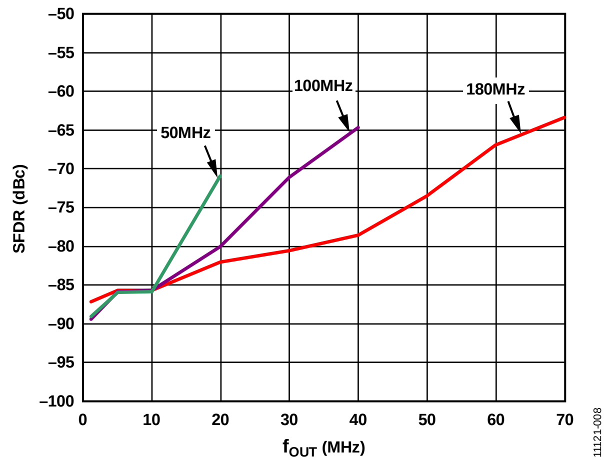


Figure 8. SFDR vs. f_{OUT}, at Three f_{DAC} Values

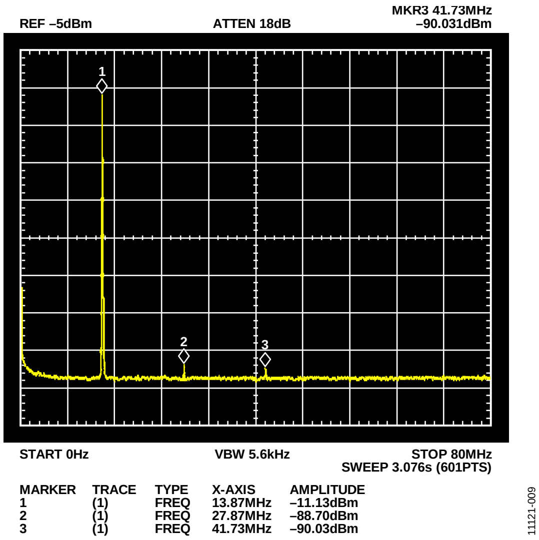


Figure 9. Output Spectrum, f_{OUT} = 13.87 MHz

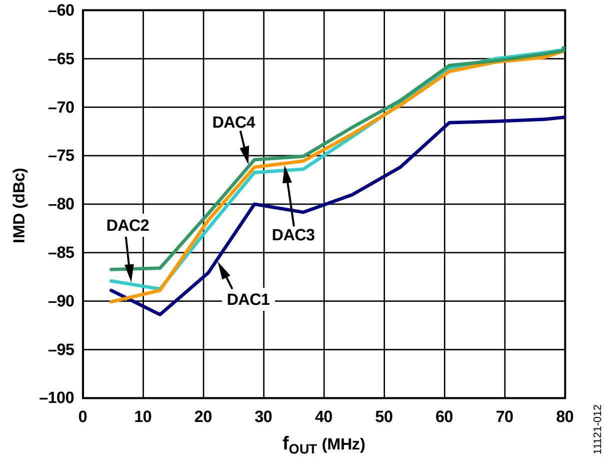


Figure 12. IMD vs. f_{OUT}, All Four DACs

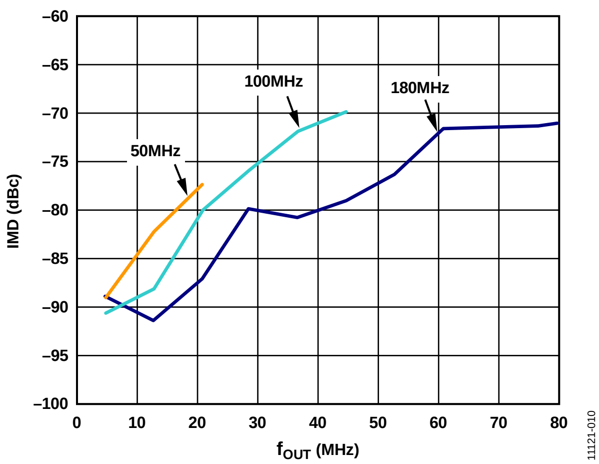


Figure 10. IMD vs. f_{OUT}, at Three f_{DAC} Values

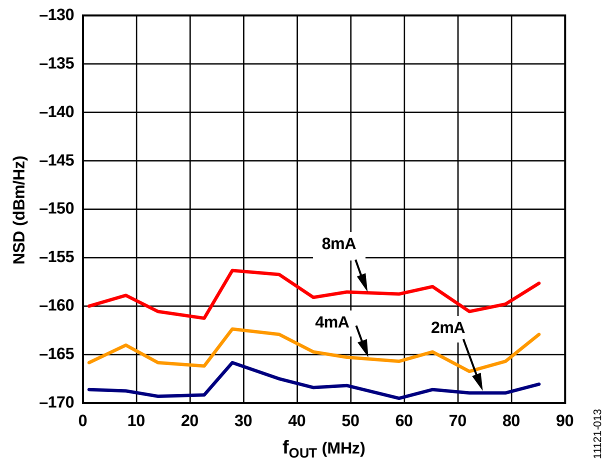


Figure 13. NSD vs. f_{OUT}, at Three I_{OUTFS} Values

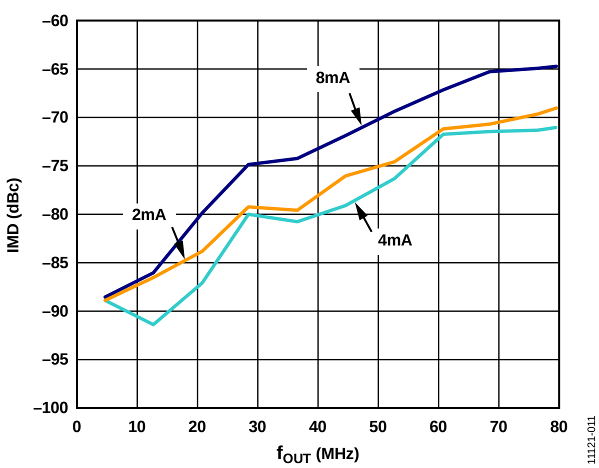


Figure 11. IMD vs. f_{OUT}, at Three I_{OUTFS} Values

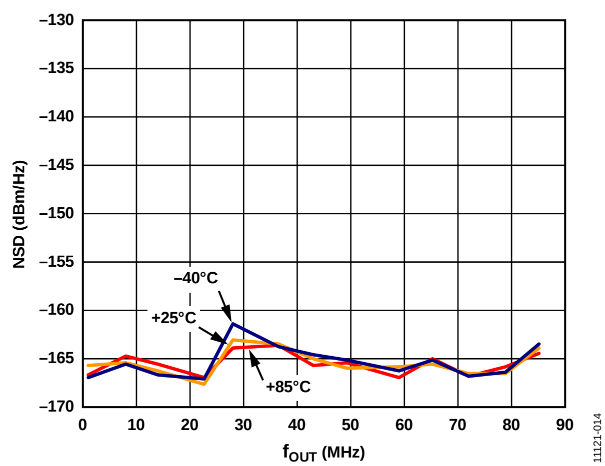


Figure 14. NSD vs. f_{OUT}, at Three Temperatures

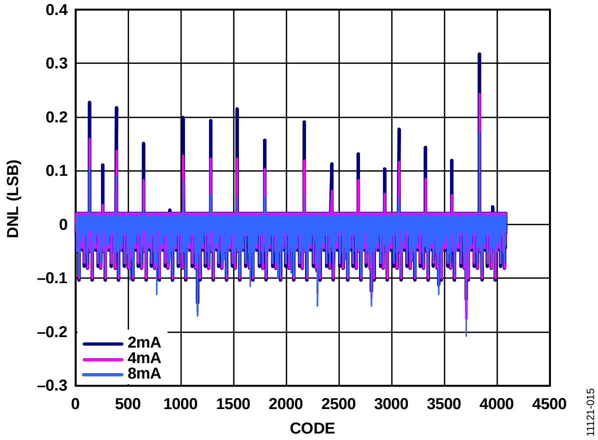


Figure 15. DNL, at Three I_{OUTFS} Values

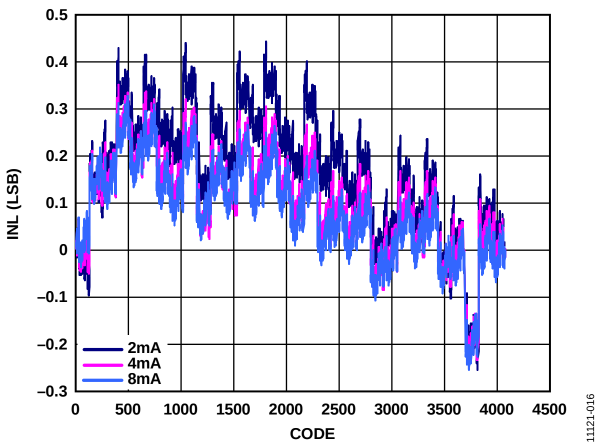


Figure 16. INL, at Three I_{OUTFS} Values

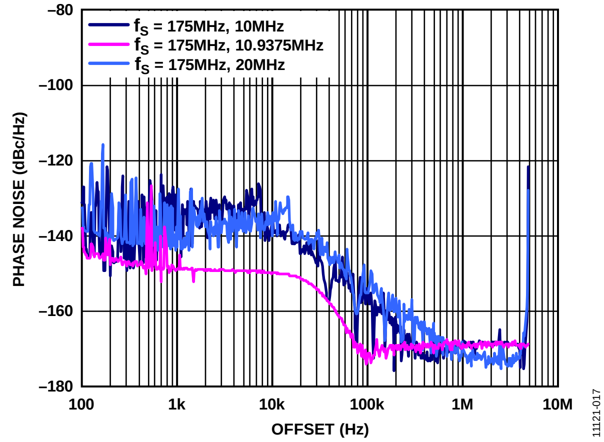


Figure 17. Phase Noise

AVDDx = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V.

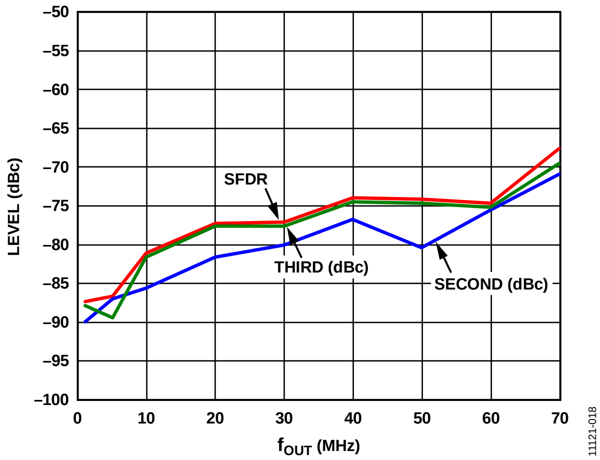


Figure 18. SFDR, Second and Third Harmonics vs. f_{OUT}, I_{OUTFS} = 4 mA

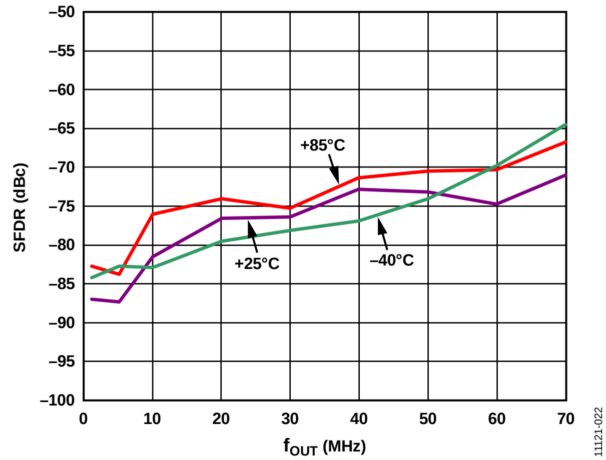


Figure 21. SFDR vs. f_{OUT}, at Three Temperatures

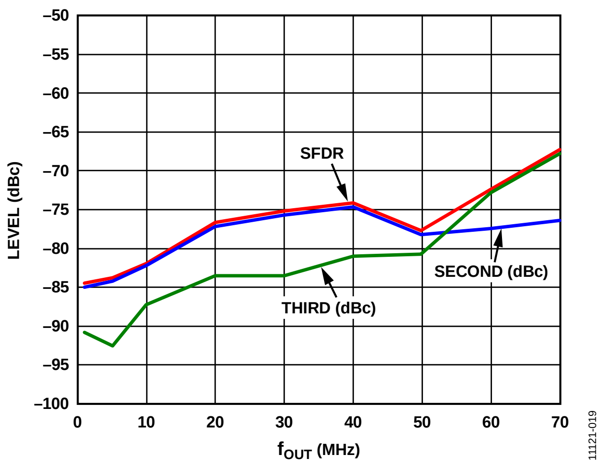


Figure 19. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 2 mA vs. f_{OUT}

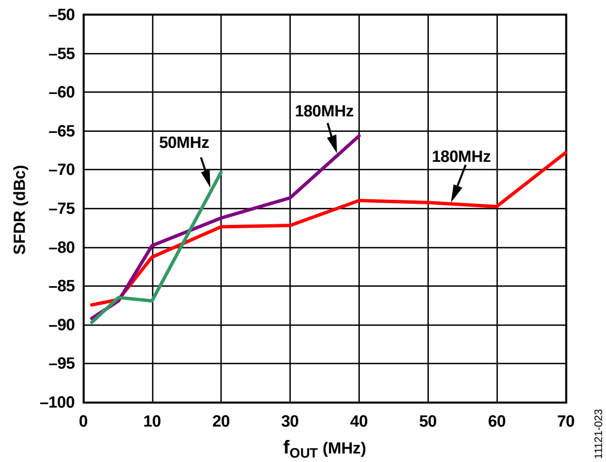


Figure 22. SFDR vs. f_{OUT}, at Three f_{DAC} Values

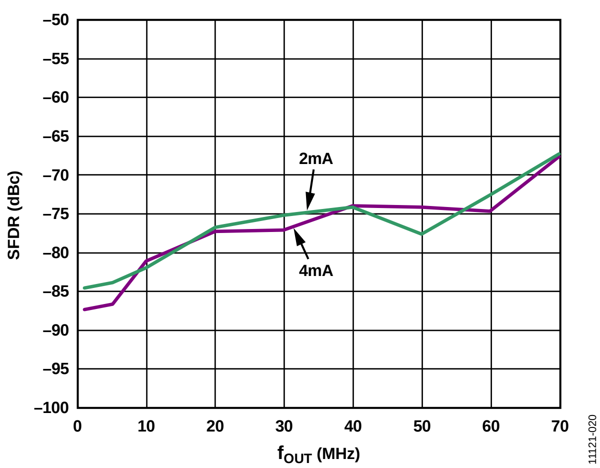


Figure 20. SFDR vs. f_{OUT}, at Two I_{OUTFS} Values

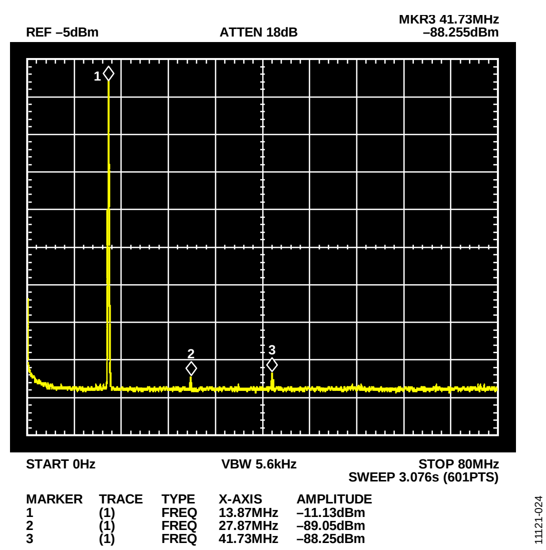


Figure 23. Output Spectrum, f_{OUT} = 13.87 MHz

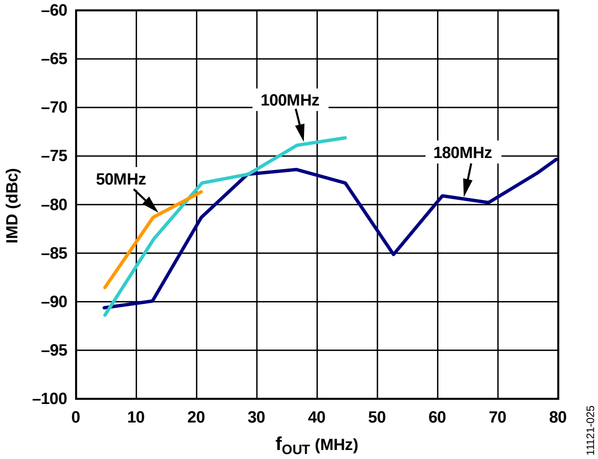


Figure 24. IMD vs. f_{OUT}, at Three f_{DAC} Values

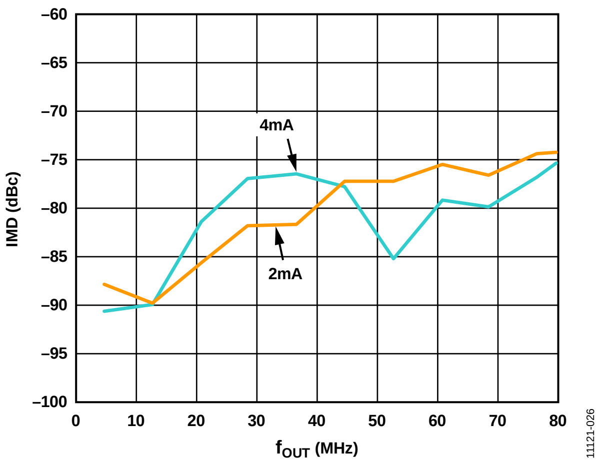


Figure 25. IMD vs. f_{OUT}, at Two I_{OUTFS} Values

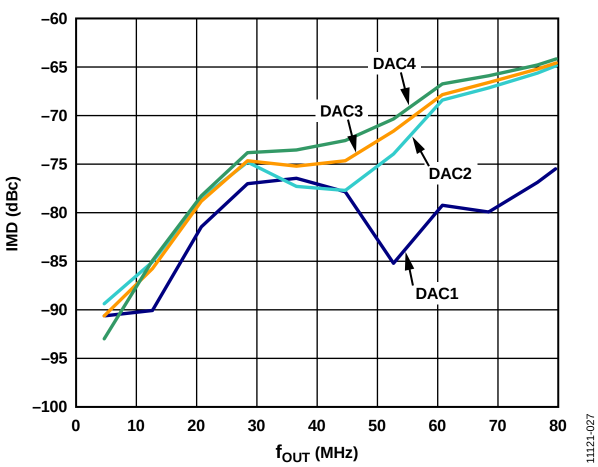


Figure 26. IMD vs. f_{OUT}, at All Four DACs

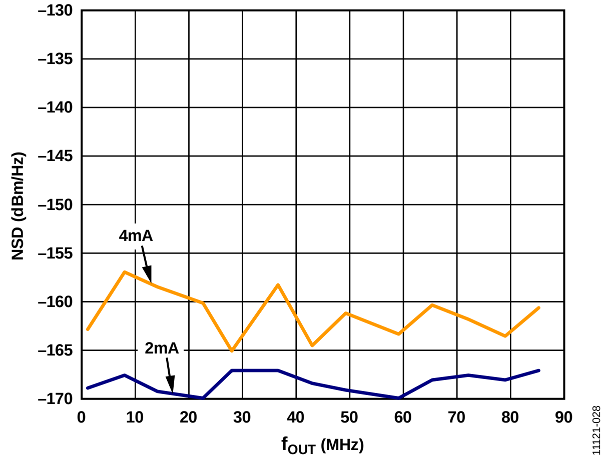


Figure 27. NSD vs. f_{OUT}, at Two I_{OUTFS} Values

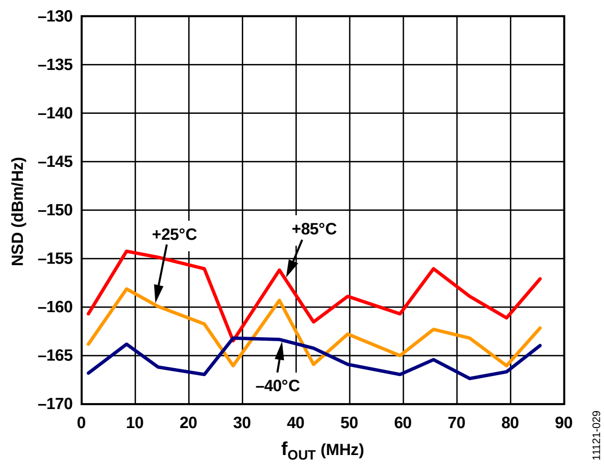


Figure 28. NSD vs. f_{OUT}, at Three Temperatures

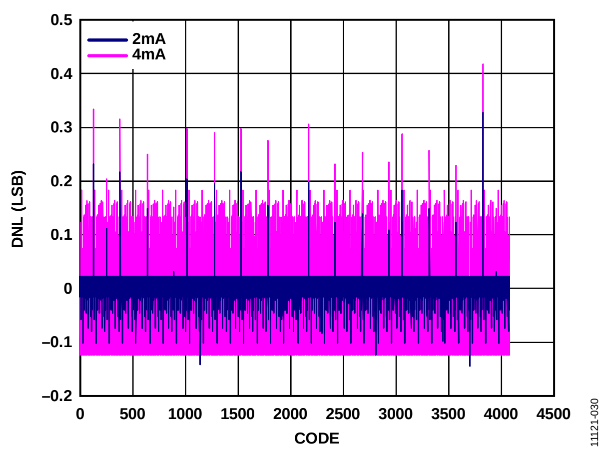


Figure 29. DNL, at Three I_{OUTFS} Values

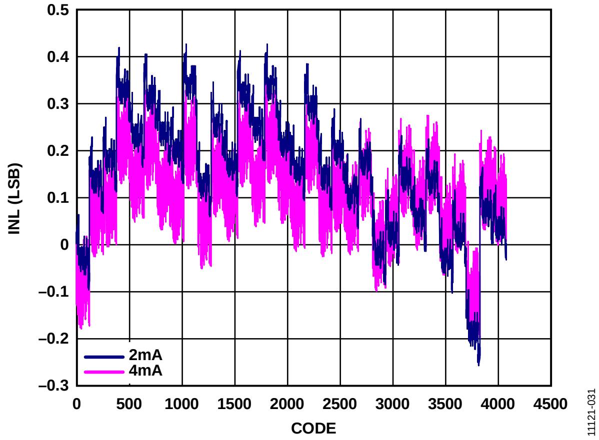


Figure 30. INL, at Two I_{OUTFS} Values

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

Offset error is the deviation of the output current from the ideal of zero. For IOUTPx, 0 mA output is expected when the inputs are all 0s. For IOUTNx, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured V_{REFIO}. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage
Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse

Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolt-seconds (pV-sec).

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)
Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

THEORY OF OPERATION

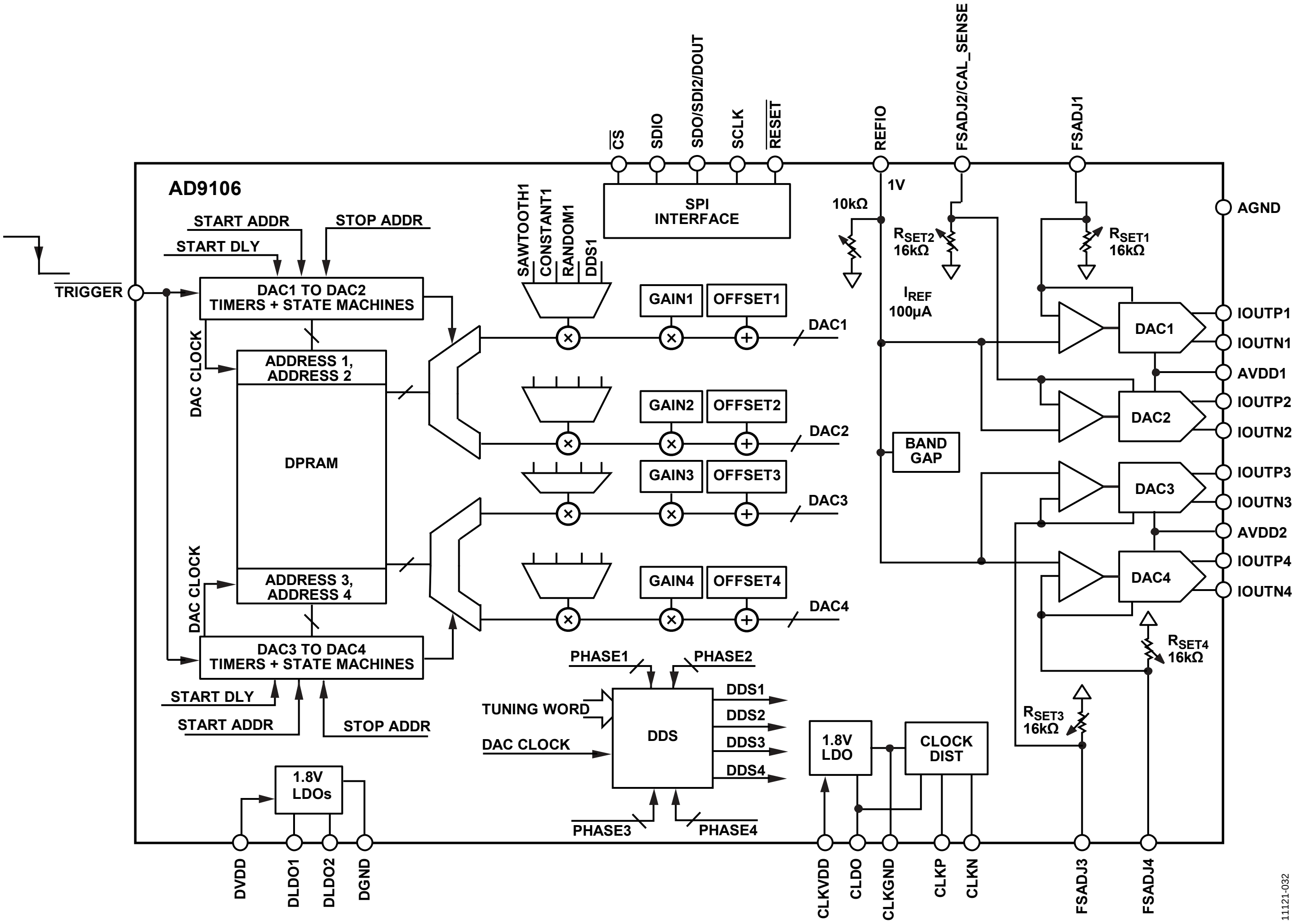


Figure 31. Block Diagram

Figure 31 is a block diagram of the AD9106. The AD9106 has four 12-bit current output DACs.

The DACs use a single common voltage reference. An on-chip band gap reference is provided. Optionally, an off-chip voltage reference can be used. Full-scale DAC output current, also known as gain, is governed by the current, I_{REFx}. I_{REFx} is the current that flows through each I_{REFx} resistor. Each DAC has its own I_{REFx} set resistor. These resistors can be on or off chip at the discretion of the user. When on-chip R_{SETx} resistors are in use, DAC gain accuracy can be improved by employing the AD9106 built in automatic gain calibration capability. Automatic calibration can be used with the on-chip reference or an external REFIO voltage. See the Automatic IOUTFSx Calibration section for a procedure for automatic gain calibration.

The power supply rails for the AD9106 are AVDDx for the analog circuits, CLKVDD/CLDO for the clock input receiver and DVDD/DLDO1/DLDO2 for the digital I/O and for the on-chip digital data path. AVDDx, DVDD, and CLKVDD can range from 1.8 V to 3.3 V nominal. DLDO1, DLDO2, and CLDO operate at 1.8 V. If DVDD = 1.8 V, DLDO1 and DLDO2 must both be connected to DVDD, with the on-chip LDOs disabled. All three supplies are provided externally in this case. Likewise, if CLKVDD = 1.8 V, CLDO must be connected to CLKVDD, with the on-chip LDO disabled.

Digital signals input to the four DACs are generated by on-chip digital waveform generation resources. From a dedicated digital data path, 12-bit samples are input to each DAC at the CLKP/CLKN sample rate. The data path of each DAC includes gain and offset corrections and a digital waveform source selection multiplexer. Waveform sources are SRAM, direct digital synthesizer (DDS), DDS output amplitude modulated by SRAM data, a sawtooth generator, dc constant, and a pseudorandom sequence generator. The waveforms output by the source selection multiplexer have programmable pattern characteristics. The waveforms can be set up to be continuous, continuous pulsed (fixed pattern period and start delay within each pattern period), or finite pulsed (a set number of pattern periods are output, then the pattern stops).

Pulsed waveforms (finite or continuous) have a programmed pattern period and start delay. The waveform is present in each pulse period following the global (applies to all four DACs) programmed pattern period start and the start delay of each DAC.

An SPI port enables loading of data into SRAM and programming of all the control registers inside the device.

SPI PORT

The AD9106 provides a flexible, synchronous serial communications (SPI) port that allows easy interfacing to application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and industry-standard microcontrollers. The interface allows read/write access to all registers that configure the AD9106 and to the on-chip SRAM. Its data rate can be up to the SCLK clock speed shown in Table 3 and Table 4.

The SPI interface operates as a standard synchronous serial communication port. $\overline{CS}$ is an active low chip select pin. When $\overline{CS}$ is active low, SPI address and data transfer begins. The first bit coming from the SPI master on SDIO is a read/write indicator (high for read, low for write). The next 15 bits are the initial register address. For multiple consecutive register write/read operations in the 0x00 to 0x60 address space, the SPI port automatically increments the register address if $\overline{CS}$ stays low beyond the first data-word, allowing writes to or reads from a set of contiguous addresses. For SRAM access in the 0x6FFF address space, the address autodecrements if $\overline{CS}$ stays low beyond the first data-word.

Table 12. Command Word

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**…**	**DB2**	**DB1**	**DB0**
$R\overline{W}$	A14	A13	A12	…	A2	A1	A0

When the first bit of this command byte is a logic low ($R\overline{W}$ bit = 0), the SPI command is a write operation. In this case, SDIO remains an input (see Figure 32).

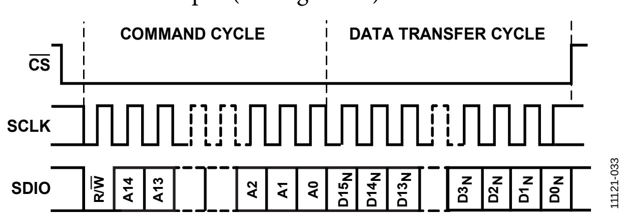


Figure 32. Serial Register Interface Timing, MSB First Write, 3-Wire SPI

When the first bit of this command byte is a logic high ($R\overline{W}$ bit = 1), the SPI command is a read operation. In this case, data is driven out of the SPI port as shown in Figure 33 and Figure 35. The SPI communication finishes after the $\overline{CS}$ pin goes high.

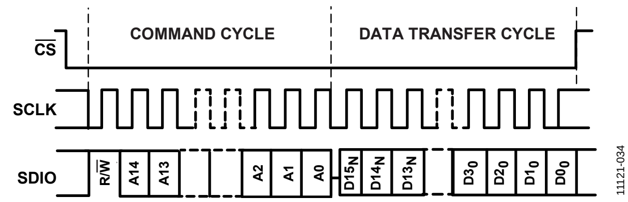


Figure 33. Serial Register Interface Timing, MSB First Read, 3-Wire SPI

Writing to On-Chip SRAM

The AD9106 includes an internal 4096 × 12-bit SRAM. The SRAM address space is 0x6000 to 0x6FFF of the AD9106 SPI address map.

During writes to or reads from multiple consecutive SRAM locations, the SPI address autodecrements.

Double SPI for Write for SRAM

The time to write data to an SRAM segment can be reduced by half using the SPI access mode shown in Figure 34. The SDO/SDI2/DOUT line becomes a second serial data input line, doubling the achievable update rate of the on-chip SRAM. SDO/SDI2/DOUT is write only in this mode. The entire SRAM can be written in $(2 + 2 \times 4096) \times 8/(2 \times f_{SCLK})$ seconds.

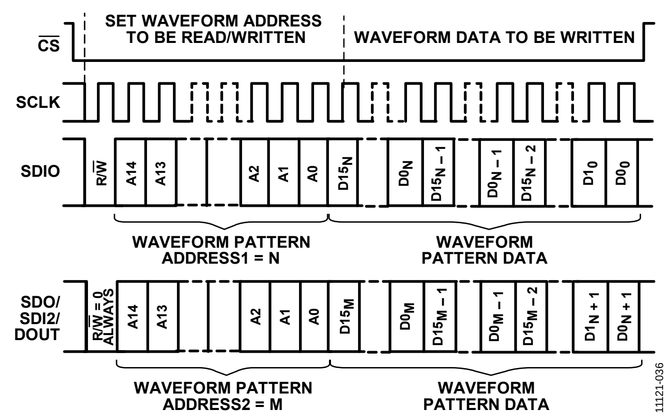


Figure 34. Double SPI Write of SRAM Data

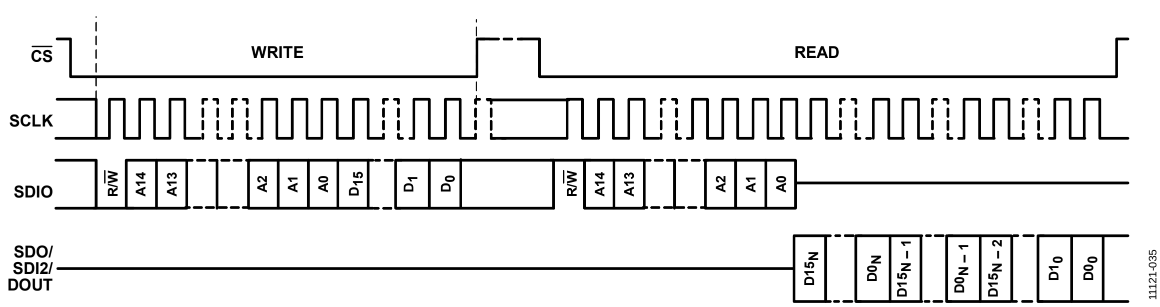


Figure 35. Serial Register Interface Timing, MSB First Read, 4-Wire SPI

Configuration Register Update Procedure

Most SPI accessible registers are double buffered. An active register set controls operation of the AD9106 during pattern generation. A set of shadow registers stores updated register values. Register updates can be written at any time, and when the configuration update is complete, a 1 is written to the update bit in the RAMUPDATE register. The update bit arms the register set for transfer from shadow registers to active registers. The AD9106 performs this transfer automatically the next time the pattern generator is off. This procedure does not apply to the 4096 × 12-bit SRAM. Refer to the SRAM section for the SRAM update procedure.

DAC TRANSFER FUNCTION

The AD9106 DACs provide four differential current outputs: IOUTP1/IOUTN1, IOUTP2/IOUTN2, IOUTP3/IOUTN3, and IOUTP4/IOUTN4.

Digital waveforms generated on chip for input to the four DACs use a twos complement number system. The sign bit of each digital waveform word is inverted immediately prior to input to each DAC core. The DACx Input Code variable in Equation 1 and Equation 2 uses an offset binary number system (twos complement with the sign bit inverted). DACx Input Code = 0 to $2^{12} - 1$.

The DAC output current equations are as follows:

$$IOUTPx = I_{OUTFSx} \times DACx\ Input\ Code/2^{12} \quad (1)$$

$$IOUTNx = I_{OUTFSx} \times ((2^{12} - 1) - DACx\ Input\ Code)/2^{12} \quad (2)$$

where:
I_{OUTFSx} is the full-scale current or DAC gain set independently for each DAC.

$$I_{OUTFSx} = 32 \times I_{REFx} \quad (3)$$

where:

$$I_{REFx} = V_{REFIO}/R_{SETx} \quad (4)$$

I_{REFx} is the current that flows through each I_{REFx} resistor. Each DAC has its own I_{REF} set resistor. I_{REFx} resistors can be on or off chip at the discretion of the user. When on-chip R_{SETx} resistors are in use, DAC gain accuracy can be improved by employing the built in automatic gain calibration capability of the device.

ANALOG CURRENT OUTPUTS

Optimum linearity and noise performance of DAC outputs can be achieved when they are connected differentially to an amplifier or a transformer. In these configurations, common-mode signals at the DAC outputs are rejected.

The output compliance voltage specifications shown in Table 1 and Table 2 must be adhered to for the performance specifications in these tables to be met.

SETTING DAC GAIN (I_{OUTFSx})

As expressed in Equation 3 and Equation 4, DAC gain (I_{OUTFSx}) is a function of the reference voltage at the REFIO terminal and R_{SETx} for each DAC.

Voltage Reference

The AD9106 contains an internal 1.0 V nominal band gap reference, V_{BG}. The internal reference can be used. Alternatively, it can be replaced by a more accurate off-chip reference. An external reference can provide tighter reference voltage tolerances and/or lower temperature drift than the on-chip band gap.

By default, the on-chip reference is powered up and ready to be used. When using the on-chip reference, the REFIO terminal needs to be decoupled to AGND using a 0.1 µF capacitor as shown in Figure 36.

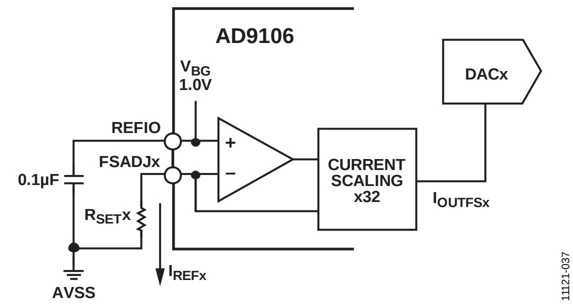


Figure 36. On-Chip Reference with External xRSET Resistor

Table 13 summarizes reference connections and programming.

Table 13. Reference Operation

Reference Mode	REFIO Pin
Internal	Connect 0.1 µF capacitor
External	Connect off-chip reference

Programming Internal V_{REFIO}

The internal REFIO voltage level is programmable.

When the internal voltage reference is in use, the BGDR field in the lower six bits in Register 0x03 adjusts the V_{REFIO} level. This adjustment adds or subtracts up to 20% from the nominal band gap voltage on REFIO. The voltage across the FSADJx resistors tracks this change. As a result, I_{REFx} varies by the same amount. Figure 37 shows V_{REFIO} vs. BGDR code for an on-chip reference with a voltage (BGDR = 0x00) of 1.04 V. The V_{REFIO} voltage at BGDR = 0x00 can vary over the internal reference voltage range shown in Table 1 and Table 2 from chip to chip.

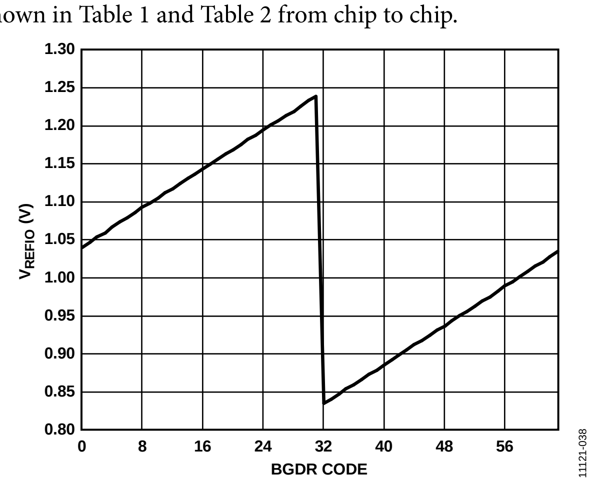


Figure 37. Typical VREF Voltage vs. BGDR Code

R_{SETx} Resistors

R_{SETx} in Equation 4 for each DAC can be an internal resistor or a board level resistor, chosen by the user, connected to the appropriate FSADJx terminal.

To make use of on-chip R_{SETx} resistors, set Bit 15 of Register 0x0C, Register 0x0B, Register 0x0A, and Register 0x09 for DAC1, DAC2, DAC3, and DAC4, respectively, to Logic 1. Use Bits[4:0] of Register 0x0C, Register 0x0B, Register 0x0A, and Register 0x09 to manually program values for the on-chip R_{SETx} associated with DAC1, DAC2, DAC3, and DAC4, respectively.

AUTOMATIC I_{OUTFSx} CALIBRATION

Many applications require tight DAC gain control. The AD9106 provides an automatic I_{OUTFSx} calibration procedure used with on-chip R_{SETx} resistors only. The voltage reference, V_{REFIO}, can be the on-chip reference or an off-chip reference. The automatic calibration procedure performs a fine adjustment of each internal R_{SETx} value and each current I_{REFx}.

When using automatic calibration, the following board level connections are required:

1. Connect FSADJ1 and FSADJ2/CAL_SENSE together.
2. Install a resistor between FSADJ2/CAL_SENSE and ground. The value of this resistor must be $R_{CAL\_SENSE} = 32 \times V_{REFIO}/I_{OUTFS}$, where I_{OUTFS} is the target full-scale current for all four DACs.

Automatic calibration uses an internal clock. This calibration clock is equal to the DAC clock divided by the division factor chosen by the CAL_CLK_DIV bits of Register 0x0D. Each calibration cycle is between 4 and 512 DAC clock cycles, depending on the value of CAL_CLK_DIV. The frequency of the calibration clock must be less than 500 kHz.

To perform an automatic calibration, follow these steps:

1. Set the calibration ranges in Register 0x08, Bits[7:0], and Register 0x0D, Bits[5:4] to their minimum values to allow best calibration.
2. Enable the calibration clock bit, CAL_CLK_EN, in Register 0x0D.
3. Set the divider ratio for the calibration clock by setting CAL_CLK_DIV bits in Register 0x0D. The default is 512.
4. Set the CAL_MODE_EN bit in Register 0x0D to Logic 1.
5. Set the START_CAL bit in Register 0x0E to Logic 1to begin the calibration of the comparator, R_{SETx}, and gain.
6. The CAL_MODE flag in Register 0x0D goes to Logic 1 while the device is calibrating. The CAL_FIN flag in Register 0x0E goes to Logic 1 when the calibration is complete.
7. Set the START_CAL bit in Register 0x0E to Logic 0.
8. After calibration, verify that the overflow and underflow flags in Register 0x0D are not set (Bits[14:9]). If they are, change the corresponding calibration range to the next larger range and begin again at Step 5.
9. If no flag is set, read the DACx_RSET_CAL, Bits[12:8], and DACx_GAIN_CAL values in the DACxRSET and DACxAGAIN registers, respectively, and write them into their corresponding DACxRSET and DACxAGAIN registers.
10. Reset the CAL_MODE_EN bit and the calibration clock bit, CAL_CLK_EN, in Register 0x0D to Logic 0 to disable the calibration clock.
11. Set the CAL_MODE_EN bit in Register 0x0D to Logic 0 to set the R_{SETx} and gain control muxes to normal operation mode.
12. Disable the calibration clock bit, CAL_CLK_EN, in Register 0x0D.

To reset the calibration, pulse the CAL_RESET bit in Register 0x0D to Logic 1 and Logic 0, pulse the $\overline{\text{RESET}}$ pin, or pulse the reset bit in the SPICONFIG register.

CLOCK INPUT

For optimum DAC performance, the AD9106 clock input signal pair (CLKP/CLKN) must be a very low jitter, fast rise time differential signal. The clock receiver generates its own common-mode voltage requiring these two inputs to be ac-coupled.

Figure 38 shows the recommended interface to a number of Analog Devices, Inc., low voltage differential signaling (LVDS) clock drivers that work well with the AD9106. A 100 Ω termination resistor and two 0.1 µF coupling capacitors are used. Figure 40 shows an interface to an Analog Devices differential positive emitter coupled logic (PECL) driver. Figure 41 shows a single-ended-to-differential converter using a balun driving CLKP/CLKN, the preferred methods for clocking the AD9106.

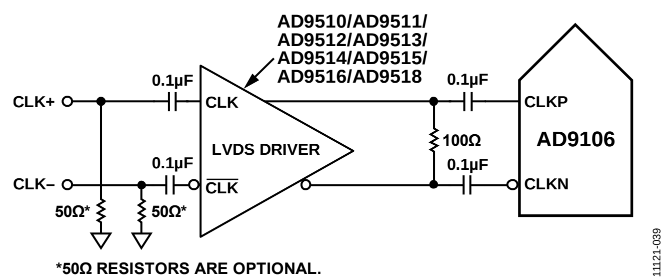


Figure 38. Differential LVDS Clock Input

In applications where the analog output signals are at low frequencies, it is acceptable to drive the AD9106 clock input with a single-ended complementary metal oxide semiconductor (CMOS) signal. Figure 39 shows such an interface. CLKP is driven directly from a CMOS gate, and the CLKN pin is bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor. The optional resistor is a series termination.

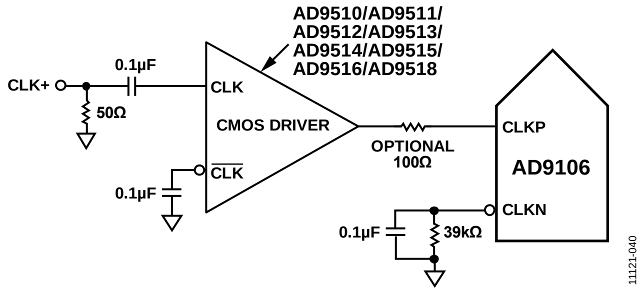


Figure 39. Single-Ended 1.8 V CMOS Sample Clock

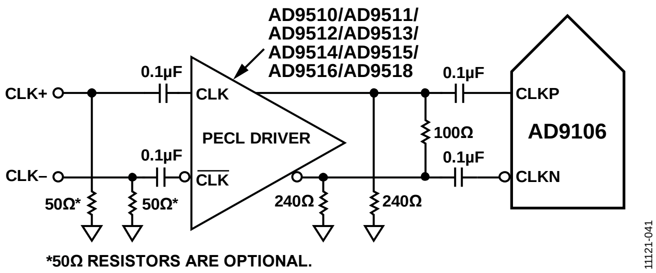


Figure 40. Differential PECL Sample Clock

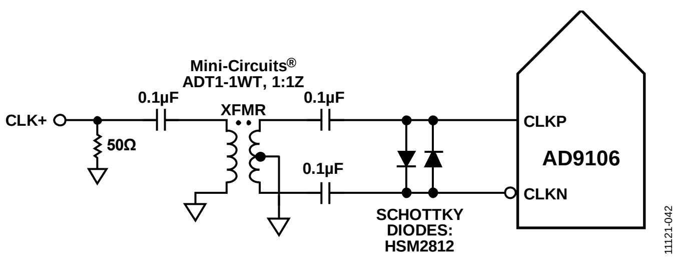


Figure 41. Transformer Coupled Clock

DAC OUTPUT CLOCK EDGE

Each of the four DACs can be configured independently to output samples on the rising or falling edge of the CLKP/CLKN clock input by configuring the DACx_INV_CLK bits in the CLOCKCONFIG register. This functionality sets the DAC output timing resolution at $1/(2 \times f_{CLKP/CLKN})$.

GENERATING SIGNAL PATTERNS

The AD9106 can generate two types of signal patterns under the control of its programmable pattern generator.

- Periodic pulse train waveforms that repeat indefinitely.
- Periodic pulse train waveforms that repeat a finite number of times.

Run Bit

Setting the run bit in the PAT_STATUS register to 1 activates the AD9106 for pattern generation. Clearing this bit shuts down the pattern generator, as shown in Figure 45.

Trigger Terminal

A falling edge on the trigger terminal starts the generation of a pattern. If the run bit is set, the falling edge of trigger starts pattern generation. As shown in Figure 43, the pattern generator state goes to pattern generator on after a number of CLKP/CLKN clock cycles following the falling edge of trigger. This delay is programmed in the PATTERN_DELAY bit field.

The rising edge on the trigger terminal is a request for the termination of pattern generation (see Figure 44).

Pattern Bit (Read Only)

The read only pattern bit in the PAT_STATUS register indicates, when set to 1, that the pattern generator is in the pattern generator on state. A 0 indicates that the pattern generator is in the pattern generator off state.

Pattern Types

- Periodic pulse trains that repeat indefinitely are waveforms that are output once during each pattern period. Pattern periods occur one after the other as long as the pattern generator is in the pattern on state.
- Periodic pulse trains that repeat a finite number of times are just like those that repeat indefinitely except that the waveforms are output during a finite number of consecutive pattern periods.

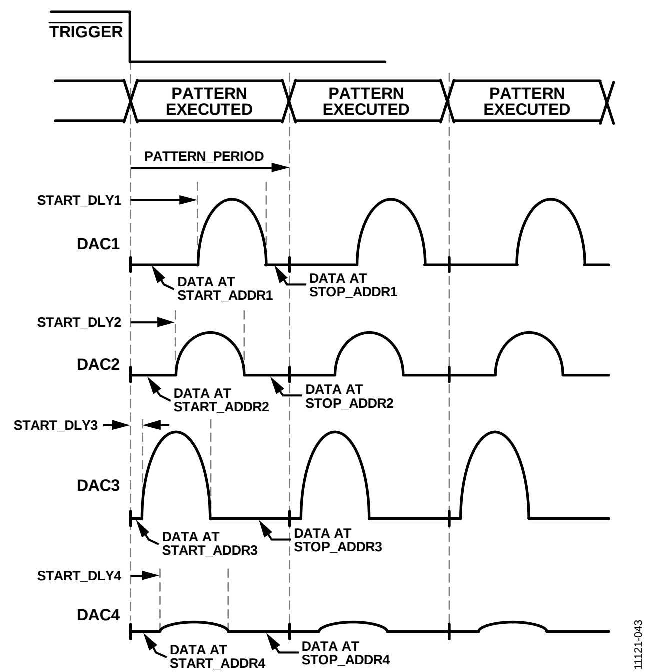


Figure 42. Periodic Pulse Trains Output on All DACx

PATTERN GENERATOR PROGRAMMING

Figure 42 shows periodic pulse train waveforms as seen at the output to each of the four DACx. The four waveforms are generated in each pattern period. Each has its own start delay (START_DLYx), a delay between the start of each pattern period and the start of the waveform. The four DACx waveforms are the same digital signal stored in SRAM and multiplied by the DACx digital gain factor. The SRAM data is read using each DACx address counter simultaneously.

Setting Pattern Period

Two register bit fields set the pattern period. The PAT_PERIOD_BASE field in the PAT_TIMEBASE register sets the number of CLKP/CLKN clocks per PATTERN_PERIOD LSB. The PATTERN_PERIOD is programmed in the PAT_PERIOD register. The longest pattern period available is 65,535 × $16/f_{CLKP/CLKN}$.

Setting Waveform Start Delay Base

The waveform start delay base is programmed in the START_DELAY_BASE field of the PAT_TIMEBASE register. Each DACx has a START_DLYx register described in the DACx Input Data Paths section. The start delay base determines how many CLKP/CLKN clock cycles there are per START_DELAYx LSB.

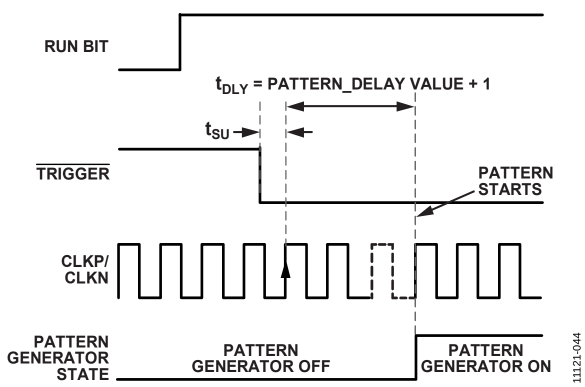


Figure 43. Trigger Initiated Pattern Start with Pattern Delay

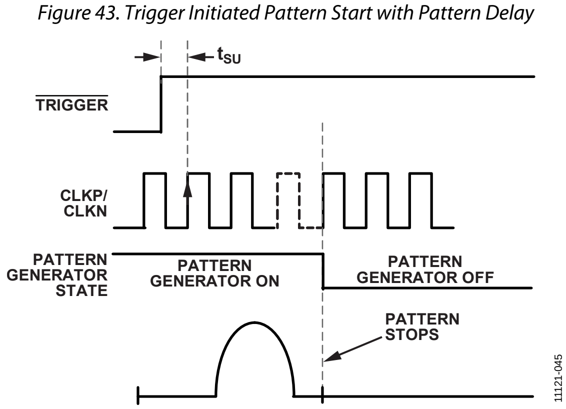


Figure 44. Trigger Rising Edge Initiated Pattern Stop

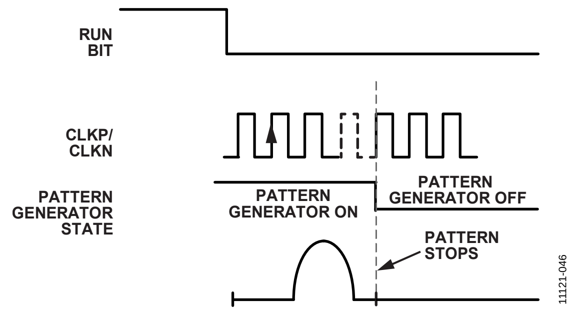


Figure 45. RUN Bit Driven Pattern Stop

DACx INPUT DATA PATHS

Each of the four DACx has its own digital data path. Timing in the DACx data paths is governed by the pattern generator. Each DACx data path includes a waveform selector, a waveform repeat controller, RAM output and DDS output multiplier (RAM output can amplitude modulate DDS output), DDSx cycle counter, DACx digital gain multiplier, and a DACx digital offset summer. DACx input data paths use a twos complement number system.

DACx Digital Gain Multiplier

On its way into each DACx, the waveform samples are multiplied by a 12-bit gain factor that has a range of ±2.0. These gain values are programmed in the DACx_DGAIN registers.

DACx Digital Offset Summer

DACx input samples are summed with a 12-bit dc offset value as well. The dc offset values are programmed in the DACxDOF registers.

DACx Waveform Selectors

Waveform selector inputs are

- DACx sawtooth generator output.
- DACx pseudorandom sequence generator output.
- DACx dc constant generator output.
- DACx pulsed, phase shifted DDS sine wave output.
- RAM output.
- DACx pulsed, phase shifted DDS sine wave output.
- Amplitude modulated by RAM output.

Waveform selection for each DACx is made by programming the WAVx_yCONFIG registers.

DACx Pattern Period Repeat Controller

The PATTERN_RPT bit in the PAT_TYPE register controls whether the pattern output automatically repeats (periodic pulse train repeats indefinitely) or repeats a number of consecutive times defined by the DACx_REPEAT_CYCLE fields. The latter are periodic pulse trains that repeat a finite number of times.

DACx, Number of DDS Cycles

Each DACx input data path establishes the pulse width of the sine wave output from the single common DDS in number of sine wave cycles. The cycle counts are programmed in the DDS_CYCx registers.

DACx DDS Phase Shift

Each DACx input data path shifts the phase of the output of the single common DDS. The phase shift is programmed using the DDSx_PHASE fields. The DDSx phase offset for each DACx data path has a range of 360° and a resolution of $360°/(2^{16} – 1)$.

DOUT FUNCTION

In applications where AD9106 DACs drive high voltage amplifiers, such as in ultrasound transducer array element driver signal chains, it can be useful to turn on and off each amplifier at precise times relative to the waveform generated by each AD9106 DAC. The SDO/SDI2/DOUT terminal can be configured to provide this function. One amplifier on/off strobe can be provided for all four DACs.

The SPI interface needs to be configured in 3-wire mode (see Figure 32 and Figure 33) by setting the SPI3WIRE or SPI3WIREM bits in the SPICONFIG register. When SPI_DRV or SPI_DRVM of the SPICONFIG register is set to Logic 1, the SDO/SDI2/DOUT terminal provides the DOUT function.

Manually Controlled DOUT

If DOUT_MODE = 0 in the DOUT_CONFIG register, DOUT can be turned on or off using the DOUT_VAL bit of that same register.

Pattern Generator Controlled DOUT

Figure 46 depicts the rising edge of a pattern generator controlled DOUT pulse. Figure 47 shows the falling edge. The pattern generator controlled DOUT pulse is set by setting DOUT_MODE = 1. Then, the start delay is programmed in the DOUT_START_DLY register and the stop delay is programmed into the DOUT_STOP field of the DOUT_CONFIG register.

DOUT goes high DOUT_START[15:0] CLKP/CLKN cycles after the falling edge of the signal input to the trigger terminal. DOUT stays high as long as a pattern is being generated. DOUT goes low DOUT_STOP[3:0] CLKP/CLKN cycles after the clock edge that causes pattern generation to stop.

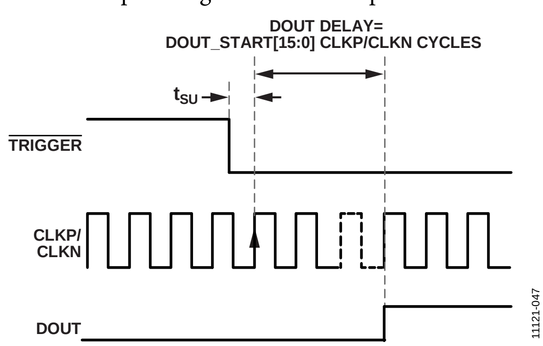


Figure 46. DOUT Start Sequence

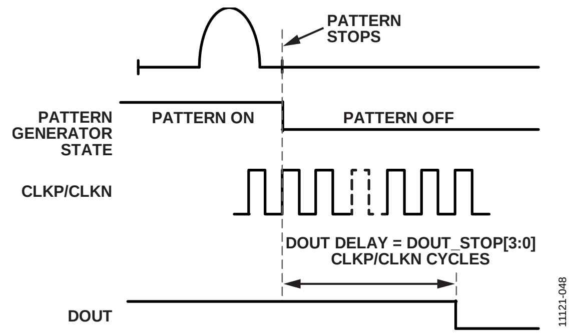


Figure 47. DOUT Stop Sequence

DIRECT DIGITAL SYNTHESIZER (DDS)

The DDS generates a single frequency sine wave that can be output on any of the four DACx. The DDS is a global shared signal resource. It can generate one sinusoid at a frequency determined by its tuning word input. The tuning word is 24 bits wide. The resolution of DDS tuning is $f_{CLKP/CLKN}/2^{24}$. The DDS output frequency is DDS_TW × $f_{CLKP/CLKN}/2^{24}$.

The DDS tuning word is programmed using one of two methods. For a fixed frequency, DDSTW_MSB and DDSTW_LSB are programmed with a constant. When the frequency of the DDS needs to change within each pattern period, a sequence of values stored in SRAM is combined with a selection of DDSTW_MSB bits to form the tuning word.

DDS Phase Offset for Each DACx

The single shared DDS has an output for each DACx data path that includes a programmable phase shifter.

SRAM

The AD9106 4096 × 12-bit SRAM can contain signal samples, amplitude modulation patterns, lists of DDS tuning words, or lists of DDS output phase offset words. Data is written to and read from the memory via the SPI port as long as the SRAM is not actively engaged in pattern generation (run = 0). To write to SRAM, set up the PAT_STATUS register as follows:

- BUF_READ = 0
- MEM_ACCESS = 1
- Run = 0

To read data from SRAM, set up the PAT_STATUS register as follows:

- BUF_READ = 1
- MEM_ACCESS = 1
- Run = 0

The SPI port address space for SRAM is Location 0x6000 through Location 0x6FFF. The SRAM SPI address autodecrements during multiple location SPI reads and writes.

SRAM can be accessed using any of the SPI operating modes shown in Figure 32 through Figure 35. Using the SPI modes of operation shown in Figure 33 and Figure 34, the entire SRAM can be written in (2 + 2 × 4096) × 8/f_{SCLK} seconds. The SRAM is a shared signal generation resource. Data from this one 4096 × 12-bit SRAM can be used to generate signals for all four DACs.

When the RUN bit = 1 (pattern generation enabled) in the PAT_STATUS register, each DACx data path has its own SRAM address counter. Each address counter has its own START_ADDRx and STOP_ADDRx. During each pattern period, data is read from RAM after the START_DELAYx period and while the each address counter is incrementing. SRAM is read simultaneously by all four DACx data paths.

The SRAM length being written must be an even number if Register 0x44, Bit 1 = 0x01. This requirement implies that the START_ADDRx and STOP_ADDRx cannot both be even or both be odd: only one of the addresses can be even, while the other address must be odd.

Clock Selection for Incrementing Pattern Generation Mode SRAM Address Counters

The DDS_MSB_ENx bits in the DDSx_CONFIG registers select the signal that clocks each address counter. When the SRAM contains waveform samples or DDS amplitude modulation samples, each of the SRAM address counters must be incremented by CLKP/CLKN (default). When the SRAM contains a list of DDS tuning words, such as when generating a chirp waveform, SRAM address counters can be incremented by CLKP/CLKN (default) or by the rising edge of the DDSx output MSB.

SAWTOOTH GENERATOR

There is a separate sawtooth signal generator for each DACx. When the sawtooth is selected in any of the PRESTORE_SELx fields in the WAV4_3CONFIG or WAV2_1 CONFIG register, the appropriate sawtooth generator is connected to the desired DACx digital data path.

Sawtooth types, shown in Figure 48, are selected using the SAW_TYPEx fields in the SAWx_yCONFIG registers. The number of samples per sawtooth waveform step is programmed in each SAW_STEPx field.

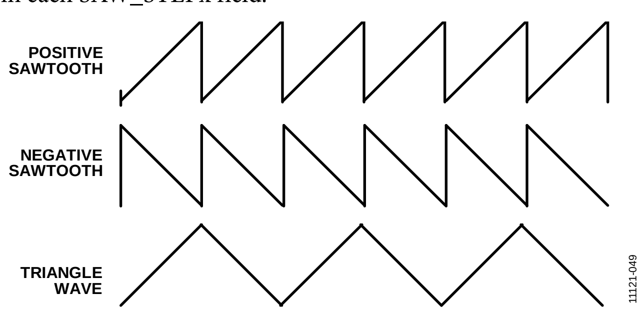


Figure 48. Sawtooth Patterns

PSEUDORANDOM SIGNAL GENERATOR

The pseudorandom noise generator generates a noise signal on each DACx output if pseudorandom sequence is selected in any of the PRESTORE_SELx fields in the WAV4_3CONFIG or WAV2_1 CONFIG register. The pseudorandom noise signals are generated as continuous waveforms only.

DC CONSTANT

A programmable dc current between 0.0 and I_{OUTFSx} can be generated on each DACx if constant value is selected in any of the PRESTORE_SELx fields of the WAV4_3CONFIG or WAV2_1 CONFIG register. DC constant currents are generated as continuous waveforms only. The dc current level is programmed by writing to the DACx_CONST field in the appropriate DACx_CST register.

POWER SUPPLY NOTES

The AD9106 supply rails are specified in Table 9. The AD9106 includes three on-chip linear regulators. The supply rails driven by these regulators operate at 1.8 V. Two usage rules for these regulators follow:

- When CLKVDD is 2.5 V or higher, the 1.8 V on-chip CLDO regulator can be used. If CLKVDD = 1.8 V, the CLDO regulator must be disabled by setting the PDN_LDO_CLK bit in the POWERCONFIG register. CLKVDD and CLDO are connected together.
- When DVDD is 2.5 V or higher, the 1.8 V on-chip DLDO1 and DLDO2 regulators can be used. If DVVD is 1.8 V, the DLDO1 and DLDO2 regulators must be disabled by setting the PDN_LDO_DIG1 and PDN_LDO_DIG2 bits in the POWERCONFIG register. DVDD, DLDO1, and DLDO2 are connected together.

POWER-DOWN CAPABILITIES

The POWERCONFIG register allows the user to place the AD9106 in a reduced power dissipation configuration while the CLKP/CLKN input is running and the power supplies are on. DAC1, DAC2, DAC3, and DAC4 can all be put to sleep by setting the DACx_SLEEP bits in the POWERCONFIG register.

Clocking of the waveform generator and the DACs can be turned off by setting the CLK_PDN bit in the CLOCKCONFIG register. Taking these actions places the AD9106 in the power-down mode specified in Table 8.

APPLICATIONS INFORMATION

SIGNAL GENERATION EXAMPLES

AD9106 waveform and pattern generation examples are provided in this section.

Figure 49 shows a different waveform being generated by each DACx. The waveforms are all stored in the 4096 × 12-bit SRAM in different segments. DACx path address counters access the SRAM simultaneously. Each waveform is repeated once during each pattern period. In each pattern period, a start delay is executed, then the pattern is read from SRAM.

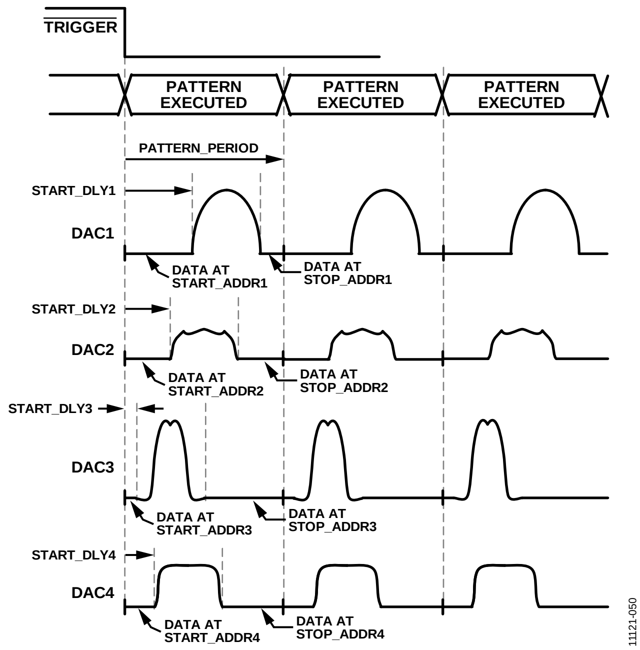


Figure 49. Pattern Using Different Waveforms Stored in SRAM

Figure 50 shows pulsed sine waves generated by each DACx. The DDS generates a sine wave at a programmed frequency. Each DACx channel is programmed with a start delay and a number of sine wave cycles to output.

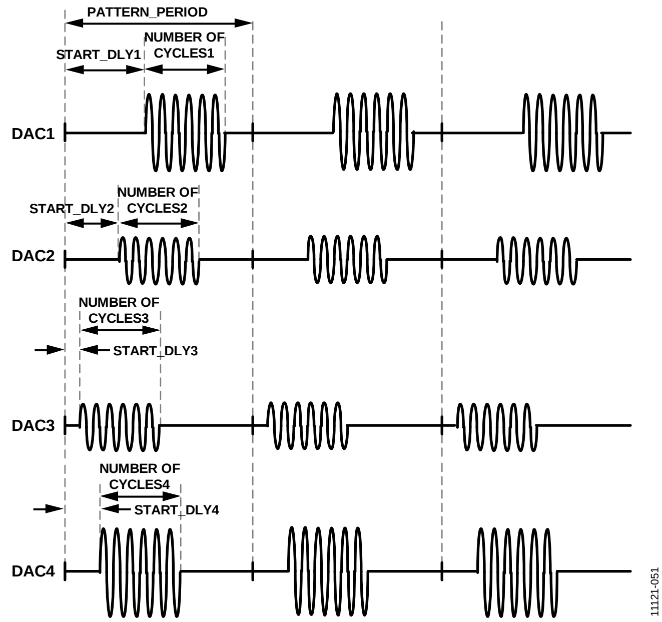


Figure 50. Pulsed Sine Waves in Pattern Periods

Figure 51 shows a pulsed sinewave generated by DAC1 and each of the three available sawtooth wave shapes generated by DAC2, DAC3, and DAC4 in successive pattern periods with start delay.

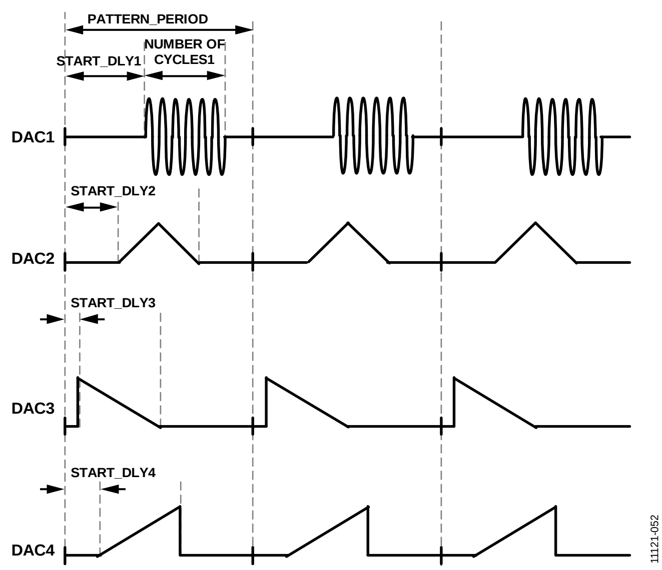


Figure 51. Pulsed Sine Waves and Sawtooth Waveforms in Pattern Periods

Figure 52 shows all DACx outputting sine waves modulated by an amplitude envelope. The sine wave is generated by the DDS, and the amplitude envelope is stored in SRAM. Different start delays and digital gain multipliers are applied by each DACx input data path.

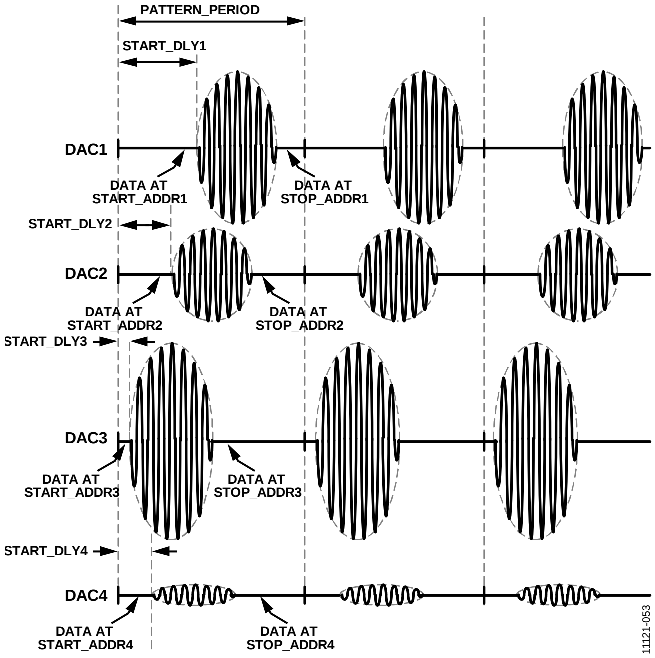


Figure 52. DDS Output Amplitude Modulated by RAM Envelope

Figure 53 and Figure 54 show the four DACs generating continuous waveforms, one with start delays, and one without.

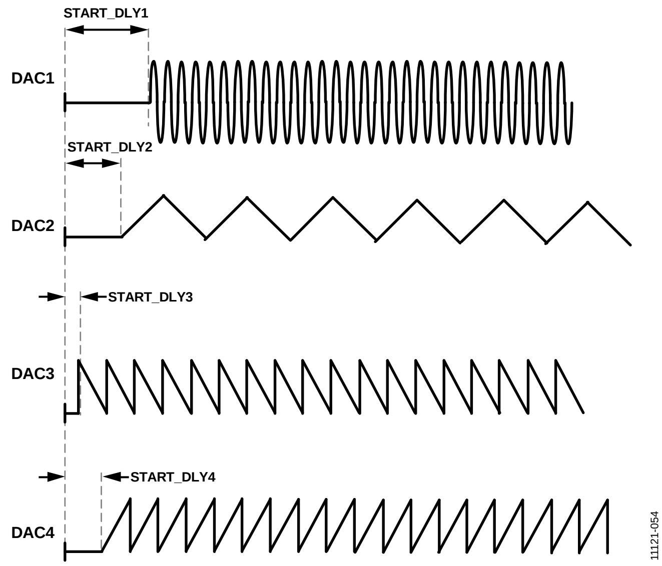


Figure 53. Waveforms with Start Delays

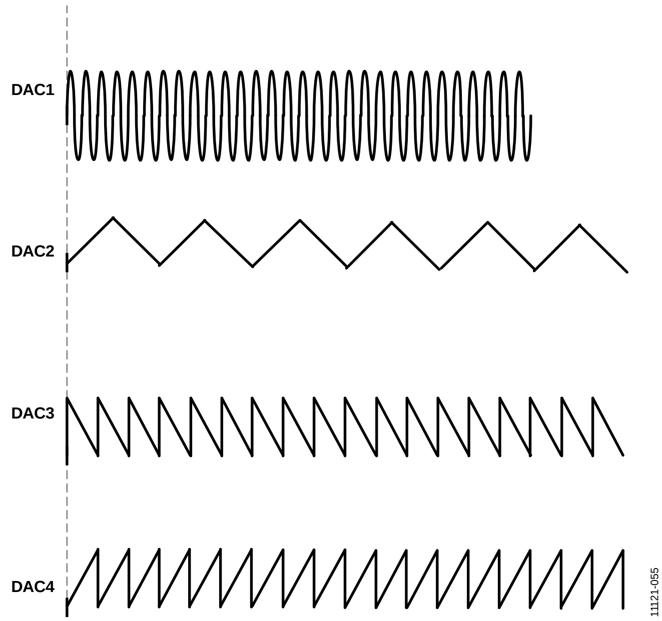
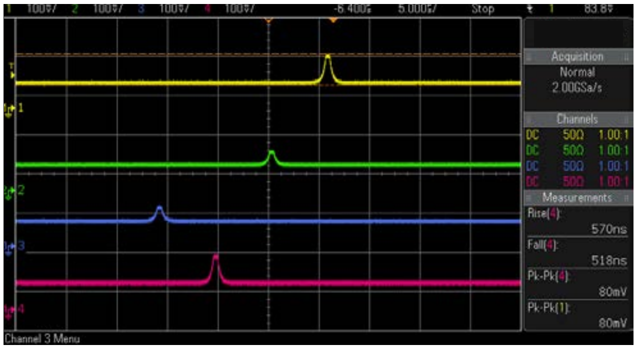


Figure 54. Waveforms Without Start Delays

WAVEFORM GENERATION SETUPS WITH READY TO USE REGISTER VALUES

Register value files and SRAM vectors can be obtained by downloading the DAC software suite from www.analog.com.

Programming Example 1: Four Gaussian Pulses with Different Start Delays and Varied Digital Gain Settings



11121-056

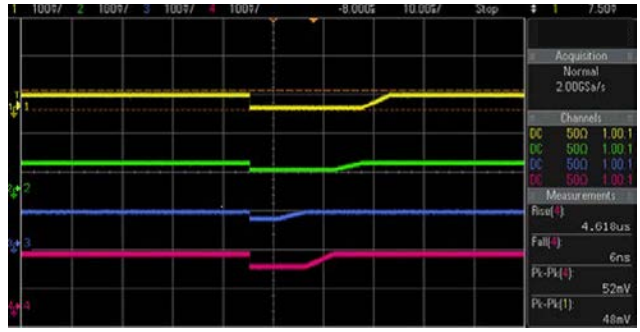
Figure 55. Programming Example 1

Table 14. Register Values for Programming Example 1

Address	Data
0x0000	0x0000
0x0001	0x0E00
0x0002	0x0000
0x0003	0x0000
0x0004	0x4000
0x0005	0x4000
0x0006	0x4000
0x0007	0x4000
0x0008	0x0000
0x0009	0x1F00
0x000A	0x1F00
0x000B	0x1F00
0x000C	0x1F00
0x000D	0x0000
0x000E	0x0000
0x000F	0x0000
0x0010	0x0000
0x0011	0x0000
0x0012	0x0000
0x0013	0x0000
0x0014	0x0000
0x0015	0x0000
0x0016	0x0000
0x0017	0x0000
0x0018	0x0000
0x0019	0x0000
0x001A	0x0000
0x001B	0x0000
0x001C	0x0000
0x001D	0x0000
0x001E	0x0000
0x001F	0x0000
0x0020	0x000E
0x0022	0x0000
0x0023	0x0000
0x0024	0x0000
0x0025	0x0000
0x0026	0x3030
0x0027	0x3030
0x0028	0x0111
0x0029	0xFFFF
0x002A	0x0101
0x002B	0x0101
0x002C	0x0003
0x002D	0x0000
0x002E	0x0000
0x002F	0x0000
0x0030	0x0000
0x0031	0x0000
0x0032	0x4000
0x0033	0x2000
0x0034	0x2000
0x0035	0x4000
0x0036	0x0001
0x0037	0x0200
0x0038	0x0000
0x0039	0x0000
0x003A	0x0000
0x003B	0x0000
0x003C	0x0000
0x003D	0x0000
0x003E	0x0000
0x003F	0x0000
0x0040	0x0000
0x0041	0x0000
0x0042	0x0000
0x0043	0x0000
0x0044	0x0000
0x0045	0x0000
0x0046	0x0000
0x0047	0x0000
0x0048	0x0000
0x0049	0x0000
0x004A	0x0000
0x004B	0x0000
0x004C	0x0000
0x004D	0x0000
0x004E	0x0000
0x004F	0x0000
0x0050	0x07D0
0x0051	0x0000
0x0052	0xFFF0
0x0053	0x0100
0x0054	0x03E8
0x0055	0x0000
0x0056	0xFFF0

Address	Data
0x0057	0x0100
0x0058	0x0BB8
0x0059	0x0000
0x005A	0xFFF0
0x005B	0x0100
0x005C	0x0FA0
0x005D	0x0000
0x005E	0xFFF0
0x005F	0x0100
0x0060	0x0000
0x0061	0x0000
0x0062	0x0000
0x0063	0x0000
0x0064	0x0000
0x0065	0x0000
0x0066	0x0000
0x0067	0x0000
0x0068	0x0000
0x0069	0x0000
0x006A	0x0000
0x006B	0x0000
0x006C	0x0000
0x006D	0x0000
0x006E	0x0000
0x006F	0x0000
0x0070	0x0000
0x0071	0x0000
0x0072	0x0000
0x0073	0x0000
0x0074	0x0000
0x0075	0x0000
0x0076	0x0000
0x0077	0x0000
0x0078	0x0000
0x0079	0x0000
0x007A	0x0000
0x007B	0x0000
0x007C	0x0000
0x007D	0x0000
0x007E	0x0000
0x007F	0x0000

Programming Example 2: Four Pulses Generated from an SRAM Vector



11121-057

Figure 56. Programming Example 2

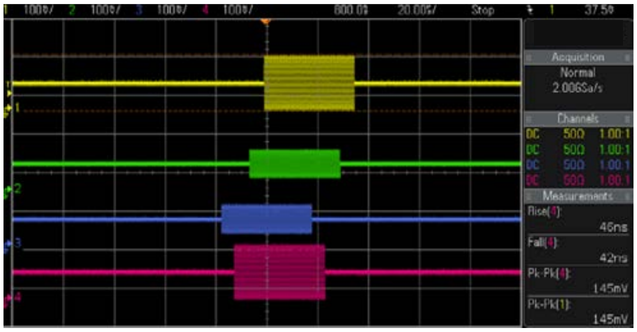
Table 15. Register Values for Programming Example 2

Address	Data
0x0000	0x0000
0x0001	0x0E00
0x0002	0x0000
0x0003	0x0000
0x0004	0x4000
0x0005	0x4000
0x0006	0x4000
0x0007	0x4000
0x0008	0x0000
0x0009	0x1F00
0x000A	0x1F00
0x000B	0x1F00
0x000C	0x1F00
0x000D	0x0000
0x000E	0x0000
0x000F	0x0000
0x0010	0x0000
0x0011	0x0000
0x0012	0x0000
0x0013	0x0000
0x0014	0x0000
0x0015	0x0000
0x0016	0x0000
0x0017	0x0000
0x0018	0x0000
0x0019	0x0000
0x001A	0x0000
0x001B	0x0000
0x001C	0x0000
0x001D	0x0000
0x001E	0x0000
0x001F	0x0000
0x0020	0x000E
0x0022	0x0000
0x0023	0x0000
0x0024	0x0000
0x0025	0x0000
0x0026	0x3030

Address	Data
0x0027	0x3030
0x0028	0x0111
0x0029	0xFFFF
0x002A	0x0101
0x002B	0x0101
0x002C	0x0003
0x002D	0x0000
0x002E	0x0000
0x002F	0x0000
0x0030	0x0000
0x0031	0x0000
0x0032	0x4000
0x0033	0x2000
0x0034	0x2000
0x0035	0x4000
0x0036	0x0001
0x0037	0x0200
0x0038	0x0000
0x0039	0x0000
0x003A	0x0000
0x003B	0x0000
0x003C	0x0000
0x003D	0x0000
0x003E	0x0000
0x003F	0x0000
0x0040	0x0000
0x0041	0x0000
0x0042	0x0000
0x0043	0x0000
0x0044	0x0000
0x0045	0x0000
0x0046	0x0000
0x0047	0x0000
0x0048	0x0000
0x0049	0x0000
0x004A	0x0000
0x004B	0x0000
0x004C	0x0000
0x004D	0x0000
0x004E	0x0000
0x004F	0x0000
0x0050	0x07D0
0x0051	0xC000
0x0052	0xFFF0
0x0053	0x0100

Address	Data
0x0054	0x03E8
0x0055	0x8000
0x0056	0xBFF0
0x0057	0x0100
0x0058	0x0BB8
0x0059	0x3FF0
0x005A	0x7FF0
0x005B	0x0100
0x005C	0x0FA0
0x005D	0x0000
0x005E	0x3FF0
0x005F	0x0100
0x0060	0x0000
0x0061	0x0000
0x0062	0x0000
0x0063	0x0000
0x0064	0x0000
0x0065	0x0000
0x0066	0x0000
0x0067	0x0000
0x0068	0x0000
0x0069	0x0000
0x006A	0x0000
0x006B	0x0000
0x006C	0x0000
0x006D	0x0000
0x006E	0x0000
0x006F	0x0000
0x0070	0x0000
0x0071	0x0000
0x0072	0x0000
0x0073	0x0000
0x0074	0x0000
0x0075	0x0000
0x0076	0x0000
0x0077	0x0000
0x0078	0x0000
0x0079	0x0000
0x007A	0x0000
0x007B	0x0000
0x007C	0x0000
0x007D	0x0000
0x007E	0x0000
0x007F	0x0000

Programming Example 3: Four Pulsed Sine Waves with Different Start Delays and Varied Digital Gain Settings Generated by DDS



11121-058

Figure 57. Programming Example 3

Table 16. Register Values for Programming Example 3

Address	Data
0x0000	0x0000
0x0001	0x0E00
0x0002	0x0000
0x0003	0x0000
0x0004	0x4000
0x0005	0x4000
0x0006	0x4000
0x0007	0x4000
0x0008	0x0000
0x0009	0x1F00
0x000A	0x1F00
0x000B	0x1F00
0x000C	0x1F00
0x000D	0x0000
0x000E	0x0000
0x000F	0x0000
0x0010	0x0000
0x0011	0x0000
0x0012	0x0000
0x0013	0x0000
0x0014	0x0000
0x0015	0x0000
0x0016	0x0000
0x0017	0x0000
0x0018	0x0000
0x0019	0x0000
0x001A	0x0000
0x001B	0x0000
0x001C	0x0000
0x001D	0x0000
0x001E	0x0000
0x001F	0x0000
0x0020	0x000E
0x0022	0x0000
0x0023	0x0000
0x0024	0x0000
0x0025	0x0000
0x0026	0x3232
0x0027	0x3232
0x0028	0x0111
0x0029	0xFFFF
0x002A	0x0101
0x002B	0x0101
0x002C	0x0003
0x002D	0x0000
0x002E	0x0000
0x002F	0x0000
0x0030	0x0000
0x0031	0x0000
0x0032	0x4000
0x0033	0x2000
0x0034	0x2000
0x0035	0x4000
0x0036	0x0001
0x0037	0x0200
0x0038	0x0000
0x0039	0x0000
0x003A	0x0000
0x003B	0x0000
0x003C	0x0000
0x003D	0x0000
0x003E	0x0A3D
0x003F	0x7100
0x0040	0x0000
0x0041	0x0000
0x0042	0x0000
0x0043	0x0000
0x0044	0x0000
0x0045	0x0000
0x0046	0x0000
0x0047	0x0000
0x0048	0x0000
0x0049	0x0000
0x004A	0x0000
0x004B	0x0000
0x004C	0x0000
0x004D	0x0000
0x004E	0x0000
0x004F	0x0000
0x0050	0x07D0
0x0051	0x0000
0x0052	0x0000
0x0053	0x0100
0x0054	0x03E8
0x0055	0x0000
0x0056	0x0000
0x0057	0x0100
0x0058	0x0BB8
0x0059	0x0000
0x005A	0x0000
0x005B	0x0100

Address	Data
0x005C	0x0FA0
0x005D	0x0000
0x005E	0x0000
0x005F	0x0100
0x0060	0x0004
0x0061	0x0000
0x0062	0x0000
0x0063	0x0000
0x0064	0x0000
0x0065	0x0000
0x0066	0x0000
0x0067	0x0000
0x0068	0x0000
0x0069	0x0000
0x006A	0x0000
0x006B	0x0000
0x006C	0x0000
0x006D	0x0000
0x006E	0x0000
0x006F	0x0000
0x0070	0x0000
0x0071	0x0000
0x0072	0x0000
0x0073	0x0000
0x0074	0x0000
0x0075	0x0000
0x0076	0x0000
0x0077	0x0000
0x0078	0x0000
0x0079	0x0000
0x007A	0x0000
0x007B	0x0000
0x007C	0x0000
0x007D	0x0000
0x007E	0x0000
0x007F	0x0000

Programming Example 4: Pulsed Sine Wave from DDS and Three Sawtooth Generator Waveforms

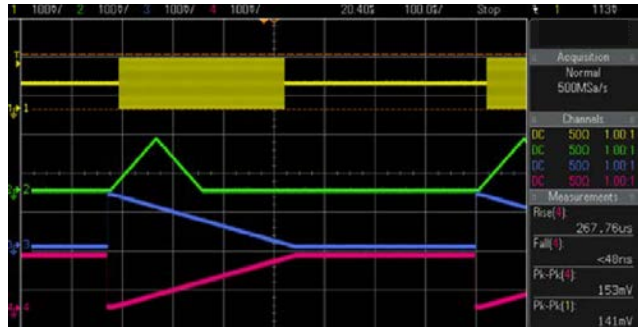


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Figure 58. Programming Example 4

Table 17. Register Values for Programming Example 4

Address	Data
0x0000	0x0000
0x0001	0x0E00
0x0002	0x0000
0x0003	0x0000
0x0004	0x4000
0x0005	0x4000
0x0006	0x4000
0x0007	0x4000
0x0008	0x0000
0x0009	0x1F00
0x000A	0x1F00
0x000B	0x1F00
0x000C	0x1F00
0x000D	0x0000
0x000E	0x0000
0x000F	0x0000
0x0010	0x0000
0x0011	0x0000
0x0012	0x0000
0x0013	0x0000
0x0014	0x0000
0x0015	0x0000
0x0016	0x0000
0x0017	0x0000
0x0018	0x0000
0x0019	0x0000
0x001A	0x0000
0x001B	0x0000
0x001C	0x0000
0x001D	0x0000
0x001E	0x0000
0x001F	0x0000
0x0020	0x000E
0x0022	0x0000
0x0023	0x0000
0x0024	0x0000
0x0025	0x0000
0x0026	0x1212

Address	Data
0x0027	0x1232
0x0028	0x0121
0x0029	0xFFFF
0x002A	0x0101
0x002B	0x0101
0x002C	0x0003
0x002D	0x0000
0x002E	0x0000
0x002F	0x0000
0x0030	0x0000
0x0031	0x0000
0x0032	0x4000
0x0033	0x4000
0x0034	0x4000
0x0035	0x4000
0x0036	0x1011
0x0037	0x0600
0x0038	0x0000
0x0039	0x0000
0x003A	0x0000
0x003B	0x0000
0x003C	0x0000
0x003D	0x0000
0x003E	0x1999
0x003F	0x9A00
0x0040	0x0000
0x0041	0x0000
0x0042	0x0000
0x0043	0x0000
0x0044	0x0000
0x0045	0x0000
0x0046	0x0000
0x0047	0x0000
0x0048	0x0000
0x0049	0x0000
0x004A	0x0000
0x004B	0x0000
0x004C	0x0000
0x004D	0x0000
0x004E	0x0000
0x004F	0x0000
0x0050	0x07D0
0x0051	0x0000
0x0052	0x0000
0x0053	0x0001

Address	Data
0x0054	0x03E8
0x0055	0x0000
0x0056	0x0000
0x0057	0x0001
0x0058	0x03E8
0x0059	0x0000
0x005A	0x0000
0x005B	0x0001
0x005C	0x0FA0
0x005D	0x0000
0x005E	0x0000
0x005F	0x16FF
0x0060	0x0004
0x0061	0x0000
0x0062	0x0000
0x0063	0x0000
0x0064	0x0000
0x0065	0x0000
0x0066	0x0000
0x0067	0x0000
0x0068	0x0000
0x0069	0x0000
0x006A	0x0000
0x006B	0x0000
0x006C	0x0000
0x006D	0x0000
0x006E	0x0000
0x006F	0x0000
0x0070	0x0000
0x0071	0x0000
0x0072	0x0000
0x0073	0x0000
0x0074	0x0000
0x0075	0x0000
0x0076	0x0000
0x0077	0x0000
0x0078	0x0000
0x0079	0x0000
0x007A	0x0000
0x007B	0x0000
0x007C	0x0000
0x007D	0x0000
0x007E	0x0000
0x007F	0x0000

Programming Example 5: Pulsed Sine Waves from DDS Amplitude Modulated by an SRAM Vector

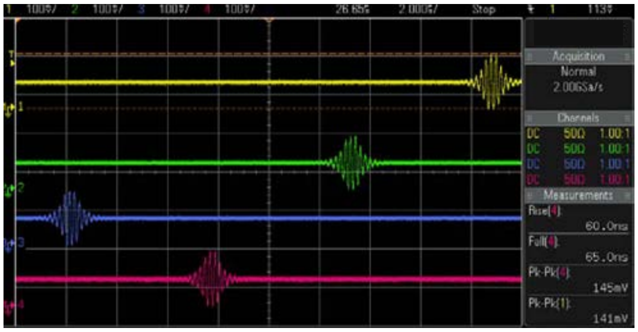

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Figure 59. Programming Example 5

Table 18. Register Values for Programming Example 5

Address	Data
0x0000	0x0000
0x0001	0x0E00
0x0002	0x0000
0x0003	0x0000
0x0004	0x4000
0x0005	0x4000
0x0006	0x4000
0x0007	0x4000
0x0008	0x0000
0x0009	0x1F00
0x000A	0x1F00
0x000B	0x1F00
0x000C	0x1F00
0x000D	0x0000
0x000E	0x0000
0x000F	0x0000
0x0010	0x0000
0x0011	0x0000
0x0012	0x0000
0x0013	0x0000
0x0014	0x0000
0x0015	0x0000
0x0016	0x0000
0x0017	0x0000
0x0018	0x0000
0x0019	0x0000
0x001A	0x0000
0x001B	0x0000
0x001C	0x0000
0x001D	0x0000
0x001E	0x0000
0x001F	0x0000
0x0020	0x000E
0x0022	0x0000
0x0023	0x0000
0x0024	0x0000
0x0025	0x0000
0x0026	0x3333
0x0027	0x3333
0x0028	0x0111
0x0029	0xFFFF
0x002A	0x0101
0x002B	0x0101
0x002C	0x0003
0x002D	0x0000
0x002E	0x0000
0x002F	0x0000
0x0030	0x0000
0x0031	0x0000
0x0032	0x4000
0x0033	0x4000
0x0034	0x4000
0x0035	0x4000
0x0036	0x0001
0x0037	0x0200
0x0038	0x0000
0x0039	0x0000
0x003A	0x0000
0x003B	0x0000
0x003C	0x0000
0x003D	0x0000
0x003E	0x0750
0x003F	0x7500
0x0040	0x0000
0x0041	0x0000
0x0042	0x0000
0x0043	0x0000
0x0044	0x0000
0x0045	0x0000
0x0046	0x0000
0x0047	0x0000
0x0048	0x0000
0x0049	0x0000
0x004A	0x0000
0x004B	0x0000
0x004C	0x0000
0x004D	0x0000
0x004E	0x0000
0x004F	0x0000
0x0050	0x07D0
0x0051	0x0000
0x0052	0xFFF0
0x0053	0x0100
0x0054	0x03E8
0x0055	0x0000
0x0056	0xFFF0
0x0057	0x0100
0x0058	0x0BB8
0x0059	0x0000
0x005A	0xFFF0
0x005B	0x0100

Address	Data
0x005C	0x0FA0
0x005D	0x0000
0x005E	0xFFF0
0x005F	0x0100
0x0060	0x0005
0x0061	0x0000
0x0062	0x0000
0x0063	0x0000
0x0064	0x0000
0x0065	0x0000
0x0066	0x0000
0x0067	0x0000
0x0068	0x0000
0x0069	0x0000
0x006A	0x0000
0x006B	0x0000
0x006C	0x0000
0x006D	0x0000
0x006E	0x0000
0x006F	0x0000
0x0070	0x0000
0x0071	0x0000
0x0072	0x0000
0x0073	0x0000
0x0074	0x0000
0x0075	0x0000
0x0076	0x0000
0x0077	0x0000
0x0078	0x0000
0x0079	0x0000
0x007A	0x0000
0x007B	0x0000
0x007C	0x0000
0x007D	0x0000
0x007E	0x0000
0x007F	0x0000

Programming Example 6: Sine Wave from DDS and Three Sawtooth Waveforms

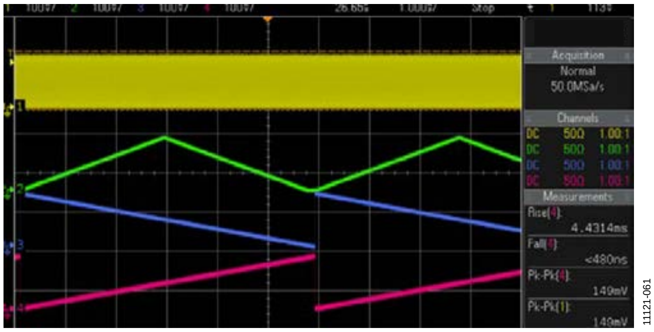

Figure 60. Programming Example 6

Table 19. Register Values for Programming Example 6

Address	Data
0x0000	0x0000
0x0001	0x0E00
0x0002	0x0000
0x0003	0x0000
0x0004	0x4000
0x0005	0x4000
0x0006	0x4000
0x0007	0x4000
0x0008	0x0000
0x0009	0x1F00
0x000A	0x1F00
0x000B	0x1F00
0x000C	0x1F00
0x000D	0x0000
0x000E	0x0000
0x000F	0x0000
0x0010	0x0000
0x0011	0x0000
0x0012	0x0000
0x0013	0x0000
0x0014	0x0000
0x0015	0x0000
0x0016	0x0000
0x0017	0x0000
0x0018	0x0000
0x0019	0x0000
0x001A	0x0000
0x001B	0x0000
0x001C	0x0000
0x001D	0x0000
0x001E	0x0000
0x001F	0x0000
0x0020	0x000E
0x0022	0x0000
0x0023	0x0000
0x0024	0x0000
0x0025	0x0000
0x0026	0x3333

Address	Data
0x0027	0x3333
0x0028	0x0111
0x0029	0xFFFF
0x002A	0x0101
0x002B	0x0101
0x002C	0x0003
0x002D	0x0000
0x002E	0x0000
0x002F	0x0000
0x0030	0x0000
0x0031	0x0000
0x0032	0x4000
0x0033	0x4000
0x0034	0x4000
0x0035	0x4000
0x0036	0x0001
0x0037	0x0200
0x0038	0x0000
0x0039	0x0000
0x003A	0x0000
0x003B	0x0000
0x003C	0x0000
0x003D	0x0000
0x003E	0x0750
0x003F	0x7500
0x0040	0x0000
0x0041	0x0000
0x0042	0x0000
0x0043	0x0000
0x0044	0x0000
0x0045	0x0000
0x0046	0x0000
0x0047	0x0000
0x0048	0x0000
0x0049	0x0000
0x004A	0x0000
0x004B	0x0000
0x004C	0x0000
0x004D	0x0000
0x004E	0x0000
0x004F	0x0000
0x0050	0x07D0
0x0051	0x0000
0x0052	0xFFF0
0x0053	0x0100

Address	Data
0x0054	0x03E8
0x0055	0x0000
0x0056	0xFFF0
0x0057	0x0100
0x0058	0x0BB8
0x0059	0x0000
0x005A	0xFFF0
0x005B	0x0100
0x005C	0x0FA0
0x005D	0x0000
0x005E	0xFFF0
0x005F	0x0100
0x0060	0x0005
0x0061	0x0000
0x0062	0x0000
0x0063	0x0000
0x0064	0x0000
0x0065	0x0000
0x0066	0x0000
0x0067	0x0000
0x0068	0x0000
0x0069	0x0000
0x006A	0x0000
0x006B	0x0000
0x006C	0x0000
0x006D	0x0000
0x006E	0x0000
0x006F	0x0000
0x0070	0x0000
0x0071	0x0000
0x0072	0x0000
0x0073	0x0000
0x0074	0x0000
0x0075	0x0000
0x0076	0x0000
0x0077	0x0000
0x0078	0x0000
0x0079	0x0000
0x007A	0x0000
0x007B	0x0000
0x007C	0x0000
0x007D	0x0000
0x007E	0x0000
0x007F	0x0000

REGISTER MAP

Table 20. Register Summary

Addr (Hex)	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	SPICONFIG	[15:8]	LSBFIRST	SPI3WIRE	RESET	DOUBLESPI	SPI_DRV	DOUT_EN	RESERVED[3:2]		0x00	RW
		[7:0]	RESERVED[1:0]		DOUT_ENM	SPI_DRVM	DOUBLESPIM	RESETM	SPI3WIREM	LSBFIRSTM		
0x01	POWERCONFIG	[15:8]	RESERVED				CLK_LDO_STAT	DIG1_LDO_STAT	DIG2_LDO_STAT	PDN_LDO_CLK	0x00	RW
		[7:0]	PDN_LDO_DIG1	PDN_LDO_DIG2	REF_PDN	REF_EXT	DAC1_SLEEP	DAC2_SLEEP	DAC3_SLEEP	DAC4_SLEEP		
0x02	CLOCKCONFIG	[15:8]	RESERVED[15:12]				DIS_CLK1	DIS_CLK2	DIS_CLK3	DIS_CLK4	0x00	RW
		[7:0]	DIS_DCLK	CLK_SLEEP	CLK_PDN	EPS	DAC1_INV_CLK	DAC2_INV_CLK	DAC3_INV_CLK	DAC4_INV_CLK		
0x03	REFADJ	[15:8]	RESERVED[9:2]								0x00	RW
		[7:0]	RESERVED[1:0]		BGDR							
0x04	DAC4AGAIN	[15:8]	RESERVED	DAC4_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC4_GAIN								
0x05	DAC3AGAIN	[15:8]	RESERVED	DAC3_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC3_GAIN								
0x06	DAC2AGAIN	[15:8]	RESERVED	DAC2_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC2_GAIN								
0x07	DAC1AGAIN	[15:8]	RESERVED	DAC1_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC1_GAIN								
0x08	DACxRANGE	[15:8]	RESERVED								0x00	RW
		[7:0]	DAC4_GAIN_RNG		DAC3_GAIN_RNG		DAC2_GAIN_RNG		DAC1_GAIN_RNG			
0x09	DAC4RSET	[15:8]	DAC4_RSET_EN	RESERVED		DAC4_RSET_CAL					0x000A	RW
		[7:0]	RESERVED			DAC4_RSET						
0x0A	DAC3RSET	[15:8]	DAC3_RSET_EN	RESERVED		DAC3_RSET_CAL					0x000A	RW
		[7:0]	RESERVED			DAC3_RSET						
0x0B	DAC2RSET	[15:8]	DAC2_RSET_EN	RESERVED		DAC2_RSET_CAL					0x000A	RW
		[7:0]	RESERVED			DAC2_RSET						
0x0C	DAC1RSET	[15:8]	DAC1_RSET_EN	RESERVED		DAC1_RSET_CAL					0x000A	RW
		[7:0]	RESERVED			DAC1_RSET						
0x0D	CALCONFIG	[15:8]	RESERVED	COMP_OFFSET_OF	COMP_OFFSET_UF	RSET_CAL_OF	RSET_CAL_UF	GAIN_CAL_OF	GAIN_CAL_UF	CAL_RESET	0x00	RW
		[7:0]	CAL_MODE	CAL_MODE_EN	COMP_CAL_RNG		CAL_CLK_EN	CAL_CLK_DIV				
0x0E	COMPOFFSET	[15:8]	RESERVED	COMP_OFFSET_CAL							0x00	RW
		[7:0]	RESERVED						CAL_FIN	START_CAL		
0x1D	RAMUPDATE	[15:8]	RESERVED[14:7]								0x00	RW
		[7:0]	RESERVED[6:0]							RAMUPDATE		
0x1E	PAT_STATUS	[15:8]	RESERVED[11:4]								0x00	RW
		[7:0]	RESERVED[3:0]				BUF_READ	MEM_ACCESS	PATTERN	RUN		
0x1F	PAT_TYPE	[15:8]	RESERVED[14:7]								0x00	RW
		[7:0]	RESERVED[6:0]							PATTERN_RPT		
0x20	PATTERN_DLY	[15:8]	PATTERN_DELAY[15:8]								0x000E	RW
		[7:0]	PATTERN_DELAY[7:0]									
0x22	DAC4DOF	[15:8]	DAC4_DIG_OFFSET[11:4]								0x00	RW
		[7:0]	DAC4_DIG_OFFSET[3:0]				RESERVED					
0x23	DAC3DOF	[15:8]	DAC3_DIG_OFFSET[11:4]								0x00	RW
		[7:0]	DAC3_DIG_OFFSET[3:0]				RESERVED					
0x24	DAC2DOF	[15:8]	DAC2_DIG_OFFSET[11:4]								0x00	RW
		[7:0]	DAC2_DIG_OFFSET[3:0]				RESERVED					
0x25	DAC1DOF	[15:8]	DAC1_DIG_OFFSET[11:4]								0x00	RW
		[7:0]	DAC1_DIG_OFFSET[3:0]				RESERVED					
0x26	WAV4_3CONFIG	[15:8]	RESERVED		PRESTORE_SEL4		RESERVED		WAVE_SEL4		0000	RW
		[7:0]	RESERVED		PRESTORE_SEL3		RESERVED		WAVE_SEL3			
0x27	WAV2_1CONFIG	[15:8]	RESERVED		PRESTORE_SEL2		MASK_DAC4	CH2_ADD	WAVE_SEL2		0x00	RW
		[7:0]	RESERVED		PRESTORE_SEL1		MASK_DAC3	CH1_ADD	WAVE_SEL1			

Addr (Hex)	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	$R\overline{W}$
0x28	PAT_TIMEBASE	[15:8]	RESERVED				HOLD				0x0111	$R\overline{W}$
		[7:0]	PAT_PERIOD_BASE				START_DELAY_BASE					
0x29	PAT_PERIOD	[15:8]	PATTERN_PERIOD[15:8]								0x8000	$R\overline{W}$
		[7:0]	PATTERN_PERIOD[7:0]									
0x2A	DAC4_3PATx	[15:8]	DAC4_REPEAT_CYCLE								0x0101	$R\overline{W}$
		[7:0]	DAC3_REPEAT_CYCLE									
0x2B	DAC2_1PATx	[15:8]	DAC2_REPEAT_CYCLE								0x0101	$R\overline{W}$
		[7:0]	DAC1_REPEAT_CYCLE									
0x2C	DOUT_START _DLY	[15:8]	DOUT_START[15:8]								0x0003	$R\overline{W}$
		[7:0]	DOUT_START[7:0]									
0x2D	DOUT_CONFIG	[15:8]	RESERVED[9:2]								0x00	$R\overline{W}$
		[7:0]	RESERVED[1:0]		DOUT_VAL	DOUT_MODE	DOUT_STOP					
0x2E	DAC4_CST	[15:8]	DAC4_CONST[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC4_CONST[3:0]				RESERVED					
0x2F	DAC3_CST	[15:8]	DAC3_CONST[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC3_CONST[3:0]				RESERVED					
0x30	DAC2_CST	[15:8]	DAC2_CONST[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC2_CONST[3:0]				RESERVED					
0x31	DAC1_CST	[15:8]	DAC1_CONST[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC1_CONST[3:0]				RESERVED					
0x32	DAC4_DGAIN	[15:8]	DAC4_DIG_GAIN[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC4_DIG_GAIN[3:0]				RESERVED					
0x33	DAC3_DGAIN	[15:8]	DAC3_DIG_GAIN[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC3_DIG_GAIN[3:0]				RESERVED					
0x34	DAC2_DGAIN	[15:8]	DAC2_DIG_GAIN[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC2_DIG_GAIN[3:0]				RESERVED					
0x35	DAC1_DGAIN	[15:8]	DAC1_DIG_GAIN[11:4]								0x00	$R\overline{W}$
		[7:0]	DAC1_DIG_GAIN[3:0]				RESERVED					
0x36	SAW4_3CONFIG	[15:8]	SAW_STEP4						SAW_TYPE4		0x00	$R\overline{W}$
		[7:0]	SAW_STEP3						SAW_TYPE3			
0x37	SAW2_1CONFIG	[15:8]	SAW_STEP2						SAW_TYPE2		0x00	$R\overline{W}$
		[7:0]	SAW_STEP1						SAW_TYPE1			
0x38 to 0x3D	RESERVED		RESERVED									
0x3E	DDS_TW32	[15:8]	DDSTW_MSB[15:8]								0x00	$R\overline{W}$
		[7:0]	DDSTW_MSB[7:0]									
0x3F	DDS_TW1	[15:8]	DDSTW_LSB								0x00	$R\overline{W}$
		[7:0]	RESERVED									
0x40	DDS4_PW	[15:8]	DDS4_PHASE[15:8]								0x00	$R\overline{W}$
		[7:0]	DDS4_PHASE[7:0]									
0x41	DDS3_PW	[15:8]	DDS3_PHASE[15:8]								0x00	$R\overline{W}$
		[7:0]	DDS3_PHASE[7:0]									
0x42	DDS2_PW	[15:8]	DDS2_PHASE[15:8]								0x00	$R\overline{W}$
		[7:0]	DDS2_PHASE[7:0]									
0x43	DDS1_PW	[15:8]	DDS1_PHASE[15:8]								0x00	$R\overline{W}$
		[7:0]	DDS1_PHASE[7:0]									
0x44	TRIG_TW_SEL	[15:8]	RESERVED[13:6]								0x00	$R\overline{W}$
		[7:0]	RESERVED[5:0]						TRIG_DELAY_EN	RESERVED		
0x45	DDSx_CONFIG	[15:8]	DDS_COS_EN4	DDS_MSB_EN4	RESERVED		DDS_COS_EN3	DDS_MSB_EN3	PHASE_MEM_EN3	RESERVED	0x00	$R\overline{W}$
		[7:0]	DDS_COS_EN2	DDS_MSB_EN2	RESERVED		DDS_COS_EN1	DDS_MSB_EN1	RESERVED	TW_MEM_EN		
0x47	TW_RAM _CONFIG	[15:8]	RESERVED				RESERVED				0x00	$R\overline{W}$
		[7:0]	RESERVED			TW_MEM_SHIFT						

Addr (Hex)	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	$R\overline{W}$
0x50	START_DLY4	[15:8]	START_DELAY4[15:8]								0x00	$R\overline{W}$
		[7:0]	START_DELAY4[7:0]									
0x51	START_ADDR4	[15:8]	START_ADDR4[11:4]								0x00	$R\overline{W}$
		[7:0]	START_ADDR4[3:0]				RESERVED					
0x52	STOP_ADDR4	[15:8]	STOP_ADDR4[11:4]								0x00	$R\overline{W}$
		[7:0]	STOP_ADDR4[3:0]				RESERVED					
0x53	DDS_CYC4	[15:8]	DDS_CYC4[15:8]								0x0001	$R\overline{W}$
		[7:0]	DDS_CYC4[7:0]									
0x54	START_DLY3	[15:8]	START_DELAY3[15:8]								0x00	$R\overline{W}$
		[7:0]	START_DELAY3[7:0]									
0x55	START_ADDR3	[15:8]	START_ADDR3[11:4]								0x00	$R\overline{W}$
		[7:0]	START_ADDR3[3:0]				RESERVED					
0x56	STOP_ADDR3	[15:8]	STOP_ADDR3[11:4]								0x00	$R\overline{W}$
		[7:0]	STOP_ADDR3[3:0]				RESERVED					
0x57	DDS_CYC3	[15:8]	DDS_CYC3[15:8]								0x0001	$R\overline{W}$
		[7:0]	DDS_CYC3[7:0]									
00x58	START_DLY2	[15:8]	START_DELAY2[15:8]								0x00	$R\overline{W}$
		[7:0]	START_DELAY2[7:0]									
0x59	START_ADDR2	[15:8]	START_ADDR2[11:4]								0x00	$R\overline{W}$
		[7:0]	START_ADDR2[3:0]				RESERVED					
0x5A	STOP_ADDR2	[15:8]	STOP_ADDR2[11:4]								0x00	$R\overline{W}$
		[7:0]	STOP_ADDR2[3:0]				RESERVED					
0x5B	DDS_CYC2	[15:8]	DDS_CYC2[15:8]								0x0001	$R\overline{W}$
		[7:0]	DDS_CYC2[7:0]									
0x5C	START_DLY1	[15:8]	START_DELAY1[15:8]								0x00	$R\overline{W}$
		[7:0]	START_DELAY1[7:0]									
0x5D	START_ADDR1	[15:8]	START_ADDR1[11:4]								0x00	$R\overline{W}$
		[7:0]	START_ADDR1[3:0]				RESERVED					
0x5E	STOP_ADDR1	[15:8]	STOP_ADDR1[11:4]								0x00	$R\overline{W}$
		[7:0]	STOP_ADDR1[3:0]				RESERVED					
00x5F	DDS_CYC1	[15:8]	DDS_CYC1[15:8]								0x0001	$R\overline{W}$
		[7:0]	DDS_CYC1[7:0]									
00x60	CFG_ERROR	[15:8]	ERROR_CLEAR	RESERVED[8:2]							0x00	R
		[7:0]	RESERVED[1:0]		DOUT_START_LG_ERR	PAT_DLY_SHORT_ERR	DOUT_START_SHORT_ERR	PERIOD_SHORT_ERR	ODD_ADDR_ERR	MEM_READ_ERR		
0x6000 to 0x6FFF	SRAM_DATA	[15:8]	SRAM_DATA[11:4]								0x0000	$R\overline{W}$
		[7:0]	SRAM_DATA[3:0]				RESERVED					

REGISTER DESCRIPTIONS

SPI Control Register (SPICONFIG, Address 0x00)

Table 21. Bit Descriptions for SPICONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
15	LSBFIRST		LSB first selection.	0	R$\overline{W}$
		0	MSB first per SPI standard (default).		
		1	LSB first per SPI standard.		
14	SPI3WIRE		Selects if SPI is using 3-wire or 4-wire interface.	0	R$\overline{W}$
		0	4-wire SPI.		
		1	3-wire SPI.		
13	RESET		Executes software reset of SPI and controllers, reloads default register values, except for Register 0x00.	0	R$\overline{W}$
		0	Normal status.		
		1	Resets whole register map, except for Register 0x00.		
12	DOUBLESPI		Double SPI data line.	0	R$\overline{W}$
		0	The SPI port has only one data line and can be used as a 3-wire or 4-wire interface.		
		1	The SPI port has two data lines: both bidirectional defining a pseudo dual 3-wire interface where $\overline{CS}$ and SCLK are shared between the two ports. This mode is only available for RAM data read or write.		
11	SPI_DRV		Double drive ability for SPI output.	0	R$\overline{W}$
		0	Single SPI output drive ability.		
		1	Two-time drive ability on SPI output.		
10	DOUT_EN		Enable DOUT signal on SDO/SDI2/DOUT pin.	0	R$\overline{W}$
		0	SDO/SDI2 function input/output.		
		1	DOUT function output.		
[9:6]	RESERVED				R$\overline{W}$
5	DOUT_ENM[1]		Enable DOUT signal on SDO/SDI2/DOUT pin.		R$\overline{W}$
4	SPI_DRVM[1]		Double drive ability for SPI output.	0	R$\overline{W}$
3	DOUBLESPIM[1]		Double SPI data line.	0	R$\overline{W}$
2	RESETM[1]		Executes software reset of SPI and controllers, reloads default register values, except for Register 0x00.	0	R$\overline{W}$
1	SPI3WIREM[1]		Selects if SPI is using 3-wire or 4-wire interface.	0	R$\overline{W}$
0	LSBFIRSTM[1]		LSB first selection.	0	R$\overline{W}$

[1] SPICONFIG[10:15] must always be set to the mirror of SPICONFIG[5:0] to allow easy recovery of the SPI operation when the LSBFIRST bit is set incorrectly. Bit 15 = Bit 0, Bit 14 = Bit 1, Bit 13 = Bit 2, Bit 12 = Bit 3, Bit 11 = Bit 4 and Bit 10 = Bit 5.

Power Status Register (POWERCONFIG, Address 0x01)

Table 22. Bit Descriptions for POWERCONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x00	$R\overline{W}$
11	CLK_LDO_STAT		Read only flag indicating the 1.8 V on-chip CLDO regulator is on.	0	R
10	DIG1_LDO_STAT		Read only flag indicating DVDD1 LDO is on.	0	R
9	DIG2_LDO_STAT		Read only flag indicating DVDD2 LDO is on.	0	R
8	PDN_LDO_CLK		Disables the 1.8 V on-chip CLDO regulator. An external supply is required.	0	$R\overline{W}$
7	PDN_LDO_DIG1		Disables the DVDD1 LDO. An external supply is required.	0	$R\overline{W}$
6	PDN_LDO_DIG2		Disables the DVDD2 LDO. An external supply is required.	0	$R\overline{W}$
5	REF_PDN		Disables 10 kΩ resistor that creates REFIO voltage. User can drive with external voltage or provide external bandgap (BG) resistor.	0	$R\overline{W}$
4	REF_EXT		Power down main BG reference including DAC bias.	0	$R\overline{W}$
3	DAC1_SLEEP		Disables DAC1 output current.	0	$R\overline{W}$
2	DAC2_SLEEP		Disables DAC2 output current.	0	$R\overline{W}$
1	DAC3_SLEEP		Disables DAC3 output current.	0	$R\overline{W}$
0	DAC4_SLEEP		Disables DAC4 output current.	0	$R\overline{W}$

Clock Control Register (CLOCKCONFIG, Address 0x02)

Table 23. Bit Descriptions for CLOCKCONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x000	$R\overline{W}$
11	DIS_CLK1		Disables the analog clock to DAC1 out of the clock distribution block.	0	$R\overline{W}$
10	DIS_CLK2		Disables the analog clock to DAC2 out of the clock distribution block.	0	$R\overline{W}$
9	DIS_CLK3		Disables the analog clock to DAC3 out of the clock distribution block.	0	$R\overline{W}$
8	DIS_CLK4		Disables the analog clock to DAC4 out of the clock distribution block.	0	$R\overline{W}$
7	DIS_DCLK		Disables the clock to core digital block.	0	$R\overline{W}$
6	CLK_SLEEP		Enables a very low power clock mode.	0	$R\overline{W}$
5	CLK_PDN		Disables and powers down main clock receiver. No clocks are active in the device.	0	$R\overline{W}$
4	EPS		Enables Power Save (EPS). Enables a low power option for the clock receiver, but maintains low jitter performance on DAC clock rising edge. The DAC clock falling edge is substantially degraded.	0	$R\overline{W}$
3	DAC1_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 1 allowing 180° phase shift in DAC1 update timing.	0	$R\overline{W}$
2	DAC2_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 2 allowing 180° phase shift in DAC2 update timing.	0	$R\overline{W}$
1	DAC3_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 3 allowing 180° phase shift in DAC3 update timing.	0	$R\overline{W}$
0	DAC4_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core 4 allowing 180° phase shift in DAC4 update timing.	0	$R\overline{W}$

Reference Resistor Register (REFADJ, Address 0x03)

Table 24. Bit Descriptions for REFADJ

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	$R\overline{W}$
[5:0]	BGDR		Adjusts the BG 10 kΩ resistor (nominal) to 8 kΩ to 12 kΩ, changes BG voltage from 800 mV to 1.2 V, respectively.	0x00	$R\overline{W}$

DAC4 Analog Gain Register (DAC4AGAIN, Address 0x04)

Table 25. Bit Descriptions for DAC4AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	$R\overline{W}$
[14:8]	DAC4_GAIN_CAL		DAC4 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	$R\overline{W}$
[6:0]	DAC4_GAIN		DAC4 analog gain control while not in calibration mode—twos complement.	0x00	$R\overline{W}$

DAC3 Analog Gain Register (DAC3AGAIN, Address 0x05)

Table 26. Bit Descriptions for DAC3AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	$R\overline{W}$
[14:8]	DAC3_GAIN_CAL		DAC3 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	$R\overline{W}$
[6:0]	DAC3_GAIN		DAC3 analog gain control while not in calibration mode—twos complement.	0x00	$R\overline{W}$

DAC2 Analog Gain Register (DAC2AGAIN, Address 0x06)

Table 27. Bit Descriptions for DAC2AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	$R\overline{W}$
[14:8]	DAC2_GAIN_CAL		DAC2 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	$R\overline{W}$
[6:0]	DAC2_GAIN		DAC2 analog gain control while not in calibration mode—twos complement.	0x00	$R\overline{W}$

DAC1 Analog Gain Register (DAC1AGAIN, Address 0x07)

Table 28. Bit Descriptions for DAC1AGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	$R\overline{W}$
[14:8]	DAC1_GAIN_CAL		DAC1 analog gain calibration output—read only.	0x00	R
7	RESERVED			0	$R\overline{W}$
[6:0]	DAC1_GAIN		DAC1 analog gain control while not in calibration mode—twos complement.	0x00	$R\overline{W}$

DAC Analog Gain Range Register (DACxRANGE, Address 0x08)

Table 29. Bit Descriptions for DACxRANGE

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x00	$R\overline{W}$
[7:6]	DAC4_GAIN_RNG		DAC4 gain range control.	0x0	$R\overline{W}$
[5:4]	DAC3_GAIN_RNG		DAC3 gain range control.	0x0	$R\overline{W}$
[3:2]	DAC2_GAIN_RNG		DAC2 gain range control.	0x0	$R\overline{W}$
[1:0]	DAC1_GAIN_RNG		DAC1 gain range control.	0x0	$R\overline{W}$

FSADJ4 Register (DAC4RSET, Address 0x09)

Table 30. Bit Descriptions for DAC4RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC4_RSET_EN		For write, enable the internal R_{SET4} resistor for DAC4; for read, R_{SET4} for DAC4 is enabled during calibration mode.	0x00	$R\overline{W}$
[14:13]	RESERVED			0x00	$R\overline{W}$
[12:8]	DAC4_RSET_CAL		Digital control value of R_{SET4} resistor for DAC4 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x00	$R\overline{W}$
[4:0]	DAC4_RSET		Digital control to set the value of R_{SET4} resistor in DAC4.	0x0A	$R\overline{W}$

FSADJ3 Register (DAC3RSET, Address 0x0A)

Table 31. Bit Descriptions for DAC3RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC3_RSET_EN		For write, enable the internal R_{SET3} resistor for DAC3; for read, R_{SET3} for DAC3 is enabled during calibration mode.	0	$R\overline{W}$
[14:13]	RESERVED			0x0	$R\overline{W}$
[12:8]	DAC3_RSET_CAL		Digital control value of R_{SET3} resistor for DAC3 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	$R\overline{W}$
[4:0]	DAC3_RSET		Digital control to set the value of R_{SET3} resistor in DAC3.	0x0A	$R\overline{W}$

FSADJ2 Register (DAC2RSET, Address 0x0B)

Table 32. Bit Descriptions for DAC2RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC2_RSET_EN		For write, enable the internal R_{SET2} resistor for DAC2; for read, R_{SET2} for DAC2 is enabled during calibration mode.	0	$R\overline{W}$
[14:13]	RESERVED			0x0	$R\overline{W}$
[12:8]	DAC2_RSET_CAL		Digital control value of R_{SET2} resistor for DAC2 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	$R\overline{W}$
[4:0]	DAC2_RSET		Digital control to set the value of R_{SET2} resistor in DAC2.	0xA	$R\overline{W}$

FSADJ1 Register (DAC1RSET, Address 0x0C)

Table 33. Bit Descriptions for DAC1RSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DAC1_RSET_EN		For write, enable the internal R_{SET1} resistor for DAC1; for read, R_{SET1} for DAC1 is enabled during calibration mode.	0x00	$R\overline{W}$
[14:13]	RESERVED			0x00	$R\overline{W}$
[12:8]	DAC1_RSET_CAL		Digital control value of R_{SET1} resistor for DAC1 after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	$R\overline{W}$
[4:0]	DAC1_RSET		Digital control to set the value of R_{SET1} resistor in DAC1.	0x0A	$R\overline{W}$

Calibration Register (CALCONFIG, Address 0x0D)

Table 34. Bit Descriptions for CALCONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0	$R\overline{W}$
14	COMP_OFFSET_OF		Compensation offset calibration value overflow.	0	R
13	COMP_OFFSET_UF		Compensation offset calibration value underflow.	0	R
12	RSET_CAL_OF		R_{SETx} calibration value overflow.	0	R
11	RSET_CAL_UF		R_{SETx} calibration value underflow.	0	R
10	GAIN_CAL_OF		Gain calibration value overflow.	0	R
9	GAIN_CAL_UF		Gain calibration value underflow.	0	R
8	CAL_RESET		Pulse this bit high and low to reset the calibration results.	0	$R\overline{W}$
7	CAL_MODE		Read only flag indicating calibration is being used.	0	R
6	CAL_MODE_EN		Enables the gain calibration circuitry.	0	$R\overline{W}$
[5:4]	COMP_CAL_RNG		Offset calibration range.	0x0	$R\overline{W}$
3	CAL_CLK_EN		Enables the calibration clock to calibration circuitry.	0	$R\overline{W}$
[2:0]	CAL_CLK_DIV		Sets divider from DAC clock to calibration clock.	0x0	$R\overline{W}$

Comp Offset Register (COMPOFFSET, Address 0x0E)

Table 35. Bit Descriptions for COMPOFFSET

Bits	Bit Field Name	Settings	Description	Reset	Access
15	RESERVED			0x00	$R\overline{W}$
[14:8]	COMP_OFFSET_CAL		The result of the offset calibration for the comparator.	0x00	R
[7:2]	RESERVED			0x00	$R\overline{W}$
1	CAL_FIN		Read only flag indicating calibration is completed.	0x00	R
0	START_CAL		Start a calibration cycle.	0x00	$R\overline{W}$

Update Pattern Register (RAMUPDATE, Address 0x1D)

Table 36. Bit Descriptions for RAMUPDATE

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x00	$R\overline{W}$
0	RAMUPDATE		Update all SPI setting with new configuration (self clearing).	0	$R\overline{W}$

Command/Status Register (PAT_STATUS, Address 0x1E)

Table 37. Bit Descriptions for PAT_STATUS

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	RESERVED			0x000	$R\overline{W}$
3	BUF_READ		Read back from updated buffer.	0	$R\overline{W}$
2	MEM_ACCESS		Memory SPI access enable.	0	$R\overline{W}$
1	PATTERN		Status of pattern being played, read only.	0	R
0	RUN		Allows the pattern generation and stop pattern after trigger.	0	$R\overline{W}$

Command/Status Register (PAT_TYPE, Address 0x1F)

Table 38. Bit Descriptions for PAT_TYPE

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0000	$R\overline{W}$
0	PATTERN_RPT		Setting this bit allows the pattern to repeat the number of times defined in DAC4_3PATx and DAC2_1PATx.	0	$R\overline{W}$
		0	Pattern continuously runs.		
		1	Pattern repeats the number of times defined in DAC4_3PATx and DAC2_1PATx.		

Trigger Start to Real Pattern Delay Register (PATTERN_DLY, Address 0x20)

Table 39. Bit Descriptions for PATTERN_DLY

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	PATTERN_DELAY		Time between trigger low and pattern start in number of DAC clock cycles + 1. Minimum = 14. Maximum = 65535. Increment = 1.	0x000E	$R\overline{W}$

DAC4 Digital Offset Register (DAC4DOF, Address 0x22)

Table 40. Bit Descriptions for DAC4DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC4_DIG_OFFSET		DAC4 digital offset.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x00	$R\overline{W}$

DAC3 Digital Offset Register (DAC3DOF, Address 0x23)

Table 41. Bit Descriptions for DAC3DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC3_DIG_OFFSET		DAC3 digital offset.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

DAC2 Digital Offset Register (DAC2DOF, Address 0x24)

Table 42. Bit Descriptions for DAC2DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC2_DIG_OFFSET		DAC2 digital offset.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x00	$R\overline{W}$

DAC1 Digital Offset Register (DAC1DOF, Address 0x25)

Table 43. Bit Descriptions for DAC1DOF

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC1_DIG_OFFSET		DAC1 digital offset.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x00	$R\overline{W}$

Wave3/Wave4 Select Register (WAV4_3CONFIG, Address 0x26)

Table 44. Bit Descriptions for WAV4_3CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:14]	RESERVED			0x00	RW
[13:12]	PRESTORE_SEL4			0x00	RW
		0	Constant value held into DAC4 constant value MSB/LSB register.		
		1	Sawtooth defined in DAC4 sawtooth configuration register (SAW4_3CONFIG).		
		2	Pseudorandom sequence.		
		3	DDS4 output.		
[11:10]	RESERVED			0x00	RW
[9:8]	WAVE_SEL4			0x1	RW
		0	Waveform read from RAM between START_ADDR4 and STOP_ADDR4.		
		1	Prestored waveform.		
		2	Prestored waveform using START_DELAY4 and PATTERN_PERIOD.		
		3	Prestored waveform modulated by waveform from RAM.		
[7:6]	RESERVED			0x00	RW
[5:4]	PRESTORE_SEL3			0x00	RW
		0	Constant value held into DAC3 constant value MSB/LSB register.		
		1	Sawtooth defined in DAC3 sawtooth configuration register (SAW4_3CONFIG).		
		2	Pseudorandom sequence.		
		3	DDS3 output.		
[3:2]	RESERVED			0x00	RW
[1:0]	WAVE_SEL3			0x1	RW
		0	Waveform read from RAM between START_ADDR3 and STOP_ADDR3.		
		1	Prestored waveform.		
		2	Prestored waveform using START_DELAY3 and PATTERN_PERIOD.		
		3	Prestored waveform modulated by waveform from RAM.		

Wave1/Wave2 Select Register (WAV2_1CONFIG, Address 0x27)

Table 45. Bit Descriptions for WAV2_1CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:14]	RESERVED			0x0	RW
[13:12]	PRESTORE_SEL2			0x0	RW
		0	Constant value held into DAC2 constant value MSB/LSB register.		
		1	Sawtooth defined in DAC2 sawtooth configuration register (SAW2_1CONFIG).		
		2	Pseudorandom sequence.		
		3	DDS2 output.		
11	MASK_DAC4		Mask DAC4 to DAC4_CONST value.	0	RW
10	CH2_ADD		Add DAC2 and DAC4, output at DAC2.	0	RW
		0	Normal operation for DAC2/DAC4.		
		1	Add DAC2 and DAC4, output from DAC2. In this START_DELAYx case, DAC4 output remains unchanged.		
[9:8]	WAVE_SEL2			0x1	RW
		0	Waveform read from RAM between START_ADDR2 and STOP_ADDR2.		
		1	Prestored waveform.		
		2	Prestored waveform using START_DELAY2 and PATTERN_PERIOD.		
		3	Prestored waveform modulated by waveform from RAM.		

Bits	Bit Field Name	Settings	Description	Reset	Access
[7:6]	RESERVED			0x0	R$\overline{W}$
[5:4]	PRESTORE_SEL1			0x0	R$\overline{W}$
		0	Constant value held into DAC1 constant value MSB/LSB register.		
		1	Sawtooth defined in DAC1 sawtooth configuration register (SAW2_1CONFIG).		
		2	Pseudorandom sequence.		
		3	DDS1 output.		
3	MASK_DAC3		Mask DAC3 to DAC3_CONST value.	0	R$\overline{W}$
2	CH1_ADD		Add DAC1 and DAC3, output at DAC1.	0	R$\overline{W}$
		0	Normal operation for DAC1/DAC3.		
		1	Add DAC1 and DAC3, and output from DAC1. In this START_DELAYx case, DAC3 output remains unchanged.		
[1:0]	WAVE_SEL1			0x1	R$\overline{W}$
		0	Waveform read from RAM between START_ADDR1 and STOP_ADDR1.		
		1	Prestored waveform.		
		2	Prestored waveform using START_DELAY1 and PATTERN_PERIOD.		
		3	Prestored waveform modulated by waveform from RAM.		

DAC Time Control Register (PAT_TIMEBASE, Address 0x28)

Table 46. Bit Descriptions for PAT_TIMEBASE

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x00	R$\overline{W}$
[11:8]	HOLD		Number of times the DAC value holds the sample (0 = DAC holds for one sample).	0x1	R$\overline{W}$
[7:4]	PAT_PERIOD_BASE		Number of DAC clock periods per PATTERN_PERIOD LSB (0 = PATTERN_PERIOD LSB = 1 DAC clock period).	0x1	R$\overline{W}$
[3:0]	START_DELAY_BASE		Number of DAC clock period per START_DELAYx LSB (0 = START_DELAYx LSB = 1 DAC clock period).	0x1	R$\overline{W}$

Pattern Period Register (PAT_PERIOD, Address 0x029)

Table 47. Bit Descriptions for PAT_PERIOD

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	PATTERN_PERIOD		Pattern period register.	0x8000	R$\overline{W}$

DAC3/DAC4 Pattern Repeat Cycles Register (DAC4_3PATx, Address 0x2A)

Table 48. Bit Descriptions for DAC4_3PATx

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	DAC4_REPEAT_CYCLE		Number of DAC4 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$
[7:0]	DAC3_REPEAT_CYCLE		Number of DAC3 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$

DAC1/DAC2 Pattern Repeat Cycles Register (DAC2_1PATx, Address 0x2B)

Table 49. Bit Descriptions for DAC2_1PATx

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	DAC2_REPEAT_CYCLE		Number of DAC2 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$
[7:0]	DAC1_REPEAT_CYCLE		Number of DAC1 pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R$\overline{W}$

Trigger Start to DOUT Signal Register (DOUT_START_DLY, Address 0x2C)

Table 50. Bit Descriptions for DOUT_START_DLY

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DOUT_START		Time between trigger low and DOUT signal high in number of DAC clock cycles. Minimum = 3. Maximum = 65535. Increment = 1.	0x0003	RW

DOUT Configuration Register (DOUT_CONFIG, Address 0x2D)

Table 51. Bit Descriptions for DOUT_CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x0000	RW
5	DOUT_VAL		Manually sets DOUT signal value, only valid when DOUT_MODE = 0 (manual mode).	0	RW
4	DOUT_MODE		Sets different enable signal mode.	0	RW
		0x0	DOUT pin is output from SDO/SDI2/DOUT pin and is manually controlled by Bit 5, DOUT_EN in Register 0x00, which must be set to use this feature.		
		0x1	DOUT pin is output from SDO/SDI2/DOUT. The pin is controlled by DOUT_START and DOUT_STOP. DOUT_EN in Register 0x00 must be set to use this feature.		
[3:0]	DOUT_STOP		Time between pattern end and DOUT signal low in number of DAC clock cycles. Minimum = 0. Maximum = 15. Increment = 1.	0x0	RW

DAC4 Constant Value Register (DAC4_CST, Address 0x2E)

Table 52. Bit Descriptions for DAC4_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC4_CONST		Most significant byte of DAC4 constant value.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC3 Constant Value Register (DAC3_CST, Address 0x2F)

Table 53. Bit Descriptions for DAC3_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC3_CONST		Most significant byte of DAC3 constant value.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC2 Constant Value Register (DAC2_CST, Address 0x30)

Table 54. Bit Descriptions for DAC2_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC2_CONST		Most significant byte of DAC2 constant value.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC1 Constant Value Register (DAC1_CST, Address 0x31)

Table 55. Bit Descriptions for DAC1_CST

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC1_CONST		Most significant byte of DAC1 constant value.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC4 Digital Gain Register (DAC4_DGAIN, Address 0x32)

Table 56. Bit Descriptions for DAC4_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC4_DIG_GAIN		DAC4 digital gain range of +2 to −2.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC3 Digital Gain Register (DAC3_DGAIN, Address 0x33)

Table 57. Bit Descriptions for DAC3_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC3_DIG_GAIN		DAC3 digital gain. Range of +2 to −2.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC2 Digital Gain Register (DAC2_DGAIN, Address 0x34)

Table 58. Bit Descriptions for DAC2_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC2_DIG_GAIN		DAC2 digital gain. Range of +2 to −2.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC1 Digital Gain Register (DAC1_DGAIN, Address 0x35)

Table 59. Bit Descriptions for DAC1_DGAIN

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	DAC1_DIG_GAIN		DAC1 digital gain. Range of +2 to −2.	0x000	RW
[3:0]	RESERVED			0x0	RW

DAC3/DAC4 Sawtooth Configuration Register (SAW4_3CONFIG, Address 0x36)

Table 60. Bit Descriptions for SAW4_3CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:10]	SAW_STEP4		Number of samples per step for DAC4.	0x01	RW
[9:8]	SAW_TYPE4		The type of sawtooth (positive, negative, or triangle) for DAC4.	0x0	RW
		0	Ramp up saw wave.		
		1	Ramp down saw wave.		
		2	Triangle saw wave.		
		3	No wave, zero.		
[7:2]	SAW_STEP3		Number of samples per step for DAC3.	0x01	RW
[1:0]	SAW_TYPE3		The type of sawtooth (positive, negative, or triangle) for DAC3.	0x0	RW
		0	Ramp up saw wave.		
		1	Ramp down saw wave.		
		2	Triangle saw wave.		
		3	No wave, zero.		

DAC1/DAC2 Sawtooth Configuration Register (SAW2_1CONFIG, Address 0x37)

Table 61. Bit Descriptions for SAW2_1CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:10]	SAW_STEP2		Number of samples per step for DAC2.	0x01	RW
[9:8]	SAW_TYPE2		The type of sawtooth (positive, negative, or triangle) for DAC2.	0x0	RW
		0	Ramp up saw wave.		
		1	Ramp down saw wave.		
		2	Triangle saw wave.		
		3	No wave, zero.		
[7:2]	SAW_STEP1		Number of samples per step for DAC1.	0x01	RW

Bits	Bit Field Name	Settings	Description	Reset	Access
[1:0]	SAW_TYPE1		The type of sawtooth (positive, negative, or triangle) for DAC1.	0x0	RW
		0	Ramp up saw wave.		
		1	Ramp down saw wave.		
		2	Triangle saw wave.		
		3	No wave, zero.		

DDS Tuning Word MSB Register (DDS_TW32, Address 0x3E)

Table 62. Bit Descriptions for DDS_TW32

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDSTW_MSB		DDS tuning word MSB.	0x0000	RW

DDS Tuning Word LSB Register (DDS_TW1, Address 0x3F)

Table 63. Bit Descriptions for DDS_TW1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	DDSTW_LSB		DDS tuning word LSB.	0x00	RW
[7:0]	RESERVED			0x00	RW

DDS4 Phase Offset Register (DDS4_PW, Address 0x40)

Table 64. Bit Descriptions for DDS4_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS4_PHASE		DDS4 phase offset.	0x0000	RW

DDS3 Phase Offset Register (DDS3_PW, Address 0x41)

Table 65. Bit Descriptions for DDS3_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS3_PHASE		DDS3 phase offset.	0x0000	RW

DDS2 Phase Offset Register (DDS2_PW, Address 0x42)

Table 66. Bit Descriptions for DDS2_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS2_PHASE		DDS2 phase offset.	0x0000	RW

DDS1 Phase Offset Register (DDS1_PW, Address 0x43)

Table 67. Bit Descriptions for DDS1_PW

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS1_PHASE		DDS1 phase offset.	0x0000	RW

Pattern Control 1 Register (TRIG_TW_SEL, Address 0x44)

Table 68. Bit Descriptions for TRIG_TW_SEL

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0000	RW
1	TRIG_DELAY_EN		Enable start delay as trigger delay for all four channels.	0	RW
		0	Delay repeats for all patterns.		
		1	Delay is only at the start of first pattern.		
0	RESERVED			0	RW

Pattern Control 2 Register (DDSx_CONFIG, Address 0x45)

Table 69. Bit Descriptions for DDSx_CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
15	DDS_COS_EN4		Enable DDS4 cosine output of DDS instead of sine wave.	0	$R\overline{W}$
14	DDS_MSB_EN4		Enable the clock for the RAM address. Increment is coming from the DDS4 MSB. Default is coming from DAC clock.	0	$R\overline{W}$
13	RESERVED			0	$R\overline{W}$
12	RESERVED			0	$R\overline{W}$
11	DDS_COS_EN3		Enable DDS3 cosine output of DDS instead of sine wave.	0	$R\overline{W}$
10	DDS_MSB_EN3		Enable the clock for the RAM address. Increment is coming from the DDS3 MSB. Default is coming from DAC clock.	0	$R\overline{W}$
9	PHASE_MEM_EN3		Enable DDS3 phase offset input coming from RAM reading START_ADDR3. Because phase word is 8 bits and RAM data is 12 bits, only 8 MSB of RAM are taken into account. Default is coming from SPI map, DDS3_PHASE.	0	$R\overline{W}$
8	RESERVED			0	$R\overline{W}$
7	DDS_COS_EN2		Enable DDS2 cosine output of DDS instead of sine wave.	0	$R\overline{W}$
6	DDS_MSB_EN2		Enable the clock for the RAM address. Increment is coming from the DDS2 MSB. Default is coming from DAC clock.	0	$R\overline{W}$
5	RESERVED			0	$R\overline{W}$
4	RESERVED			0	$R\overline{W}$
3	DDS_COS_EN1		Enable DDS1 cosine output of DDS instead of sine wave.	0	$R\overline{W}$
2	DDS_MSB_EN1		Enable the clock for the RAM address. Increment is coming from the DDS1 MSB. Default is coming from DAC clock.	0	$R\overline{W}$
1	RESERVED			0	$R\overline{W}$
0	TW_MEM_EN		Enable DDS tuning word input coming from RAM reading using START_ADDR1. Because tuning word is 24 bits and RAM data is 12 bits, 12 bits are set to 0s depending on the value of the TW_MEM_SHIFT bits in the TW_RAM_CONFIG register. Default is coming from the SPI map, DDSTW.	0	$R\overline{W}$

TW_RAM_CONFIG Register (TW_RAM_CONFIG, Address 0x47)

Table 70. Bit Descriptions for TW_RAM_CONFIG

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x000	$R\overline{W}$
[4:0]	TW_MEM_SHIFT		TW_MEM_EN must be set = 1 to use this bit field.	0x00	$R\overline{W}$
		0x00	DDSTW = (RAM[11:0],12'b0)		
		0x01	DDSTW = (DDSTW[23],RAM[11:0],11'b0)		
		0x02	DDSTW = (DDSTW[23:22],RAM[11:0],10'b0)		
		0x03	DDSTW = (DDSTW[23:21],RAM[11:0],9'b0)		
		0x04	DDSTW = (DDSTW[23:20],RAM[11:0],8'b0)		
		0x05	DDSTW = (DDSTW[23:19],RAM[11:0],7'b0)		
		0x06	DDSTW = (DDSTW[23:18],RAM[11:0],6'b0)		
		0x07	DDSTW = (DDSTW[23:17],RAM[11:0],5'b0)		
		0x08	DDSTW = (DDSTW[23:16],RAM[11:0],3'b0)		
		0x09	DDSTW = (DDSTW[23:15],RAM[11:0],4'b0)		
		0x0A	DDSTW = (DDSTW[23:14],RAM[11:0],2'b0)		
		0x0B	DDSTW = (DDSTW[23:13],RAM[11:0],1'b0)		
		0x0C	DDSTW = (DDSTW[23:12],RAM[11:0])		
		0x0D	DDSTW = (DDSTW[23:11],RAM[11:1])		
		0x0E	DDSTW = (DDSTW[23:10],RAM[11:2])		
		0x0F	DDSTW = (DDSTW[23:9],RAM[11:3])		
		0x10	DDSTW = (DDSTW[23:8],RAM[11:4])		
		0x11 to 0x1F	Reserved.		

Start Delay4 Register (START_DLY4, Address 0x50)

Table 71. Bit Descriptions for START_DLY4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY4		Start delay of DAC4.	0x0000	$R\overline{W}$

Start Address4 Register (START_ADDR4, Address 0x51)

Table 72. Bit Descriptions for START_ADDR4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR4		RAM address where DAC4 starts to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x00	$R\overline{W}$

Stop Address4 Register (STOP_ADDR4, Address 0x52)

Table 73. Bit Descriptions for STOP_ADDR4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR4		RAM address where DAC4 stops to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x00	$R\overline{W}$

DDS Cycle4 Register (DDS_CYC4, Address 0x53)

Table 74. Bit Descriptions for DDS_CYC4

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC4		Number of sine wave cycles when DDS prestored waveform with start and stop delays is selected for DAC4 output.	0x0001	$R\overline{W}$

Start Delay3 Register (START_DLY3, Address 0x54)

Table 75. Bit Descriptions for START_DLY3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY3		Start delay of DAC3.	0x0000	$R\overline{W}$

Start Address3 Register (START_ADDR3, Address 0x55)

Table 76. Bit Descriptions for START_ADDR3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR3		RAM address where DAC3 starts to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

Stop Address3 Register (STOP_ADDR3, Address 0x56)

Table 77. Bit Descriptions for STOP_ADDR3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR3		RAM address where DAC3 stops to read waveform.	0x0000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

DDS Cycles3 Register (DDS_CYC3, Address 0x57)

Table 78. Bit Descriptions for DDS_CYC3

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC3		Number of sine wave cycles when DDS prestored waveform with start and stop delays is selected for DAC3 output.	0x0001	$R\overline{W}$

Start Delay2 Register (START_DLY2, Address 0x58)

Table 79. Bit Descriptions for START_DLY2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY2		Start delay of DAC2.	0x0000	$R\overline{W}$

Start Address2 Register (START_ADDR2, Address 0x59)

Table 80. Bit Descriptions for START_ADDR2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR2		RAM address where DAC2 starts to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

Stop Address2 Register (STOP_ADDR2, Address 0x5A)

Table 81. Bit Descriptions for STOP_ADDR2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR2		RAM address where DAC2 stops to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

DDS Cycle2 Register (DDS_CYC2, Address 0x5B)

Table 82. Bit Descriptions for DDS_CYC2

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC2		Number of sine wave cycles when DDS prestored waveform with start and stop delays is selected for DAC2 output.	0x0001	$R\overline{W}$

Start Delay1 Register (START_DLY1, Address 0x5C)

Table 83. Bit Descriptions for START_DLY1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	START_DELAY1		Start delay of DAC1.	0x0000	$R\overline{W}$

Start Address1 Register (START_ADDR1, Address 0x5D)

Table 84. Bit Descriptions for START_ADDR1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	START_ADDR1		RAM address where DAC1 starts to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

Stop Address1 Register (STOP_ADDR1, Address 0x5E)

Table 85. Bit Descriptions for STOP_ADDR1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR1		RAM address where DAC1 stops to read waveform.	0x000	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

DDS Cycle1 Register (DDS_CYC1, Address 0x5F)

Table 86. Bit Descriptions for DDS_CYC1

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC1		Number of sine wave cycles when DDS prestored waveform with start and stop delays is selected for DAC1 output.	0x0001	$R\overline{W}$

CFG Error Register (CFG_ERROR, Address 0x60)

Table 87. Bit Descriptions for CFG_ERROR

Bits	Bit Field Name	Settings	Description	Reset	Access
15	ERROR_CLEAR		Writing this bit clears all errors.	0	R
[14:6]	RESERVED			0x00	R
5	DOUT_START_LG_ERR		When DOUT_START is larger than pattern delay, this error is toggled.	0	R
4	PAT_DLY_SHORT_ERR		When pattern delay value is smaller than default value, this error is toggled. The actual PATTERN_DELAY_SHORT is 65536 – (14 – PATTERN_DELAY_SHORT).	0	R
3	DOUT_START_SHORT_ERR		When DOUT_START value is smaller than default value, this error is toggled. The actual DOUT_START is 65536 – (3 – DOUT_START).	0	R
2	PERIOD_SHORT_ERR		When period register setting value is smaller than pattern play cycle, this error is toggled.	0	R
1	ODD_ADDR_ERR		When memory pattern play is not even in length in trigger delay mode, this error flag is toggled.	0	R
0	MEM_READ_ERR		When there is a memory read conflict, this error flag is toggled.	0	R

SRAM Data Register (SRAM_DATA, Address 0x6000 to Address 0x6FFF)

Table 88. Bit Descriptions for SRAM_DATA

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	SRAM_DATA		SRAM_DATA[11:4]. The 8 MSBs of the programmable 12-bit SRAM_DATA.	0x00	$R\overline{W}$
[7:4]	SRAM_DATA		SRAM_DATA[3:0]. The 4 LSBs of the programmable 12-bit SRAM_DATA.	0x0	$R\overline{W}$
[3:0]	RESERVED			0x0	$R\overline{W}$

OUTLINE DIMENSIONS

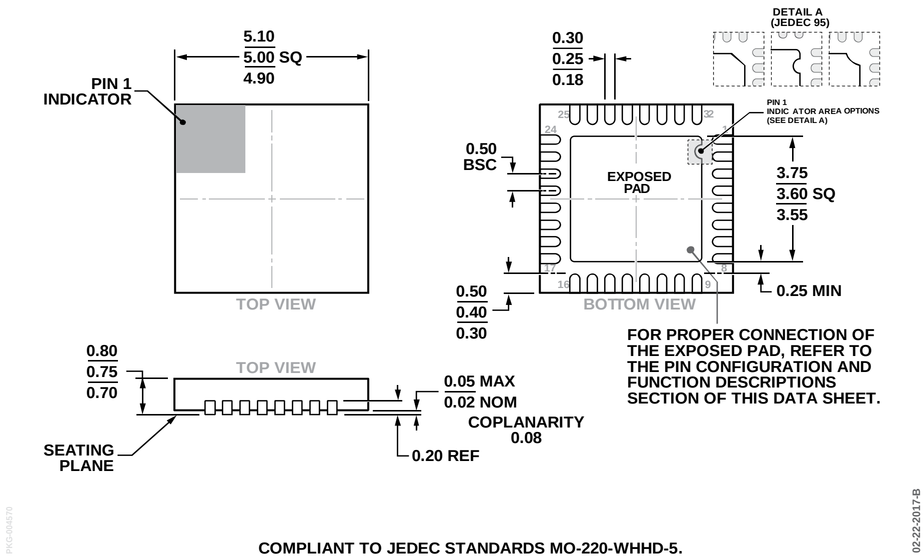

Figure 61. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9106BCPZ	−40°C to +85°C	32-Lead LFCSP	CP-32-12
AD9106BCPZRL7	−40°C to +85°C	32-Lead LFCSP	CP-32-12
AD9106-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.