This Document contains our journal for milestone 1. Please note that we worked on everything in the project as a group in the presence of both of us. We also included a more detailed log of changes for every module included in the header as suggested by the coding guidelines.

November 3, 1:00pm: We meet at the Arch Lab to start working on the project by reading the requirements and reviewing the files that we were given

November 3, 1:20pm: We start by refactoring our lab code to fix the naming as per the coding guidelines and replace all ranges with the given macros.

November 3, 1:30pm: We fixed some errors that we left from Lab 6 that were fixed in lab 7 but were then used in the pipelined version so we had to redo them. These errors were mainly concerned with the PC register size and all related changes.

November 3, 4:00pm: We finished the refactoring and the code fixes and started adding the new immgen and implementing the ALU along with changing the ALUControl unit and the control unit

November 3, 9:00pm: We finalized the control units without testing and starting adding the new hardware to support the new instructions, this was mainly done by adding a branch control unit and multiple multiplixers to control the data flow correctly.

November 3, 11:00pm: We were done with the code but without any testing, we tried to synthesize, but it wouldn't finish so we left it as is to fix later.

November 5, 1:00pm: We met at the lab to try to fix the synthesis issue and then test the code.

November 5, 1:30pm: We fixed the synthesis error and started testing each instruction, and fixing any logical error as we find them