

*HIGH-VOLTAGE MIXED-SIGNAL IC*

# UC8156

All-in-one driver IC w/ TCON for  
EPD Application

ES Specifications  
Datasheet Revision: 0.71

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**ULTRACHIP**

*The Coolest EPD Driver, Ever!*

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# UC8156

*All-in-one driver IC with TCON for EPD application*

## INTRODUCTION

The UC8156 is an all-in-one driver with timing controller for EPD displays. Its outputs are with 4 gray level resolutions per pixel. The timing controller provides control signals for the source and gate drivers.

The DC-DC controller allows it to generate the source output voltage VSH/VSL (+/-8~-/-15V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire SPI serial interface.

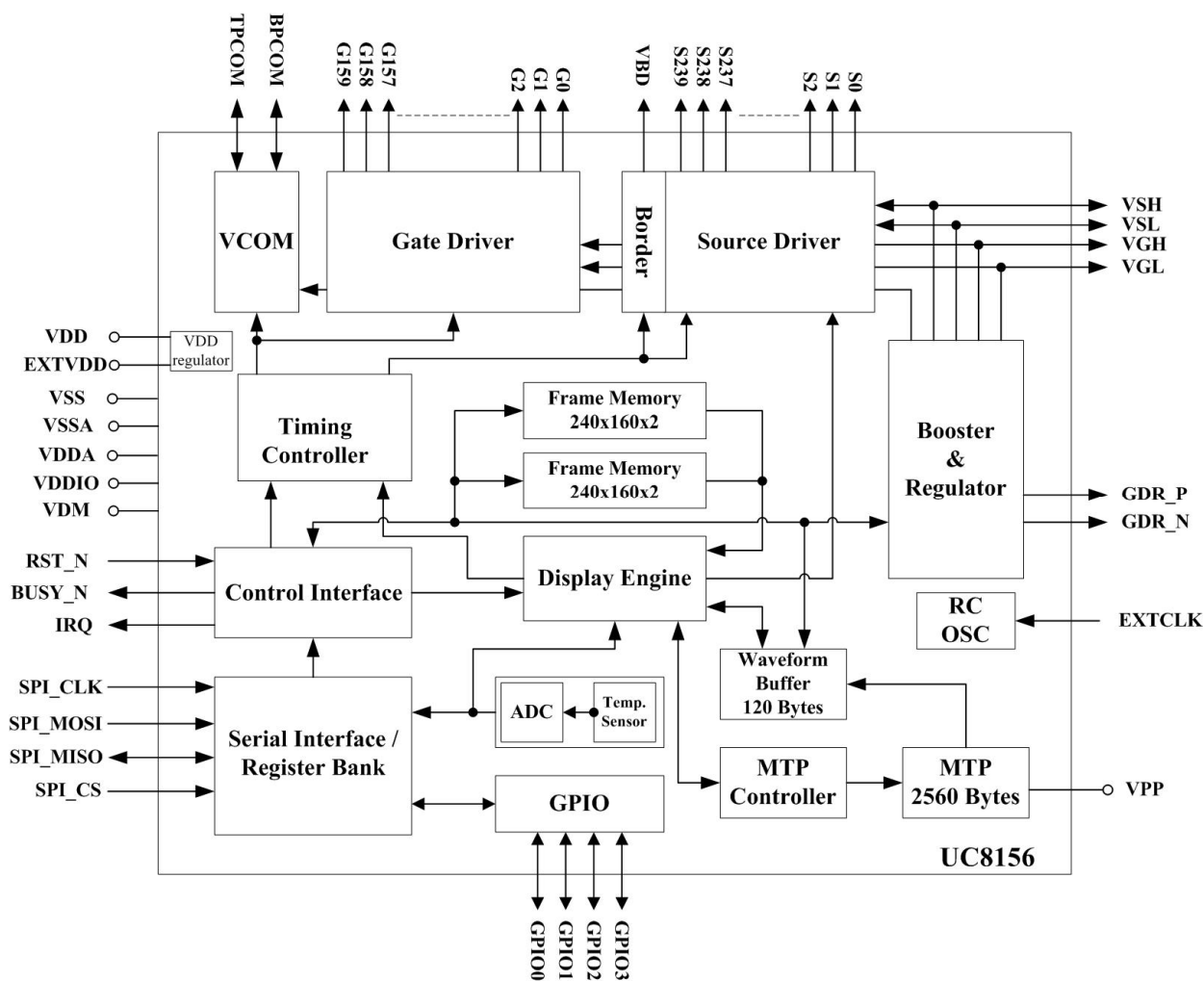
## FEATURE HIGHLIGHTS

- System-on-chip (SOC) for EPD displays
- Support up to 240(sources)x160(gates) @ 300Hz
- Up to 2-bit grayscale waveforms (4 level grey-shades)
- Source driver: VSL -8 to -15V, VSH +8 to +15V
- Gate driver: VGL -20 to -27V, VGH +15 to +22V
- DC VCOM: -4V to +10V with a 30mV resolution
- AC VCOM:  $VCOML = VSL + VCOM\_DC$   
 $VCOMH = VSH + VCOM\_DC$

- Individual switches for power supplies.
- Transparency write support
- Built-in temperature sensor
- Supports external LM75 Digital Temperature sensor and compatible devices
- MTP Memory for Waveform storage
- Power Management Integrated Circuit (PMIC)
- Serial peripheral interface (4-wire SPI)
- Built-in Frame memory (Max.): 240x160x2bitx2
- Support UT1 waveform format
- IO interface supply voltage: 1.7~ 3.6V
- Display frame rate: 1Hz ~ 300Hz
- Operating temperature range -30°C to 85°C
- Package: COG, COP (COF compatible)

**Remark:** Contact UltraChip for a visual inspection document (03-DOC-093).

## BLOCK DIAGRAM



**ORDERING INFORMATION**

Part Number	Description
UC8156cGAD-M0P2-3	Gold Bump Die, 280uM thick, dry polish, and without PI
UC8156cGAD-M0PT-3	Gold Bump Die, 200uM thick, dry polish, and without PI
UC8156cGAD-M0P1-3	Gold Bump Die, 150uM thick, dry polish, and without PI

**General Notes****APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

**BARE DIE DISCLAIMER**

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post wafer saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into wafer pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

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**PIN DESCRIPTION**

Type: I: Input, O: Output, I/O: Input/Output, P: Power, C: Capacitor pin

\* Pin Count is based on 60uM PAD pitch.

Pin (Pad) Name	Pin Count *	Type	Description
<b>POWER SUPPLY</b>			
VDDA	8	P	Analog Power.
VDD	6	P	Core Logic Power.VDD can be regulated internally from VDDA. A capacitor should be connected between VDD and VSS.
VDDIO	4	P	Power Supply for the interface.
VSSA	8	P	Analog and Pump Ground.
VSS	7	P	Core Logic Ground.
VDM	8	P	Driver Ground.
VPP	6	P	MTP programming voltage input
<b>SERIAL COMMUNICATION INTERFACE</b>			
SPI_CS	2	I	Serial communication chip select.
SPI_CLK	2	I	Serial communication clock input.
SPI_MOSI	2	I	Serial communication data input.
SPI_MISO	2	O	Serial communication data output.
<b>CONTROL INTERFACE</b>			
IRQ	2	O	This output pin is the Host IRQ.
GPIO[0..3] (GPIO0~GPIO3)	2x4	I/O	These are the General Purpose Input/Output pins.
EXTVDD	2	I	EXTVDD connected VSSA, internal regulator is on. EXTVDD connected VDDA, internal regulator is off, need an external 1.8V supply to VDD.
EXTCLK	2	I	External clock input.
RST_N	2	I (Pull-up)	Global reset pin. Low: reset. When RST_N become low, driver will reset. All register will be reset to default value, and all driver functions will be disabled. SD output and VCOM will base on previous condition; and they may have two conditions: 0v or floating.
BUSY_N	2	O	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
<b>OUTPUT DRIVER</b>			
S[0..239] ( S<0>~S<239> )	240	O	Source driver output signals.
G[0..159] ( G<0>~G<159> )	160	O	Gate driver output signals.
VBD (VBD<0>~VBD<3>)	1x4	O	Border Output signal
<b>VCOM GENERATOR</b>			
TPCOM	12	O	TPCOM output signal.
BPCOM	6	O	BPCOM output signal.

Pin (Pad) Name	Pin Count *	Type	Description
<b>POWER CIRCUIT</b>			
GDR_N	4	O	N-MOS gate control
GDR_P	4	O	P-MOS gate control
VGH	8	C	Positive Gate voltage.
VGL	8	C	Negative Gate voltage.
VSH	6	C	Positive Source voltage.
VSL	6	C	Negative Source voltage.
<b>MISC. PINS</b>			
TEST0~7	2x8	--	Test pins. Reserved for testing. For TEST0~TEST2, connect to GND. For TEST3~TEST7, leave them open.
TAI	2	--	Test pins. Reserved for testing. Leave them open.
TAO	2	--	Test pins. Reserved for testing. Leave them open.
Dummy	16	--	Dummy pins.

## COMMAND TABLE

Ndx: Index code, R/W: Read / Write RS: Reset Setting / Default values

#	Command	Ndx	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Action	RS
1.	Revision	00H	R	#	#	#	#	#	#	#	#	Read RevID [7:0]	56h
2.	Panel Setting	01H	RW	-	-	#	#	#	#	#	#	GVS[1:0], GSD, SOD, SOO, SFO	00h
3.	Driver Voltage Setting	02H	R/W	-	#	#	#	-	#	#	#	VGH_LV[2:0], VGL_LV[2:0]	50h
			R/W	#	#	#	#	#	#	#	#	VSH_LV[3:0], VSL_LV[3:0]	FFh
4.	Power Control Setting	03H	R/W	#	#	#	#	#	#	#	#	CLKSEL[1:0], CLKSRC, CLKEN, VPP_SEL, VSEXT, VGEXT, PWRON	C0h
5.	Boost Setting	04H	R/W	-	#	#	#	-	#	#	#	BSTNDC[2:0], BSTSDC[2:0]	32h
			R/W	-	-	#	#	-	#	#	#	BSTFR[1:0], BSTSC[2:0]	24h
6.	VCOM and Data Interval Setting	05H	R/W	-	-	#	#	#	#	#	#	FI[5:0]	11h
			R/W	-	-	#	#	#	#	#	#	CDI[5:0]	01h
7.	TCOM Timing Setting	06H	R/W	#	#	#	#	#	#	#	#	GAP[7:0]	03h
			R/W	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	11h
8.	Temperature Sensor Configuration	07H	R/W	-	-	-	-	#	#	#	#	TDSS[1:0], TAR, TRO	00h
9.	Temperature Value Register	08H	R/W	#	#	#	#	#	#	#	#	TV[7:0]	00h
10.	GPIO Configuration Register	09H	R/W	#	#	#	#	#	#	#	#	GDIR[3:0], GDATA[3:0]	00h
11.	GPIO Interrupt Register	0AH	R/W	#	#	#	#	#	#	#	#	GIS1[1:0], GIS0[1:0], GIT1[1:0], GIT0[1:0]	00h
12.	GPIO Port Type Register	0BH	R/W	#	#	#	#	#	#	#	#	GCN[3:0], GPH[3:0]	00h
13.	Panel Resolution Setting	0CH	R/W	#	#	#	#	#	#	#	#	SRC_S[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	SRC_E[7:0]	EFh
			R/W	#	#	#	#	#	#	#	#	GATE_S[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	GATE_E[7:0]	9Fh
14.	Write Pixel Rectangular Setting	0DH	R/W	#	#	#	#	#	#	#	#	X_S[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	X_E[7:0]	EFh
			R/W	#	#	#	#	#	#	#	#	Y_S[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	Y_E[7:0]	9Fh
15.	Pixel Access Position Setting	0EH	R/W	#	#	#	#	#	#	#	#	PAX[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	PAY[7:0]	00h
16.	Data Entry Mode Setting	0FH	R/W	-	-	#	#	-	#	#	#	SPIOEN, RAMSEL, DEM[2:0]	20h
17.	Write RAM	10H	W	#	#	#	#	#	#	#	#	PIXEL(n+3)[1:0], PIXEL(n+2)[1:0], PIXEL(n+1)[1:0], PIXEL(n)[1:0]	00h
18.	Read RAM	11H	R	#	#	#	#	#	#	#	#	PIXEL(n+3)[1:0], PIXEL(n+2)[1:0], PIXEL(n+1)[1:0], PIXEL(n)[1:0]	00h
19.	Bypass Update Setting	12H	R/W	-	-	#	#	#	#	#	#	BPRAM, BCRAM, PPLV[1:0], CPLV[1:0]	00h
20.	Initial Update Setting	13H	R/W	#	#	#	#	#	#	#	#	INITLC[3:0], INITTS[3:0]	30h
21.	Display Engine Control Register	14H	R/W	#	#	#	#	#	#	#	#	TKV[1:0], DM[1:0], TDEN, PART_DISP, WSS, DWTRG	00h
22.	Status Register	15H	R	-	-	-	#	#	#	#	#	MTPTO, MBUSY, PRDY, TBUSY, DBUSY	00h
23.	Interrupt Enable Register	16H	R/W	-	#	#	#	#	#	#	#	AMVIE, GPIO1IE, GPIO0IE, MIE, PIE, TIE, DIE	00h
24.	Interrupt Status Register	17H	R/W	-	#	#	#	#	#	#	#	AMVIS, GPIO1IS, GPIO0IS, MIS, PIS, TIS, DIS	00h



#	Command	Ndx	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Action	RS
25.	VCOM Configuration Register	18H	R/W	#	#	#	#	#	#	-	#	TPCOM_SEL[1:0], BPCOM_SEL[1:0], BPCOM_LV[1:0], VCOM_SEL	54h
			R/W	-	-	-	-	-	-	#	#	VG_SEL[1:0]	00h
			R/W	-	-	#	#	#	#	#	#	SO_OTHER, SO_COMH, SO_COML	24h
			R/W	-	-	-	-	#	#	#	#	COM_SEL_NF, COM_SEL_IDLE	0Ah
26.	Auto Measure VCOM	19H	R/W	#	#	#	#	#	#	#	#	AMVT[5:0], AMVS, AMVE	14h
27.	VCOM Measure Value	1AH	R	#	#	#	#	#	#	#	#	VMV[7:0]	00h
			R	-	-	-	-	-	-	#	#	VMV[9:8]	00h
28.	VCOM DC Setting	1BH	R/W	#	#	#	#	#	#	#	#	VCOM_DC[7:0]	-
			R/W	-	-	-	-	-	#	#	#	VCOM_DC[10:8]	-
29.	Waveform LUT Setting	1CH	R/W	#	#	#	#	#	#	#	#	SW1_0[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	SW1_1[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	SW1_2[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	SW1_3[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	SW2_0[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	...	00h
			R/W	#	#	#	#	#	#	#	#	SW24_3[7:0]	00h
			R/W	#	#	#	#	#	#	#	#	VW1[3:0], FC1[3:0]	00h
			R/W	#	#	#	#	#	#	#	#	...	00h
			R/W	#	#	#	#	#	#	#	#	VW24[3:0], FC24[3:0]	00h
30.	Vborder Setting	1DH	R/W	#	#	#	#	#	#	#	#	VBST[3:0], VBLV[1:0], VBINIT, VBEN	30h
31.	Power Sequence Setting	1FH	R/W	-	#	#	#	-	#	#	#	GSP[2:0], SGP[2:0]	11h
			R/W	-	#	#	#	-	#	#	#	NF1[2:0], NF2[2:0]	11h
			R/W	-	#	#	#	-	-	-	-	NF3[2:0]	11h
32.	Software Reset	20H	W	-	-	-	-	-	-	-	-		-
33.	Sleep Mode	21H	W	-	-	-	-	-	-	-	-		-
34.	Program WS MTP	40H	R/W	#	#	#	#	-	#	#	#	PGRS[3:0], VPPSEL, MARS, PST	F0h
35.	MTP Address Setting	41H	R/W	#	#	#	#	#	#	#	#	MTPADDR[7:0]	00h
			R/W	-	-	-	-	-	#	#	#	MTPADDR[10:8]	00h
36.	MTP One Byte Program	42H	W	#	#	#	#	#	#	#	#	MTPWD[7:0]	00h
37.	MTP Read	43H	R	#	#	#	#	#	#	#	#	MTPRD[7:0]	00h

## COMMAND DESCRIPTION

Ndx: Index code, R/W: Read / Write RS: Reset Setting / Default values

### (1) Revision (Index: 00h) (Default: 56h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Read Revision	R	0	1	0	1	0	1	1	0

These bits indicate the revision code. (Read only)

### (2) Panel Setting (Index: 01h) (Default: 00h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel	RW	-	-	GVS[1:0]		GSD	SOD	SOO	SFO

**GVS[1:0]:** Gate driver output Voltage Select.

00: Selected gate output as VGH, non-selected gate output as VGL

01: Selected gate output as VGL, non-selected gate output as VGH

10: All Gate output voltage level as VGL

11: All Gate output voltage level as VGH

**GSD:** Gate driver Scan Direction.

0: Scan up. First line to Last line: G0, G1, G2... G159

1: Scan down. First line to Last line: G159, G158, G157... G0

**SOD:** Source driver Output Direction.

0: Shift right. First data to Last data: S0, S1, S2... S239

1: Shift left. First data to Last data: S239, S238, S237... S0

**SOO:** Source driver Output Order.

0: S0, S1, S2, S3...S239

1: S0, S120, S1, S121 ... S118, S238, S119, S239 (left and right source interlaced)

**SFO:** Source driver First Output

0: S0 is the 1st source output channel

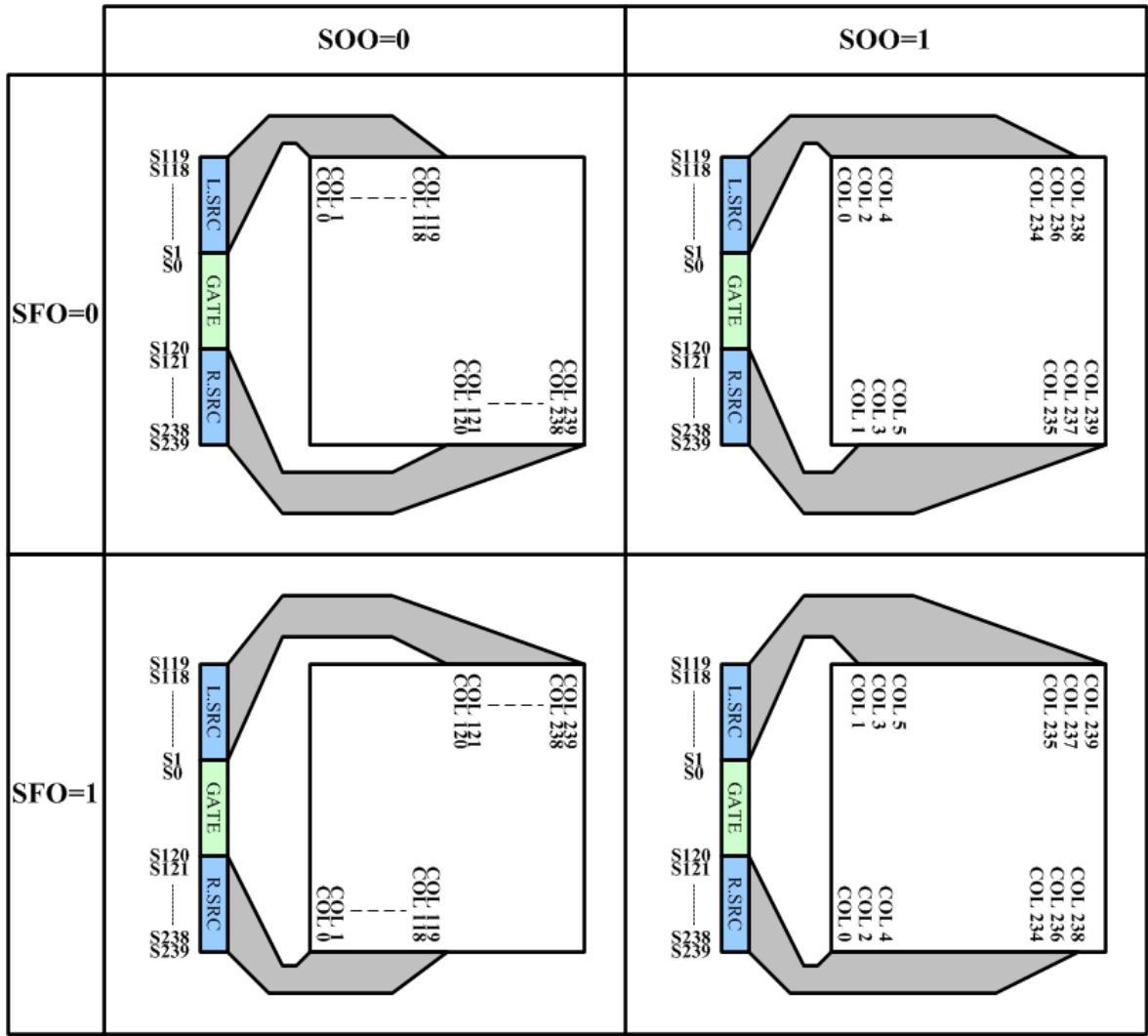
1: S120 is the 1st source output channel

This command can be active only when DBUSY = "0".

Output pin assignment sequence is shown as below

Driver	SOO=0		SOO=1	
	SFO=0	SFO=1	SFO=0	SFO=1
S0	COL0	COL120	COL0	COL1
S1	COL1	COL121	COL2	COL3
S2	COL2	COL122	COL4	COL5
S3	COL3	COL123	COL6	COL7
:	:	:	:	:
S118	COL118	COL238	COL236	COL237
S119	COL119	COL239	COL238	COL239
S120	COL120	COL0	COL1	COL0
S121	COL121	COL1	COL3	COL2
:	:	:	:	:
S236	COL236	COL116	COL233	COL232
S237	COL237	COL117	COL235	COL234
S238	COL238	COL118	COL237	COL236
S239	COL239	COL119	COL239	COL238

Output pin assignment on different Source Output Mode Setting is shown as below:



**(3) Driver Voltage Setting (Index: 02h) (Default: 50h, FFh)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set Driver Voltage	R/W	-	VGH_LV[2:0]			-	VGL_LV[2:0]		
	R/W	VSH_LV[3:0]				VSL_LV[3:0]			

**VGH\_LV[2:0]:** VGH power selection.

VGH_LV[2:0]	VGH power	VGH_LV[2:0]	VGH power
000	15V	100	19V
001	16V	101	20V
010	17V	110	21V
011	18V	111	22V

**VGL\_LV [2:0]:** VGL power selection.

VGL_LV[2:0]	VGL power	VGL_LV[2:0]	VGL power
000	-20V	100	-24V
001	-21V	101	-25V
010	-22V	110	-26V
011	-23V	111	-27V

**VSH\_LV [3:0]:** VSH power selection.

VSH_LV[3:0]	VSH power	VSH_LV[3:0]	VSH power
0000	8V	1000	12V
0001	8.5V	1001	12.5V
0010	9V	1010	13V
0011	9.5V	1011	13.5
0100	10V	1100	14V
0101	10.5V	1101	14.5V
0110	11V	1110	15V
0111	11.5V	1111	

**VSL\_LV [3:0]:** VSL power selection.

VSL_LV[3:0]	VSL power	VSL_LV[3:0]	VSL power
0000	-8V	1000	-12V
0001	-8.5V	1001	-12.5V
0010	-9V	1010	-13V
0011	-9.5V	1011	-13.5
0100	-10V	1100	-14V
0101	-10.5V	1101	-14.5V
0110	-11V	1110	-15V
0111	-11.5V	1111	

This command can be active only when BUSY\_N = "1".

If VGH-VGL is under 42V, ensure the IC safety, we will limit the VGL output voltage.

**(4) Power Control Setting (Index: 03h) (Default: C0h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Power Control Setting	R/W	CLKSEL[1:0]		CLKSRC	CLKEN	VPP_SEL	VSSEL	VGSEL	PWRON

**CLKSEL[1:0]:** TCON clock frequency Select . (Divided by clock source)

00: 15.6KHz (ClockPeriod=64us)      01: 125KHz (ClockPeriod=8us)  
 10: 500KHz (ClockPeriod=2us)      11: 1MHz (ClockPeriod=1us)

**CLKSRC:** Clock source select.

0: Internal clock source. (1Mhz)  
 1: External clock source

**CLKEN:** Internal clock auto enable.

0: Internal clock automatic enable or disable.  
 1: Internal clock always enable. (Not recommended use this setting)

**VPP\_SEL:** Vpp selection.

0: Vpp supply MTP programming power.  
 1: when VSH supply MTP programming power, need turn on BOOST and set VSH

**VSSEL:** Source power selection

0: Internal DC/DC function for generating VSH/VSL  
 1: External source power from VSH/VSL pins

**VGSEL:** Gate power selection

0: Internal DC/DC function for generating VGH/VGL  
 1: External gate power from VGH/VGL pins

**PWRON:** Power On

0: Power OFF. The driver will power OFF based on the Power-off sequence, BUSY\_N will become "0". This setting will turn off charge pump, T-con, source/gate driver, and VCOM, but register data will be kept until VDD becomes OFF. SD output and Vcom will remain as previous condition. It may have 2 conditions: 0V or floating.

1: Power ON. The driver will be powered ON following the Power-on sequence. After the Power ON command and all power sequence are ready, the BUSY\_N signal will become "1". Refer to the Power ON Sequence section.

This command can be active only when BUSY\_N = "1"

**(5) Boost Setting (Index: 04h) (Default: 32h, 24h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set Boost	R/W	-	BSTNDC			-	BSTSDC		
	R/W	-	-	BSTFR		-	BSTSC		

**BSTNDC[2:0]:** Normal mode duty cycle setting.

**BSTSDC[2:0]:** Soft start duty cycle setting.

BSTNDC[2:0], BSTSDC[2:0]	Duty Cycle	BSTNDC[2:0], BSTSDC[2:0]	Duty Cycle
000	10%	100	50%
001	20%	101	60%
010	30%	110	70%
011	40%	111	80%

**BSTFR[1:0]:** Boost Frequency setting.

00b: (Reserved)      01b: 500KHz      10b: 250KHz      11b: 125KHz

Tr/Tf	125KHz	250KHz	500KHz
10%	Pass	Fail	Fail
20%	Pass	Pass	Fail
30%	Pass	Pass	Pass
40%	Pass	Pass	Pass
50%	Pass	Pass	Pass
60%	Pass	Pass	Pass
70%	Pass	Pass	Fail
80%	Pass	Fail	Fail

**BSTSC[2:0]:** Soft start clock cycle setting.

BSTSC[2:0]	Clock Count	BSTSC[2:0]	Clock Count
000	128	100	2048
001	256	101	4096
010	512	110	8192
011	1024	111	16384

This command can be active only when BUSY\_N = "1".

#### (6) VCOM and Data interval Setting (Index: 05h) (Default: 01h, 01h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set VCOM and Data Interval	R/W	-	-	FI[5:0]					
	R/W	-	-	CDI[5:0]					

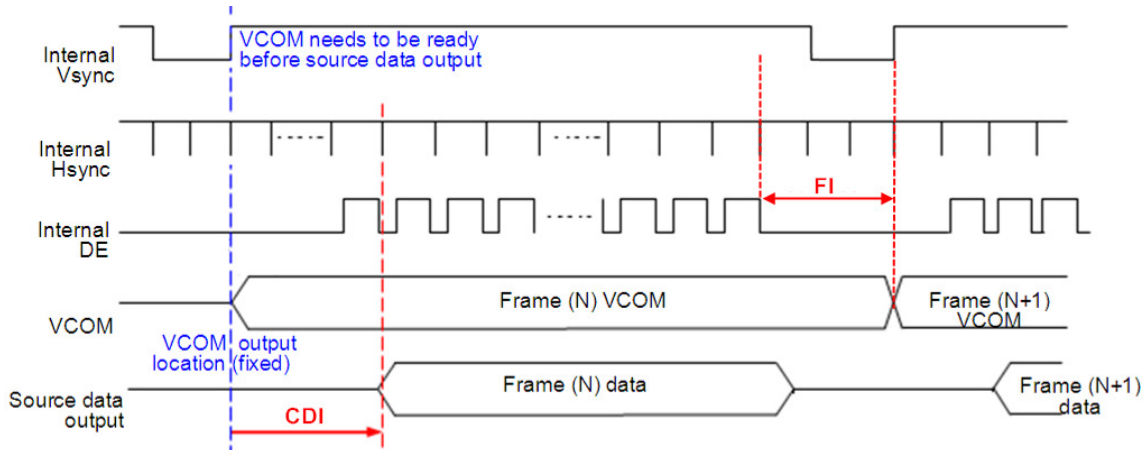
This command indicates the interval of Frame and interval of Vcom and data output.

This command can be active only when BUSY\_N = "1".

**FI[5:0]:** Frame interval

FI[5:0] , CDI[5:0]	Interval
000000	1 hsync
<b>000001</b>	2 hsync
000010	3 hsync
...	...
111111	64 hsync

**CDI[5:0]:** Vcom and data interval



#### (7) TCON Timing Setting (Index: 06h) (Default: 03h, 11h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Set TCOM Timing	R/W	GAP[7:0]							
	R/W	S2G[3:0]				G2S[3:0]			

This command defines Gate-high period and non-overlap period of Gate and Source.

This command can be active only when BUSY\_N = "1".

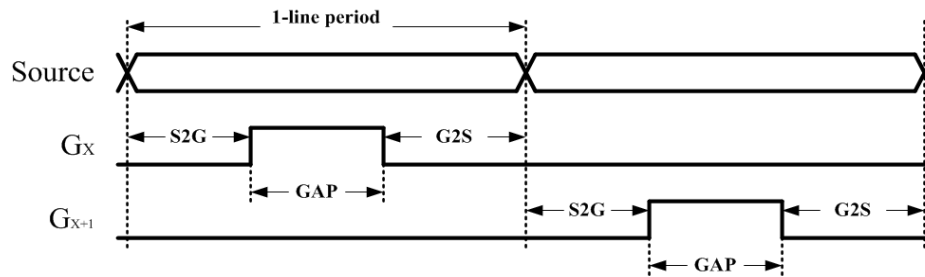
**GAP[7:0]:** Gate Active Period. Period = ClockPeriod \* (GAP + 12)

**S2G[3:0]:** Source to Gate Non-overlap period. Period = ClockPeriod \* S2G

**G2S[3:0]:** Gate to Source Non-overlap period. Period = ClockPeriod \* G2S

$$\text{FrameRate} = \frac{1}{\text{LineNumbers} * \text{LinePeriod}}$$

$$= \frac{1}{(\text{FI} + \text{CDI} + \text{GATE\_E} - \text{GATE\_S} + 1) * ((\text{GAP} + 12 + \text{S2G} + \text{G2S}) * \text{ClkPeriod})}$$

**(8) Temperature Sensor Configuration (Index: 07h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Config. Temp. Sensor	R/W	-	-	-	-	TDSS[1:0]		TAR	TRO

This command selects temperature device source.

**TDSS[1:0]:** Temperature Device Source Select.

00, 01: Direct refer TV[7:0] setting

10: Using internal temperature sensor.

11: Using external temperature sensor. External temperature sensor must be connection to GPIO[3:2] port.

**TAR:** Temperature Auto Retrieval.

This bit determines whether the internal or external temperature is auto retrieved at the beginning of an update.

0: temperature retrieval is disabled.

1: temperature retrieval is enabled.

**TRO:** Temperature sensor read operation. (Write only)

0: No effect.

1: Trigger an temperature sensor read operation and also update the temperature value to TV[7:0] at operation end.

TDSS[1] must set to '1'.

**(9) Temperature Value Register (Index: 08h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Value Register	R/W	TV[7:0]							

**TV[7:0]:**

These bits store the temperature value which will be used for Waveform retrieval on the next display update operation. When TDSS[1]='1' and TAR='1' (R07h), these bits are automatically updated on every frame update operation.

If TDSS='0x', write this registers can direct setting the temperature value.

If TDSS='10', read this registers to obtain internal sensor value. This registers will automatic update when write TRO=1 or TAR=1.

If TDSS='11', read this registers to obtain external sensor value. This registers will automatic update when write TAR=1.

**(10) GPIO Configuration Register (Index: 09h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Configuration Register	R/W	GDIR[3:0]				GDATA[3:0]			

**GDIR[3:0]:** These bits configure each individual GPIO pin between an input or an output.

0: the corresponding GPIO pin is configured as an input pin.

1: the corresponding GPIO pin is configured as an output pin.

**GDATA[3:0]:**

When GPIOx is configured as an input, a read from this bit returns the state of the corresponding GPIOx pin.

When GPIOx is configured as an output, a write to this bit drives the output state of the corresponding GPIOx pin.

**(11) GPIO Trigger Setting (Index: 0Ah) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Interrupt Register	R/W	GIS1[1:0]		GIS0[1:0]		GIT1[1:0]		GIT0[1:0]	

**GISx[1:0]:** GPIOx triggered status.

00: Both edge trigger has not occurred.

01: Positive edge trigger has occurred.

10: Negative edge trigger has occurred.

11: Both edge trigger has occurred.

Write '11b' to clear these bit.

**GITx[1:0]:** GPIOx pin is triggered on the which edge.

00: Positive edge.

01: Negative edge.

1x: Both edges.

**(12) GPIO Port Type (Index: 0Bh) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Port Type Register	R/W	GCN[3:0]				GPH[3:0]			

**GCN[3:0]:** GPIOx output type setting.

0: Push-pull

1: Open-drain, need external pull-high circuit

**GPH[3:0]:** GPIOx input pull-up resistor setting.

0: Disable GPIOx input pull-up resistor.

1: Enable GPIOx input pull-up resistor.

**(13) Panel Resolution Setting (Index: 0Ch) (Default: 00h, EFh, 00h, 9Fh)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Panel Resolution Setting	R/W	SRC_S[7:0]							
	R/W	SRC_E[7:0]							
	R/W	GATE_S[7:0]							
	R/W	GATE_E[7:0]							

This command defines alternative resolution.

**SRC\_S[7:0]:** First active SOURCE channel

**SRC\_E[7:0]:** Last active SOURCE channel

**GATE\_S[7:0]:** First active GATE channel

**GATE\_E[7:0]:** Last active GATE channel

EX : SRC\_S=0Ah, SRC\_E=BDh, GATE\_S=10h, GATE\_E=8Fh

Resolution: 180 x 128 (BDh-0Ah+1=180, 8Fh-10h+1=128)

First active SOURCE channel = S10,

Last active SOURCE channel = S189

First active GATE channel = G16,

Last active GATE channel = G143

This command can be active only when BUSY\_N = "1".



**(14) Write Pixel Rectangular Setting (Index: 0Dh) (Default: 00h, EFh, 00h, 9Fh)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Write Pixel Rectangular Setting	R/W	X_S[7:0]							
	R/W	X_E[7:0]							
	R/W	Y_S[7:0]							
	R/W	Y_E[7:0]							

These bits specify the rectangular of the image write.

**X\_S[7:0]:** Set SOURCE start position of the rectangular area.

**X\_E[7:0]:** Set SOURCE end position of the rectangular area.

**Y\_S[7:0]:** Set GATE start position of the rectangular area.

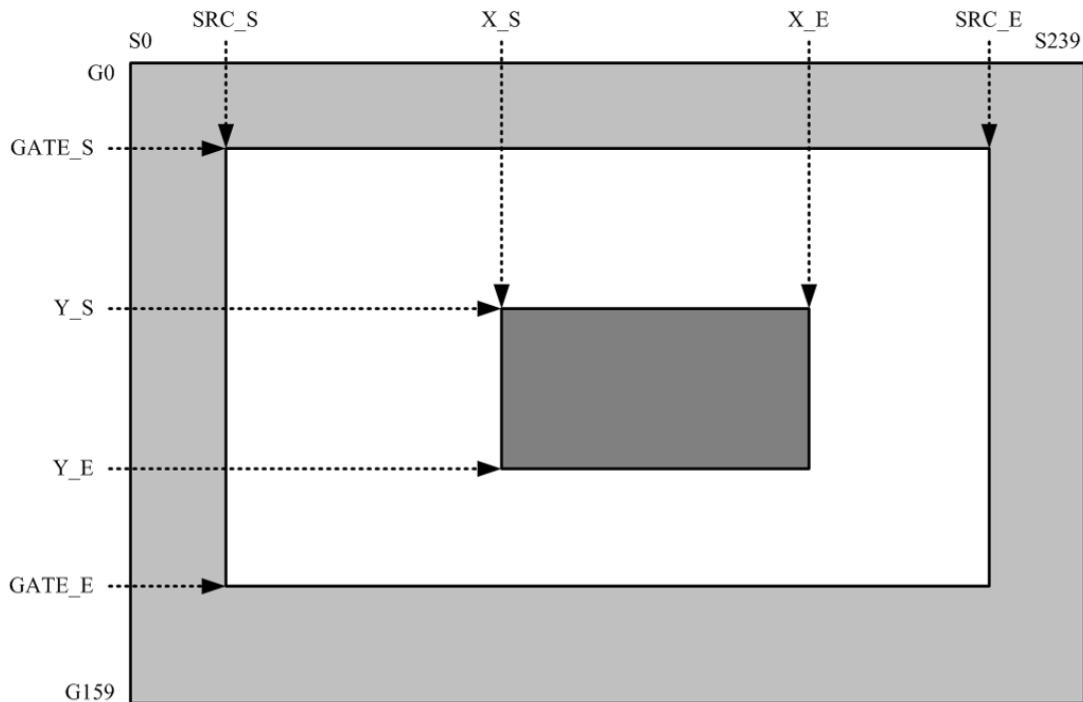
**Y\_E[7:0]:** Set GATE end position of the rectangular area.

**Note:**

X direction ( $X\_S + X\_E + 1$ ) must be 4 times pixel unit in the X-mode (R0Fh DEM[2]=0).

Y direction ( $Y\_S + Y\_E + 1$ ) must be 4 times pixel unit in the Y-mode (R0Fh DEM[2]=1).

This command can be active only when BUSY\_N = "1".

**(15) Pixel Access Position Setting (Index: 0Eh) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Pixel Access Position Setting	R/W	PAX[7:0]							
	R/W	PAY[7:0]							

**PAX[7:0]:** Set the X start address for RAM access

**PAY[7:0]:** Set the Y start address for RAM access

After RAM data are accessed, the address counter is automatically updated according to the settings with DEM[2:0] bits and the setting for a new RAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address setting should be made within the area designated with rectangular area which is controlled by the "Data Entry Setting (R0Fh)" and "Write Pixel Rectangular Setting (R0Dh)". Otherwise undesirable image will be displayed on the Panel.

**(16) Data Entry Mode Setting (Index: 0Fh) (Default: 20h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Data Entry Mode Setting	R/W	-	-	SPIOEN	RAMSEL	-	DEM[2:0]		

**SPIOEN:** SPI output tristate enable.

0: Tristate disable.

1: Tristate enable, spi\_miso will tri-state at non output period. (Default)

**RAMSEL:** Select the RAM of image write or read.

0: Current RAM buffer.

1: Previous RAM buffer.

**DEM[2]:** Set the direction in which the address counter is updated automatically after data are written to the RAM.

0: the address counter is updated in the X direction.

1: the address counter is updated in the Y direction.

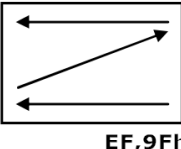
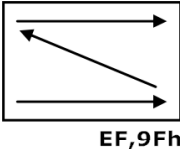
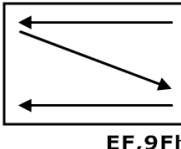

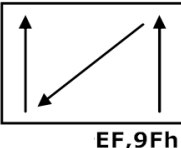

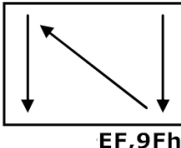
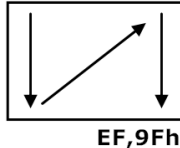
**DEM[1:0]:**

00: Y increment, X increment,

01: Y increment, X decrement,

10: Y decrement, X increment,

11: Y decrement, X decrement.

	<b>DEM[1:0]="11"</b> X: decrement Y: decrement	<b>DEM[1:0]="10"</b> X: increment Y: decrement	<b>DEM[1:0]="01"</b> X: decrement Y: increment	<b>DEM[1:0]="00"</b> X: increment Y: increment
<b>DEM[2]="0"</b> X-mode	00,00h  EF,9Fh	00,00h  EF,9Fh	00,00h  EF,9Fh	00,00h  EF,9Fh
<b>DEM[2]="1"</b> Y-mode	00,00h  EF,9Fh	00,00h  EF,9Fh	00,00h  EF,9Fh	00,00h  EF,9Fh

**(17) Write RAM (Index: 10h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Write RAM	W	Pixel(0)		Pixel(1)		Pixel(2)		Pixel(3)	
		:		:		:		:	
		Pixel(n-4)		Pixel(n-3)		Pixel(n-2)		Pixel(n-1)	

After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.

Pixel(x)[1:0]=00 → GS0

Pixel(x)[1:0]=01 → GS1

Pixel(x)[1:0]=10 → GS2

Pixel(x)[1:0]=11 → GS3

where x=0 ~ n-1

This command can be active only when DBUSY = "0".

**(18) Read RAM (Index: 11h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Read RAM	R	Pixel(0)		Pixel(1)		Pixel(2)		Pixel(3)	
		:		:		:		:	
		Pixel(n-4)		Pixel(n-3)		Pixel(n-2)		Pixel(n-1)	

After this command, data read on the MCU bus will fetch data from RAM, until another command is written. Address pointers will advance accordingly. This command can be active only when DBUSY = "0".

**(19) Bypass Update Setting (Index: 12h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Bypass Update Setting	R/W	-	-	BPRAM	BCRAM	PPLV[1:0]		CPLV[1:0]	

**BPRAM:** Bypass Previous RAM buffer.

0: Using previous RAM buffer for display update.

1: Using PPLV[1:0] for display update.

**BCRAM:** Bypass Current RAM buffer.

0: Using current RAM buffer for display update.

1: Using CPLV[1:0] for display update.

**PPLV[1:0]/CPLV[1:0]:** Previous Pixel level setting / Current Pixel level setting

00: GS0      01: GS1      10: GS2      11: GS3

This command can be active only when DBUSY = "0".

**(20) Initial Update Setting (Index: 13h) (Default: 33h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Initial Update Setting	R/W	INITLC[3:0]				INITTS[3:0]			

**INITLC[3:0]:** Initial update Loop Count.

init\_loop\_cnt = INITLC[3:0] + 1

default is loop 4 times, INITLC[3:0]=3

**INITTS[3:0]:** Initial update transitions setting.

INITTS	Transitions	INITTS	Transitions
0000	GS0→GS0	1000	GS2→GS0
0001	GS0→GS1	1001	GS2→GS1
0010	GS0→GS2	1010	GS2→GS2
<u>0011</u>	GS0→GS3	1011	GS2→GS3
0100	GS1→GS0	1100	GS3→GS0
0101	GS1→GS1	1101	GS3→GS1
0110	GS1→GS2	1110	GS3→GS2
0111	GS1→GS3	1111	GS3→GS3

**For Example:** Assume INITLC=0011b & INITTS=1100b

When we trigger an initial update, the pixel value of panel area will be the below sequence.

GS3→GS0→GS3→GS0→GS3→GS0→GS3→GS0

This command can be active only when DBUSY = "0".

**(21) Display Engine Control Register (Index: 14h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display Engine Control Register	R/W	TKV[1:0]		DM[1:0]		TDEN	PART_DISP	WSS	DWTRG

**TKV[1:0]:** Transparency Key Value.

00:GS0 01:GS1 10:GS2 11:GS3

**DM[1:0]:** Display Mode Select, these bits select the display mode that is triggered when the DWTRG bit is set(R12H bit0=1b).

00: Full Display Update. The update area of rectangular is defined in R0Ch.

01: Initial Update. The update area of rectangular is defined in R0Ch.

10: Area Display Update. The update area of rectangular is defined in R0Dh.

11: Area Display Update (disable non-select gate line). The update area of rectangular is defined in R0Dh.

**TDEN:** Transparency Display Enable

0: Transparency Off.

1: Transparency On.

**PART\_DISP:** Partial Display. When Old\_data=New\_data, the pixel is not updated. The default of the source driver output voltage can be modified by so\_other.

0: OFF (Normal Display)

1: Partial Display.

**WSS:** Waveform source select

0: Read waveform from LUT (R1Ch)

1: Read waveform from MT

**DWTRG:** Display Write Trigger, This bit can be active only when BUSY\_N = "1". (Write Only)

0: No effect.

1: Triggers a new display operation.

**(22) Status Register (Index: 15h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Status Register	R	-	-	-	MTPTO	MBUSY	PRDY	TBUSY	DBUSY

**MTPTO:** 0: MTP programming normally. 1: MTP programming time out has occurred.

**MBUSY:** 0: MTP idle. 1: MTP internal operation busy.

**PRDY:** 0: Internal Pump not ready. 1: Internal Pump is ready.

**TBUSY:** 0: Temperature device is idle. 1: Temperature device is busy. (This device coordinates of R07h TDDS setting)

**DBUSY:** 0: Display Engine is idle. 1: Display Engine is busy.

**(23) Interrupt Enable Register (Index: 16h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Enable Register	R/W	-	AVMIE	GPIO1IE	GPIO0IE	MIE	PIE	TIE	DIE

**VMVIE:** Auto VCOM Measure Interrupt Enable

0: Disable

1: Enable

**GPIO1IE:** GPIO1 trigger Interrupt Enable

0: Disable

1: Enable

**GPIO0IE:** GPIO0 trigger Interrupt Enable

0: Disable

1: Enable

**MIE:** MTP programming finish Interrupt Enable

0: Disable

1: Enable

**PIE:** Pump ready Interrupt Enable

0: Disable

1: Enable

**TIE:** Temperature read operation complement Interrupt Enable

0: Disable

1: Enable

**DIE:** Display update complement Interrupt Enable

0: Disable

1: Enable

**(24) Interrupt Raw Status Register (Index: 17h) (Default: 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Status Register	R/W	-	AVMIS	GPIO1IS	GPIO0IS	MIS	PIS	TIS	DIS

**VMVIS:** Auto VCOM Measure Interrupt Raw Status

0: VMV register (R1Ah) has NOT updated.

1: VMV register has updated.

**GPIO1IS:** GPIO1 trigger Interrupt Raw Status

0: GPIO1 trigger has NOT occurred.

1: GPIO1 trigger has occurred.

**GPIO0IS:** GPIO0 trigger Interrupt Raw Status

0: GPIO0 trigger has NOT occurred.

1: GPIO0 trigger has occurred.

**MIS:** MTP programming finish Interrupt Raw Status

0: MTP programming finish has NOT occurred.

1: MTP programming finish has occurred.

**PIS:** Pump ready Interrupt Raw Status

0: Pump ready interrupt has NOT occurred.

1: Pump ready interrupt has occurred.

**TIS:** Temperature read operation complement Interrupt Raw Status

0: Temperature read complement has NOT occurred.

1: Temperature read complement has occurred.

**DIS:** Display update complement Interrupt Raw Status (Include Auto Vcom measue complement)

0: Display update complement has NOT occurred.

1: Display update complement has occurred.

Write '1' to clear these registers.

**(25) VCOM Configuration Register (Index: 18h) (Default: 54h, 00h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
VCOM Configuration Register	R/W	TPCOM_SEL[1:0]		BPCOM_SEL[1:0]		BPCOM_LV[1:0]		-	VCOM_SEL
	R/W	-	-	-	-	-	-	VG_SEL[1:0]	
	R/W	-	-	SO_OTHER[1:0]		SO_COMH[1:0]		SO_COML[1:0]	
	R/W	-	-	-	-	COM_SEL_NF[1:0]		COM_SEL_IDLE[1:0]	

**TPCOM\_SEL[1:0]:** Define the TPCOM level at end of an update.

**BPCOM\_SEL[1:0]:** Define the BPCOM level at end of an update.

**BPCOM\_LV[1:0]:** Define the BPCOM level during update.

	00b	01b	10b	11b
TPCOM_SEL[1:0] / BPCOM_SEL[1:0] / BPCOM_LV[1:0]	GND	Hi-Z	VCOM	VCOM

**VCOM\_SEL:**

0: DC VCOM, VCOM output voltage will be fixed in VCOM\_DC voltage (R1Bh).

1: AC VCOM, VCOM output voltage will base on VCOM setting in VW LUT or VW MTP.

**VG\_SEL[1:0]:** Define the All GATE driver level at end of an update.

00: GND      01: Hi-Z      1x: Non-select (VGH or VGL according R00h GVS setting)

**SO\_OTHER[1:0]:** Define source driver output voltage when non-update and VCOM=(COM\_DC, GND, HiZ). Default: 10b

**SO\_COMH[1:0]:** Define source driver output voltage when non-update and VCOM=COM\_H. Default: 01b

**SO\_COML[1:0]:** Define source driver output voltage when non-update and VCOM=COM\_L. Default: 00b

	00b	01b	10b	11b
SO_OTHER[1:0] / SO_COMH[1:0] / SO_COML[1:0]	VSL VSL VSL	VSH VSH VSH	GND GND GND	HiZ HiZ HiZ

**COM\_SEL\_NF[1:0]:** Define TPCOM output voltage when null-frame period. Default: 10b

**COM\_SEL\_IDLE[1:0]:** Define TPCOM output voltage when display-idle period. Default: 10b

	00b	01b	10b	11b
COM_SEL_NF[1:0] / COM_SEL_IDLE[1:0]	GND	HiZ	(keep)	VCOM_DC

This command can be active only when BUSY\_N = "1".

**(26) Auto Measure VCOM (Index: 19h) (Default: 14h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Auto Measure VCOM	R/W	AMVT[5:0]						AMVS	AMVE

This command reads the IC status.

**AMVT[5:0]:** Auto Measure Vcom Time

Total Vcom measure time = 24 \* AMVT[5:0] \* FramePeriod = 24 \* AMVT[5:0] \* LineNumbers \* LinePeriod

Note1: the term of LineNumbers and LinePeriod please refer to R06h.

Note2: AMVT[5:0] >= 1

**AMVS:** Auto Measure Vcom Select.

0: Get Vcom value using internal circuit and stored in VMV registers (R1Ah).

1: Get Vcom value using external circuit.

**AMVE:** Auto Measure Vcom Enable (write only)

0: No effect

1: Trigger auto Vcom sensing.

This command can be active only when BUSY\_N = "1".

**(27) VCOM Measure Value (Index: 1Ah)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
VCOM Measure Value	R	VMV[7:0]							
	R	-	-	-	-	-	-	VMV[9:8]	

This command gets the Vcom value with a 30mV resolution.

If VMV[9]=0 , VCOM measure value is + VMV[9:0] \* 30mV

If VMV[9]=1 , VCOM measure value is - VMV[9:0] \* 30mV

**(28) VCOM DC Setting (Index: 1Bh) (Default: VCOM\_DC value from MTP)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
VCOM DC Setting	R/W	VCOM_DC[7:0]							
	R/W	-	-	-	-	-	VCOM_DC[10:8]		

This command sets VCOM\_DC value with a 30mV resolution. After power on (REG03h bit0), the VCOM\_DC register will loaded with MTP value. If MTP has not been programmed, then default will be 000h

**VCOM\_DC[9:0]:** Vcom Value

VCOM_DC [10]	VCOM_DC[9:0]	VCOM	VCOM_DC [10]	VCOM_DC[9:0]	VCOM
0	000h	0.00 V	1	000h	-0.00 V
0	001h	0.03 V	1	001h	-0.03 V
0	002h	0.06 V	1	002h	-0.06 V
0	003h	0.09 V	1	003h	-0.09 V
0	...	...	1	...	...
0	084h	3.96 V	1	084h	-3.96 V
0	085h	3.99 V	1	085h	-3.99 V
0	086h	4.02 V	1	086h	-4.02 V
0	...	...	1	087h ~ 3FFh	Reserved
0	14Ch	9.96 V			
0	14Dh	9.99 V			
0	14Eh	10.02 V			
0	14Fh ~ 3FFh	Reserved			

Write this command can be active only when DBUSY = "0"

## (29) Waveform LUT Setting (Index: 1Ch) (Default: 00h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Waveform LUT Setting	R/W	SW1_0							
		SW1_1							
		SW1_2							
		SW1_3							
		SW2_0							
		:							
		SW24_3							
		FC1				VW1			
		FC2				VW2			
		FC3				VW3			
		:				:			
		FC24				VW24			

Write this command can be active only when DBUSY = "0"

Source Waveforms LUT content define.

	D7	D6	D5	D4	D3	D2	D1	D0
<b>SWn_0</b>	GS0→GS3	GS0→GS2	GS0→GS1	GS0→GS0	GS0→GS3	GS0→GS2	GS0→GS1	GS0→GS0
<b>SWn_1</b>	GS1→GS3	GS1→GS2	GS1→GS1	GS1→GS0	GS1→GS3	GS1→GS2	GS1→GS1	GS1→GS0
<b>SWn_2</b>	GS2→GS3	GS2→GS2	GS2→GS1	GS2→GS0	GS2→GS3	GS2→GS2	GS2→GS1	GS2→GS0
<b>SWn_3</b>	GS3→GS3	GS3→GS2	GS3→GS1	GS3→GS0	GS3→GS3	GS3→GS2	GS3→GS1	GS3→GS0

Source waveform voltage transitions define.

code	Vsource waveform
<b>00</b>	VSL
<b>01</b>	VSH
<b>10</b>	GND
<b>11</b>	HiZ

VCOM Waveforms LUT content define.

code	VCOM Waveform
<b>0000</b>	GND
<b>0001</b>	VCOM_DC
<b>0010</b>	VSH+VCOM_DC
<b>0011</b>	VSL+VCOM_DC
<b>other</b>	HiZ

Frame Count LUT content define.

code	Frame Count
<b>0000</b>	Frame skipped
<b>0001</b>	1-frame
<b>0010</b>	2-frame
<b>0011</b>	.....
<b>1110</b>	14-frame
<b>1111</b>	15-frame

**(30) VBorder Setting (Index: 1Dh) (Default: 30h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Vborder Setting	R/W	VBST[3:0]				VBLV[1:0]		VBINIT	VBEN

**VBST[3:0]:** Selection VBD transitions.

VBST	VBD Transitions	VBST	VBD Transitions
0000	GS0→GS0	1000	GS2→GS0
0001	GS0→GS1	1001	GS2→GS1
0010	GS0→GS2	1010	GS2→GS2
0011	GS0→GS3	1011	GS2→GS3
0100	GS1→GS0	1100	GS3→GS0
0101	GS1→GS1	1101	GS3→GS1
0110	GS1→GS2	1110	GS3→GS2
0111	GS1→GS3	1111	GS3→GS3

**VBLV[1:0]:** Selection VBD level during “non-update time”.

00: HiZ

01: VCOM

1x: GND

**VBINIT:** Selection which transitions for initialize update.

0: Use initial transitions. (R13h INITTS)

1: Use VBD transitions.

**VBEN:** Selection whether to switch the border during next update or not.

0: VBD update Disable.

1: VBD update Enable.

This command can be active only when DBUSY = “0”.

**(31) Power Sequence Setting (Index: 1Fh) (Default: 11h, 11h, 10h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Power Sequence Setting	R/W	-	GSP[2:0]			-	SGP[2:0]		
	R/W	-	NF1[2:0]			-	NF2[2:0]		
	R/W	-	NF3[2:0]			-	-	-	-

Power On/Off Sequence Setting, This command can be active only when BUSY\_N = “1”.

**GSP[2:0]:** GATE voltage ON to SOURCE voltage ON period.

**SGP[2:0]:** SOURCE voltage OFF to GATE voltage OFF period.

GSP[2:0]; SGP[2:0]	Period
000b	no delay
001b	1ms
010b	2ms
011b	3ms
100b	4ms
101b	5ms
110b	Reserved
111b	Reserved

**NF1[2:0]:** Null Frame1 period.

**NF2[2:0]:** Null Frame1 period.

**NF3[2:0]:** Null Frame1 period.

NF(x)[2:0]	Period
000b	Zero delay
001b	1-Frame time
010b	2-Frame time
011b	3-Frame time
100b	4-Frame time
101b	5-Frame time
110b	6-Frame time
111b	7-Frame time



**(32) Software Reset (Index: 20h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Software Reset	W	-	-	-	-	-	-	-	-

Write any data to this command, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SOURCE driver output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

**(33) Sleep Mode (Index: 21h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Sleep Mode	W	-	-	-	-	-	-	-	-

Write any data to the command, the driver will be entry sleep mode. Insert a rise pulse on RST\_N pin then back to normal mode.

**(34) Program WS MTP (Index: 40h) (Default: F0h)**

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Program WS MTP	R/W	PGRS[3:0]				-	-	MARS	PST

Program MTP of Waveform Setting, the contents should be written into RAM before sending this command.

**PGRS[3:0]:** Program Range Setting.

PGRS[3:0]	MTP Program Range	Description
0000b	000h ~ 077h	WS1
0001b	078h ~ 0EFh	WS2
0010b	0F0h ~ 167h	WS3
0011b	168h ~ 1DFh	WS4
0100b	1E0h ~ 257h	WS5
0101b	258h ~ 2CFh	WS6
0110b	2D0h ~ 347h	WS7
0111b	348h ~ 3BFh	WS8
1000b	3C0h ~ 437h	WS9
1001b	438h ~ 4AFh	WS10
1010b	4B0h ~ 4B8h	TS
1011b	000h ~ 4B8h	WS1 ~ WS10 +TS
1100b~1111b	--	Reserved

**MARS:** MTP Access Region Selection.

0: Select type1 region

1: Select type2 region

**PST:** Program Start (Write Only).

0: No effect.

1: Start a MTP program operation. (Writing '1' can be active only when BUSY\_N = "1".)

For Programming the WS and TR, Write RAM is required, and the configurations should be

C 0D	Command 0Dh	Command (14) "Write Pixel Rectangular Setting"
D 00	Parameter 1 default 00h	Sets RAM X-Address for S0
D EF	Parameter 2 default EFh	Sets RAM X-Address for S239
D 00	Parameter 3 default 00h	Sets RAM Y-Address for G0
D 9F	Parameter 4 default 9Fh	Sets RAM Y-Address for G159
C 0E	Command 0Eh	Command (15) "Pixel Access Position Setting"
D 00	Parameter 1 default 00h	Sets start X-address for S0
D 00	Parameter 2 default 00h	Sets start Y-address for G0
C 0F	Command 0Fh	Command (16) "Data Entry mode"
D 00	Parameter 1 default 00h	Sets "Address automatic increment" to "X increment" and "Y increment"
		Sets "Address counter updated" to "in X direction" (rather than Y direction)
		Selects to use "current" RAM buffer (rather than "previous")

## MTP Content Address Mapping

Write RAM Start Address (R0Eh)		MTP Content
PAX	PAY	
0	0	WS1
0	2	WS2
0	4	WS3
0	6	WS4
0	8	WS5
0	10	WS6
0	12	WS7
0	14	WS8
0	16	WS9
0	18	WS10
0	20	TS

## (35) MTP Address Setting (Index: 41h) (Default: 00h, 00h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
MTP Address Setting	R/W	MTPADDR[7:0]							
	R/W	-	-	-	-	-	MTPADDR[10:8]		

MTPADDR valid range is 000h to 4FFh.

After each byte is accessed, the content of the MTPADDR is automatically incremented.

## (36) MTP One Byte Program (Index: 42h) (Default: 00h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
MTP One Byte Program	W	MTPWD[7:0]							

Write this byte will generate an internal MTP program operation; cause MTPDATA to be written to MTPADDR.

This command can be active only when BUSY\_N = "1".

## (37) MTP Read (Index: 43h) (Default: 00h)

Action	R/W	D7	D6	D5	D4	D3	D2	D1	D0
MTP Read	R	MTPRD[7:0]							

Read one byte MTP content to MTPRD, the MTP address according to the MTPADDR.

This command can be active only when BUSY\_N = "1".

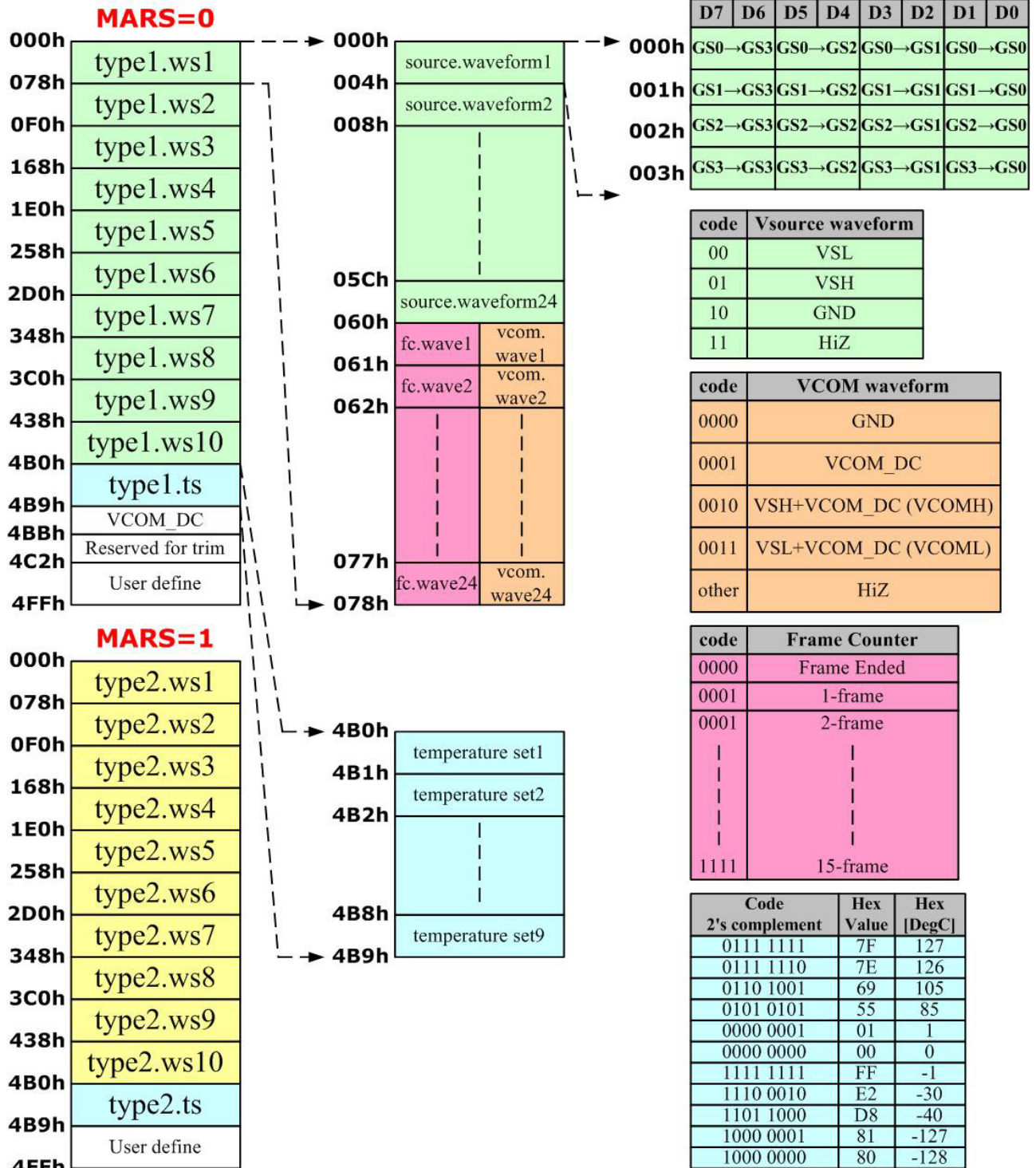
## MTP

The MTP is the non-volatile memory and stored the information:

10 sets of WAVEFORM SETTING (WS) [100bytes x 10]

9 sets of TEMPERATURE SETTING (TS) [1byte x 9]

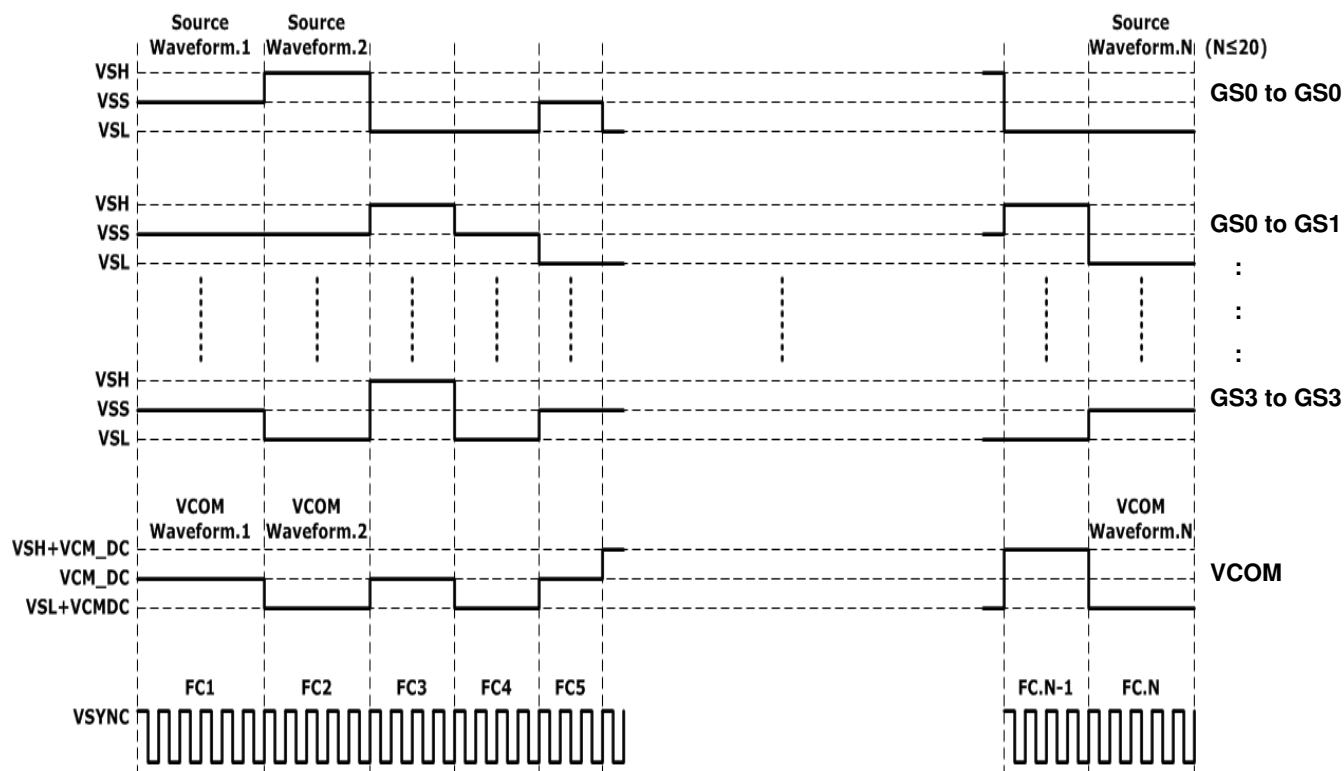
### MTP Content and Address Mapping



## Temperature setting mechanism

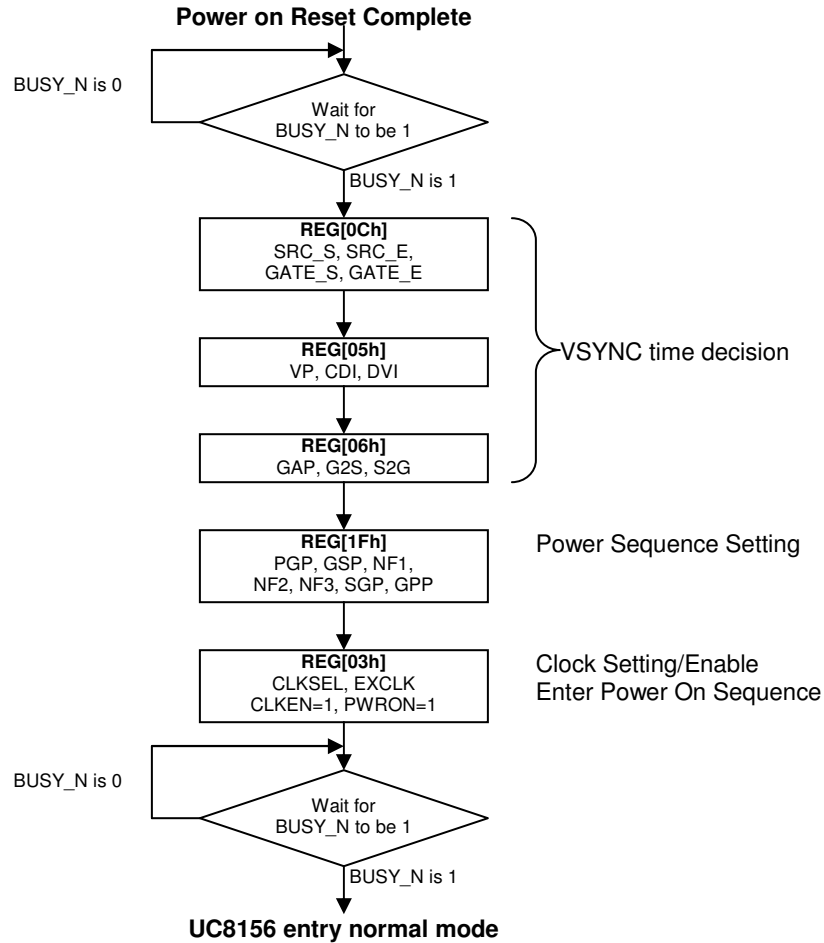
Ambient Temperature	Select of waveform setting
temperature < temp1	ws1
temp1 $\leq$ temperature < temp2	ws2
temp2 $\leq$ temperature < temp3	ws3
temp3 $\leq$ temperature < temp4	ws4
temp4 $\leq$ temperature < temp5	ws5
temp5 $\leq$ temperature < temp6	ws6
temp6 $\leq$ temperature < temp7	ws7
temp7 $\leq$ temperature < temp8	ws8
temp8 $\leq$ temperature < temp9	ws9
temp9 $\leq$ temperature	ws10

## Programmable Source and Gate waveform illustration

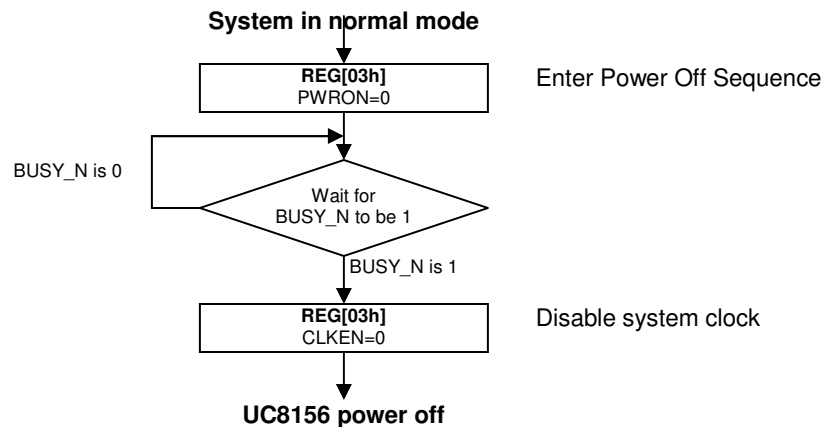


## Typical Operating Sequence

### ■ POWER ON



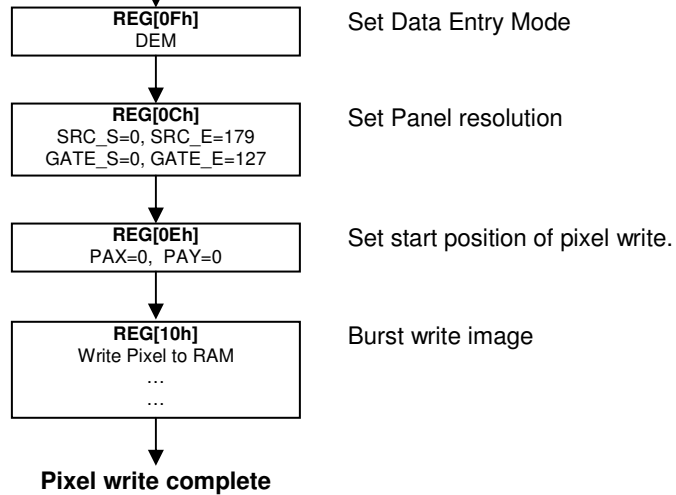
### ■ POWER OFF



## ■ FULL IMAGE PIXEL WRITE

Resolution: 180x128

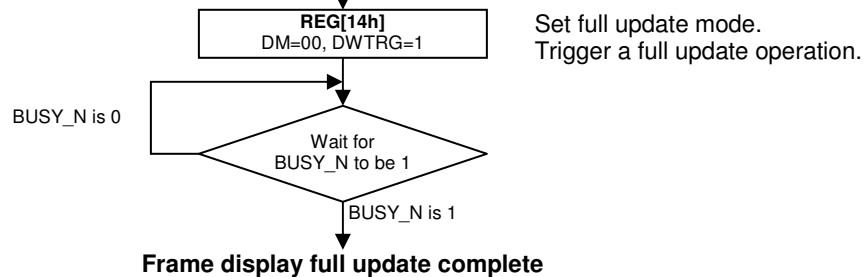
System in normal mode



## ■ FULL IMAGE UPDATE

System in normal mode

Host finished writing to image buffer

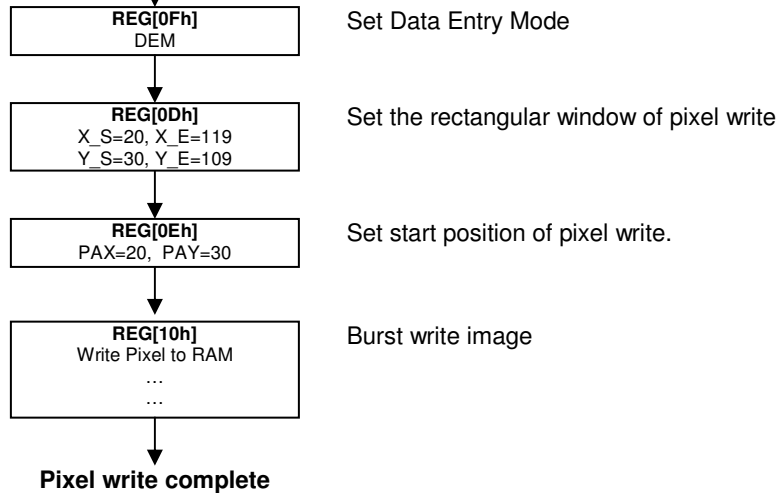


## ■ AREA IMAGE PIXEL WRITE

Windows size: 100x80

Upper left location of the windows: (20,30)

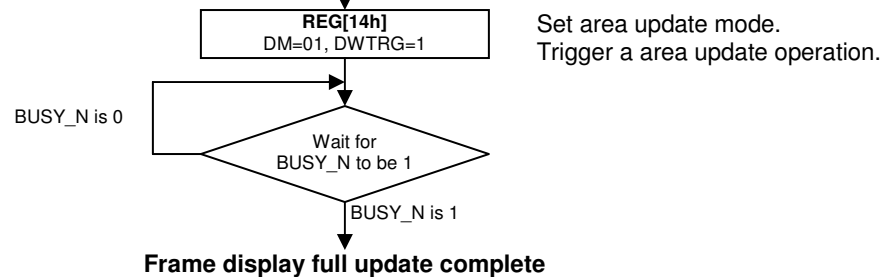
System in normal mode



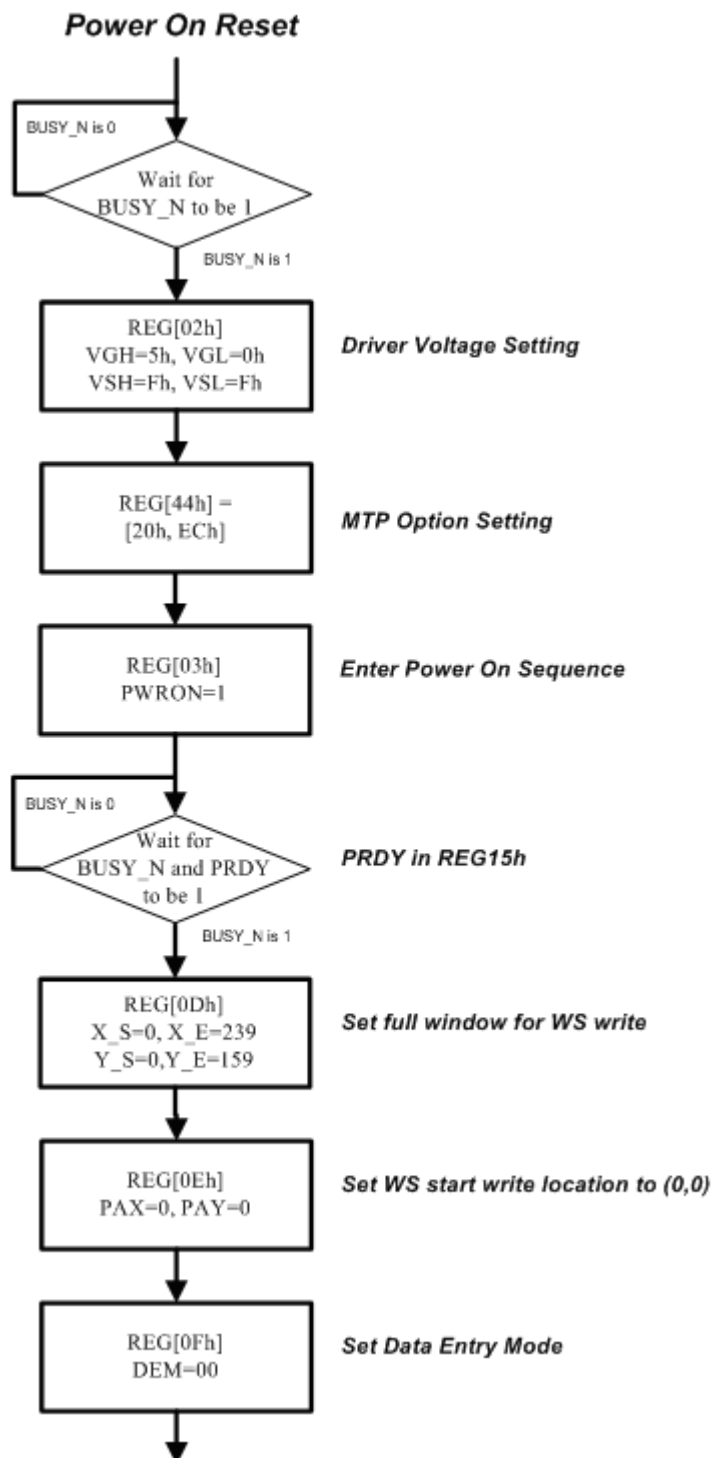
## ■ AREA WINDOW IMAGE UPDATE

System in normal mode

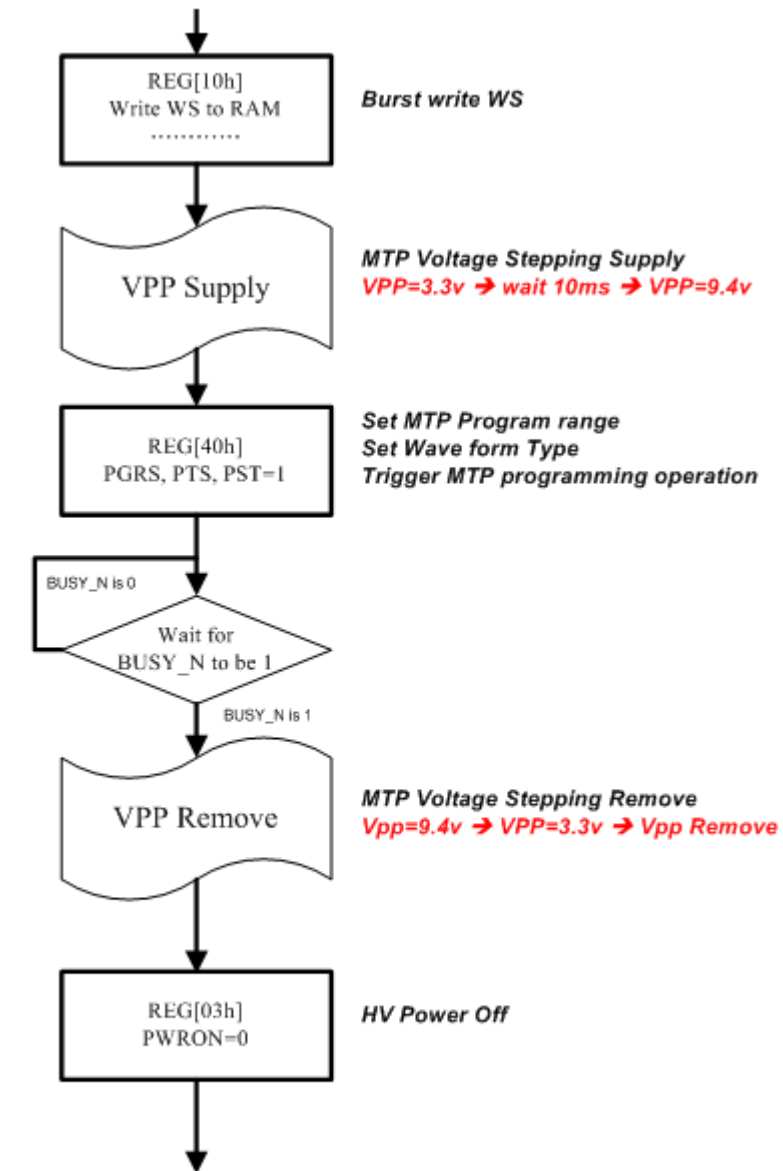
Host finished writing to image buffer



## ■ WS MTP PROGRAMMING

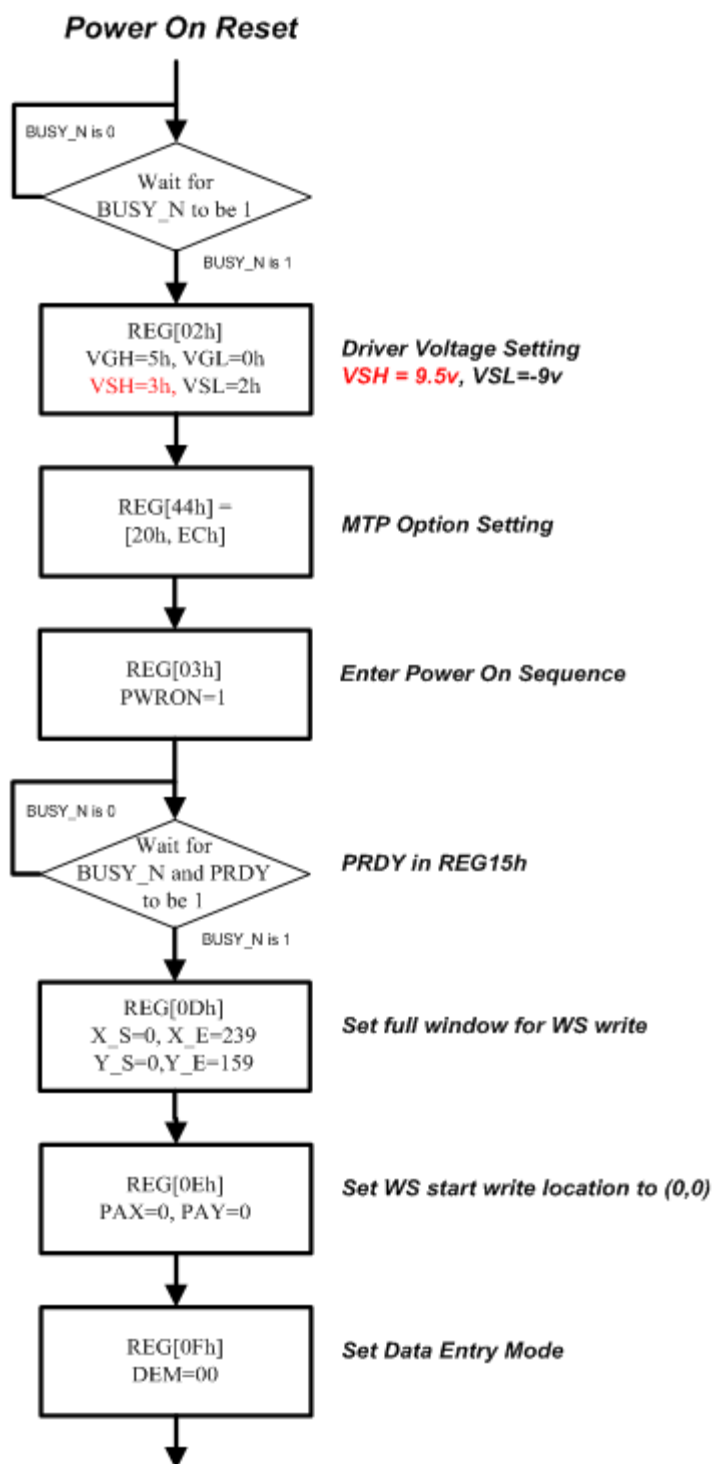
With External VPP Voltage

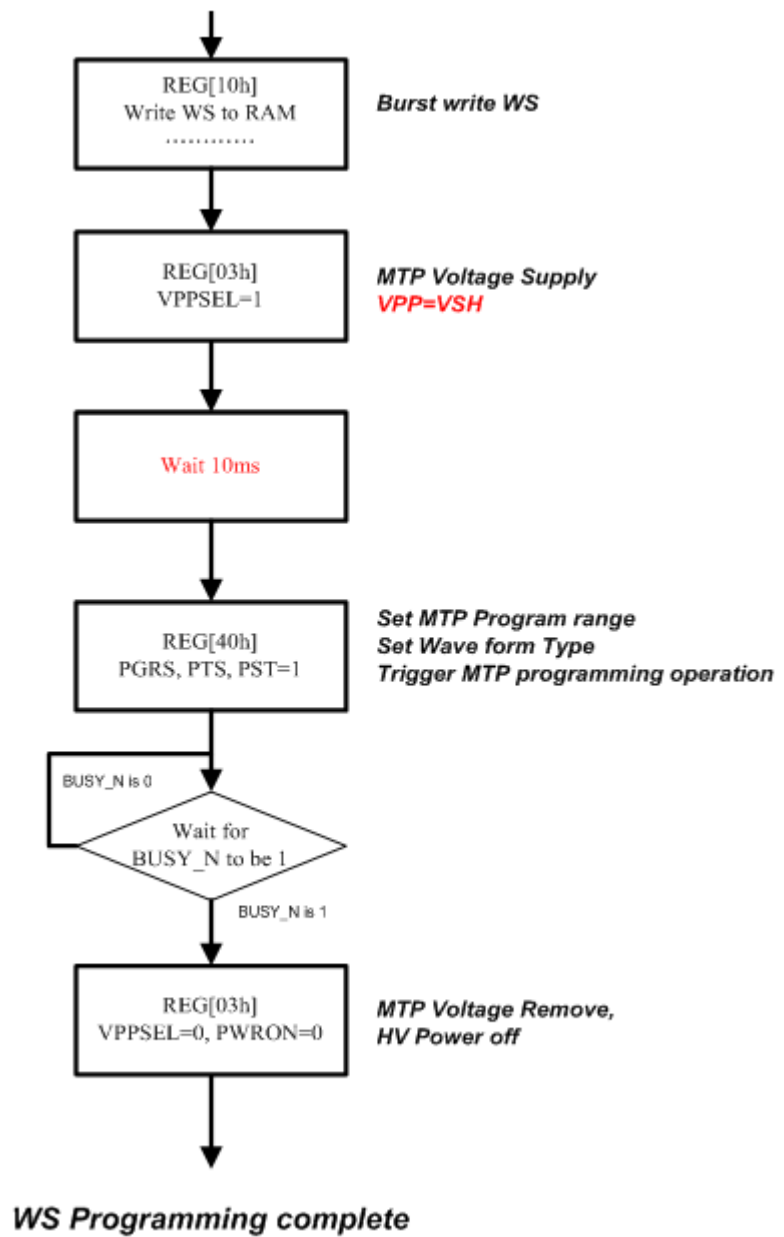




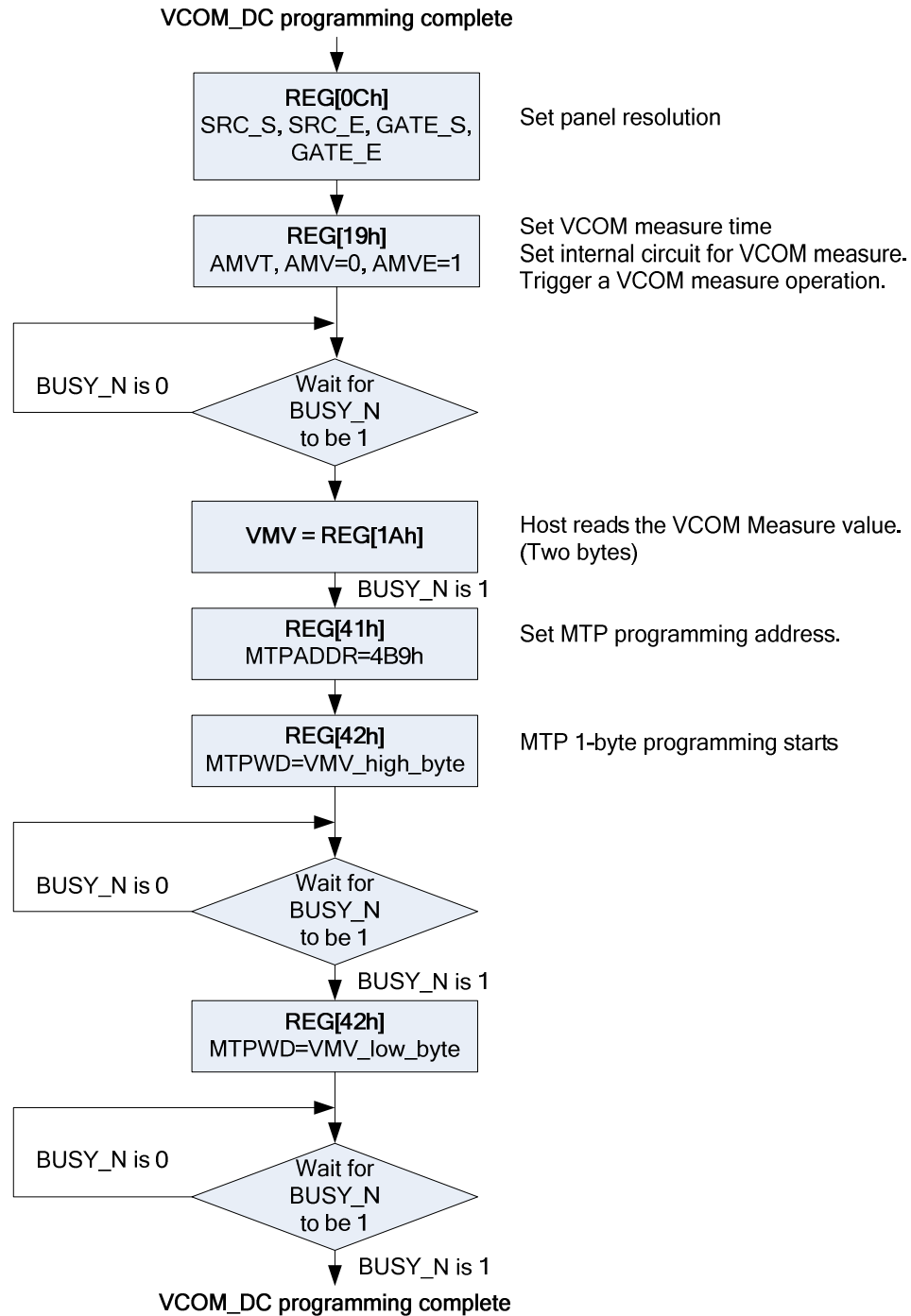
**WS Programming complete**

**Note:** VPP Current Clamp 10mA

With Internal VSH



## ■ VCOM SENSING AND MTP PROGRAMMING

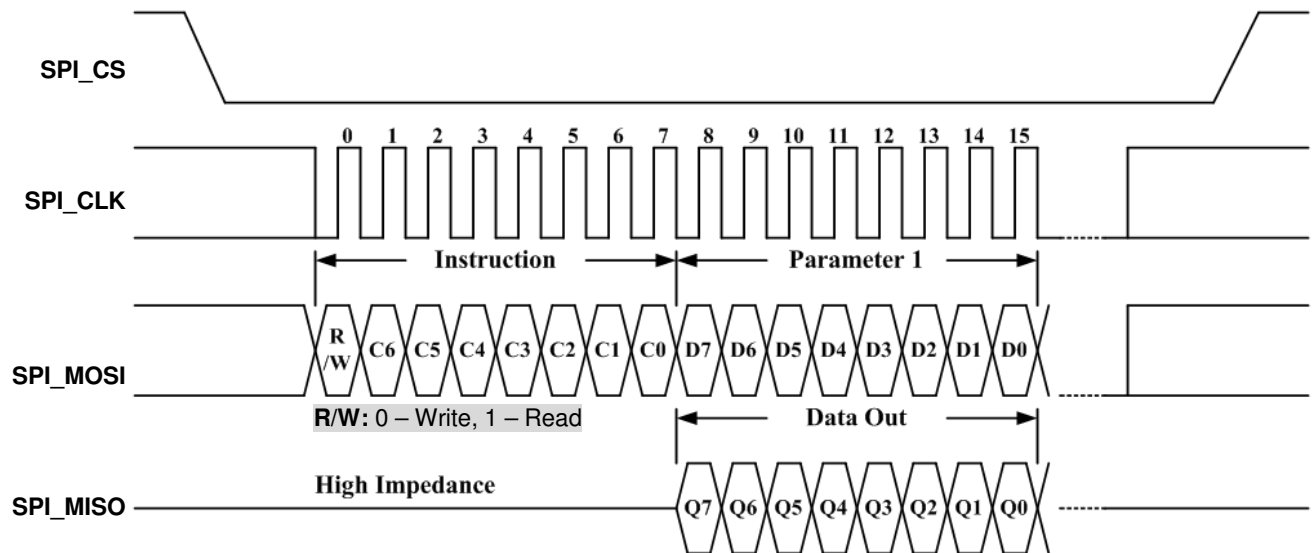


## HOST INTERFACES

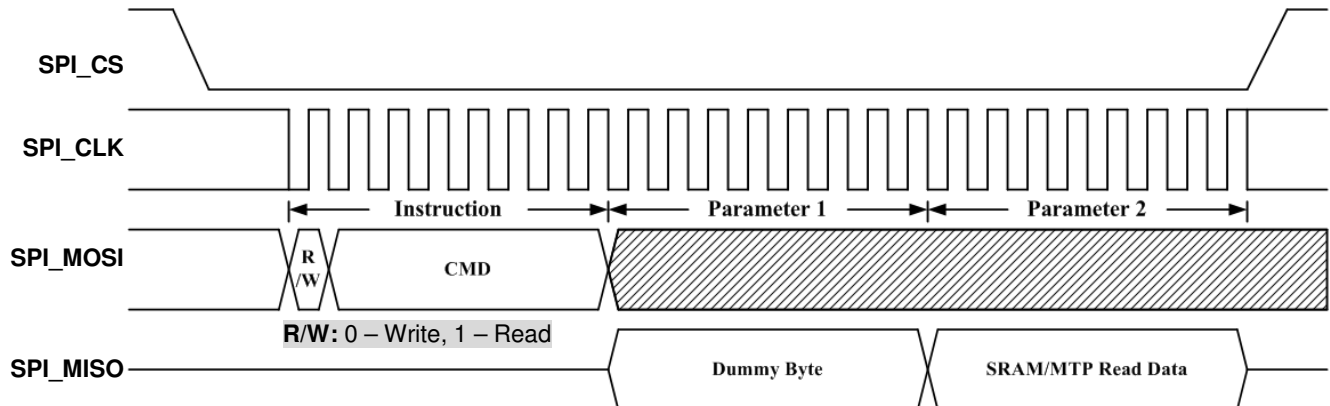
All commands, addresses and data are shifted in and out of the device, most significant bit first.

SPI\_MOSI (Serial Data Input) is sampled on the first rising edge of SPI\_CLK (Serial Clock) after SPI\_CS (Chip Select) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on SPI\_MOSI, each bit being latched on the rising edges of SPI\_CLK.

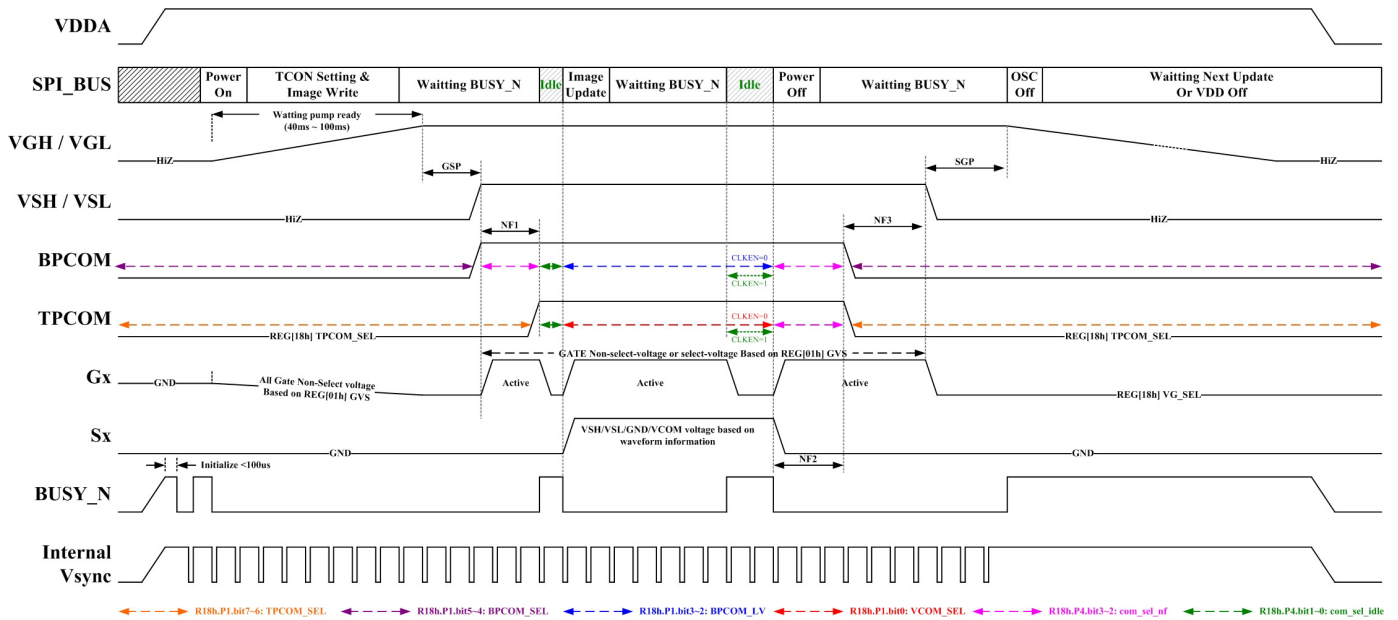
Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by data bytes or none. SPI\_CS must be driven high after the last bit of the instruction sequence has been shifted in.



Read SRAM data or MTP data need insert a dummy read.



## POWER MANAGEMENT



**ABSOLUTE MAXIMUM RATINGS**

Signal	Item	Min	Max.	Unit
VDD	Chip Supply voltage	- 0.3	+3.6	V
VDDIO	IO Supply voltage	-0.3	+3.6	V
<b>Source</b>				
VSH	Analog supply voltage – positive		+16	V
VSL	Analog supply voltage -- negative	-16		V
<b>Gate</b>				
VGH	Analog supply voltage – positive		+22	V
VGL	Analog supply voltage -- negative	-27		V
VGH-VGL	Voltage Range of VGH – VGL		42	V
IVGH	Input rush current for VGH	(TBD)	(TBD)	mA
IVGL	Input rush current for VGL	(TBD)	(TBD)	mA
TSTG	Storage temperature range	-40	+125	°C

**Warning:**

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

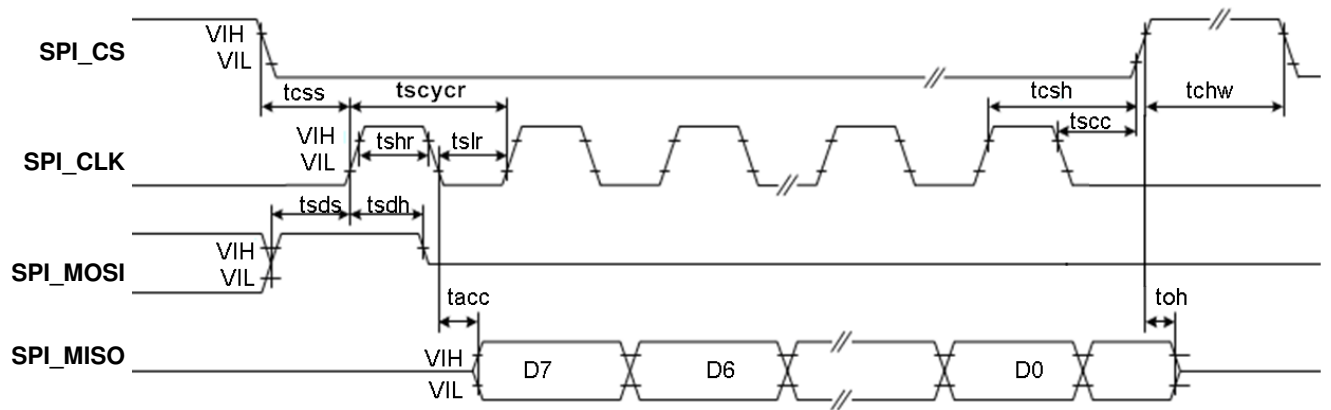
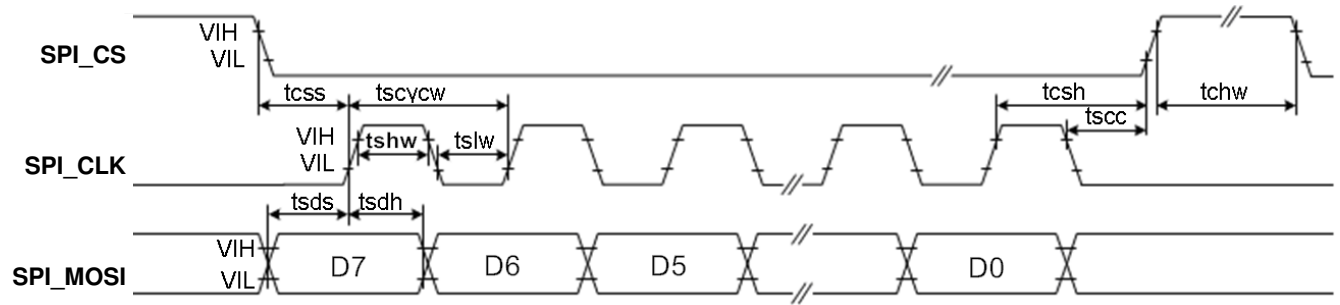
## DC CHARACTERISTICS

DIGITAL DC CHARACTERISTICS						
Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO Supply voltage		1.7	3.3	3.6	V
VDDA	Analog Supply voltage		3.0	3.3	3.6	V
VDD	Core Supply voltage	When EXTVDD=1, internal regulator tune off and using VDD to supply core power.	1.7	1.8	2.0	V
VPP	MTP supply voltage		8.5	9	9.5	V
VIL	LOW Level input voltage	Logic input pins	0	--	0.3xVDDIO	V
VIH	HIGH Level input voltage	Logic input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Logic output pins, IOH=400uA	VDDIO-0.4	--	--	V
VOL	LOW Level output voltage	Logic output pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
ISLVDD	Sleep current	Sleep mode		100		nA
ISTVDD	Standby current	Non-update, No load		35		uA
IOPVDD	Operating current		2	4		mA
RIN	Pull-up/down impedance			200		KΩ
RON	EPD driver ON resistance	ta=25°C, for Source			15	KΩ
		ta=25°C, for Gate			8	
Top	Operating temperature		-30		85	°C



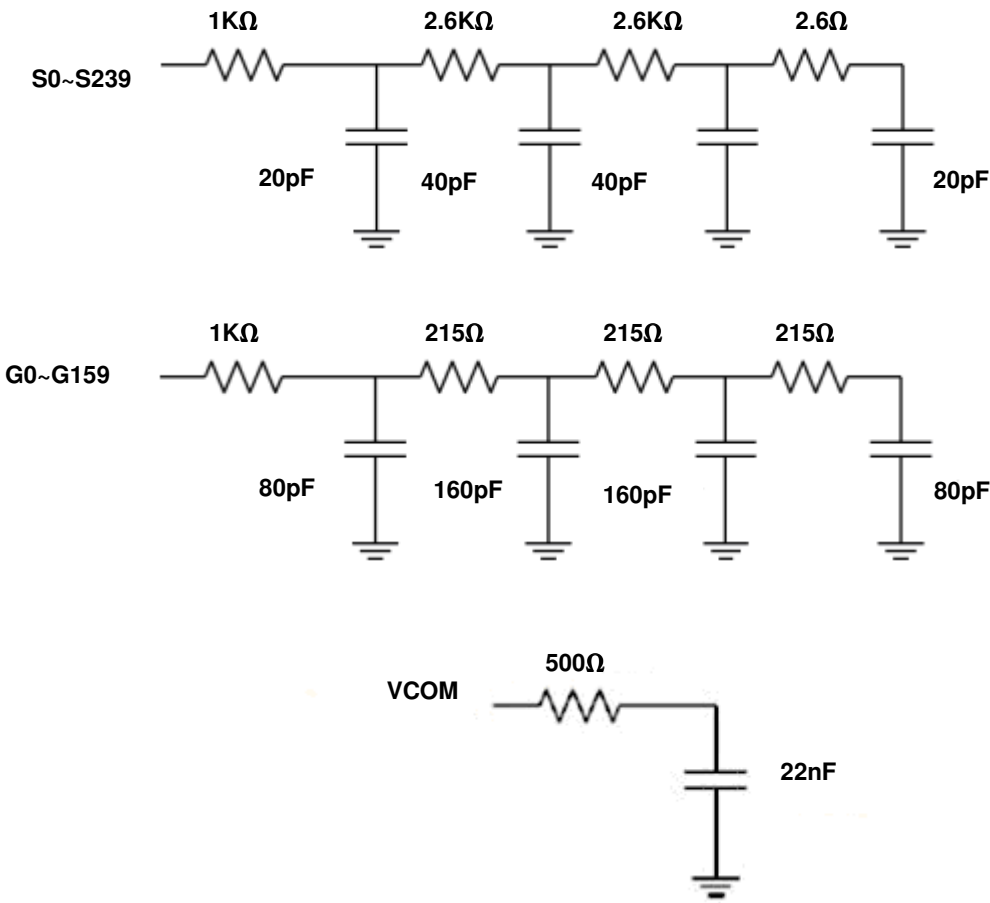
ANALOG DC CHARACTERISTICS						
Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VSH	Supply Voltage	For source driver/VCOM		15		V
dVSH	Supply Voltage Deviation		-300	0	300	mV
VSL	Supply Voltage	For source driver/VCOM		-15		V
dVSL	Supply Voltage Deviation		-300	0	300	mV
VSH+VSL	Voltage Range of VSH + VSL	VSH and VSL is symmetric	-200	0	200	mV
VCOM	VCOM Voltage		-4		10	V
dVCOM	VCOM Voltage Deviation	VCOM: 2V~5V	-300	0	300	mV
		VCOM<2V, or VCOM>5V	-500	0	500	mV
VGH-VGL	Voltage Range of VGH – VGL				42	V
VGL	VGL voltage Range	For gate driver	-27		-20	V
dVGL	VGL Supply Voltage Deviation		-500		500	mV
VGH	VGH voltage Range	For gate driver	15		22	V
dVGH	VGH Supply Voltage Deviation		-500		500	mV
I <sub>VDD</sub>	Digital deep sleep current	VDD OFF	--	0.02	--	uA
	Digital stand-by current	All stopped	--	5.0	50.0	uA
	Digital operating current		--	38	--	mA
I <sub>VDDIO</sub>	IO deep sleep current	VDD OFF	--	0.01	--	uA
	IO stand-by current	Booster OFF	--	0.03	--	uA
	IO operating current	No load	--	--	0.08	mA
I <sub>VDDA</sub>	DCDC deep sleep current	VDD OFF	--	0.03	--	uA
	DCDC stand-by current	Booster OFF	--	20	30.0	uA
		Booster ON	--	85	--	uA
	DCDC operating current	Source output VSH/VSL, duty=0.5, Period =126us, VCOM DC External cap: 415pF, NMOS=340pF	--	0.02	1	mA

## AC CHARACTERISTICS



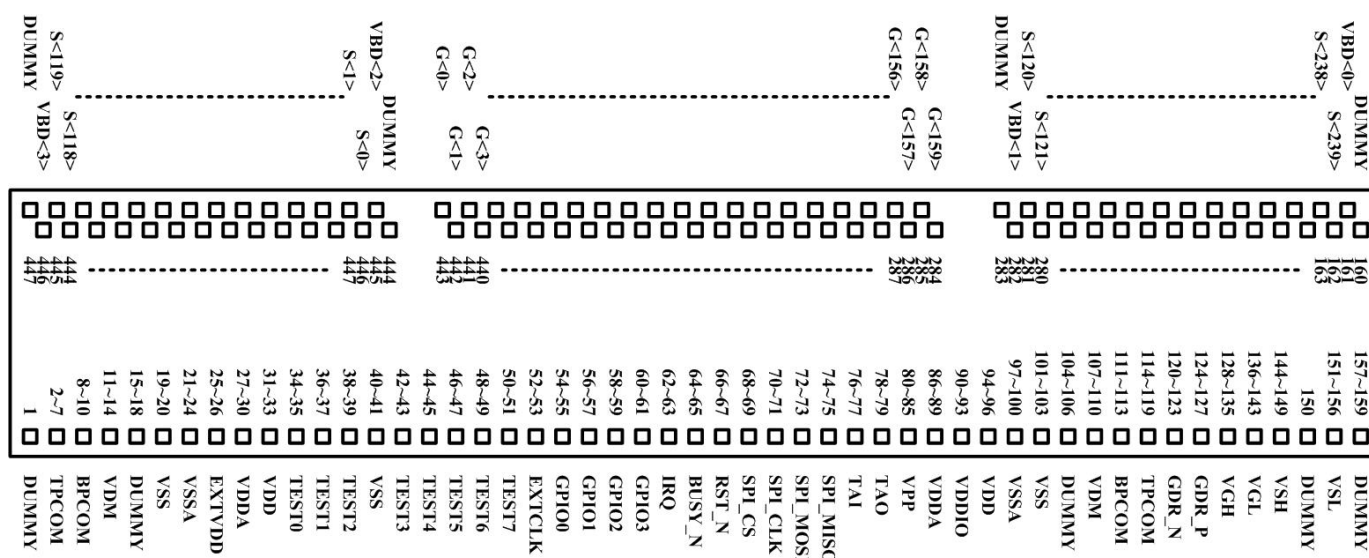
SYMBOL	SIGNAL	Parameter	Condition	MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION							
tcss	SPI_CS	Chip select setup time		60			ns
tcsh		Chip select hold time		65			ns
tsc		Chip select setup time		20			ns
tch		Chip select width		40			ns
tscycw	SPI_CLK	Serial clock cycle (Write)		100			ns
tsh		SPI_CLK “H” pulse width (Write)		40			ns
tsl		SPI_CLK “L ” pulse width (Write)		40			ns
tscycr		Serial clock cycle (Read)		150			ns
tshr		SPI_CLK “H” pulse width (Read)		60			ns
tslr		SPI_CLK “L ” pulse width (Read)		60			ns
tsds	SPI_MOSI	Data setup time		30			ns
tsdh		Data hold time		30			ns
tacc	SPI_MISO	Access time				30	ns
toh		Output disable time				20	ns
DRIVER							
trS		Source driver rise time	CL=120pF 10% to 90%		12	20	us
tFS		Source driver fall time			12	20	us
trG		Gate driver rise time	CL=480pF,		12	20	us

SYMBOL	SIGNAL	Parameter	Condition	MIN.	TYP.	MAX.	UNIT
tFG		Gate driver fall time	10% to 90%		12	20	us
trCOM		VCOM rise time	RL_COM=500ohm CL_COM=22nF		60		us
tFCOM		VCOM fall time			60		us
RC LOADING							
RL_S		Source driver output loading			8.8		K Ω
CL_S					120		pf
RL_G		Gate driver output loading			1.645		KΩ
CL_G					480		pf



## PHYSICAL DIMENSIONS

### Circuit / Bump View: (Temporary)



Die Size:  $(9640\mu\text{M} \pm 40\mu\text{M}) \times (1240\mu\text{M} \pm 40\mu\text{M})$

Die Thickness:  $280\mu\text{M} \pm 20\mu\text{M}$

Die TTV:  $(D_{\text{MAX}} - D_{\text{MIN}})$  within die  $\leq 2\mu\text{M}$

Bump Height:  $15 \mu\text{M} \pm 3\mu\text{M}$

$(H_{\text{MAX}} - H_{\text{MIN}})$  within die  $\leq 2\mu\text{M}$

Hardness: 65Hv  $\pm$  15Hv

Shear:  $\geq 5\text{g} / \text{mil}^2$

Bump Size: 18μM x 75 μM ± 2μM

Bump Pitch: 44μM

Bump Gap:  $26 \mu\text{M} \pm 3\mu\text{M}$

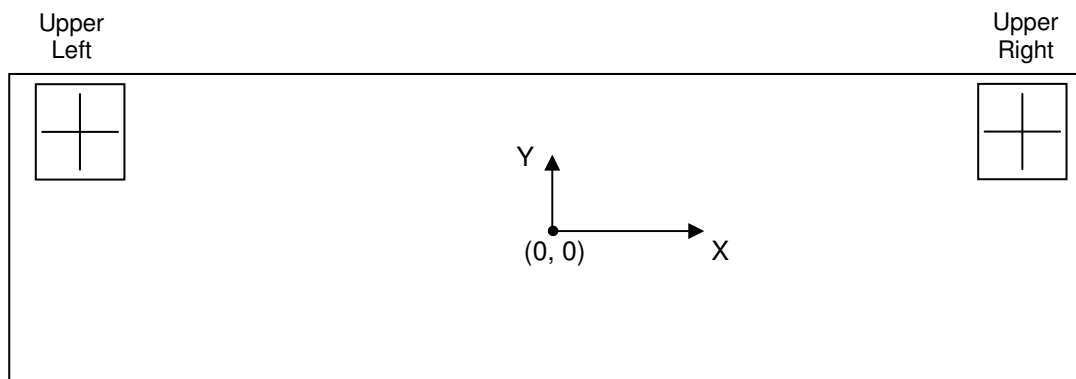
Bump Area: 1350  $\mu\text{M}^2$

Coordinate origin: Chip center

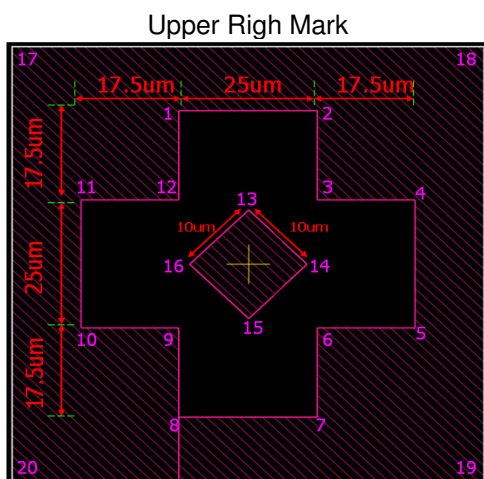
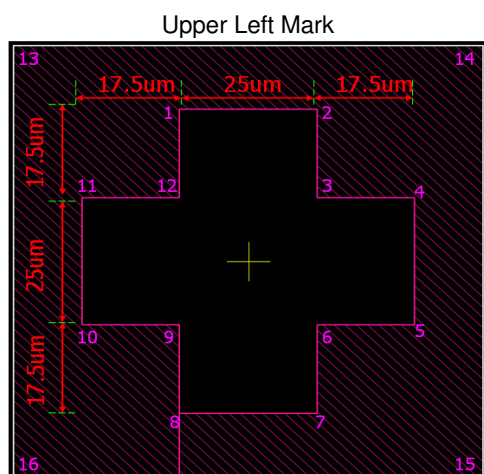
Pad reference:    Pad center

## ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:



Point Coordinates:

Point	Upper Left		Upper Right	
	X	Y	X	Y
Center	-4698	460	4718	460
1	-4710.5	490	4705.5	490
2	-4685.5	490	4730.5	490
3	-4685.5	472.5	4730.5	472.5
4	-4668	472.5	4748	472.5
5	-4668	447.5	4748	447.5
6	-4685.5	447.5	4730.5	447.5
7	-4685.5	430	4730.5	430
8	-4710.5	430	4705.5	430
9	-4710.5	447.5	4705.5	447.5
10	-4728	447.5	4688	447.5
11	-4728	472.5	4688	472.5
12	-4710.5	472.5	4705.5	472.5
13	-4740.5	502.5	4718	470.607
14	-4655.5	502.5	4728.607	460
15	-4655.5	417.5	4718	449.393
16	-4740.5	417.5	4707.393	460
17	—	—	4675.5	502.5
18	—	—	4760.5	502.5
19	—	—	4760.5	417.5
20	—	—	4675.5	417.5

## PAD COORDINATES

NO.	NAME	X	Y	W	H
1	DUMMY	-4740	-550	40	50
2	TPCOM	-4680	-550	40	50
3	TPCOM	-4620	-550	40	50
4	TPCOM	-4560	-550	40	50
5	TPCOM	-4500	-550	40	50
6	TPCOM	-4440	-550	40	50
7	TPCOM	-4380	-550	40	50
8	BPCOM	-4320	-550	40	50
9	BPCOM	-4260	-550	40	50
10	BPCOM	-4200	-550	40	50
11	VDM	-4140	-550	40	50
12	VDM	-4080	-550	40	50
13	VDM	-4020	-550	40	50
14	VDM	-3960	-550	40	50
15	DUMMY	-3900	-550	40	50
16	DUMMY	-3840	-550	40	50
17	DUMMY	-3780	-550	40	50
18	DUMMY	-3720	-550	40	50
19	VSS	-3660	-550	40	50
20	VSS	-3600	-550	40	50
21	VSSA	-3540	-550	40	50
22	VSSA	-3480	-550	40	50
23	VSSA	-3420	-550	40	50
24	VSSA	-3360	-550	40	50
25	EXTVDD	-3300	-550	40	50
26	EXTVDD	-3240	-550	40	50
27	VDDA	-3180	-550	40	50
28	VDDA	-3120	-550	40	50
29	VDDA	-3060	-550	40	50
30	VDDA	-3000	-550	40	50
31	VDD	-2940	-550	40	50
32	VDD	-2880	-550	40	50
33	VDD	-2820	-550	40	50
34	TEST0	-2760	-550	40	50
35	TEST0	-2700	-550	40	50
36	TEST1	-2640	-550	40	50
37	TEST1	-2580	-550	40	50
38	TEST2	-2520	-550	40	50
39	TEST2	-2460	-550	40	50
40	VSS	-2400	-550	40	50
41	VSS	-2340	-550	40	50
42	TEST3	-2280	-550	40	50
43	TEST3	-2220	-550	40	50
44	TEST4	-2160	-550	40	50
45	TEST4	-2100	-550	40	50
46	TEST5	-2040	-550	40	50
47	TEST5	-1980	-550	40	50
48	TEST6	-1920	-550	40	50
49	TEST6	-1860	-550	40	50
50	TEST7	-1800	-550	40	50
51	TEST7	-1740	-550	40	50
52	EXTCLK	-1680	-550	40	50
53	EXTCLK	-1620	-550	40	50
54	GPIO0	-1560	-550	40	50
55	GPIO0	-1500	-550	40	50
56	GPIO1	-1440	-550	40	50
57	GPIO1	-1380	-550	40	50
58	GPIO2	-1320	-550	40	50

NO.	NAME	X	Y	W	H
59	GPIO2	-1260	-550	40	50
60	GPIO3	-1200	-550	40	50
61	GPIO3	-1140	-550	40	50
62	IRQ	-1080	-550	40	50
63	IRQ	-1020	-550	40	50
64	BUSY_N	-960	-550	40	50
65	BUSY_N	-900	-550	40	50
66	RST_N	-840	-550	40	50
67	RST_N	-780	-550	40	50
68	SPI_CS	-720	-550	40	50
69	SPI_CS	-660	-550	40	50
70	SPI_CLK	-600	-550	40	50
71	SPI_CLK	-540	-550	40	50
72	SPI_MOSI	-480	-550	40	50
73	SPI_MOSI	-420	-550	40	50
74	SPI_MISO	-360	-550	40	50
75	SPI_MISO	-300	-550	40	50
76	TAI	-240	-550	40	50
77	TAI	-180	-550	40	50
78	TAO	-120	-550	40	50
79	TAO	-60	-550	40	50
80	VPP	0	-550	40	50
81	VPP	60	-550	40	50
82	VPP	120	-550	40	50
83	VPP	180	-550	40	50
84	VPP	240	-550	40	50
85	VPP	300	-550	40	50
86	VDDA	360	-550	40	50
87	VDDA	420	-550	40	50
88	VDDA	480	-550	40	50
89	VDDA	540	-550	40	50
90	VDDIO	600	-550	40	50
91	VDDIO	660	-550	40	50
92	VDDIO	720	-550	40	50
93	VDDIO	780	-550	40	50
94	VDD	840	-550	40	50
95	VDD	900	-550	40	50
96	VDD	960	-550	40	50
97	VSSA	1020	-550	40	50
98	VSSA	1080	-550	40	50
99	VSSA	1140	-550	40	50
100	VSSA	1200	-550	40	50
101	VSS	1260	-550	40	50
102	VSS	1320	-550	40	50
103	VSS	1380	-550	40	50
104	DUMMY	1440	-550	40	50
105	DUMMY	1500	-550	40	50
106	DUMMY	1560	-550	40	50
107	VDM	1620	-550	40	50
108	VDM	1680	-550	40	50
109	VDM	1740	-550	40	50
110	VDM	1800	-550	40	50
111	BPCOM	1860	-550	40	50
112	BPCOM	1920	-550	40	50
113	BPCOM	1980	-550	40	50
114	TPCOM	2040	-550	40	50
115	TPCOM	2100	-550	40	50
116	TPCOM	2160	-550	40	50

NO.	NAME	X	Y	W	H
117	TPCOM	2220	-550	40	50
118	TPCOM	2280	-550	40	50
119	TPCOM	2340	-550	40	50
120	GDR_N	2400	-550	40	50
121	GDR_N	2460	-550	40	50
122	GDR_N	2520	-550	40	50
123	GDR_N	2580	-550	40	50
124	GDR_P	2640	-550	40	50
125	GDR_P	2700	-550	40	50
126	GDR_P	2760	-550	40	50
127	GDR_P	2820	-550	40	50
128	VGH	2880	-550	40	50
129	VGH	2940	-550	40	50
130	VGH	3000	-550	40	50
131	VGH	3060	-550	40	50
132	VGH	3120	-550	40	50
133	VGH	3180	-550	40	50
134	VGH	3240	-550	40	50
135	VGH	3300	-550	40	50
136	VGL	3360	-550	40	50
137	VGL	3420	-550	40	50
138	VGL	3480	-550	40	50
139	VGL	3540	-550	40	50
140	VGL	3600	-550	40	50
141	VGL	3660	-550	40	50
142	VGL	3720	-550	40	50
143	VGL	3780	-550	40	50
144	VSH	3840	-550	40	50
145	VSH	3900	-550	40	50
146	VSH	3960	-550	40	50
147	VSH	4020	-550	40	50
148	VSH	4080	-550	40	50
149	VSH	4140	-550	40	50
150	DUMMY	4200	-550	40	50
151	VSL	4260	-550	40	50
152	VSL	4320	-550	40	50
153	VSL	4380	-550	40	50
154	VSL	4440	-550	40	50
155	VSL	4500	-550	40	50
156	VSL	4560	-550	40	50
157	DUMMY	4620	-550	40	50
158	DUMMY	4680	-550	40	50
159	DUMMY	4740	-550	40	50
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175	S<226>	4279	537.5	18	75
176	S<225>	4257	417.5	18	75

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183	S<218>	4103	537.5	18	75
184	S<217>	4081	417.5	18	75
185	S<216>	4059	537.5	18	75
186	S<215>	4037	417.5	18	75
187	S<214>	4015	537.5	18	75
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189	S<212>	3971	537.5	18	75
190	S<211>	3949	417.5	18	75
191	S<210>	3927	537.5	18	75
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193	S<208>	3883	537.5	18	75
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196	S<205>	3817	417.5	18	75
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211	S<190>	3487	537.5	18	75
212	S<189>	3465	417.5	18	75
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242	S<159>	2805	417.5	18	75
243	S<158>	2783	537.5	18	75
244	S<157>	2761	417.5	18	75
245	S<156>	2739	537.5	18	75
246	S<155>	2717	417.5	18	75
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249	S<152>	2651	537.5	18	75
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253	S<148>	2563	537.5	18	75
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258	S<143>	2453	417.5	18	75
259	S<142>	2431	537.5	18	75
260	S<141>	2409	417.5	18	75
261	S<140>	2387	537.5	18	75
262	S<139>	2365	417.5	18	75
263	S<138>	2343	537.5	18	75
264	S<137>	2321	417.5	18	75
265	S<136>	2299	537.5	18	75
266	S<135>	2277	417.5	18	75
267	S<134>	2255	537.5	18	75
268	S<133>	2233	417.5	18	75
269	S<132>	2211	537.5	18	75
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271	S<130>	2167	537.5	18	75
272	S<129>	2145	417.5	18	75
273	S<128>	2123	537.5	18	75
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275	S<126>	2079	537.5	18	75
276	S<125>	2057	417.5	18	75
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281	S<120>	1947	537.5	18	75
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283	DUMMY	1903	537.5	18	75
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287	G<156>	1683	537.5	18	75
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289	G<154>	1639	537.5	18	75
290	G<153>	1617	417.5	18	75
291	G<152>	1595	537.5	18	75
292	G<151>	1573	417.5	18	75
293	G<150>	1551	537.5	18	75
294	G<149>	1529	417.5	18	75
295	G<148>	1507	537.5	18	75
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NO.	NAME	X	Y	W	H
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303	G<140>	1331	537.5	18	75
304	G<139>	1309	417.5	18	75
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306	G<137>	1265	417.5	18	75
307	G<136>	1243	537.5	18	75
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310	G<133>	1177	417.5	18	75
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313	G<130>	1111	537.5	18	75
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315	G<128>	1067	537.5	18	75
316	G<127>	1045	417.5	18	75
317	G<126>	1023	537.5	18	75
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319	G<124>	979	537.5	18	75
320	G<123>	957	417.5	18	75
321	G<122>	935	537.5	18	75
322	G<121>	913	417.5	18	75
323	G<120>	891	537.5	18	75
324	G<119>	869	417.5	18	75
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326	G<117>	825	417.5	18	75
327	G<116>	803	537.5	18	75
328	G<115>	781	417.5	18	75
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332	G<111>	693	417.5	18	75
333	G<110>	671	537.5	18	75
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356	G<87>	165	417.5	18	75



NO.	NAME	X	Y	W	H
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364	G<79>	-11	417.5	18	75
365	G<78>	-33	537.5	18	75
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367	G<76>	-77	537.5	18	75
368	G<75>	-99	417.5	18	75
369	G<74>	-121	537.5	18	75
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371	G<72>	-165	537.5	18	75
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377	G<66>	-297	537.5	18	75
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380	G<63>	-363	417.5	18	75
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384	G<59>	-451	417.5	18	75
385	G<58>	-473	537.5	18	75
386	G<57>	-495	417.5	18	75
387	G<56>	-517	537.5	18	75
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389	G<54>	-561	537.5	18	75
390	G<53>	-583	417.5	18	75
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393	G<50>	-649	537.5	18	75
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395	G<48>	-693	537.5	18	75
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407	G<36>	-957	537.5	18	75
408	G<35>	-979	417.5	18	75
409	G<34>	-1001	537.5	18	75
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411	G<32>	-1045	537.5	18	75
412	G<31>	-1067	417.5	18	75
413	G<30>	-1089	537.5	18	75
414	G<29>	-1111	417.5	18	75
415	G<28>	-1133	537.5	18	75
416	G<27>	-1155	417.5	18	75

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421	G<22>	-1265	537.5	18	75
422	G<21>	-1287	417.5	18	75
423	G<20>	-1309	537.5	18	75
424	G<19>	-1331	417.5	18	75
425	G<18>	-1353	537.5	18	75
426	G<17>	-1375	417.5	18	75
427	G<16>	-1397	537.5	18	75
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436	G<7>	-1595	417.5	18	75
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467	S<21>	-2409	537.5	18	75
468	S<22>	-2431	417.5	18	75
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471	S<25>	-2497	537.5	18	75
472	S<26>	-2519	417.5	18	75
473	S<27>	-2541	537.5	18	75
474	S<28>	-2563	417.5	18	75
475	S<29>	-2585	537.5	18	75
476	S<30>	-2607	417.5	18	75

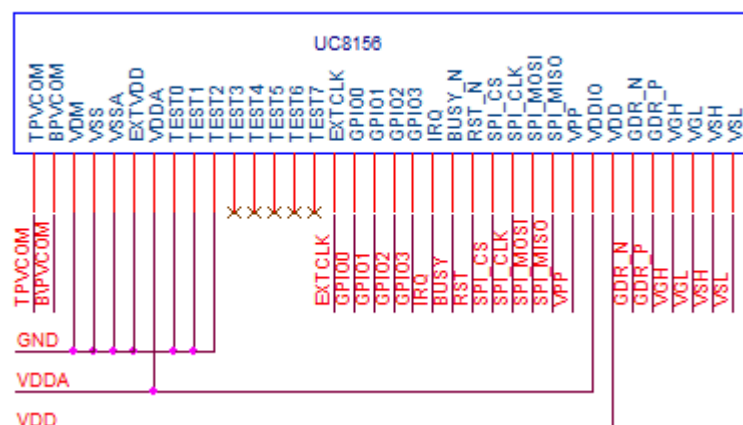
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478	S<32>	-2651	417.5	18	75
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482	S<36>	-2739	417.5	18	75
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484	S<38>	-2783	417.5	18	75
485	S<39>	-2805	537.5	18	75
486	S<40>	-2827	417.5	18	75
487	S<41>	-2849	537.5	18	75
488	S<42>	-2871	417.5	18	75
489	S<43>	-2893	537.5	18	75
490	S<44>	-2915	417.5	18	75
491	S<45>	-2937	537.5	18	75
492	S<46>	-2959	417.5	18	75
493	S<47>	-2981	537.5	18	75
494	S<48>	-3003	417.5	18	75
495	S<49>	-3025	537.5	18	75
496	S<50>	-3047	417.5	18	75
497	S<51>	-3069	537.5	18	75
498	S<52>	-3091	417.5	18	75
499	S<53>	-3113	537.5	18	75
500	S<54>	-3135	417.5	18	75
501	S<55>	-3157	537.5	18	75
502	S<56>	-3179	417.5	18	75
503	S<57>	-3201	537.5	18	75
504	S<58>	-3223	417.5	18	75
505	S<59>	-3245	537.5	18	75
506	S<60>	-3267	417.5	18	75
507	S<61>	-3289	537.5	18	75
508	S<62>	-3311	417.5	18	75
509	S<63>	-3333	537.5	18	75
510	S<64>	-3355	417.5	18	75
511	S<65>	-3377	537.5	18	75
512	S<66>	-3399	417.5	18	75
513	S<67>	-3421	537.5	18	75
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515	S<69>	-3465	537.5	18	75
516	S<70>	-3487	417.5	18	75
517	S<71>	-3509	537.5	18	75
518	S<72>	-3531	417.5	18	75
519	S<73>	-3553	537.5	18	75
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521	S<75>	-3597	537.5	18	75
522	S<76>	-3619	417.5	18	75
523	S<77>	-3641	537.5	18	75

NO.	NAME	X	Y	W	H
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525	S<79>	-3685	537.5	18	75
526	S<80>	-3707	417.5	18	75
527	S<81>	-3729	537.5	18	75
528	S<82>	-3751	417.5	18	75
529	S<83>	-3773	537.5	18	75
530	S<84>	-3795	417.5	18	75
531	S<85>	-3817	537.5	18	75
532	S<86>	-3839	417.5	18	75
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534	S<88>	-3883	417.5	18	75
535	S<89>	-3905	537.5	18	75
536	S<90>	-3927	417.5	18	75
537	S<91>	-3949	537.5	18	75
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539	S<93>	-3993	537.5	18	75
540	S<94>	-4015	417.5	18	75
541	S<95>	-4037	537.5	18	75
542	S<96>	-4059	417.5	18	75
543	S<97>	-4081	537.5	18	75
544	S<98>	-4103	417.5	18	75
545	S<99>	-4125	537.5	18	75
546	S<100>	-4147	417.5	18	75
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550	S<104>	-4235	417.5	18	75
551	S<105>	-4257	537.5	18	75
552	S<106>	-4279	417.5	18	75
553	S<107>	-4301	537.5	18	75
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556	S<110>	-4367	417.5	18	75
557	S<111>	-4389	537.5	18	75
558	S<112>	-4411	417.5	18	75
559	S<113>	-4433	537.5	18	75
560	S<114>	-4455	417.5	18	75
561	S<115>	-4477	537.5	18	75
562	S<116>	-4499	417.5	18	75
563	S<117>	-4521	537.5	18	75
564	S<118>	-4543	417.5	18	75
565	S<119>	-4565	537.5	18	75
566	VBD<3>	-4587	417.5	18	75
567	DUMMY	-4609	537.5	18	75

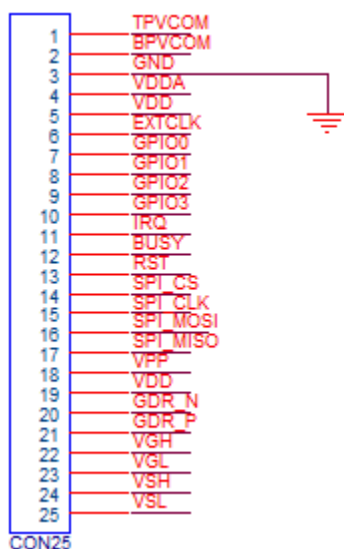
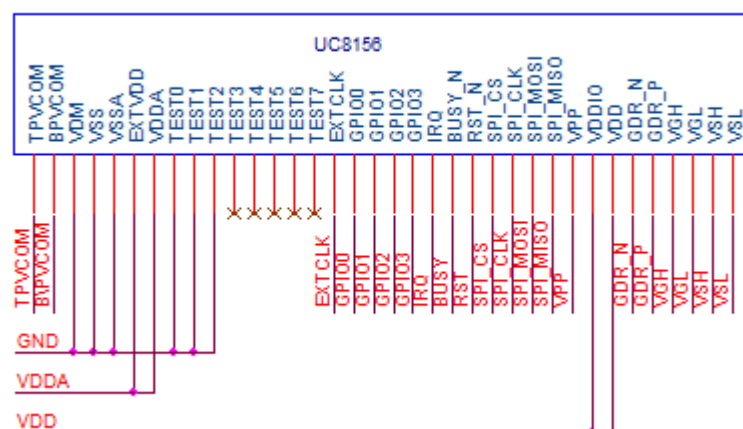
## APPLICATION

Application diagram with SPI interface (Temporary)

## For 3.3V Interface

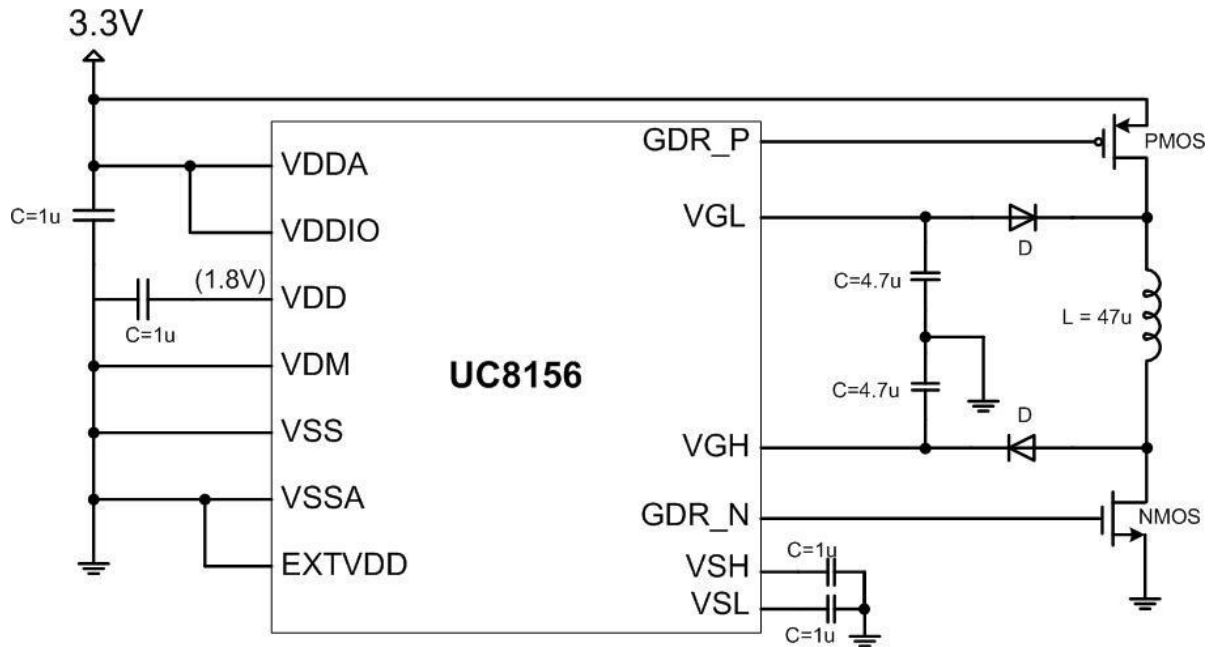
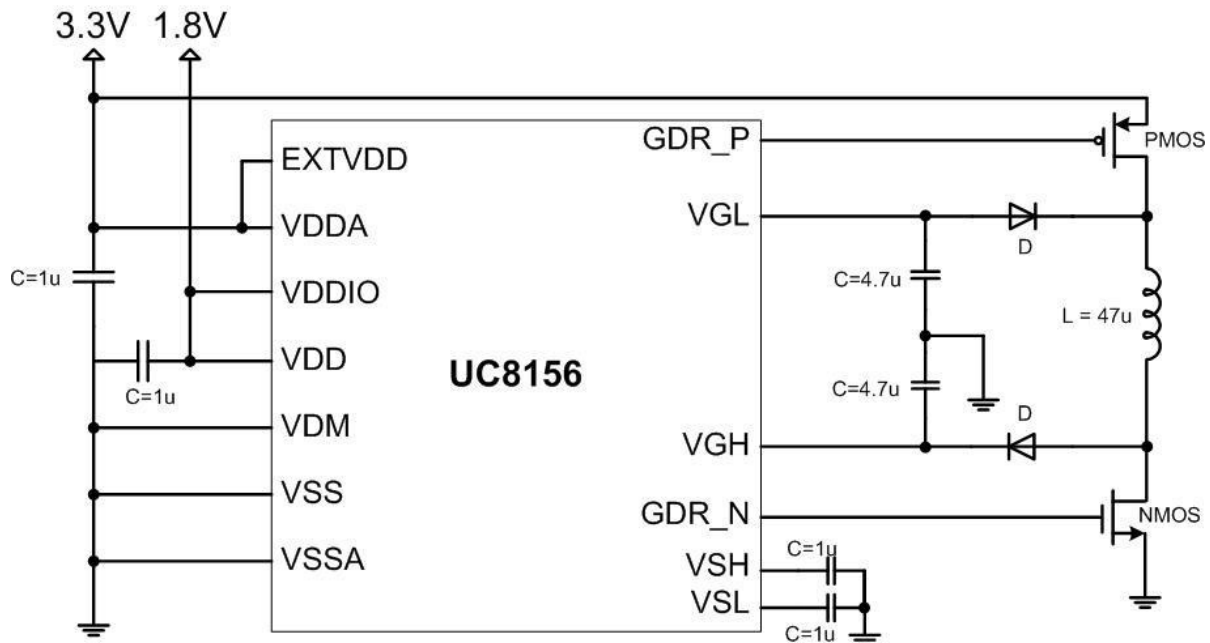


## For 1.8V Interface



Pin Name	Connect to	LCM output	Note
VDDA	Interface	V	
VDD	Interface	V	
VDDIO	Interface	V	Either 3.0V or 1.8V - needs to be wired out
EXTVDD	GND / VDDA	X	When interface=3.3V, EXTVDD connects to GND When interface=1.8V, EXTVDD connects to VDDA
VSSA	GND	V	Connected together on the panel.
VSS	Interface	V	
VDM	GND	V	
VPP	Interface	V	If not used, leave them open.
SPI_CS	Interface	V	
SPI_CLK	Interface	V	
SPI_MOSI	Interface	V	
SPI_MISO	Interface	V	
TAI		X	Leave them open.
TAO		X	Leave them open.
Test0~7		X	Test pins. Reserved for testing. Test0~Test2: connect to GND. Test3~Test7: leave them open.
IRQ	Interface	V	Connect to MCU. If not used, leave them open.
GPIO_0	Interface	V	Sensor trigger.
GPIO_1	Interface	V	If not used, leave them open
GPIO_2	Interface	V	Used to connect an external temperature sensor.
GPIO_3	Interface	V	If not used, leave them open.
EXCLK	Interface	V	If not used, connect to GND.
RST_N	Interface	V	
BUSY_N	Interface	V	
TPCOM	Interface	V	
BPCOM	Interface	V	
GDR_N	Interface	V	
GDR_P	Interface	V	
VGH	Interface	V	
VGL	Interface	V	
VSH	Interface	V	
VSL	Interface	V	

## Booster Connection Diagram (Temporary)

**For 3.3V Interface**

**For 1.8V Interface**


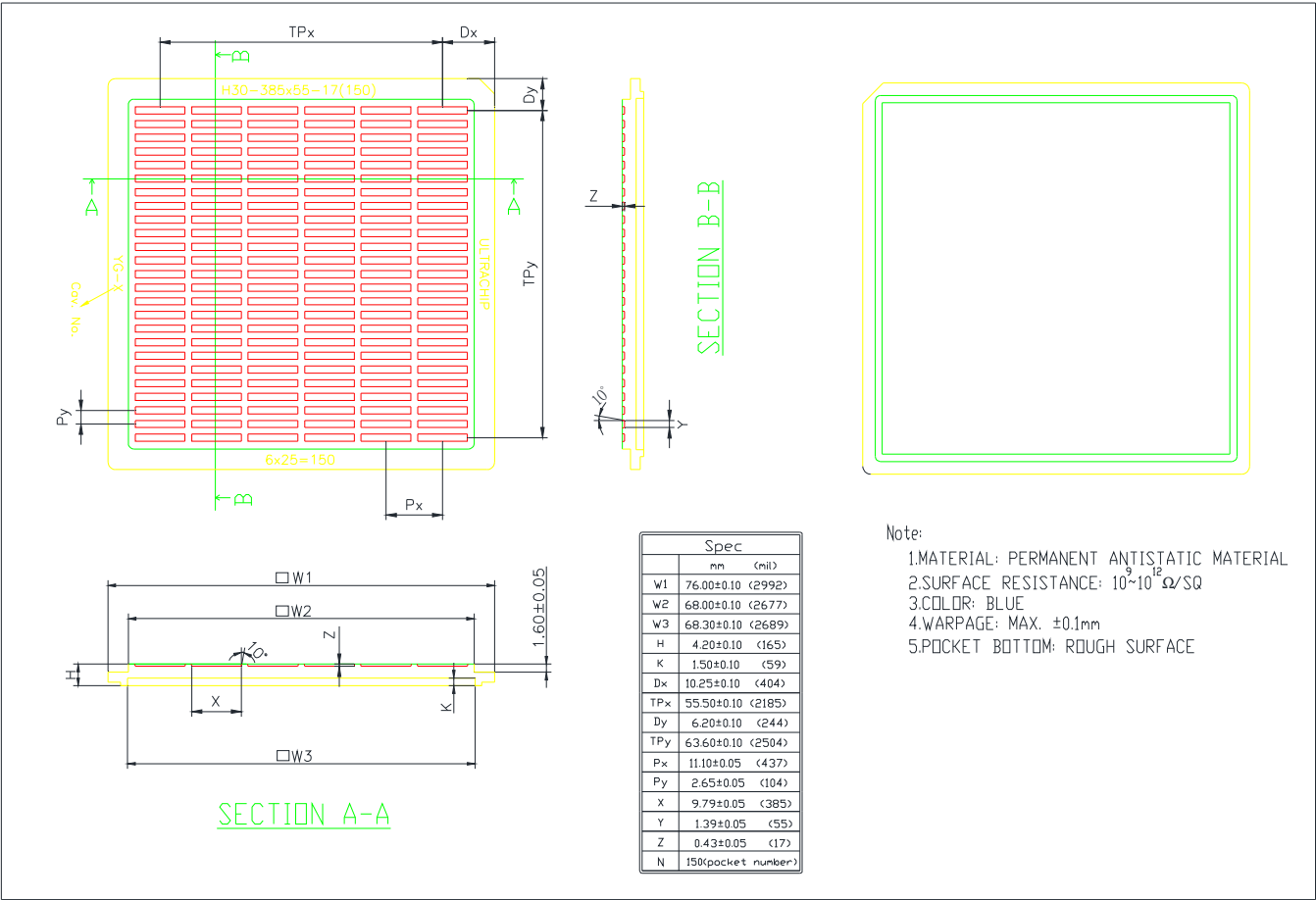
For Diode,

- $I_{FSM}$  (Peak Forward Surge Current) > 500mA
- $V_{RM}$  (Peak Reverse Voltage) > 32V
- $I_R$  (Reverse Leakage Current) < 1mA

For MOS

- $V_{DS}$  (Drain-Source Breakdown Voltage), PMOS  $V_{DS}$  > 32V, NMOS  $V_{DS}$  > 25V
- $I_D$  (Continuous Drain Current) > 500 mA
- $V_{TH}$  (Gate-Source Threshold Voltage) < 1.8V
- $C_{ISS}$  (Input Capacitance) < 200pF

TRAY INFORMATION



**REVISION HISTORY**

Revision	Contents	Date
0.6	(First Release)	Nov. 25, 2016
0.7	Some unused registers are removed.	Dec. 21, 2016
	The Note for DC Characteristics is removed.	
0.71	The description of command (5) Boost Setting is enriched.	May 8, 2017