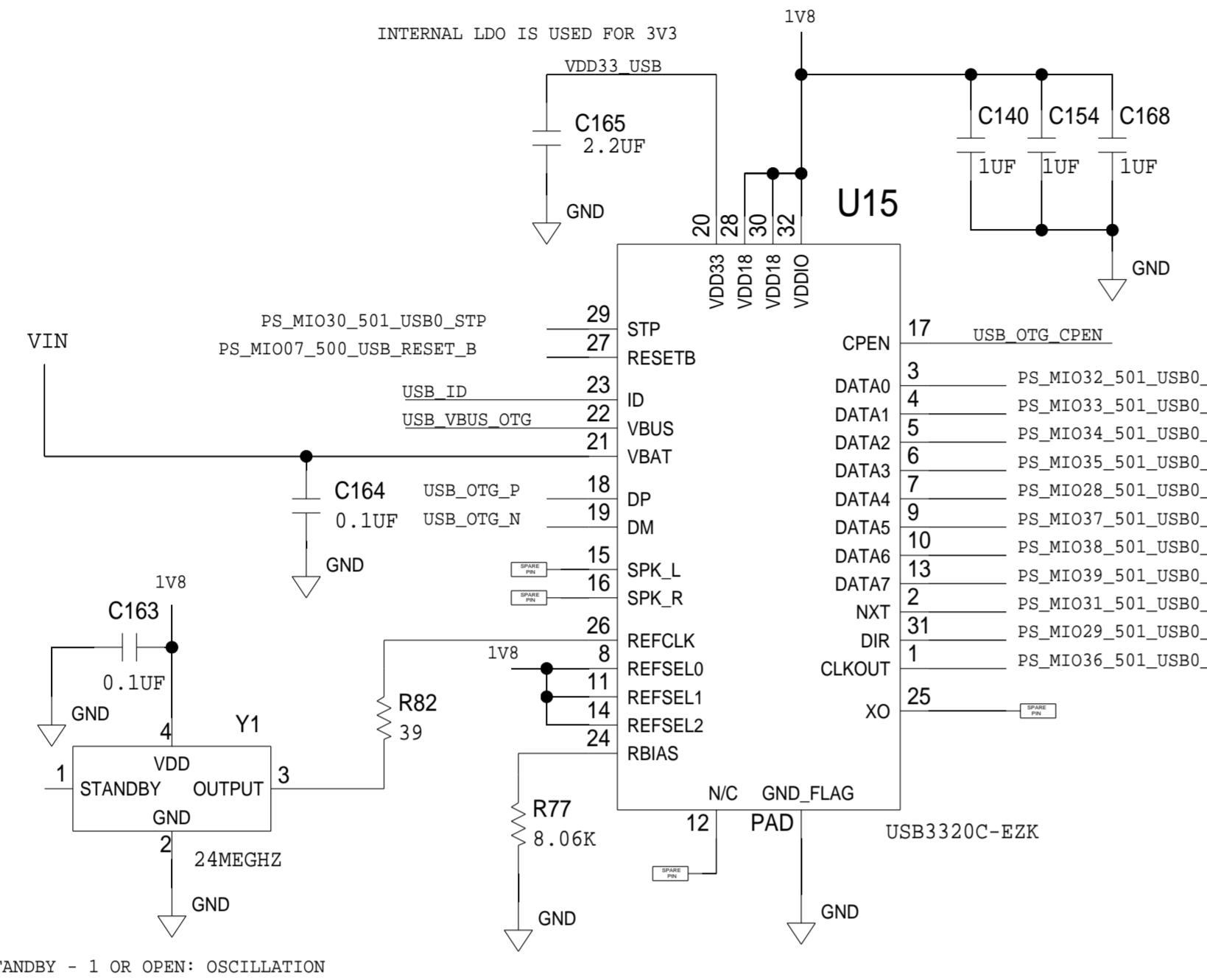




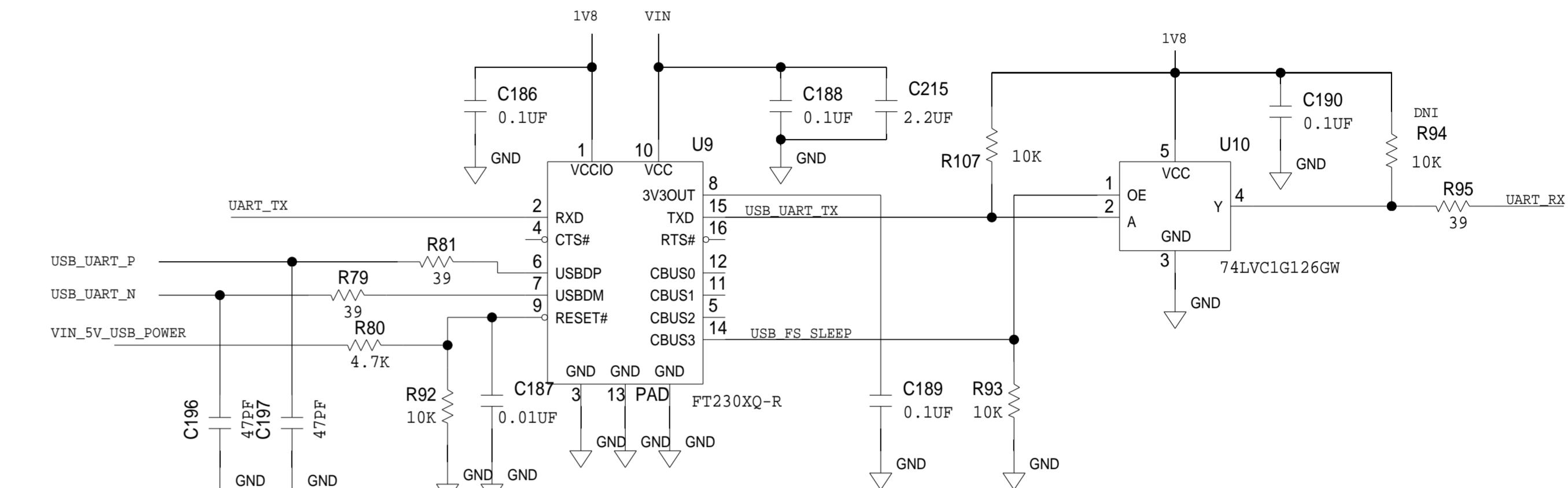
## REVISIONS

REV	DESCRIPTION	DATE	APPROVED

# USB PHY

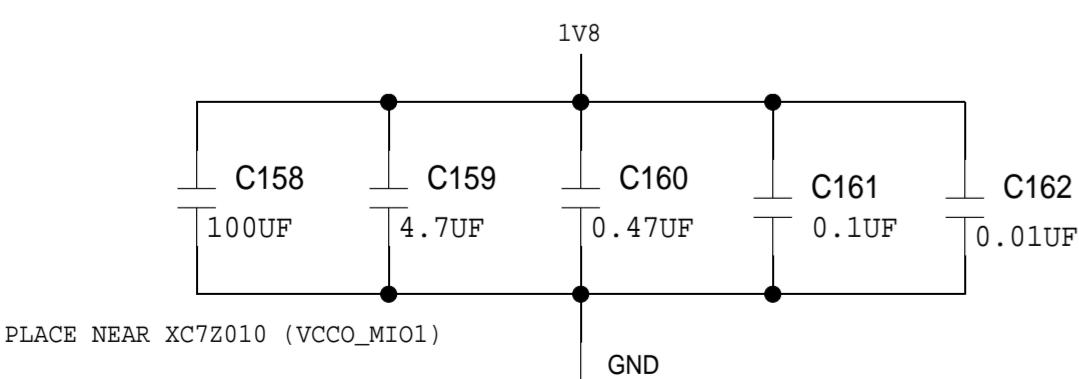
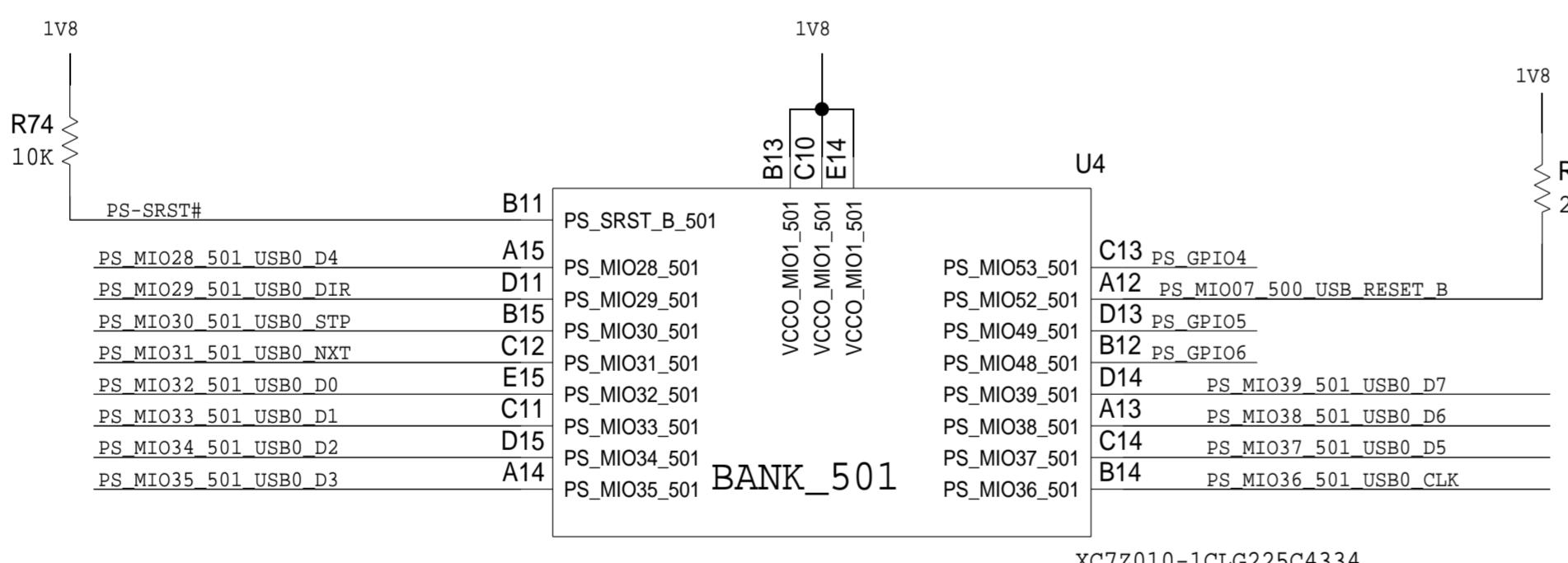


# USB TO UART



# Released to Production

ZYNQ BANK 501



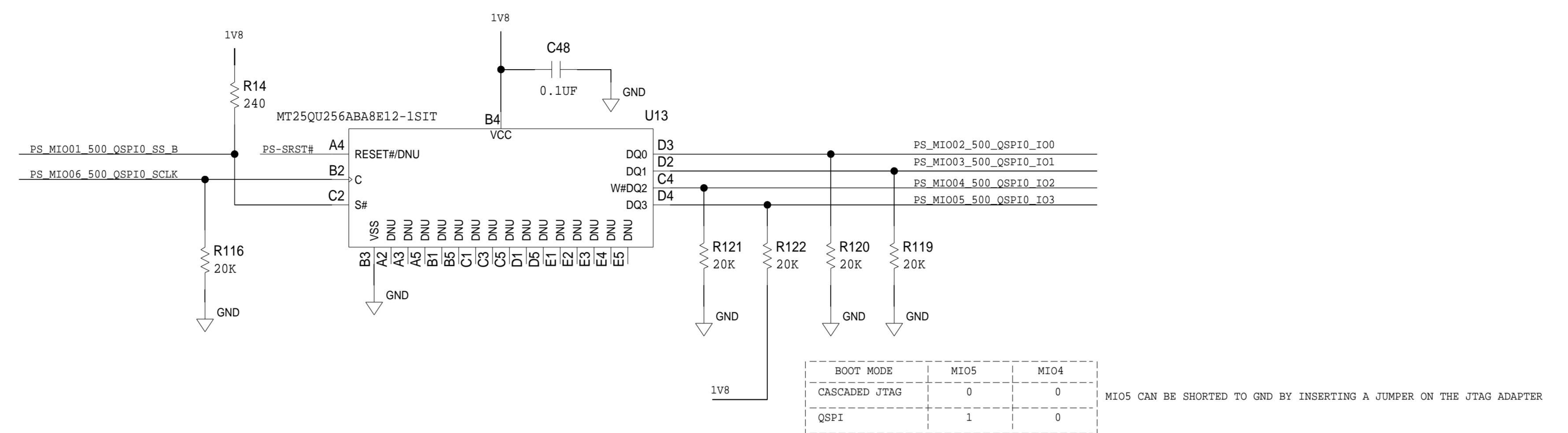
SCHEMATIC

HW TYPE : Customer Evaluation Z		
Product(s) : ad9363		
: NA		
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_043758	REV D
PTD ENGINEER M. BANCISOR	SIZE <b>D</b>	SCALE 1:1
		SHEET 2 OF 9

## REVISIONS

REV	DESCRIPTION	DATE	APPROVED

## QSPI FLASH

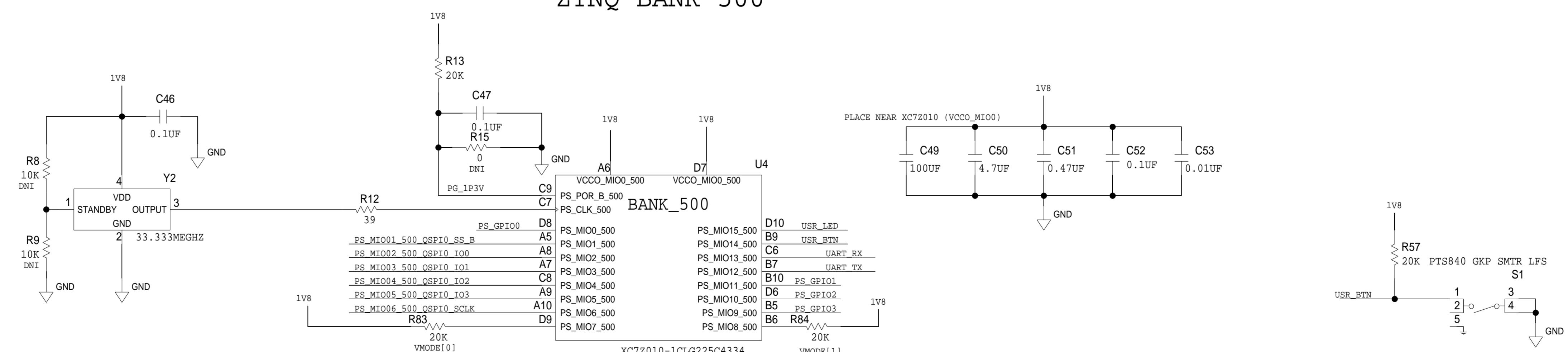


WHEN USING THE ADAPTER, AND WANTING TO HAVE JTAG BOOT (DEVICE DOESN'T BOOT U-BOOT, OR KERNEL):  
 - INSERT THE JUMPER ON THE ADAPTER (JTAG BOOT)  
 - POWER UP PLUTO  
 - REMOVE THE JUMPER ON THE ADAPTER, SO YOU CAN TALK TO THE SPI FLASH  
 - DEBUG AS NORMAL.

<https://www.xilinx.com/support/answers/47596.html>

Released to Production

## ZYNQ BANK 500



## SCHEMATIC

HW TYPE : Customer Evaluation Z  
 Product(s) : ad9363  
 : NA

DESIGN VIEW  
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DRAWING NO.  
 02\_043758

REV  
 D

PTD ENGINEER  
 M. BANCISOR

SIZE  
 D

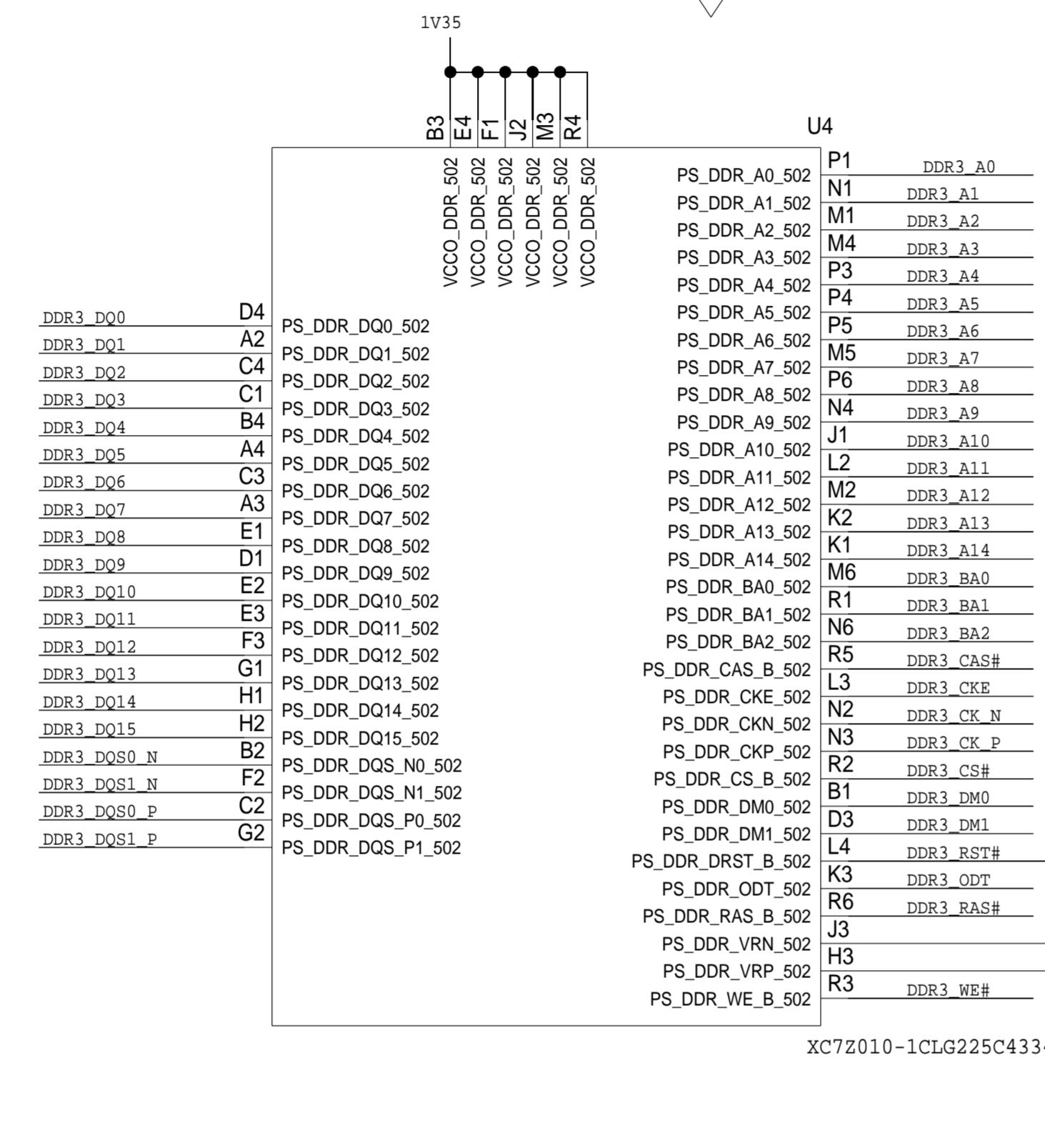
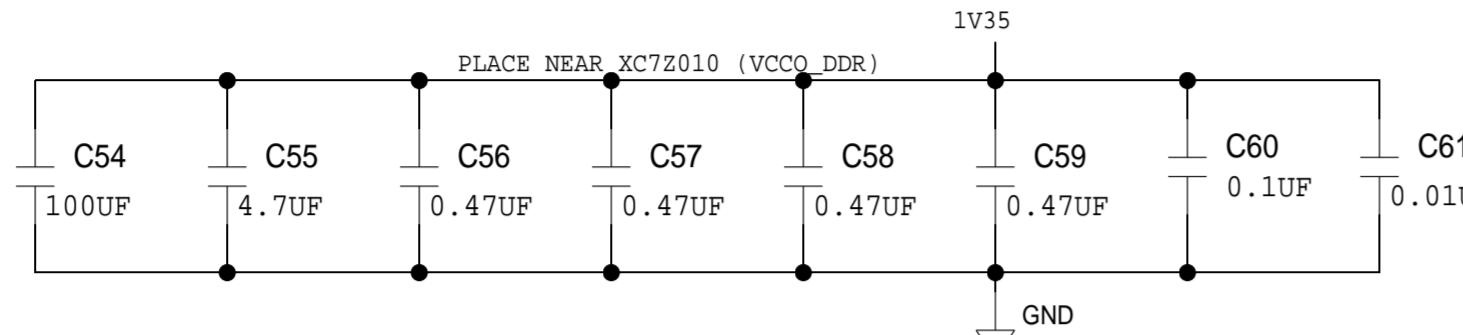
SCALE  
 1:1

SHEET  
 3 OF 9

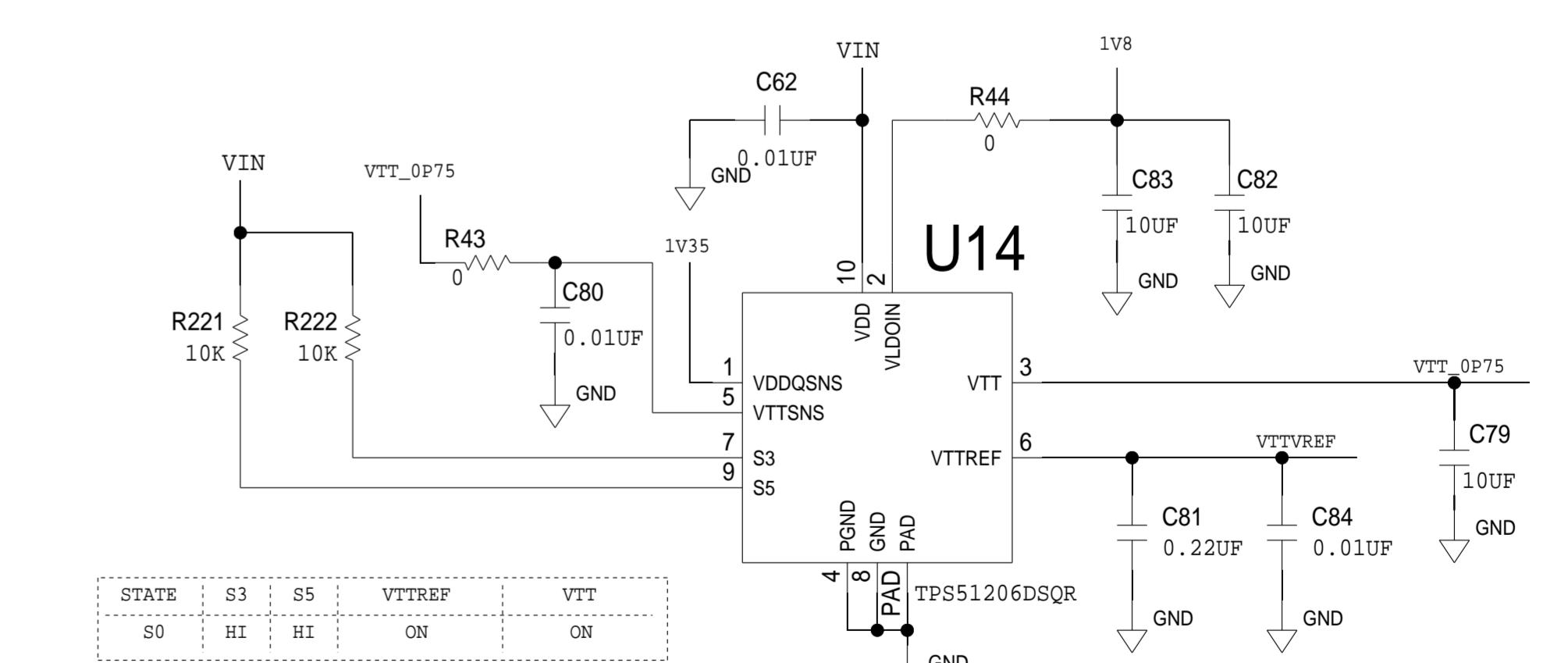
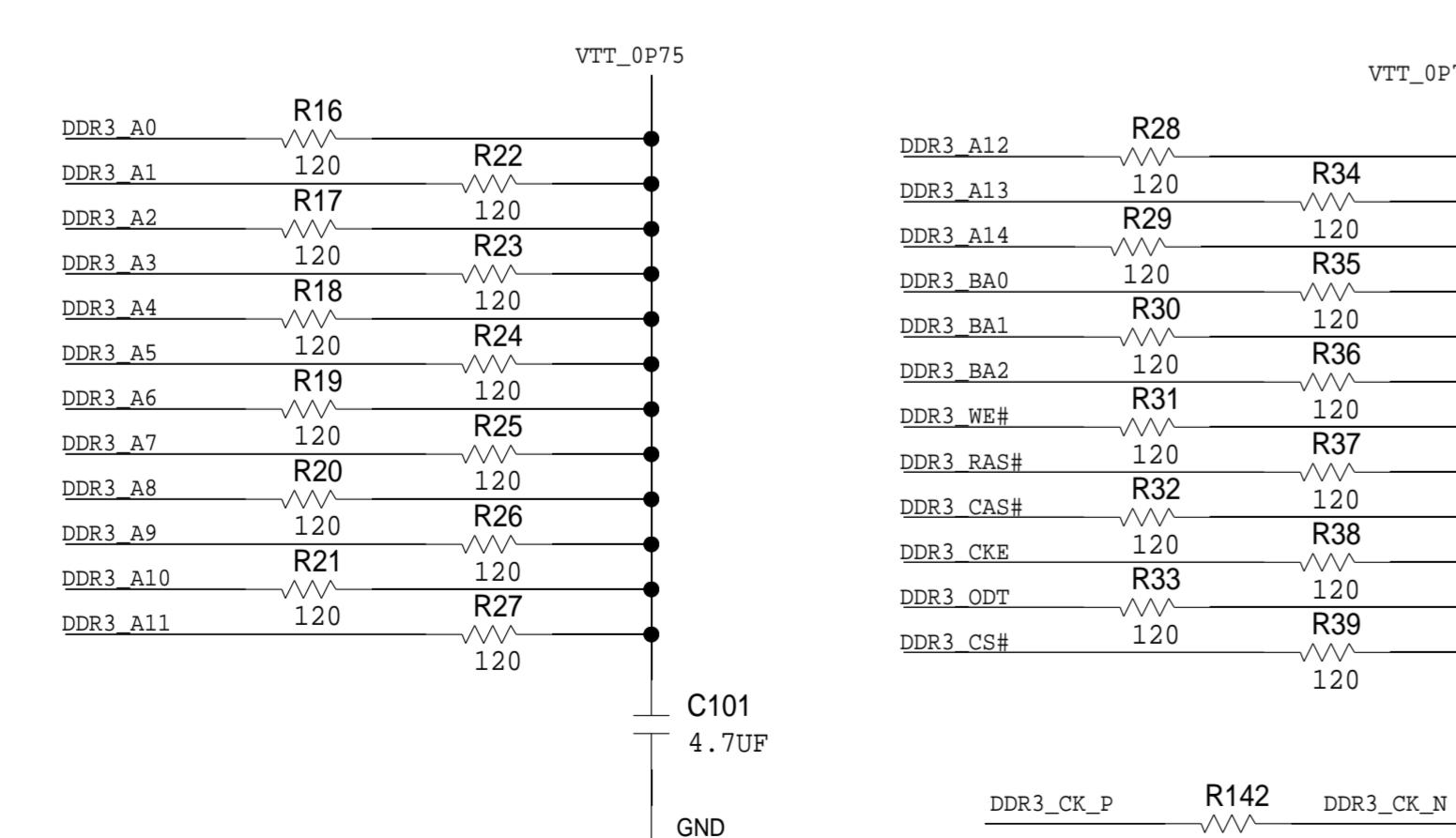
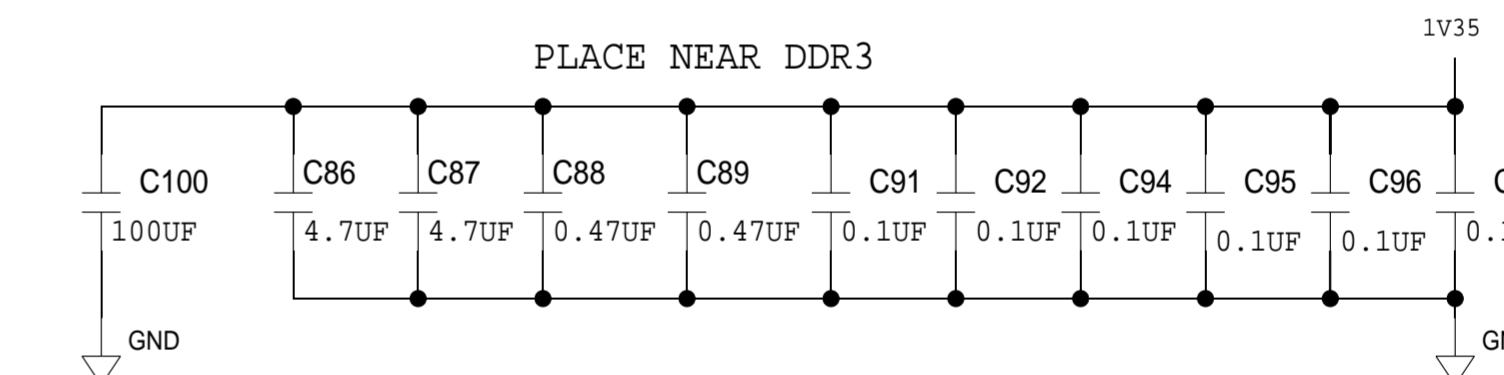
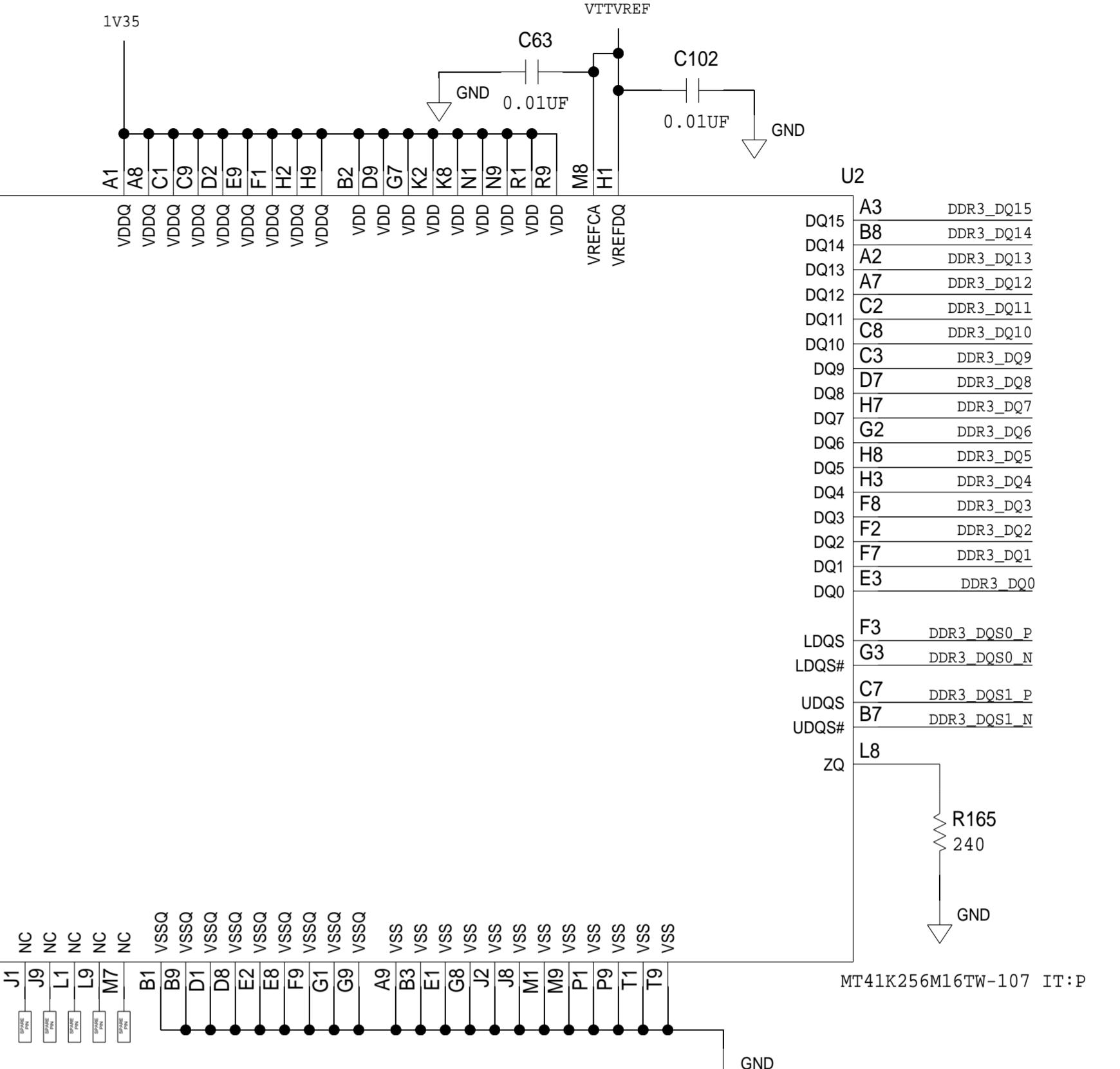
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

DDR 3



# Released to Production



## SCHEMATIC

HW TYPE : Customer Evaluation Z  
Product(s): ad9363  
  : NA

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OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS  
OF ANALOG DEVICES.  
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS

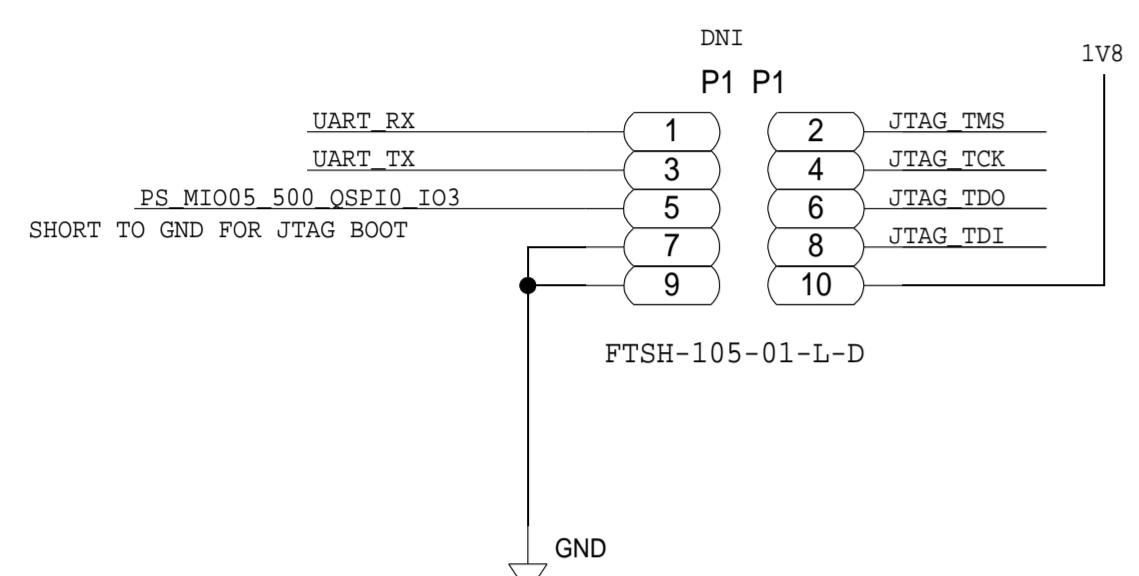
• NA  
DESIGN VIEW  
<DESIGN\_VIEW>  
PTD ENGINEER  
M. BANGI SOD

	DRAWING NO. 02_043758	REV D
SIZE 	SCALE 1 : 1	SHEET 4 OF 9

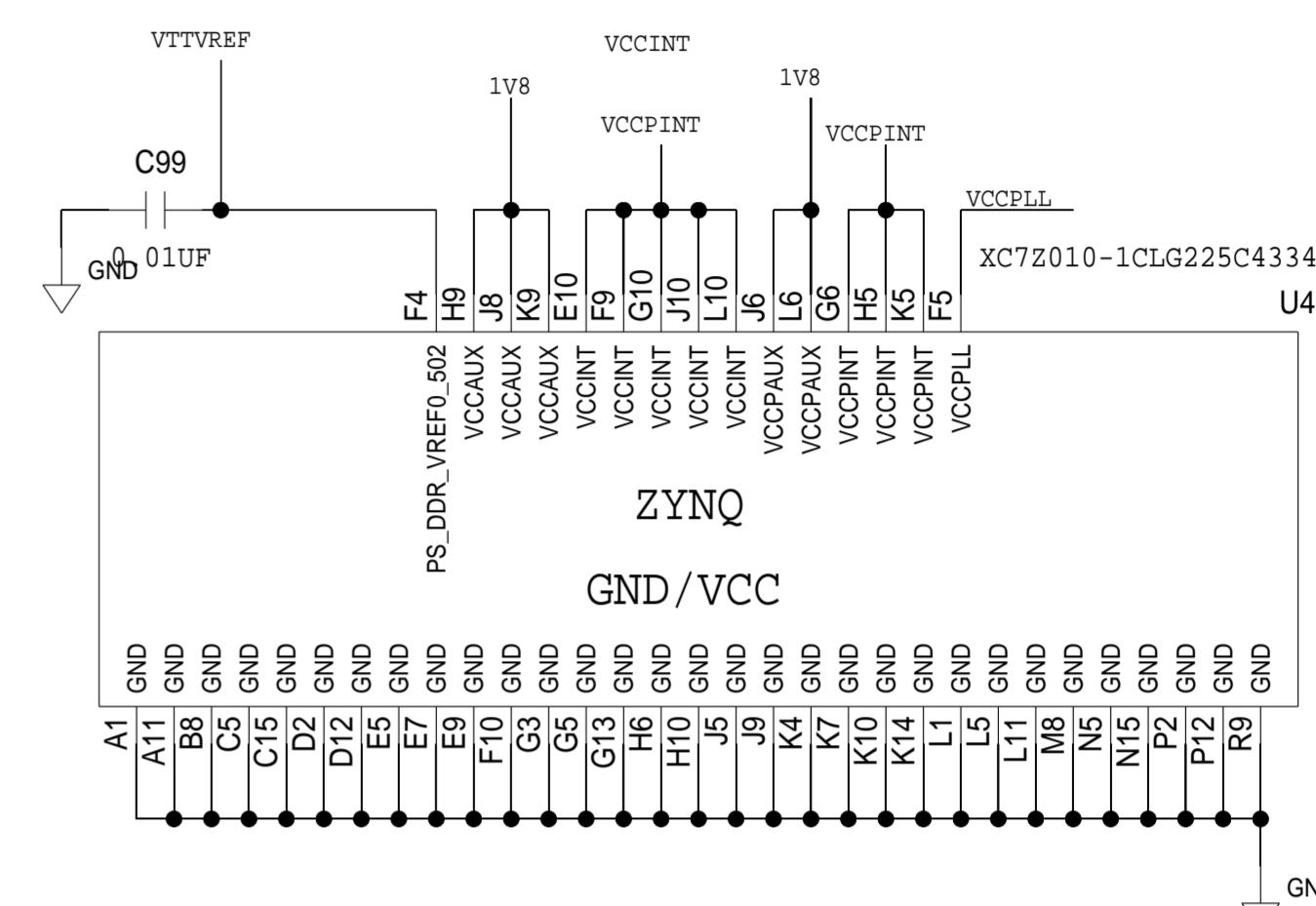
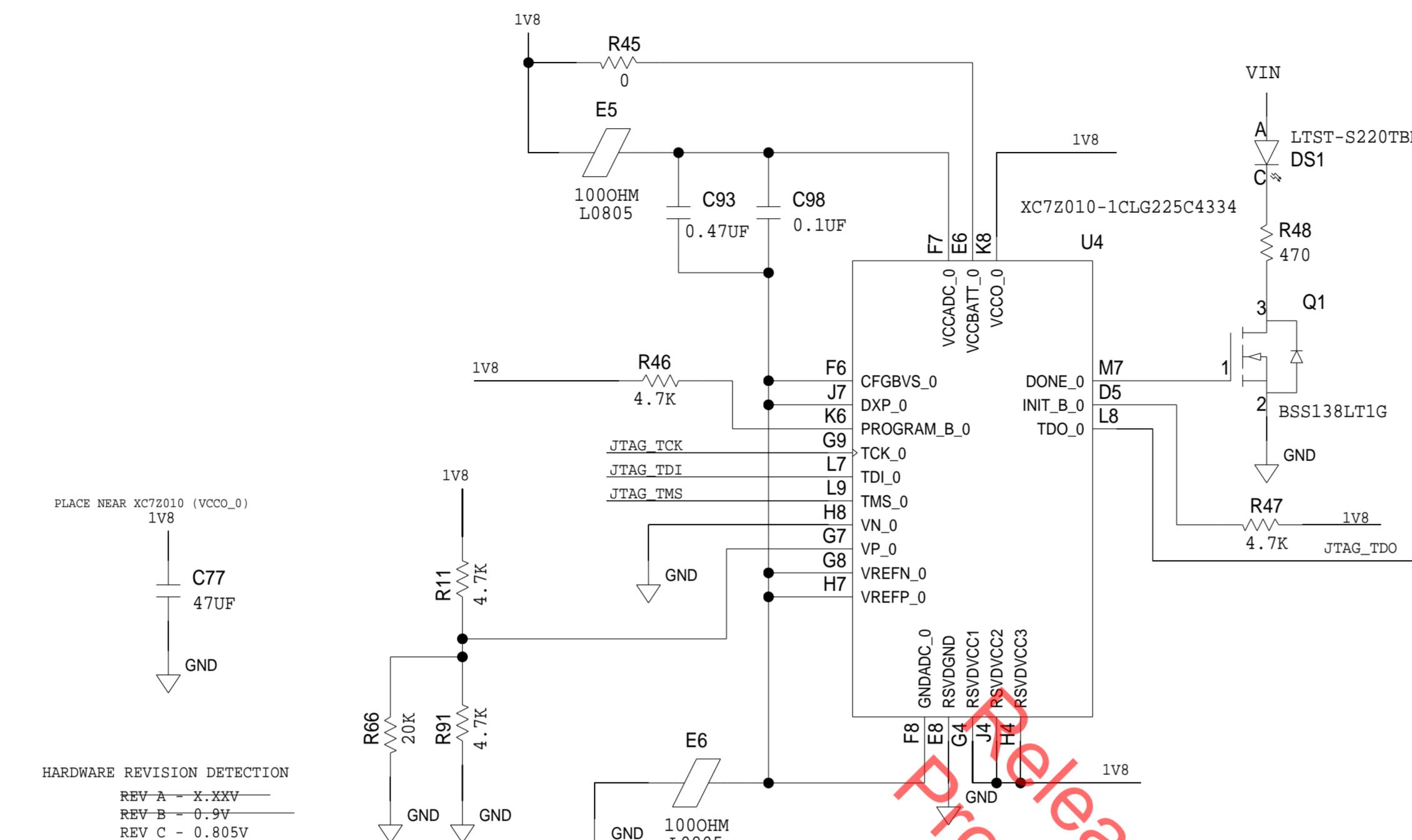
## REVISIONS

REV	DESCRIPTION	DATE	APPROVED

## 0.05 PITCH JTAG AND UART CONNECTOR

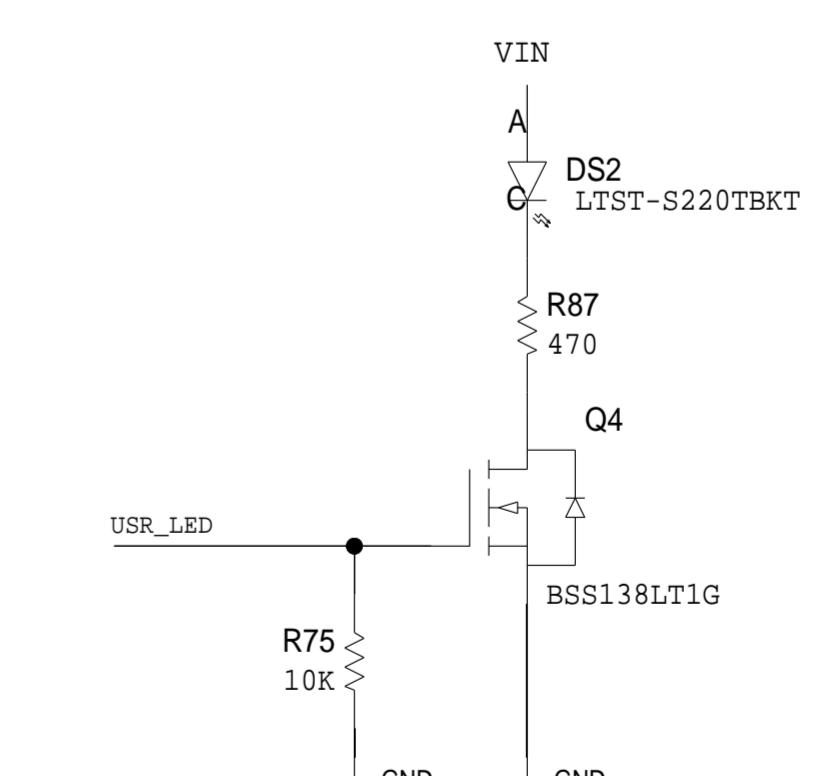
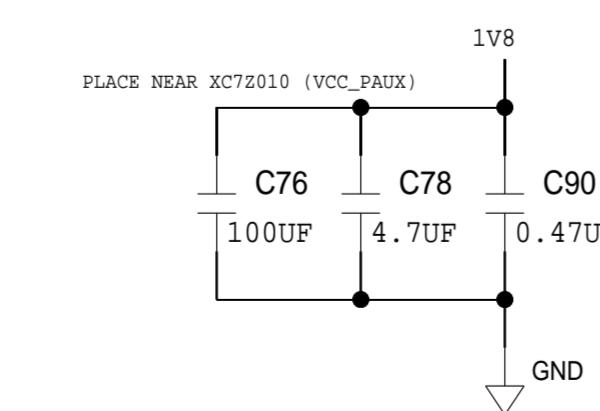
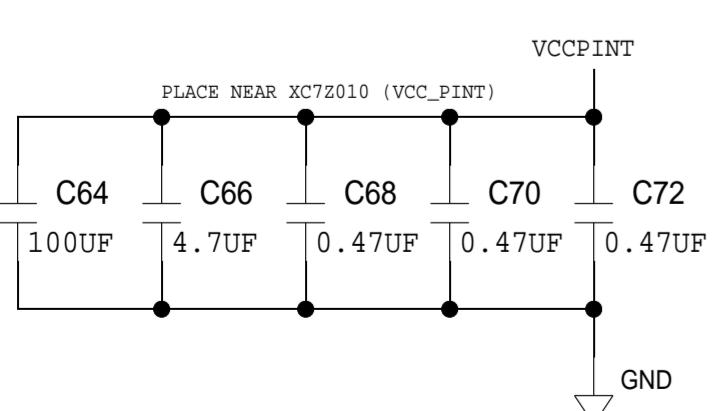
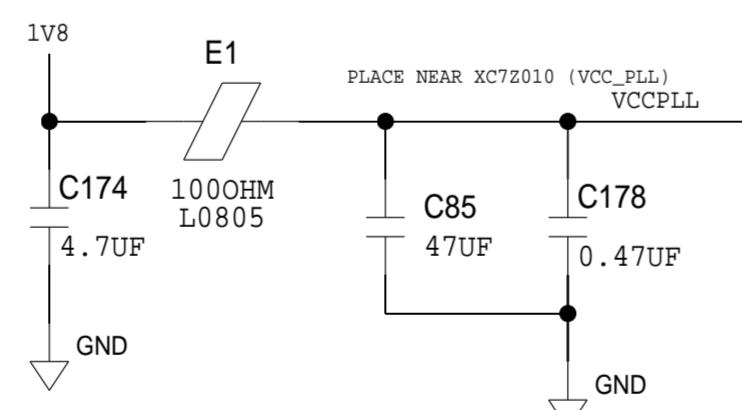
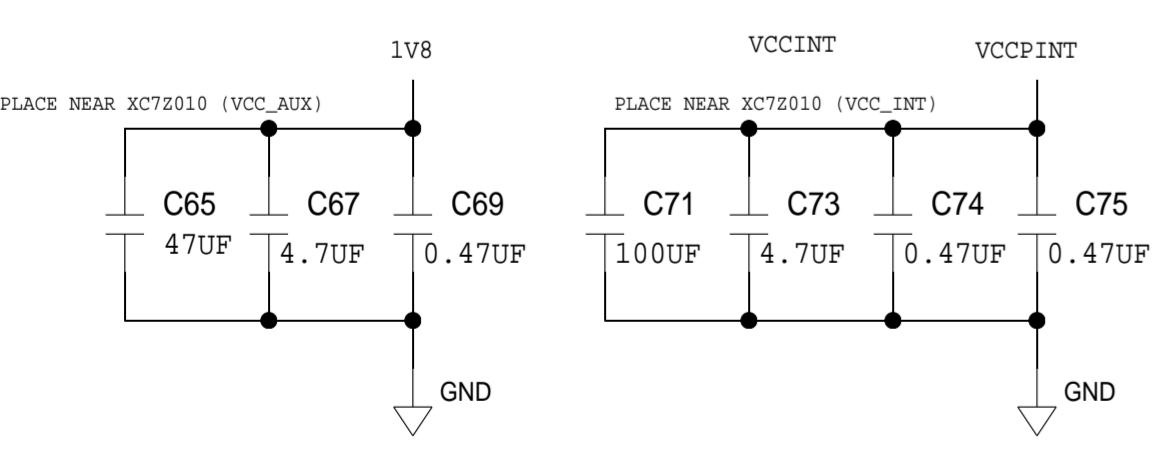


ZYNQ BANK 0



The diagram shows a vertical array of pins. From top to bottom, they are labeled F8, E8, G4, J4, H4, and GND. A horizontal line labeled '1V8' is located above the pins. A red watermark with the text 'Released to Production' is diagonally oriented across the entire image.

USER LED



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## SCHEMATIC

HW TYPE : Customer Evaluation Z  
Product(s): ad9363  
: NA

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## DESIGN VIEW

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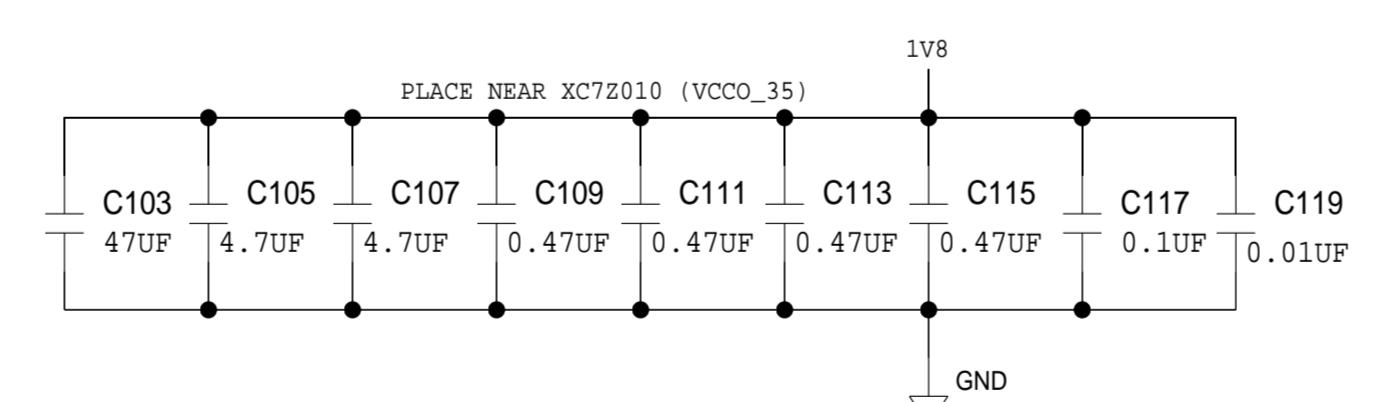
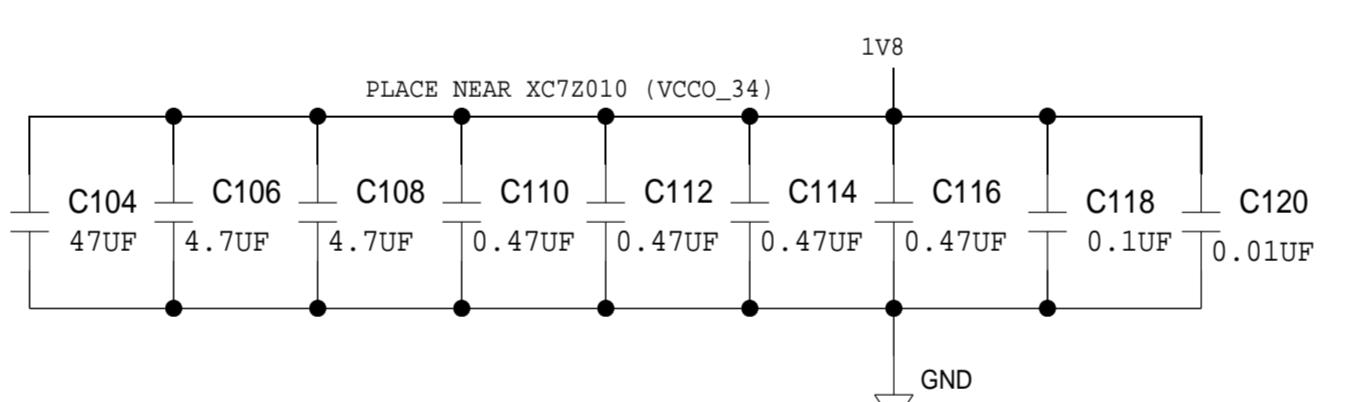
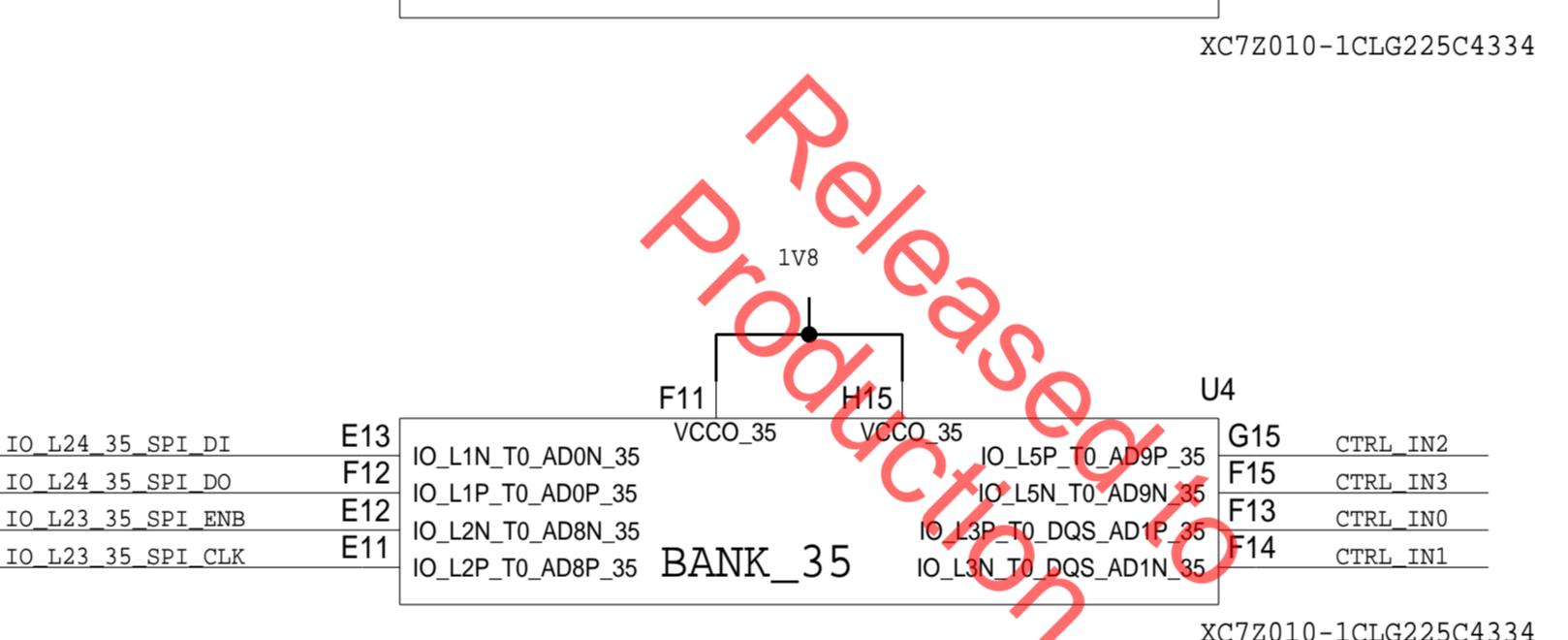
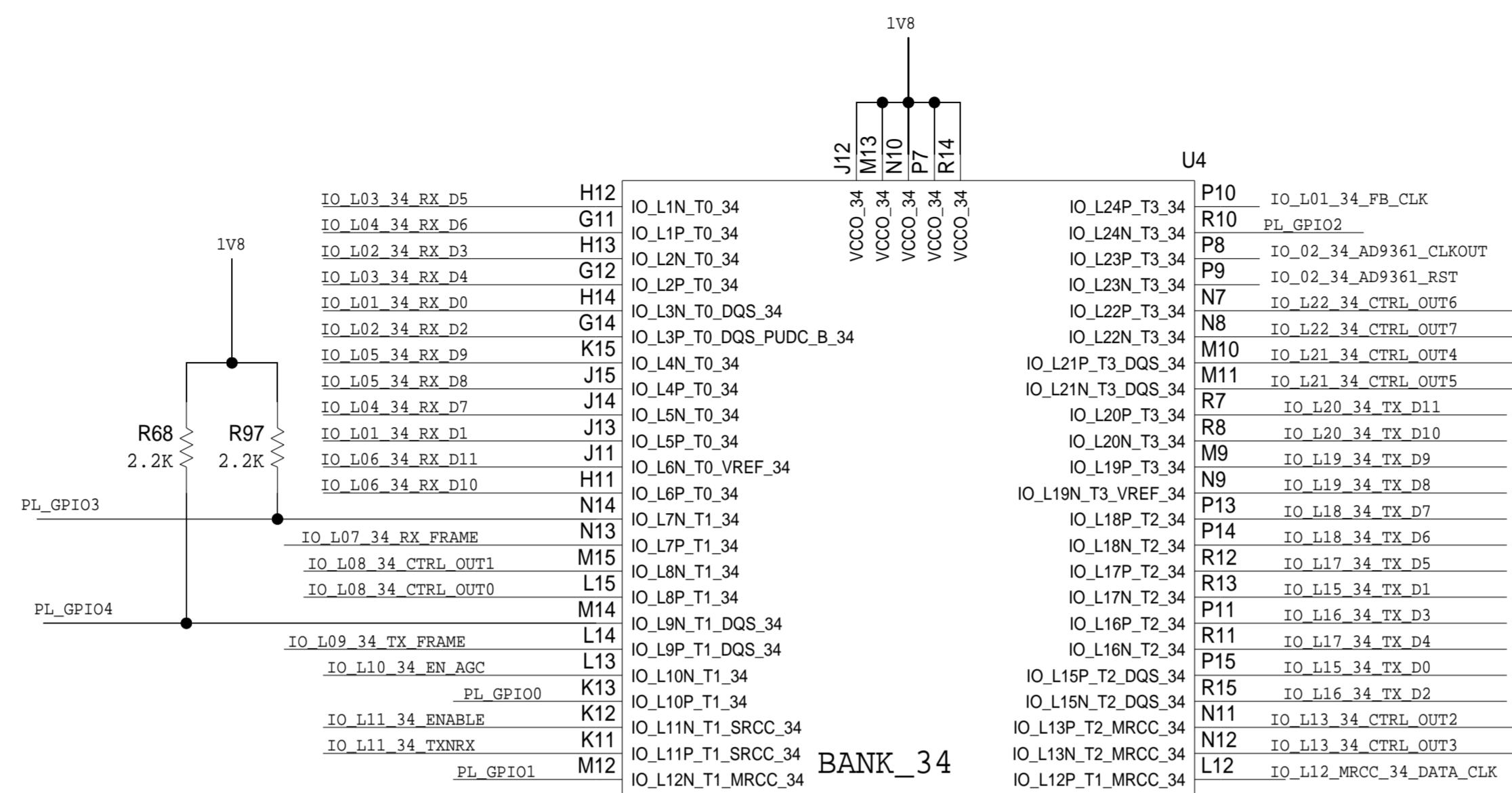
PTD ENGINEER  
M. BANCISOR

	DRAWING NO. 02_043758	REV D
SIZE <b>P</b>	SCALE 1:1	SHEET 5 OF 9

## REVISIONS

REV	DESCRIPTION	DATE	APPROVED

## ZYNQ BANK 34, 35

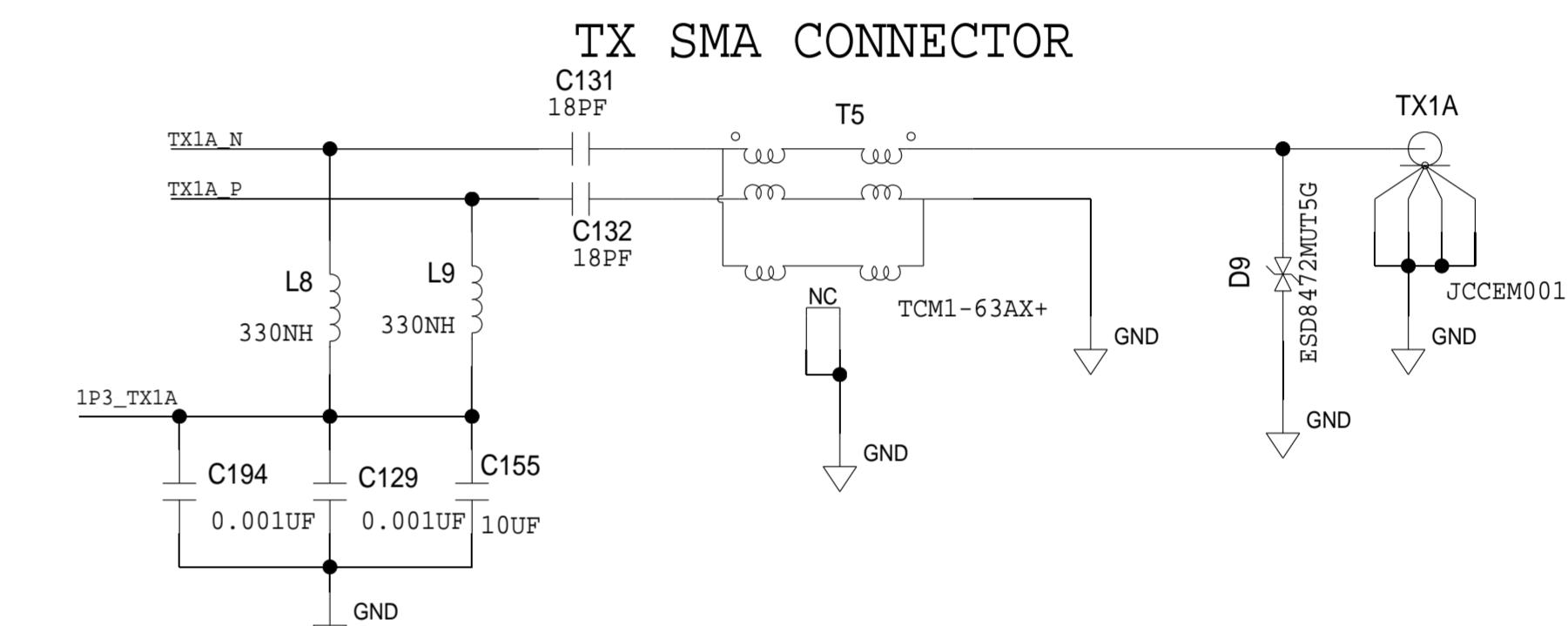
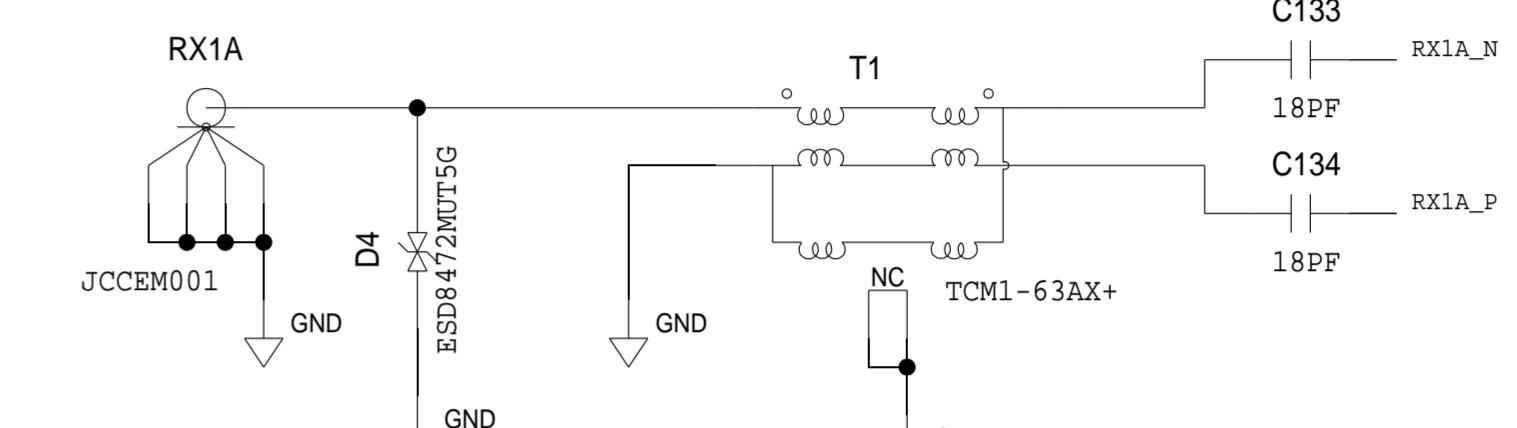
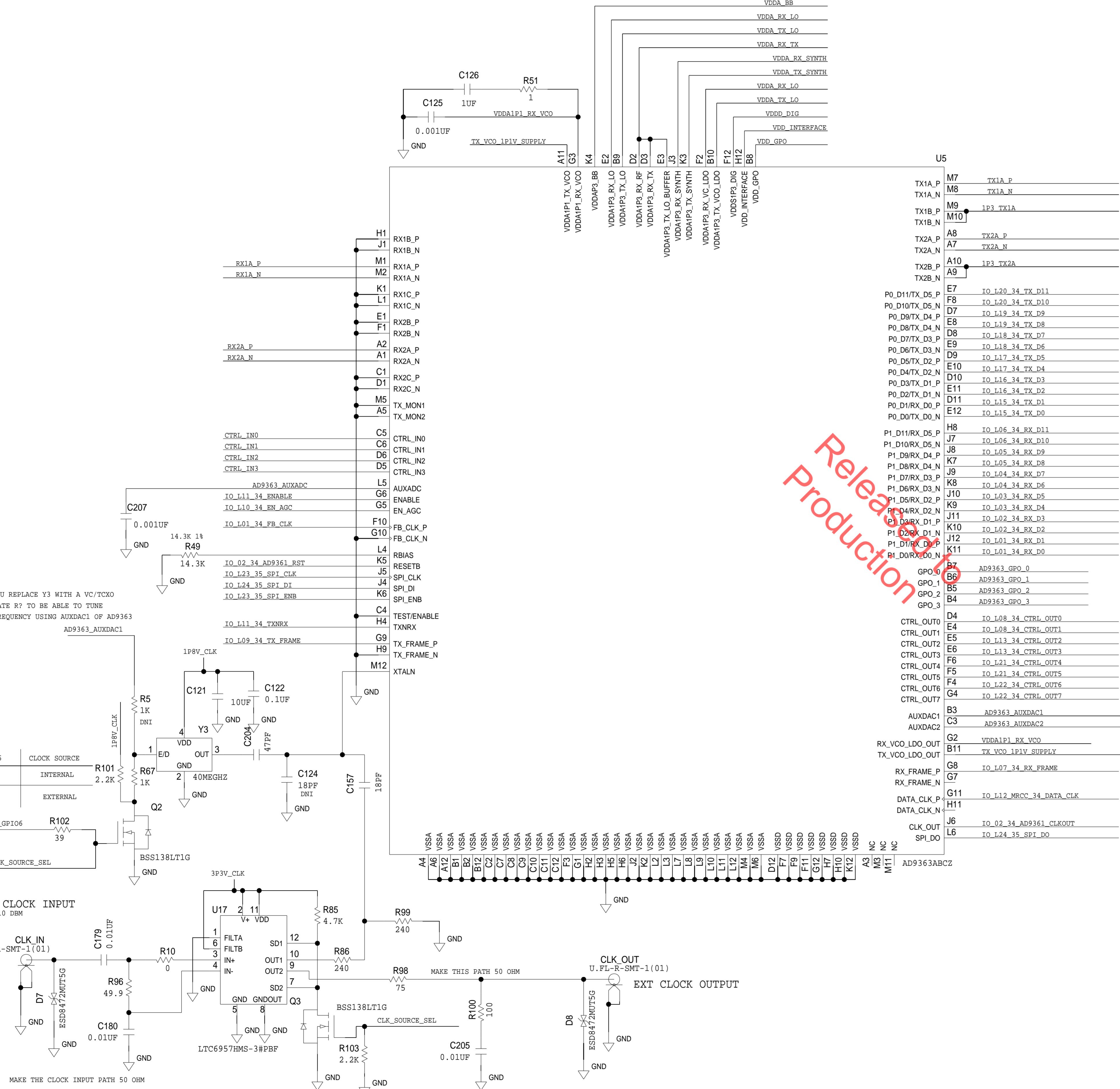


SCHEMATIC	
HW TYPE : Customer Evaluation Z	Product(s): ad9363 : NA
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_043758
PTD ENGINEER M. BANCISOR	REV D SIZE D SCALE 1:1 SHEET 6 OF 9

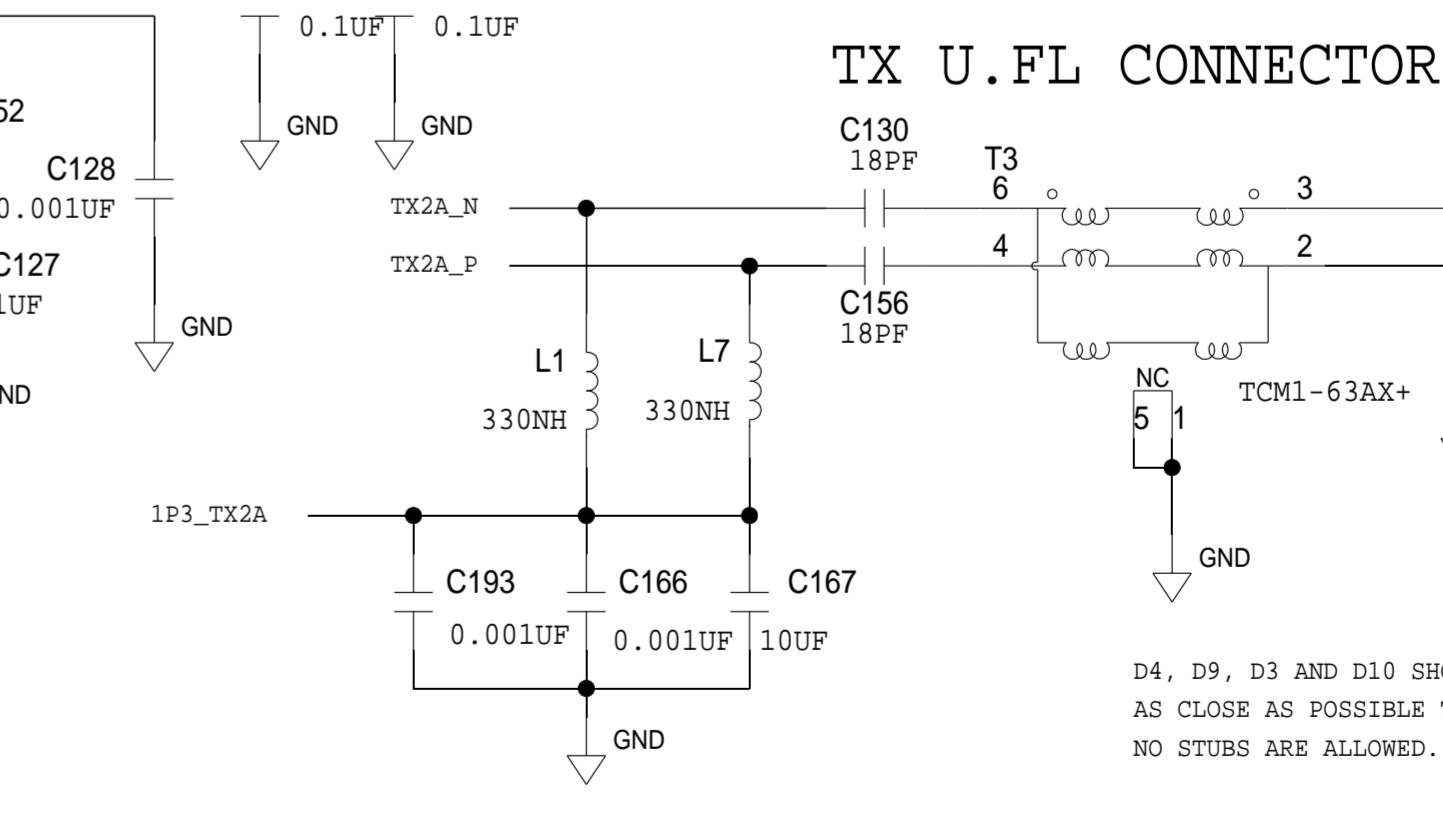
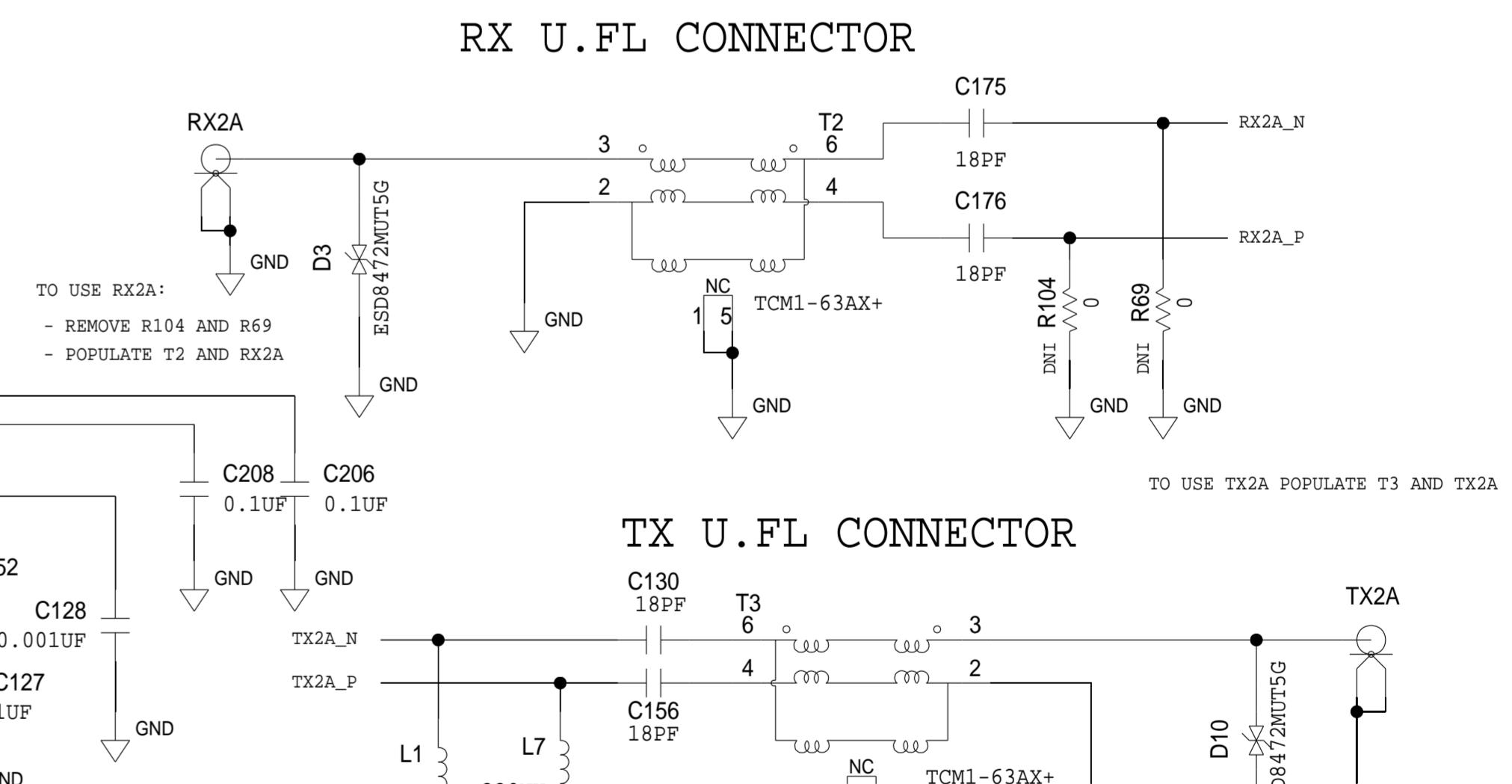
AD9363

REVISIONS		
DESCRIPTION	DATE	APPROVED

	H8
	J7
	J8
	K7
	J9
	K8
	J10
	K9
	J11
	K10
	J12
	K11
P1_D11/RX_D5_P	B7
P1_D10/RX_D5_N	B6
P1_D9/RX_D4_P	GPO_0
P1_D8/RX_D4_N	GPO_1
P1_D7/RX_D3_P	GPO_2
P1_D6/RX_D3_N	
P1_D5/RX_D2_P	
P1_D4/RX_D2_N	
P1_D3/RX_D1_P	
P1_D2/RX_D1_N	
P1_D1/RX_D0_P	
P1_D0/RX_D0_N	



NOTE: WHEN BOTH RF CHANNELS ARE USED THE MAXIMUM DATA RATE IS 30.72 MSPS.



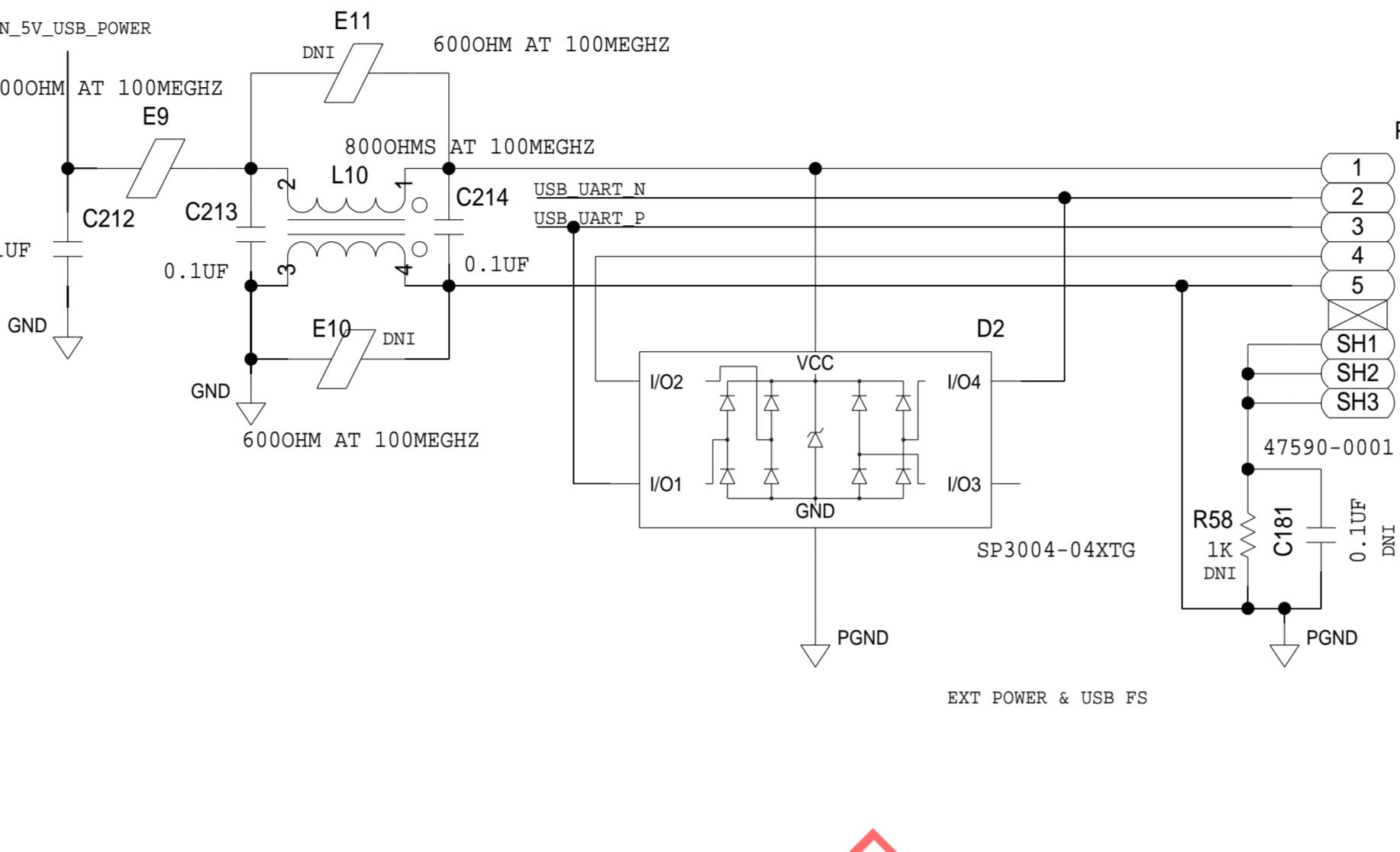
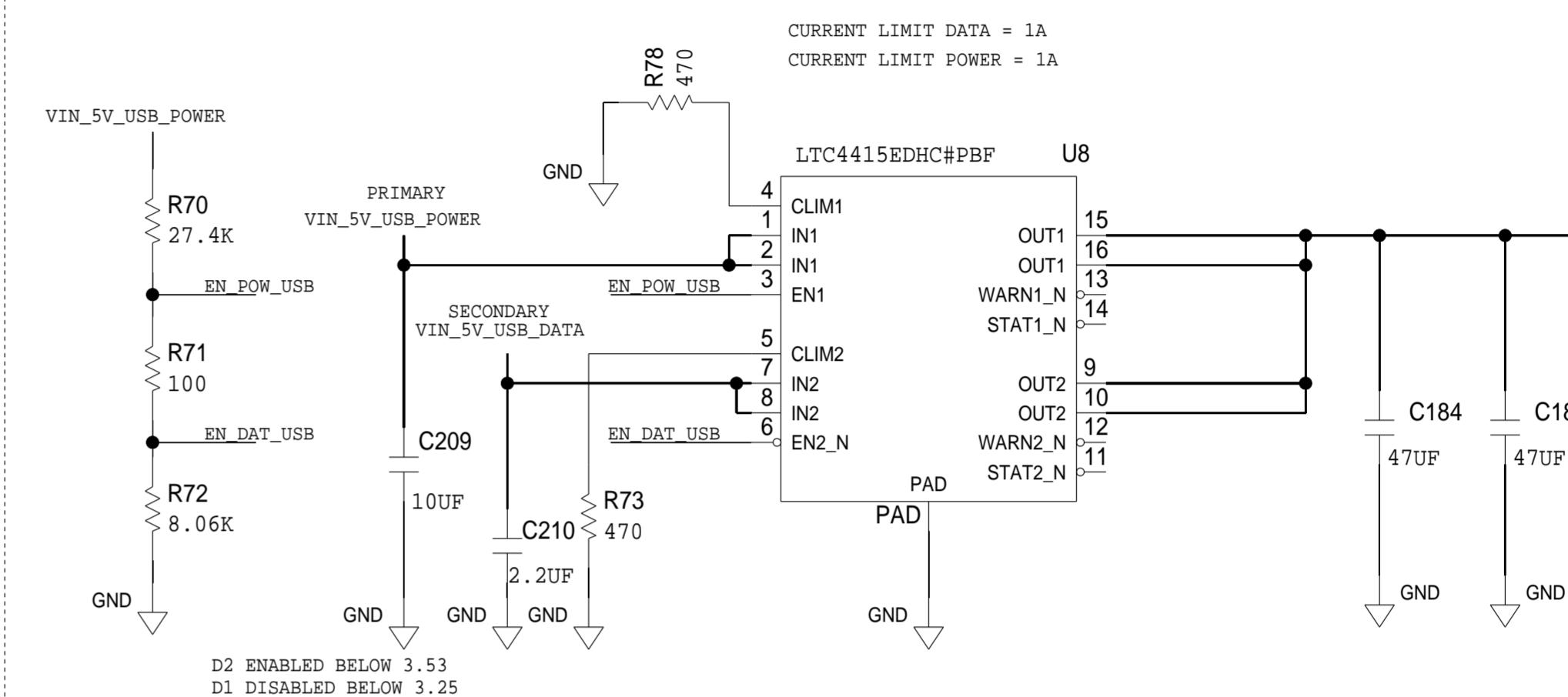
D4, D9, D3 AND D10 SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CONNECTOR.

 <b>ANALOG DEVICES</b>	<h1>SCHEMATIC</h1>		
	HW TYPE : Customer Evaluation Z Product(s): ad9363 : NA		
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	PTD ENGINEER M. BANCISOR	SIZE <b>P</b>	SCALE 1:1
		SHEET	7 OF 9

## REVISIONS

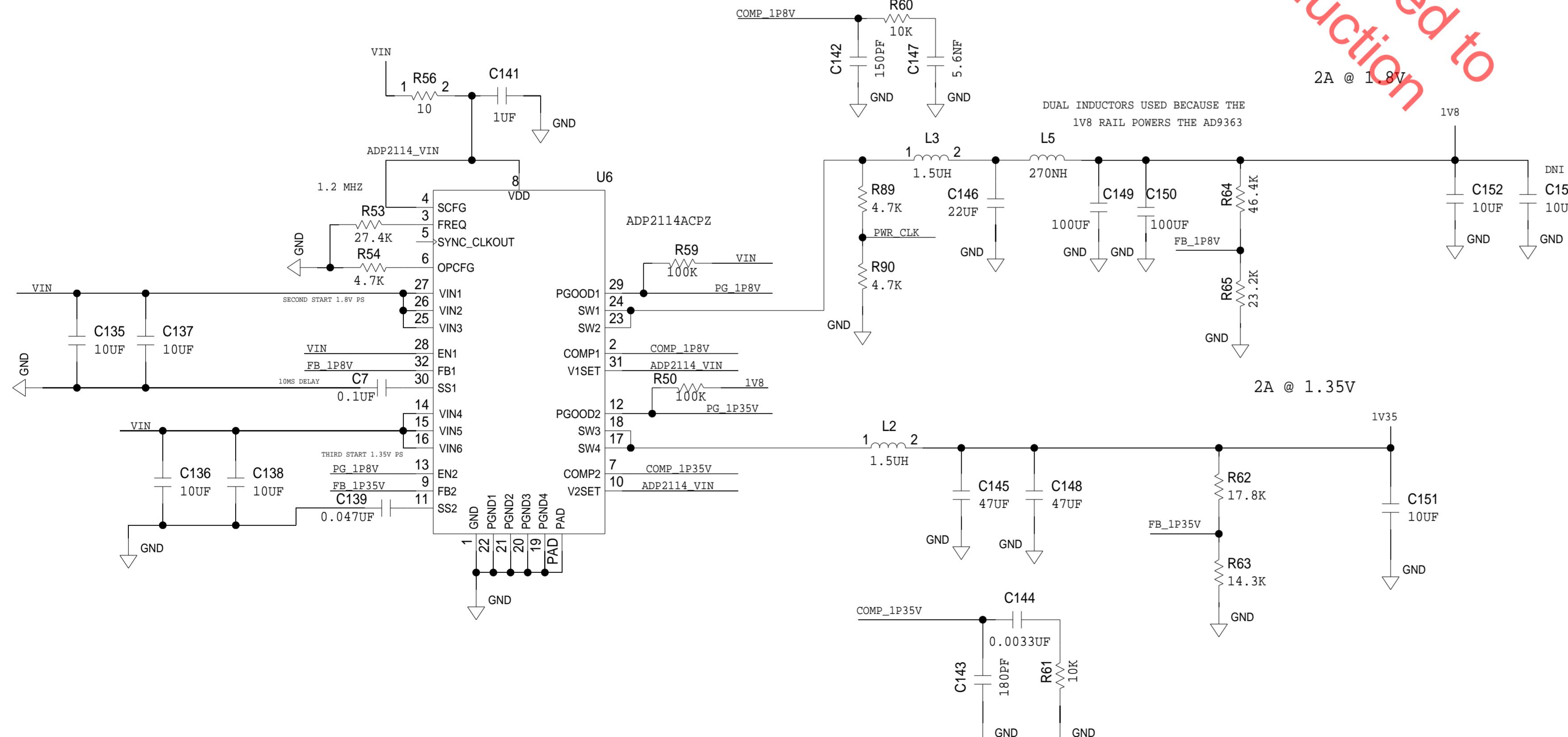
REV	DESCRIPTION	DATE	APPROVED

## USB CONNECTORS

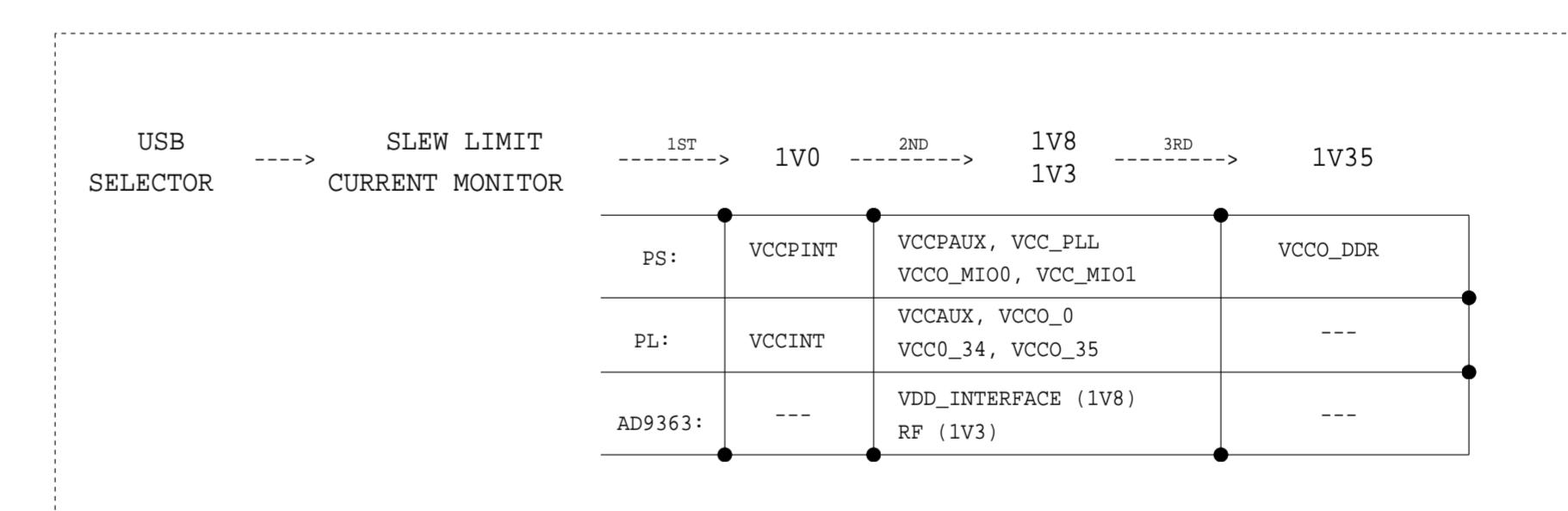
POWER SELECTOR  
INRUSH AND OVERCURRENT PROTECTION

Released to Production

## USING POWER USB IF AVAILABLE



## POWER SEQUENCE:



## SCHEMATIC

HW TYPE : Customer Evaluation Z  
Product(s) : ad9363  
: NA

DESIGN VIEW  
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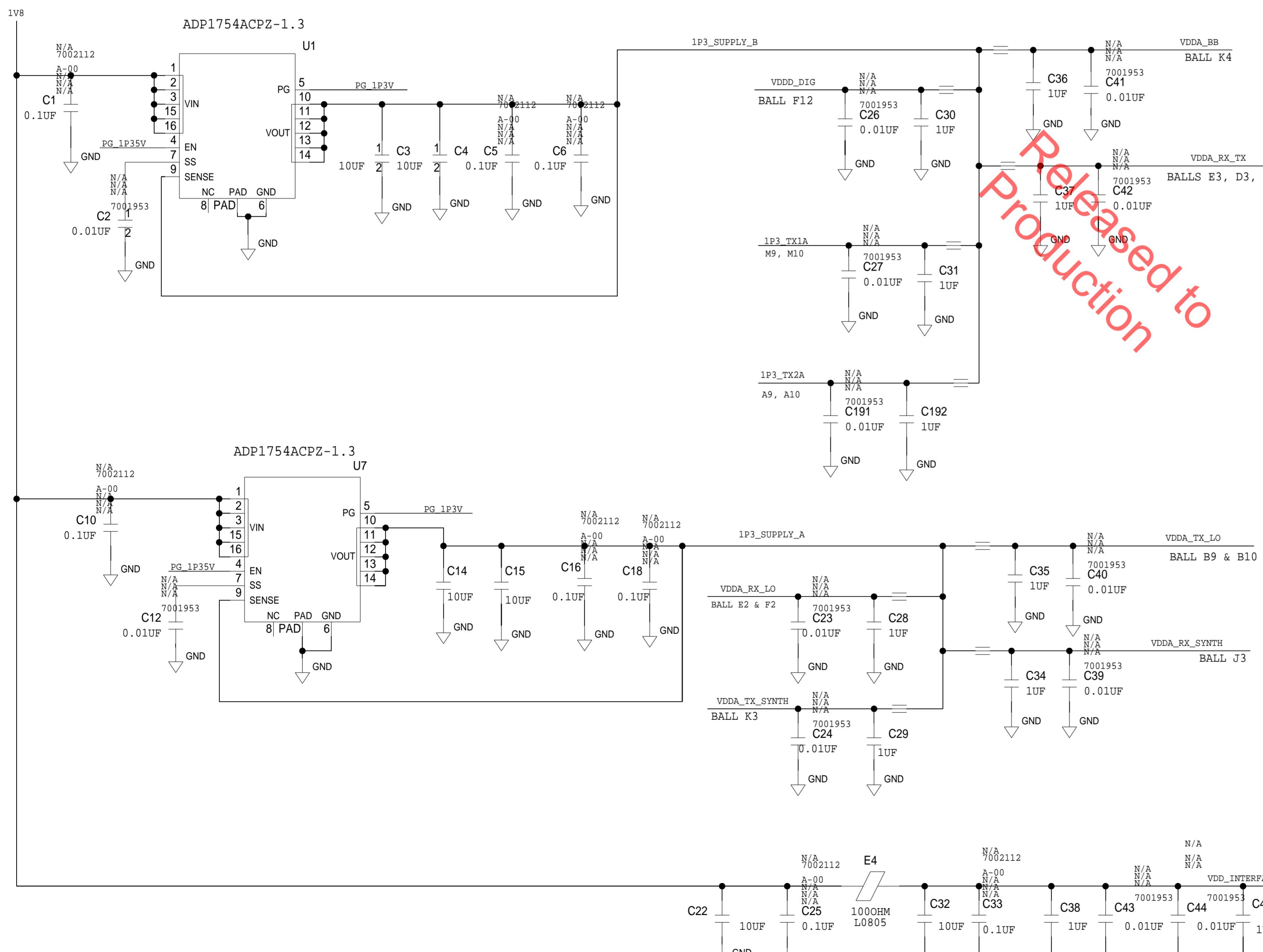
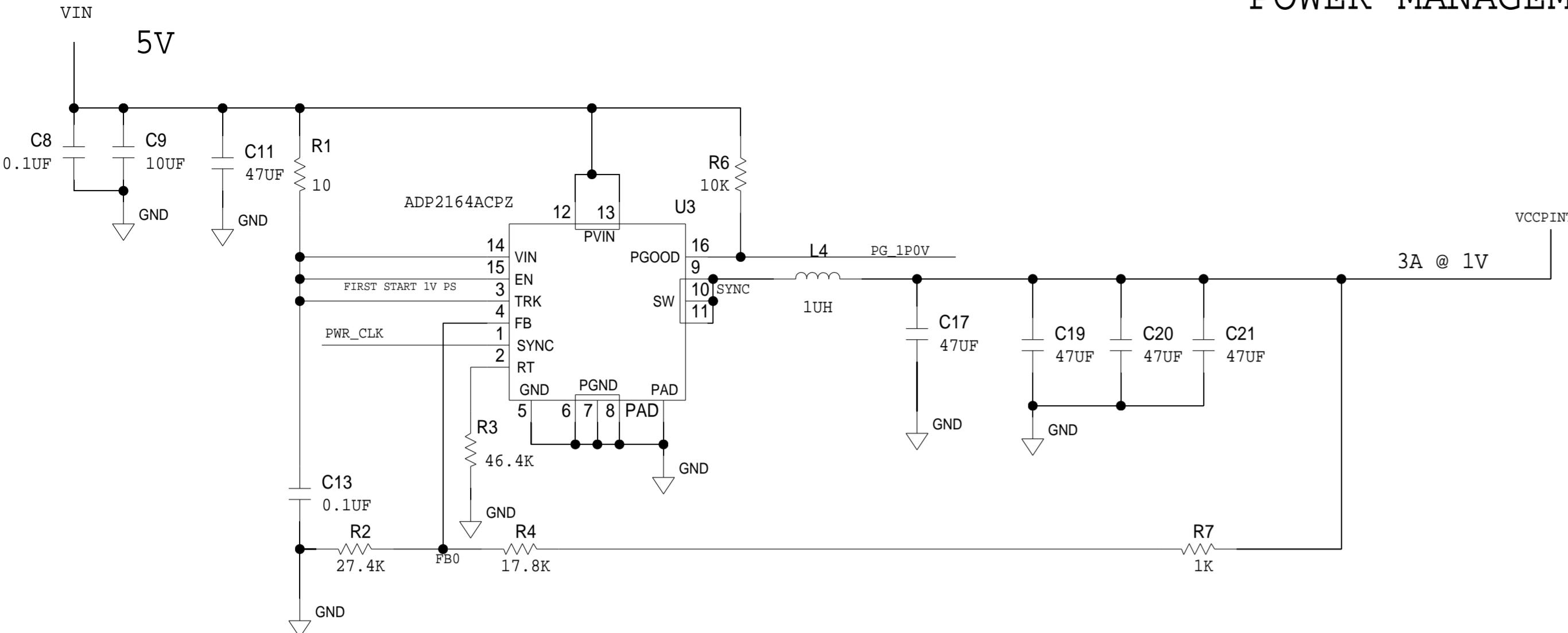
DRAWING NO.  
02\_043758

REV  
D

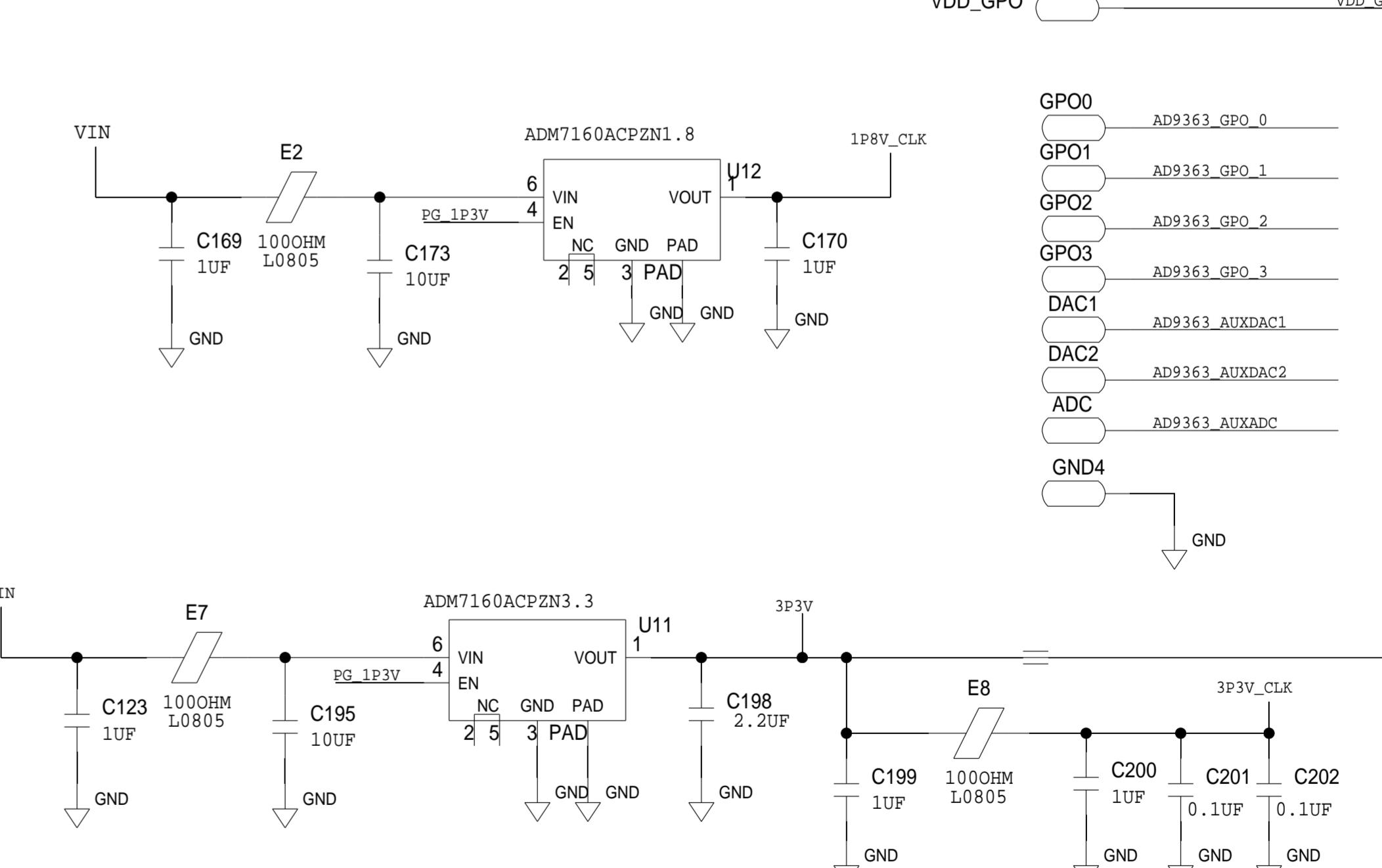
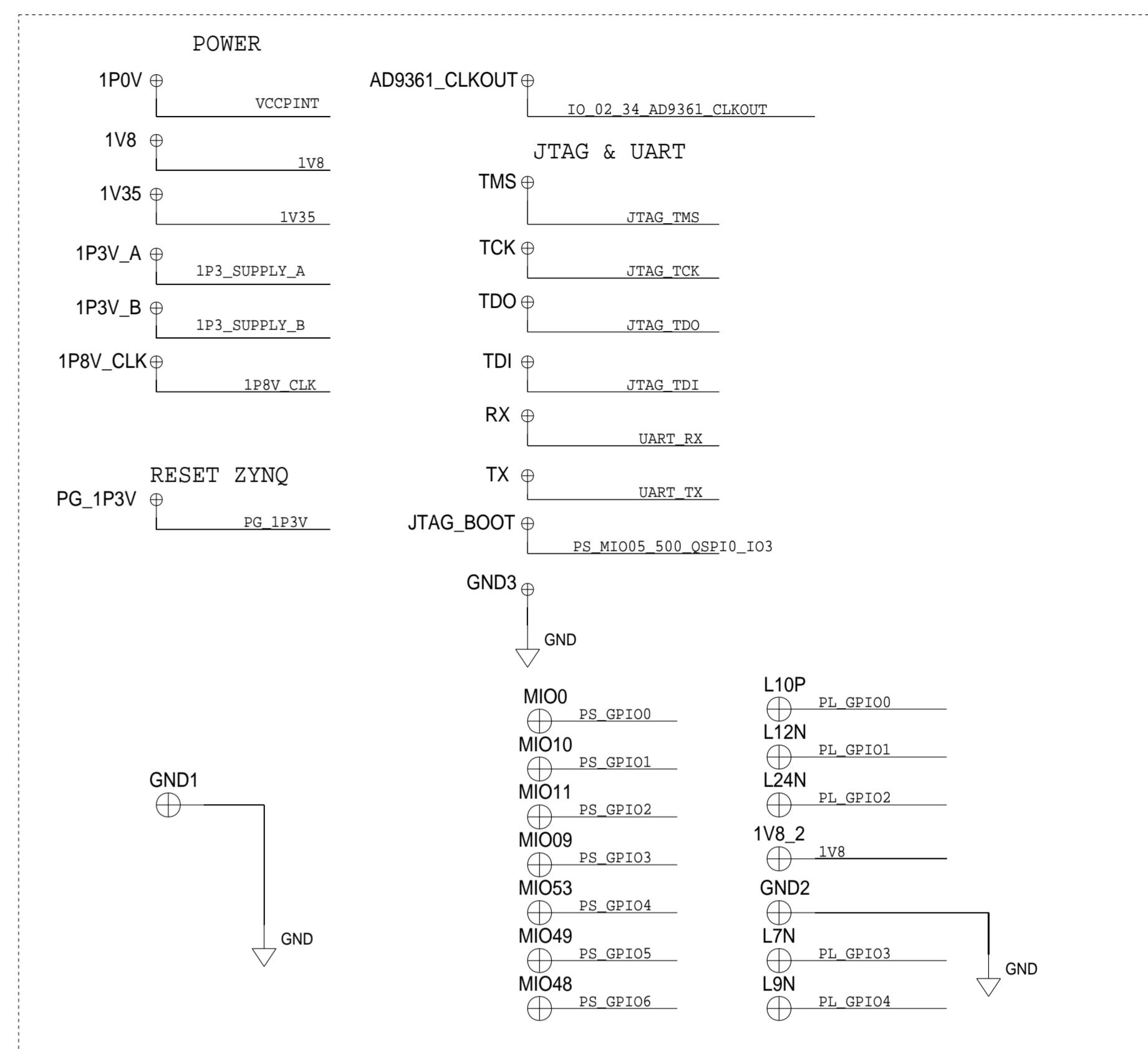
PTD ENGINEER  
M. BANCISOR

SIZE **D** SCALE 1:1 SHEET 8 OF 9

## POWER MANAGEMENT SECTION



## TEST PADS

ANALOG  
DEVICESSCHEMATIC  
HW TYPE : Customer Evaluation Z  
Product(s): ad9363  
: NADESIGN VIEW  
<DESIGN\_VIEW>DRAWING NO.  
02\_043758REV  
DPTD ENGINEER  
M. BANCISORSIZE  
D  
SCALE  
1:1SHEET  
9  
OF  
9