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Simulation Result Functional simulation Completed Simulation Completed Simulation Functional simulation Completed Simulation Functional simulation Fu	NAME 莫寶琳		
Functional simulation Completed simulation Gate-level simulation Completed simulation Completed simulation Completed Completed	Student ID F64081169		
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Description of your design 我的 FSM 設計有四個 state,分別為 IDLE,READ,BILINE. IDLE state: 等待 in_en signal,讀到進入 READ state。	21.0		
我的 FSM 設計有四個 state,分別為 IDLE,READ,BILINE. IDLE state: 等待 in_en signal,讀到進入 READ state。	25.27		
IDLE state: 等待 in_en signal,讀到進入 READ state。	Description of your design		
我的 FSM 設計有四個 state,分別為 IDLE,READ,BILINEAR,FINISH。 IDLE state: 等待 in_en signal,讀到進入 READ state。 READ state: read input pattern 時存入各自的 r,g,b memory。 BILINEAR state: 讀完全部 pattern 後進入 bilinear state,處理以下四個 case。 (a) ex: center = 129,b(129) = [b(128)+b(130)] >> 1,r(129) = [r(1)+r(257)] >> 1 (b) ex: center = 130,g(130) = [g(129)+g(131)+g(2)+g(258)] >> 2,r(130) = [r(1)+r(3)+r(257)+r(259)] >> 2 (c) ex: center = 257,g(257) = [g(256)+g(258)+g(129)+g(385)] >> 2,b(257) = [b(128)+b(130)+b(384)+b(386)] >> 2 (d) ex: center = 258,b(258) = [b(130)+b(386)] >> 1,r(258) = [r(257)+r(259)] >> 1			

Scoring = average PSNR of the six test images

 $[\]boldsymbol{\ast}$ PSNR of all interpolation results should meet at least the baseline.