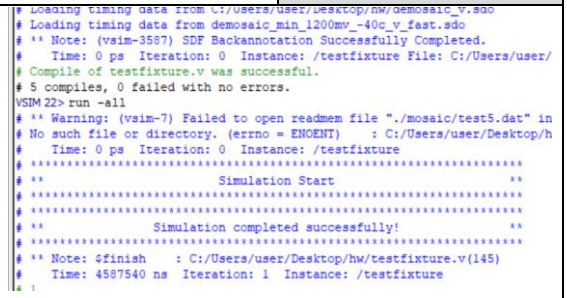
2023 Digital IC Design Homework 5

NAME	莫寶琳		
Student ID	F64081169		
Simulation Result			
Functional simulation	Completed	Gate-level simulation	Completed
			
Evaluation Results			
test1.png	25.29	test2.png	24.78
test3.png	29.13	test4.png	21.0
test5.png	21.98	test6.png	25.27
Description of your design			

我的 FSM 設計有四個 state，分別為 IDLE,READ,BILINEAR,FINISH。

IDLE state: 等待 in_en signal，讀到進入 READ state。

READ state : read input pattern 時存入各自的 r,g,b memory。

BILINEAR state:

讀完全部 pattern 後進入 bilinear state，處理以下四個 case。

(a) ex: center = 129，b(129) = [b(128)+b(130)] >> 1 , r(129) = [r(1) + r(257)] >> 1

(b) ex: center = 130，g(130) = [g(129)+g(131)+g(2)+g(258)] >>2，r(130) = [r(1)+r(3)+r(257)+r(259)] >>2

(c) ex: center = 257，g(257) = [g(256)+g(258)+g(129)+g(385)] >>2，b(257) = [b(128)+b(130)+b(384)+b(386)] >>2

(d) ex: center = 258，b(258) = [b(130)+b(386)] >> 1 , r(258) = [r(257) + r(259)] >> 1

FINISH state: 程式完成 done set high。

Scoring = average PSNR of the six test images

*** PSNR of all interpolation results should meet at least the baseline.**