


2023 Digital IC Design Homework 4

NAME	莫寶琳																														
Student ID	F64081169																														
Simulation Result																															
Functional simulation	100	Gate-level simulation	100																												
<div><pre> VSM2>run -all ----- # START!!! Simulation Start # # # ----- # Layer 0 output is correct ! # Layer 1 output is correct! # # ----- # SUMMARY # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 46087 cycle # # ** Note: \$finish : C:/Users/user/Desktop/file/testfixture.v(178) # Time: 2304350 ns Iteration: 0 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/user/Desktop/file/testfixture.v line 178</pre></div> <div><pre>Transcript ----- # Loading timing data from C:/Users/user/Desktop/file/ATCONV_min_1200mv_40c_v_310w.sdc # Loading timing data from C:/Users/user/Desktop/file/ATCONV_min_1200mv_40c_v_fast.sdo # Loading timing data from C:/Users/user/Desktop/file/ATCONV_v.sdo # Loading timing data from ATCONV_min_1200mv_40c_v_fast.sdo # ** Note: (vsim-3587) SDF Backannotation Successfully Completed. # Time: 0 ps Iteration: 0 Instance: /testfixture File: C:/Users/user/Desktop/file/test VSM2>run -all ----- # START!!! Simulation Start # # # ----- # Layer 0 output is correct ! # Layer 1 output is correct! # # ----- # SUMMARY # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 46087 cycle # # ** Note: \$finish : C:/Users/user/Desktop/file/testfixture.v(178) # Time: 2304355958 ps Iteration: 0 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/user/Desktop/file/testfixture.v line 178 ----- 1</pre></div>																															
Synthesis Result																															
Total logic elements	554																														
Total memory bits	0																														
Embedded multiplier 9-bit elements	0																														
Total cycle used	46087																														
Flow Summary																															
<div><div></div><<Filter>></div> <table><tr><td>Flow Status</td><td>Successful - Thu May 18 02:20:05 2023</td></tr><tr><td>Quartus Prime Version</td><td>20.1.1 Build 720 11/11/2020 SJ Lite Edition</td></tr><tr><td>Revision Name</td><td>ATCONV</td></tr><tr><td>Top-level Entity Name</td><td>ATCONV</td></tr><tr><td>Family</td><td>Cyclone IV E</td></tr><tr><td>Device</td><td>EP4CE55F23A7</td></tr><tr><td>Timing Models</td><td>Final</td></tr><tr><td>Total logic elements</td><td>554 / 55,856 (< 1 %)</td></tr><tr><td>Total registers</td><td>131</td></tr><tr><td>Total pins</td><td>82 / 325 (25 %)</td></tr><tr><td>Total virtual pins</td><td>0</td></tr><tr><td>Total memory bits</td><td>0 / 2,396,160 (0 %)</td></tr><tr><td>Embedded Multiplier 9-bit elements</td><td>0 / 308 (0 %)</td></tr><tr><td>Total PLLs</td><td>0 / 4 (0 %)</td></tr></table>				Flow Status	Successful - Thu May 18 02:20:05 2023	Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition	Revision Name	ATCONV	Top-level Entity Name	ATCONV	Family	Cyclone IV E	Device	EP4CE55F23A7	Timing Models	Final	Total logic elements	554 / 55,856 (< 1 %)	Total registers	131	Total pins	82 / 325 (25 %)	Total virtual pins	0	Total memory bits	0 / 2,396,160 (0 %)	Embedded Multiplier 9-bit elements	0 / 308 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																															

我將電路設計成 4 個 state，分別為 IDLE,LAYER_0,LAYER_1,FINISH。

以下是這四個 state 的行為:

IDLE:讀 Ready 訊號，將 busy 設為 1，指定對 layer0 Mem 做 write 操作，進入 LAYER_0。

LAYER_0:一個 pixel 需要做 10 個 cycle，共做 64*64 pixels，用>>操作來完成 kernel 小數乘法，由於 kernel 中間為 1，最後再將中間的值(正數)與周圍八個小數乘法後的值做相減，來符合周圍八個值負數的想法。最後與 bias(-0.75)做相加，判斷第 13 位是否為 1，是的話代表負數，RELU 後等於 0，不是的話等於原本的值。

因為不想浪費 register 去存 padding 的值，所以我有額外做 Padding case 的判斷。每次做一個 pixel 的 convolution 動作，需要存取原圖 9 個 pixels 的值，所以我 9 個位置都有根據不同的邊緣 case、一般 case 以 iaddr 為變數推公式。

LAYER_1: 一個 pixel 需要做 5 個 cycle，共做 32*32 pixels，用一個 max_value 來存最大值，前四次依序讀取 layer0(csel = 0,crd = 1,cwr = 0)的值並更新 max_value，最後一次要將 max_value 無條件進位後存入 layer1(csel = 1,crd = 0,cwr = 1)。

位置的公式我用 current 與 address 去計算，current 每回+2 再%64 代表目前在 64 pixel 第幾直行。Address 為做到 32*32 的 layer1 的第幾個 pixel。

公式如下:

左上: $\text{current} + (\text{address} \gg 5 \ll 7)$

右上: $\text{current} + 1 + (\text{address} \gg 5 \ll 7)$

左下: $\text{current} + 64 + (\text{address} \gg 5 \ll 7)$

右下: $\text{current} + 65 + (\text{address} \gg 5 \ll 7)$

無條件進位我的寫法是:判斷最右邊四位是否大於 0?是的話就 $\text{max_value} + 16 - \text{max_value}[3:0]$ 。

FINISH:將 busy 設為 0，等待輸出。

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**