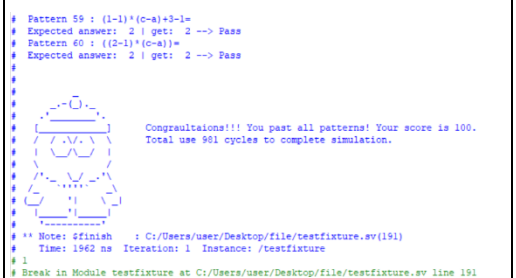
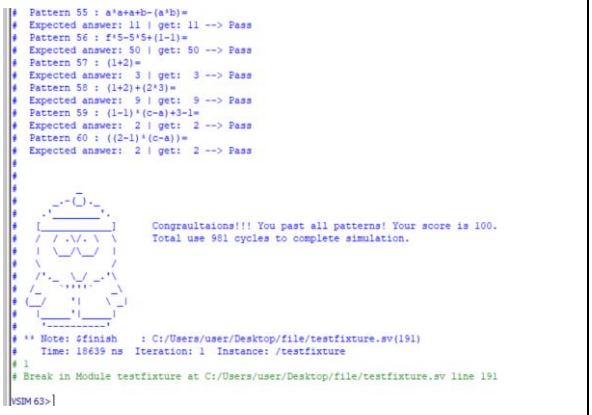
2023 Digital IC Design Homework 3

NAME	莫寶琳
Student ID	F64081169

Simulation Result

Functional simulation	100	Gate-level simulation	100





Synthesis Result

Total logic elements	723
Total memory bits	0
Embedded multiplier 9-bit elements	4
Total cycle used	981
Clock width	19.005

Flow Status	Successful - Mon Apr 24 00:29:17 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AEC
Top-level Entity Name	AEC
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	723 / 55,856 (1 %)
Total registers	136
Total pins	19 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	4 / 308 (1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

有四個 state 分別為 `READY = 0,NUMBER = 1,EQUAL_POP = 2,RESULT = 3;`

以下是各個 state 的行為:

READY: 等待 ready==1。當收到 ready 信號後，切換到 NUMBER state，開始處理輸入。

NUMBER: 將數字逐個加入 stack 中，如果遇到乘號 “*” 則將 mul_flag 設置為 1。當遇到等號 “=” 時，切換到 EQUAL_POP 狀態。

EQUAL_POP:從 operator stack 頂部取出一個 operator，根據 operator 進行計算，直到 operator stack 被拿完，切換到 RESULT 狀態。

RESULT:將結果寫入 result，並將 valid raise high。切換回 READY，等待下一次 input。

其他細節:
若讀到*，因為*永遠最高 priority，所以先做，若遇到()*()的 case 則要存入 operator stack，其他+,-存入 operator stack；若遇到(，紀錄 para_flag，並在裡面用 flag 做判斷+-*優先權看要不要及時計算或存入 operator stack。

*Scoring = Area cost * Timing cost*

*Area cost = Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used * Clock width*

*** Total logic elements must not exceed 1500.**