Manuscript pulse width modulator for ET RF Power Amplifier

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DJ1MR

V1.1

06/01/2018

motivation

The published in [1] contribution to a pulse width modulator for envelopes PAs after the EER principle provides with its high and low voltage section is a complex circuit solution that requires a lot of experience both in building and in balance. The number of matching elements is not insignificant in this solution. But advantage of the proposed solution was the independence of the used transceiver type. The author was now after three years of experience with the presented in 2014 PWM solution, the desire to simplify the circuit in conjunction with a Hermes transceiver significantly, and a solution for both MOSFET PAs with an operating voltage of 50 volts (for LDMOS PAs) and to provide MOSFET-PAs with operating voltages of up to 150 volts. Furthermore, the new solution should contain no more adjustment elements, thus allowing the lighter replica. For the switching MOSFET MOSFET technologies Searched for newer, which are thermally more stable and have smaller input capacity in order to further reduce the required gate drive power.

The presented new PWM solution is particularly suitable for the presented by the author in [2] envelope tracking PA project. This project was carried out with an operating voltage of 105 volts.

Envelope tracking method ET

When envelope tracking method, the control of the PWM modulator no longer with the original rectified envelope, but with a modified and sculpted shape envelope occurs. The modification of the envelope takes place in the shape of that at no or very low SSB signal, the operating voltage is not zero volts but above the respectively used Mosfetkniespannung, for example at 10 volts, is located. This has the advantage that the Ausgangsmosfets must not be operated in the triode region and thus unwanted distortion, among others caused by the high nonlinear capabilities arise. With increasing modulation of the operating voltage is then incremented in the rhythm of SSBHüllkurve, that is, the linear voltage control operation as in the EER and EER-H usual method, the power supply characteristic approaches to.

Figure 1 shows with the green curve is the desired operating voltage modulation curve. Thus, the voltage control characteristic curve has a discontinuous increase, which is characterized by two values.

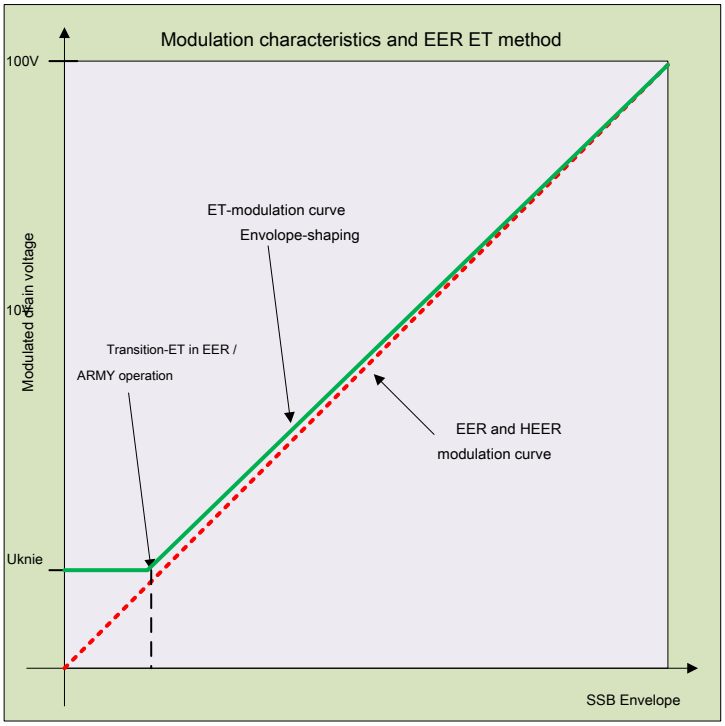


Figure 1: Modulated drain voltage as a function of the SSB input power

in every area you have to make sure that always sufficient supply voltage is available to provide the required instantaneous power.

Circuit descriptions of the pulse width modulator

The following are the new pulse width modulator solution for envelopes PAs is described. It enables in conjunction with the Hermes transceivers provide the variable operating voltage for the output stages. Figure 2 shows the basic structure of the power unit. One can see very quickly that the circuit arrangement a step-down converter (Buck converter or class-S modulator) to [3] is similar, and indeed how it works. The signal provided on the Hermes daughterboard PWM signal drives the gate of transistor T1. With the high level T1 conducts and C1 charges over L1. In this case, the longer T1 is conductive, the greater the voltage across C1. In the blocking phase of T1 (low level at the gate) of the freewheeling diode D1 takes over the energy flow from L1, which turns their polarity voltage abruptly. The output power can thus be maintained in the blocking phase of T1. The prerequisite is that the stored during the conducting period of T1 energy is sufficient in L1. then referred to as a "non-intermittent" operation. the energy content of L1 is not sufficient, then C1 is discharged through the load resistance more or less. There may be an interruption of the current flow (UDD = zero volts) are what a so-called "intermittent" operation entails. The whole procedure is very similar to the principles in switching power supplies. The main difference is that in switching power supplies by a "feedback control", the pulse width is changed for T1 so that there is always a constant output voltage. This here is not wanted,

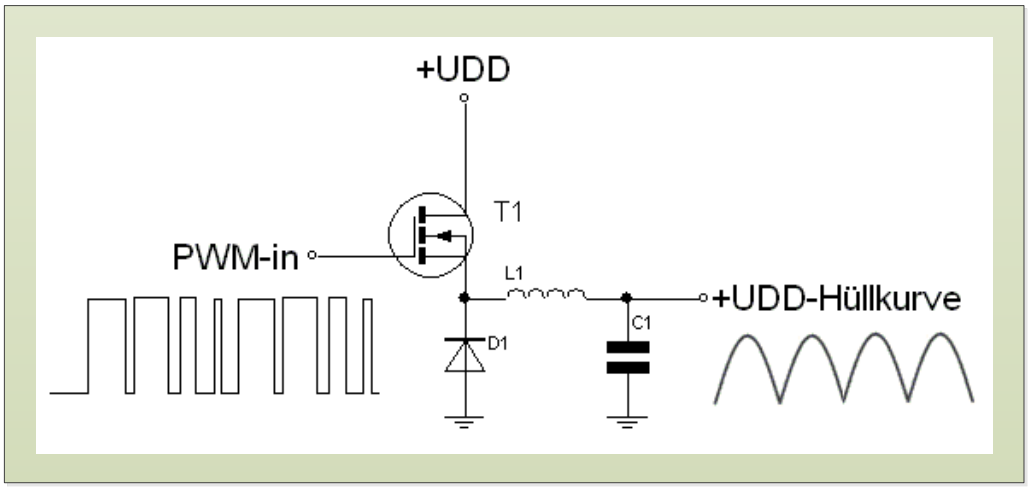


Figure 2: Activation of the buck converter (Class-S modulator) with PWM signal from the Hermes transceiver.

Figure 3 shows the generated from the Hermes-board digital PWM signal for a two-tone modulation. At a switching frequency of 240 KHz (fixed in the Altera FPGA of Hermes boards specified) the period is approximately 4.16 microseconds.

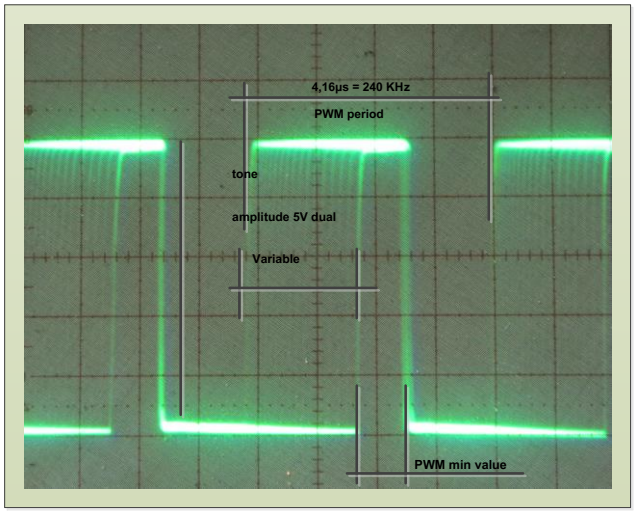


Figure 3: PWM control signal from the Hermes transceiver for a two-tone.

It can clearly be seen, the set for the minimum operating voltage of fixed value with PWM min = 100th During this period, the operating voltage is constant and is approximately 10 volts (Mosfetkniespannung). The exact value can be finely adjusted and is dependent on the Mosfettyp in the PA. The variable amplitudes can guess the "slurred" display area of imaging. 3 The generated with this PWM-modulated setting operating voltage is illustrated in Figure 4.

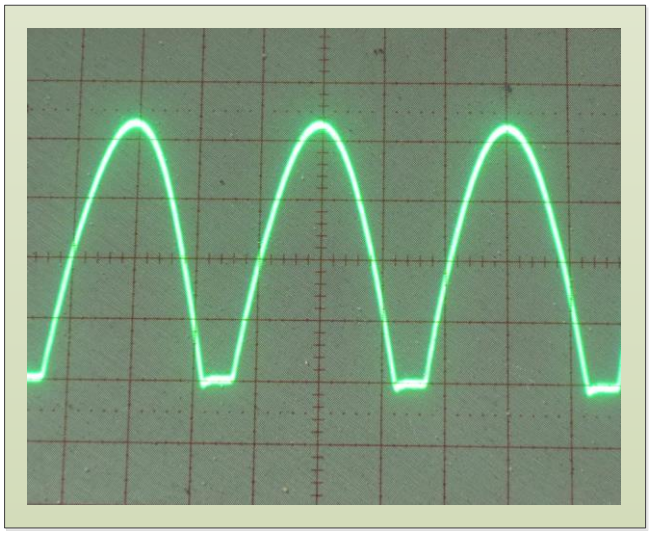


Figure 4: modulated operating voltage curve for a two-tone with limitation of the minimum value.

PWM power unit

The PWM power section has the object to provide the generated PWM signal from the Hermes-board in a modulated in the rhythm of the envelope of operating voltage for the power amplifier PA.

The of the daughterboard [see 2] coming digital PWM signal shown in Figure 3 has an amplitude level of approximately 5 volts and is amplified in the input driver IC type MCP14E11 to an output level of 12 volts, and at its two outputs 5 and 7 to 180 ° out of phase with the low and high side driver IC type UCC27714 the company TEXAS INSTRUMENTS fed. Figure 5 shows the steep edges are regenerated illustrated 12 volt PWM pulses.

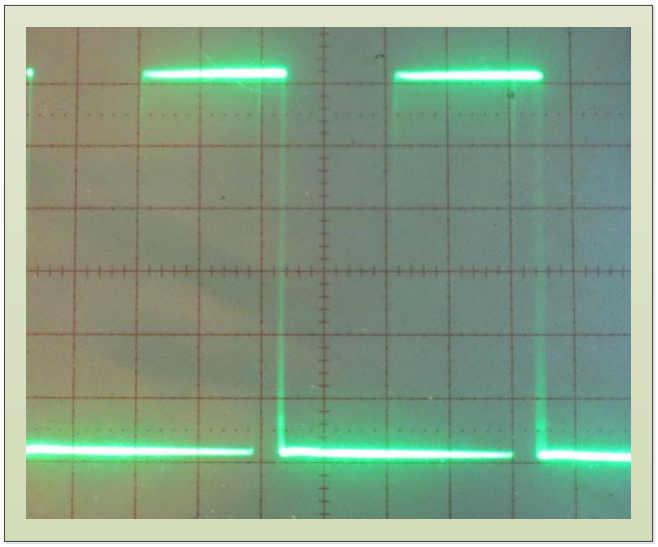


Figure 5: steep-edged 12 volts PWM pulses behind the input driver.

Figure 6 shows the complete circuit diagram of the new PWM solution. The author has compared to the publication in 2014 in the FA solution with a high-low-side driver IR2113

decided by International Rectifier for High-Low-Side Driver UCC27714 TEXAS INSTRUMENTS because this can apply each 4 Amp gate drive current. The IR2113 can drive on its outputs only 2 amps. All other technical parameters are almost identical between the two types.

On PTTin input of the modulator is activated. About the high-active input (enable input) EN (pin 4) is linked with the UCC27714 the PTT controller via T1, so as to ensure that no switching occurs in the case of reception.

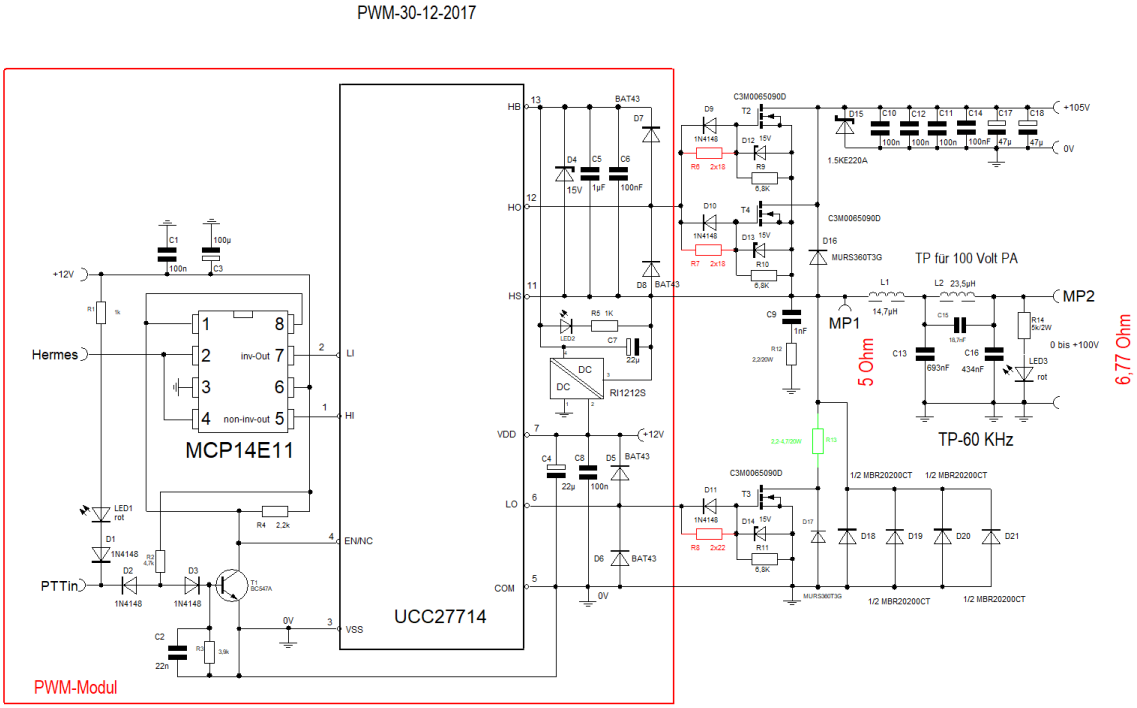


Figure 6: diagram of the PWM modulator

In the IC itself, there is a so-called high-voltage level shifter, provides the Gateansteuerimpulse for the high-side in the floating mode at the output HO (pin 12). Figure 7 shows the basic circuit of the UCC27714.

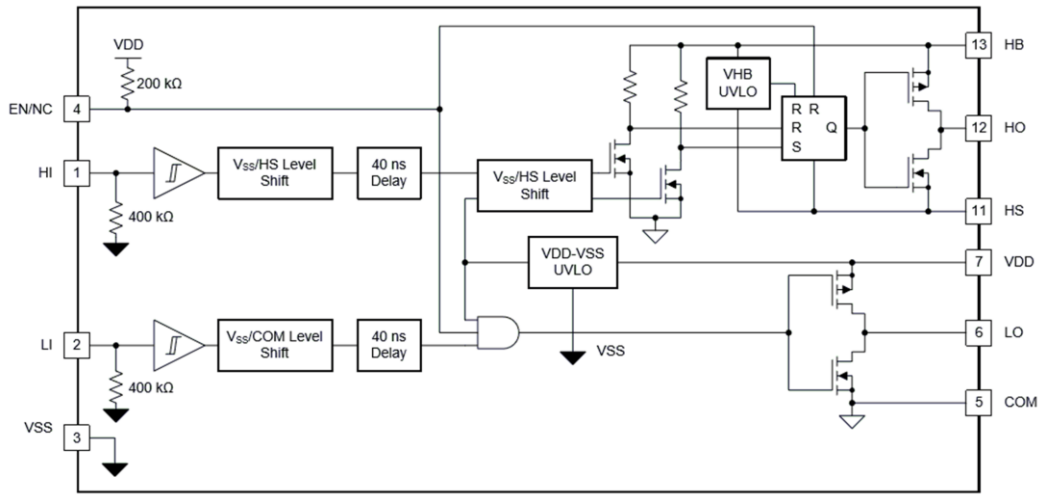


Figure 7: block diagram of the UCC27714 (Source TI sheet UCC27714, [6])

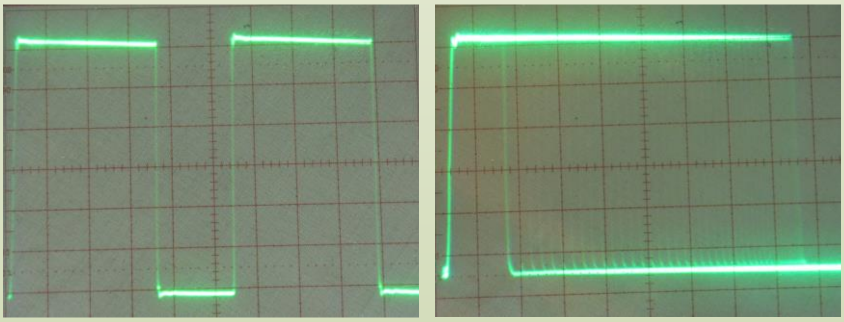
The outputs HO and LO are each equipped with a complementary Mosfetendstufe and therefore allow both the source and sink operating the same maximum output current. On the high- and low-side side there is a so-called "under Voltage-

lockout (UVLO) protection "feature which HO and LO outputs regardless of the status of the inputs" deactivated HI "and" LI ", when either the voltage (to VDD $V_{VDD (off)}$, Pin 7) and / or the voltage between HB and HV ($V_{VHB (off)}$, Pin 13-pin 11) to the minimum voltage value ((VVDD off)) is less than 4 volts.

The output signal for the high-side control pulses HO at pin 12 toggles between HB and HS having a maximum amplitude of approximately 12 volts. The voltage potentials to HB and HS are directly influenced by switching condition of T2 and T4. The targeted maximum duty cycle values of> 90%, it makes sense to resort to the power supply of the high-side to a DC / DC converter. As a DC / DC converter of the type RI1212S the company International Recom is used with galvanic separation to voltages up to 1000 volts here. Its insulation capacity is from 30 to 85 pF, making it small enough to decouple the primary and secondary sides.

The diodes D4 to D8 support the protection of the outputs against voltage spikes. In addition to 15 volt zener diodes fast Schottky diodes of the type BAT43 come at this point are used. The gate resistors R6 to R8 are too blunt an overshooting of the steep-sided switching pulses, often called "ringing" minimized. It is at this point in the short, low inductance connections between the outputs of the UCC27714 and the gate terminals of the switch MOSFETs. The exact value of these resistors is inter alia dependent on the applied Mosfettypen. The diodes D9 to D11 to accelerate turning off the MOSFET, making it between T2 and T4 is related to T3 no significant Einschaltphasenüberlappung. The resistor R13 additionally limits the current during this short overlapping phases. Its value lies with the 50 volt LDMOS variant at about 2.2 ohms and 100 volt version 4.7 ohms. A dead time is not required in this buck converter as opposed to a full-bridge circuit.

The central point (MP1) in the PWM power section form the connections between L1, the source terminals of the MOSFET T2 and T4, the PIN 11 (HS) and the cathodes of the flywheel diodes D18 to D21. The pulses at this point (MP1) can be seen input and adjoining envelope signal from the Hermes transceiver in Figure 8 with active PTTin.



Pulses to MP1 for an unmodulated RF carrier

Pulses to MP1 for a two-tone SSB

Figure 8: PWM pulses at the measuring point MP1 with an amplitude of 100 volts for a fixed HFTräger and an SSB dual tone

It is very important to avoid strong overshoot at this point. The reasons for this are firstly the necessary surge protection and on the other to the requirements for modulation accuracy, especially at low output voltages. To support the overshoot damping the Snupper network was introduced consisting of C9, R12. It should also be realized by the PCB layout a low-inductance wiring. There are switching MOSFETs to use with small possible Gehäuseinduktivitätswerten. The sum of all three measures brings an effective suppression of overshoots to the existing at this point steilflankigen 100 volt pulses. The driver IC has the data sheet a dielectric strength of 600 volts, the freewheeling diodes MBR 20200CT of 200 volts and the selected MOSFET type C3M0065090D of up to 900 volts. The freewheeling diodes as the switching MOSFETs also effectively cool. For the switching MOSFETs already indicated powerful Mosfets were as initially selected in Silicon Carbide technology from CREE. This can supply a continuous current of 36 amperes and an RDS (on) value of about 65 mOhm. A special feature of the inserted here Silicon Carbide MOSFET compared to the "normal" Schaltermosfets better thermal stability, of which the author was able to convince. Since two Mosfets are provided on the high-side side, a maximum output current of 72 amps would be theoretically possible. In a 1 KW LDMOS PA with 50 volt operating voltage can be expected with a maximum peak current of 30 to 35 amperes. For the author in the FA stitching 5 and 6 2017vorgestellte 100 volts PA project the maximum peak current reaches values of up to 15 amps. In this case, only a Mosfet must be fitted on the high side. A look at the data sheet of this type Mosfet reveals a maximum input capacitance at the gate of 660 pF. This is extremely convenient for Mosfets this performance class. Thus, the employed in the solution of 2014 between driver IC can be eliminated. but the MOSFET type C3M0065090D also has disadvantages compared to the Schaltermosfets the company IXYS. The drain terminal is on the metal back of the TO housing 247-3, resulting in isolation by means of mica insulation discs to the heatsink For the author in the FA stitching 5 and 6 2017vorgestellte 100 volts PA project the maximum peak current reaches values of up to 15 amps. In this case, only a Mosfet must be fitted on the high side. A look at the data sheet of this type Mosfet reveals a maximum input capacitance at the gate of 660 pF. This is extremely convenient for Mosfets this performance class. Thus, the employed in the solution of 2014 between driver IC can be eliminated. but the MOSFET type C3M0065090D also has disadvantages compared to the Schaltermosfets the company IXYS. The drain terminal is on the metal back of the TO housing 247-3, resulting in isolation by means of mica insulation discs to the heatsink For the author in the FA stitching 5 and 6 2017vorgestellte 100 volts PA project the maximum peak current reaches values of up to 15 amps. In this case, only a Mosfet must be fitted on the high side. A look at the data sheet of this type Mosfet reveals a maximum input capacitance at the gate of 660 pF. This is extremely convenient for Mosfets this performance class. Thus, the employed in the solution of 2014 between driver IC can be eliminated. but the MOSFET type C3M0065090D also has disadvantages compared to the Schaltermosfets the company IXYS. The drain terminal is on the metal back of the TO housing 247-3, resulting in isolation by means of mica insulation discs to the heatsink In this case, only a Mosfet must be fitted on the high side. A look at the data sheet of this type Mosfet reveals a maximum input capacitance at the gate of 660 pF. This is extremely convenient for Mosfets this performance class. Thus, the employed in the solution of 2014 between driver IC can be eliminated. but the MOSFET type C3M0065090D also has disadvantages compared to the Schaltermosfets the company IXYS. The drain terminal is on the metal back of the TO housing 247-3, resulting in isolation by means of mica insulation discs to the heatsink In this case, only a Mosfet must be fitted on the high side. A look at the data sheet of this type Mosfet reveals a maximum input capac

requires. In addition to the C3M0065090D in TO147-3 package is available from the company CREE also the same type MOSFET in a D2PAK-7L package. Figure 9 shows both against Package forms.

Figure 9: Two different versions of the package C3M0065090 Mosfets (Source: CREE sheet, [5])

The MOSFET in 7L-D2PAK housing is wired as shown in Figure 10 degrees. is clearly evident that 5 pins are wired in parallel to reduce the source Terminal inductance. In addition, the input circuit to pin 2 is decoupled induktivitätsmäßig.

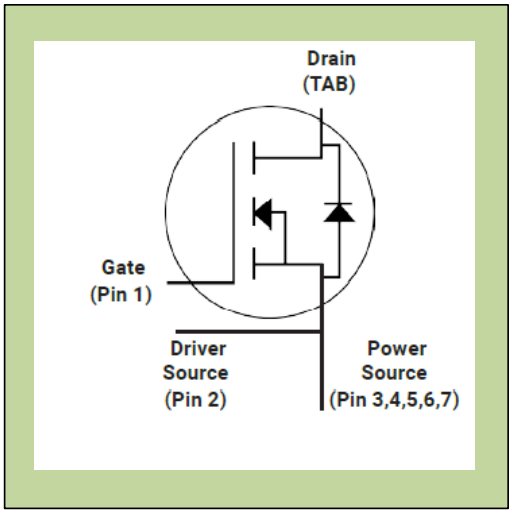


Figure 10: wiring of the J-MOSFETs in 7L-D2PAK housing (Source: CREE sheet, [5])

The drain terminal has no connecting legs, but is directly connected to the metal back of the housing. The advantages of this measure are obvious. The amount of the induced voltage on a conductor line or connecting leg depends on the particular magnitude of the inductance and the rate of change of current (di / dt). In general:

Uind = 1 / T * Integral (L * di / dt), time limits t = 0 to T

As shown above, flow about 30 to 35 amps at 50 volts LDMOS PA in the tip. Every millimeter Anschlussbein- and trace length has an extremely detrimental effect on the function of the circuit. In addition, steep-edged pulses are expected, which attracts a large di / dt to be. The author therefore recommends the use of the 50 volt version, the package form 7L-D2PAK. For the 100 volt version, the Mosfet variant ranges TO147-3 housing.

The lower low-side driver strand in the UCC27714 would for a simple buck converter not really necessary, as it indeed shows the block diagram in Figure 2. It is used as a drive channel for the tail-biter MOSFET T3 in this case. T3 switched in opposite phase at T2 and T4. it ensures via the resistor R13 when switching off of T2 and T4 for a steep-sided drop of the signal at the center point M1 of the PWM. This has the linearity of the PWM arrangement at low output voltages, which in turn requires very narrow short pulses of about 100 ns, significantly improves the advantage. The minimum output voltage of the PWM is ca.0,5 volts. With a maximum voltage of 100 volts, this means a linear dynamic range of 200 and logarithmically of 43 dBu. The objective set for the PA development was 40 dBu dynamic range, which has been well achieved through the use of the tail BiterMosfets. Figure 11 shows the influence of the tail BiterMosfets on the falling edge of the narrow output pulses.

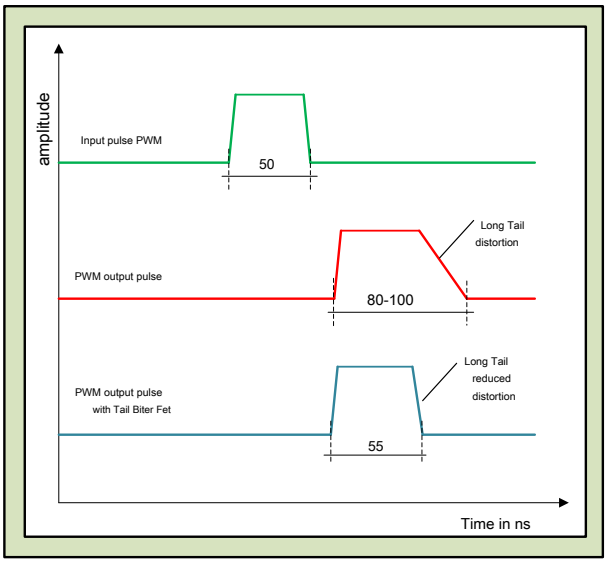


Figure 11: Effect of tail BiterMosfets to the output pulse shape

PWM output low pass

Supplied by the Hermes transceiver digital PWM signal containing the spectral signal components shown in Figure 12th The sidebands grouped around the 240 KHz PWM switching frequency and its harmonics with a bandwidth of approximately 60 KHz. The blue curve in Figure 12 shows the original 3 KHz wide useful band of SSBSignals, but which in a digital PWM signal by a factor of 8 to 10 to about 25 to 30 KHz widens (green curve). This fact must be taken into account when designing the PWM bandwidth and the output low-pass filter.

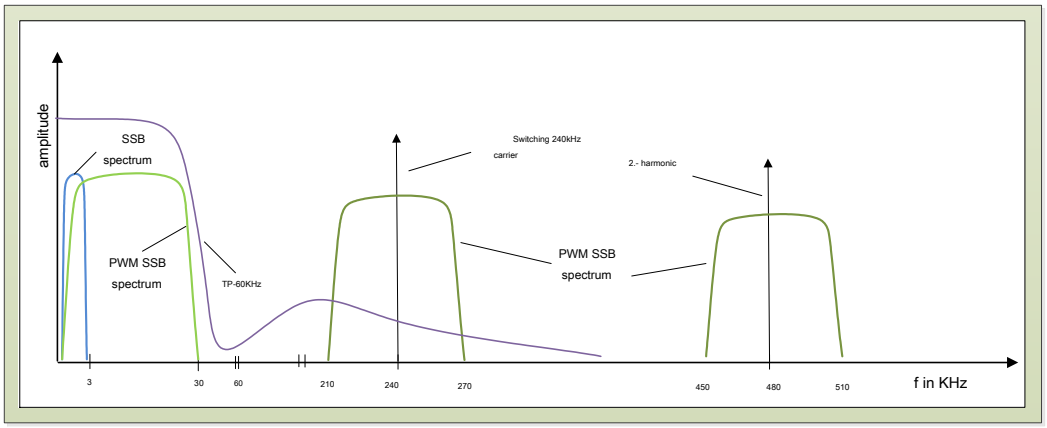


Figure 12: Spectral shares in the PWM signal interference in SSB useful band

For this it is necessary to separate the higher PWM signal components from the SSB useful spectrum and filter the interference components to at least 40 dB below the wanted signal. In the overall circuit diagram of the PWM as shown in Figure 6, this is done by the 60 KHz low-pass output. When dimensioning the component values of the output low-pass filter the RFSim99 [4] program was used. With a target maximum output of one kilowatt and a maximum operating voltage of 100 volts, a maximum peak current of 15 amperes flows. This results for the dynamic internal resistance of the ET-final stage, a value of about 6.66 ohms. Since the low pass from 4 elements, input and output impedance are not equal. In order to achieve a Z value of 6.66 ohms at the output is to be expected with this arrangement having an input Z value of 5 ohms. Figure 13 shows the found with the program RFSim99 values for a 100 volt 1KW PA (left) and a 50 volt 1KW LDMOS PA (right). It is very clear that the TP for the 50 volt PA must be very low impedance, by the time necessary for 1 KW output current for a 50 volt LDMOS PA longer be able to supply about 30 amperes. The voltage and current ratios are much cheaper at 100 volts PA.

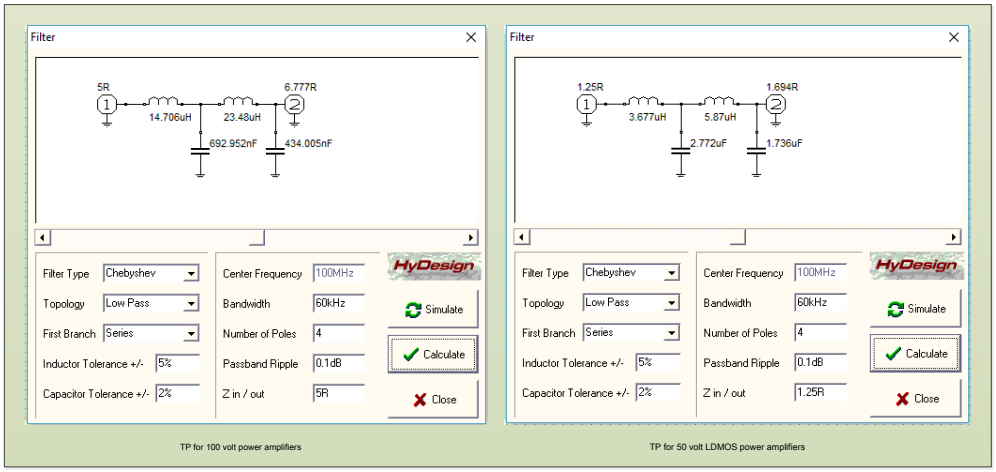


Figure 13: Determination of the components values for the output of the low-pass PWM means RFSim99

the 4-pole low-pass filter is supplemented whose resonance frequency is a Cauer-pole at 240 KHz. This measure increases the filter effect of the low-pass filter in addition to the intended switching frequency of the PWM. With about 60 dB attenuation of the 240 KHz switching frequency and the lower sideband a good suppression of the harmonics of the PWM signal is achieved.

A four-pole 60 kHz Chebyshev low pass (purple curve in Figure 12) has an average group delay of approximately 7 microseconds. This additional delay is compensated with the digital delay line in the Power SDR software. Figure 14 shows the appropriate settings in the Power SDR software.

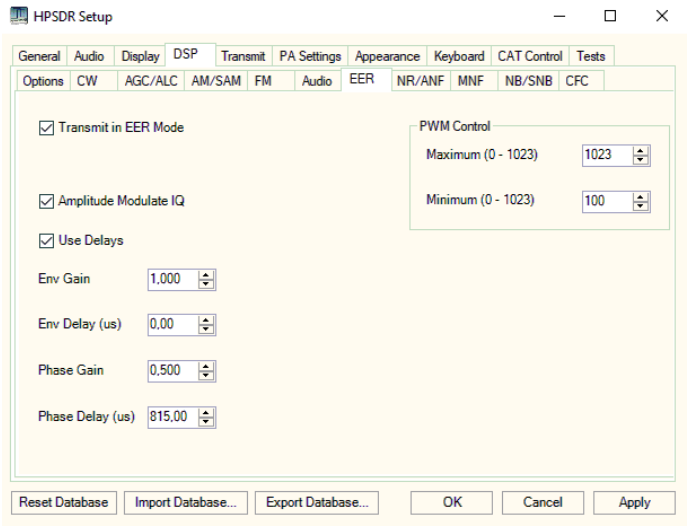


Figure 14: With the value in the "phase delay", the duration of the PWM low-pass filter is balanced with.

Approximately 808 ïS need the PC and the Hermes FPGA and 7µS brings the low pass of the PWM with one, so that overall a delay line value of 815 .mu.S results. This value may vary slightly in practice, depending on the PC system. One checks the necessary for the system delay value for the phase signal by means of a two-beam. Figure 15 shows this for an SSB dual tone of 1.2 kHz. The envelope signal of the PWM

and the phase signal of the SSB must lie exactly time-synchronous with each other. A tolerance of 1 to 2 microseconds are tolerable.

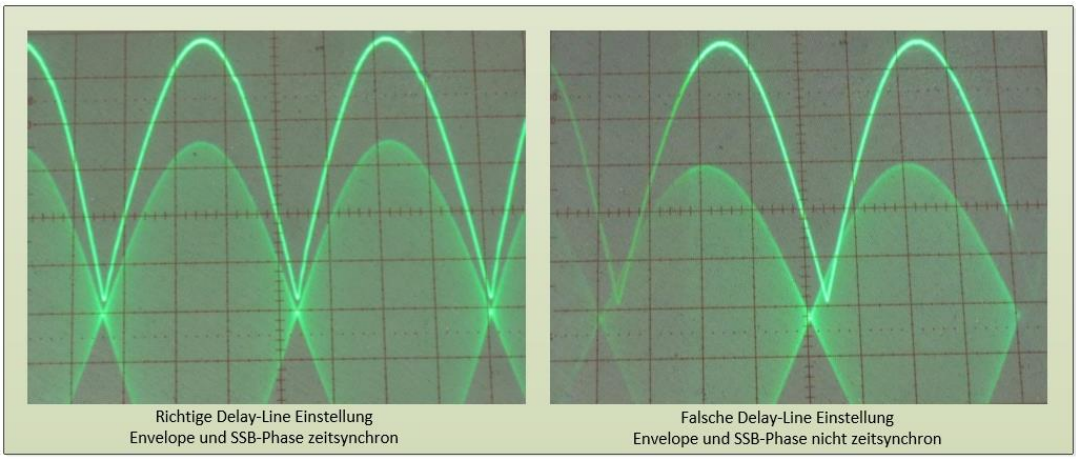


Figure 15: time-synchrony between Envelope and phase signal of the two-tone SSB

For the favored here Envelope-tracking process, it makes sense for the reasons already mentioned, adjust the minimum lower operating voltage on the knee voltage value of the PA Endstufenmosfets. If we choose, for example, for the PWM min setting a value of 100, is then obtained for the PWM output voltage of the provided in Figure 16 PA-voltage curve.

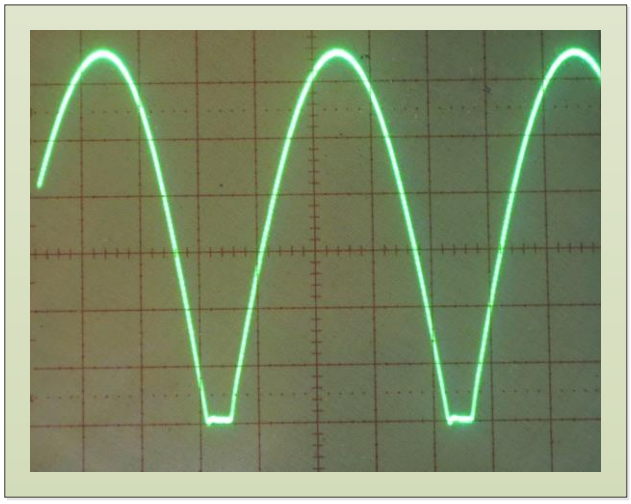


Figure 16: output voltage of a PWM min value of 100 volts

At a supply voltage of the PWM of about 105 volts, the minimum voltage value is then about 10 volts. This value is sufficiently above the knee voltage of the PA Endstufenmosfets type VRF3933 [see also 2].

How to build the PWM

The prototype of the pulse width modulator has been built on a 75mm x 160 mm double laminated circuit board. Figure 17 the layout of the PWM base board and Figure 18 shows the plug of the PWM module.

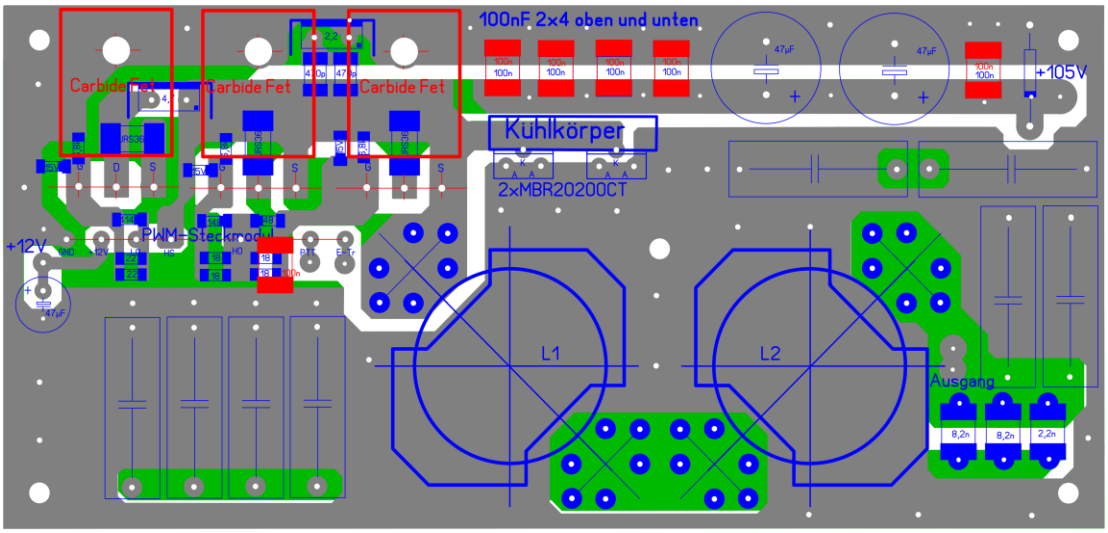


Figure 17: layout and component placement, the PWM base board

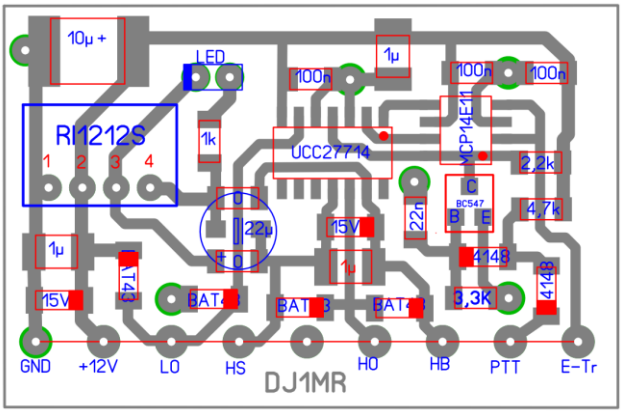


Figure 18: layout and assembly of the PWM plug-in module

For the realization of the inductances L1 and L2 of the PWM RM cores were 14 material used N41 with an air gap of one millimeter. The AL value is 250 nH per turn. As ferrite material is suitable for higher switching frequencies, in particular the material N87 and N97, however, these cores are only offered without an air gap. With acceptance of something higher losses Also, the material is N41. The windings L1 and L2 were prepared twisted for the 100 volt variant of 7x0.75 mm Cul. The Figure 19 shows the completely assembled plug-in module and PWM Figure 20 the structure of the PWM on a fishing heat sink having dimensions of 75 mm x 160 mm.

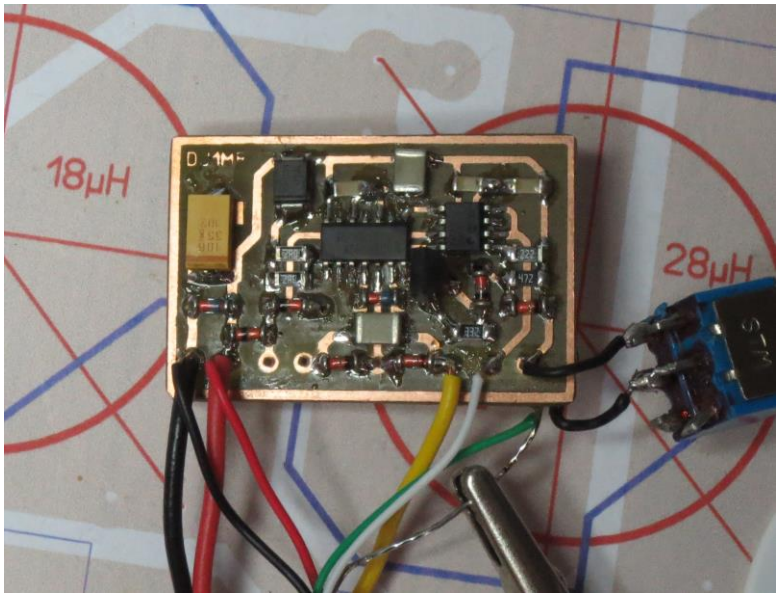


Figure 19: Prototype PWM plug-in module here still without DC / DC converter with charging diode

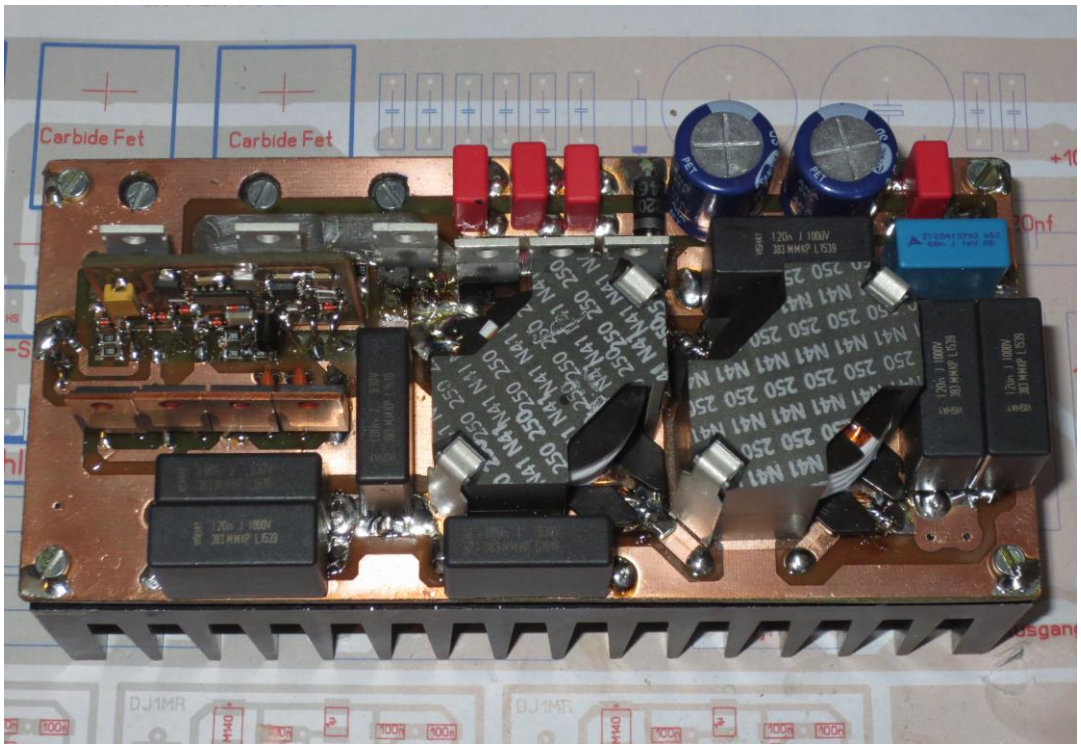


Figure 20: Completely assembled PWM prototype before commissioning

conclusion

The presented in this article PWM Solution to increase the efficiency of short-wave amplifiers shows that can be achieved through the use of modern power SDR software, hardware and modern components such as carbides MOSFETs easily crucial efficiency gains.

The presented pulse width modulator is not a beginner project. Both extensive experience in the development of RF circuits, as well as extensive experience in the construction of switching regulators and switching power supplies are required. The author recommends a better understanding of all the relationships associated with this project to read the articles specified in [1,2 and 3]. The presentation of further contexts outside of the concern of this paper.

Special thanks goes to the author of the OM Phil Harman, VK6APH, Warren C. Pratt, NR0V firmware in the FPGA of Hermes transceiver boards for the provision of the EER (Hermes firmware V3.3) and software modules within the Power SDR software as shown in Figure 14th the EER Hermes firmware V3.3 can be ordered as needed by the author

references

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[6] Data TEXAS INSTRUMENTS "high-speed, 600-V high-side low-side gate drivers with 4-A peak output UCC27714"

[7] Data Sheet MICROCHIP MCP14E9 / 10/11 "3.0A Dual High-Speed Power MOSFET Driver With Enable"

[8] Data Sheet ON Semiconductor "MBR20200CTSwitch - mode Power Rectifier Dual Schottky Rectifier "