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Software-controlled envelope tracking PA envelope for the short wave band

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Modern electronic devices must meet the requirements of time and are energy efficient as possible. This has so far been difficult to achieve in the short-wave PAs without software support. Thanks to modern software such.
As the "Power-SDR" Software of HPSDR group now exists the possibility also to control not only the control of the actual SDR transceiver, the PA energy efficient means of envelope tracking method. This paper uses the example of a 1kW MOSFET PA on a way to implement this goal into practice.

Power amplifier design for envelope tracking operation

Almost all short-wave amplifiers used in amateur radio, be it tube or transistor-PAs are characterized in that they are operated with a fixed operating voltage. The result is that a considerable proportion of DC power is converted into heat. The design of the present short-wave amplifier was chosen so that it can be operated with a fixed operating voltage and with modulated operating voltage. The different envelopes PA procedures and principles, the author has been described in detail in [3]. For the presented final stage, the envelope tracking method (short-ET) has been selected for use with modulated operating voltage. The operating voltage for the modulator output stage of the pulse width modulator (PWM) described by the author in [3] is used.

The semiconductor industry has powerful LDMOS transistors published in the recent presence in 50 volt technology, have been successfully implemented with several PA DIY projects. The author has not decided in this project due to the operating voltage of 100 volts desire for the known current LDMOS transistors. In general, devices with higher voltage can expect good transmission parameters due to the favorable dimensioning of the output transformers. Also, the maximum currents can be reduced to less than 20 amperes at a maximum operating voltage of 100 volts. The choice fell on the vertical N-channel RF-power MOSFET type VRF3933 the company Microsemi.

This paper is designed to encourage interested selbstbau OMs to gain experience with Hüllkurvenkurzwellen PAs. This is, inter alia, also facilitated in that the power SDR software for the Hermes transceiver board can provide the control signal for the PWM also the same.

ET method

The ET process provides the least demands on the precision modulation of the operating voltage for the output stage of the three envelope-PA method. In this process the amplitude information of the PA input signal is not cut off, but continue to be used by the AB output stage and amplified. The control of the ET-end stage of the PWM is carried out not with the original rectified envelope, but is performed by the power SDR software with a modified geshapten envelope. The modification of the PWM envelope takes place in the shape of that at no or very low SSB signal, the operating voltage for the output stage is not zero volts but above the respectively used Mosfetkniespannung located. This has the advantage that the Ausgangsmosfets must not be operated in the triode region and therefore unwanted distortions, caused inter alia by the non-linear high capacity arise. With increasing modulation of the operating voltage is then incremented in the rhythm of the SSB envelope, ie, the linear voltage control operation as in the EER and EER-H usual method, the power supply characteristic approaches to. Figure 1 shows this process (dotted blue and green curve).

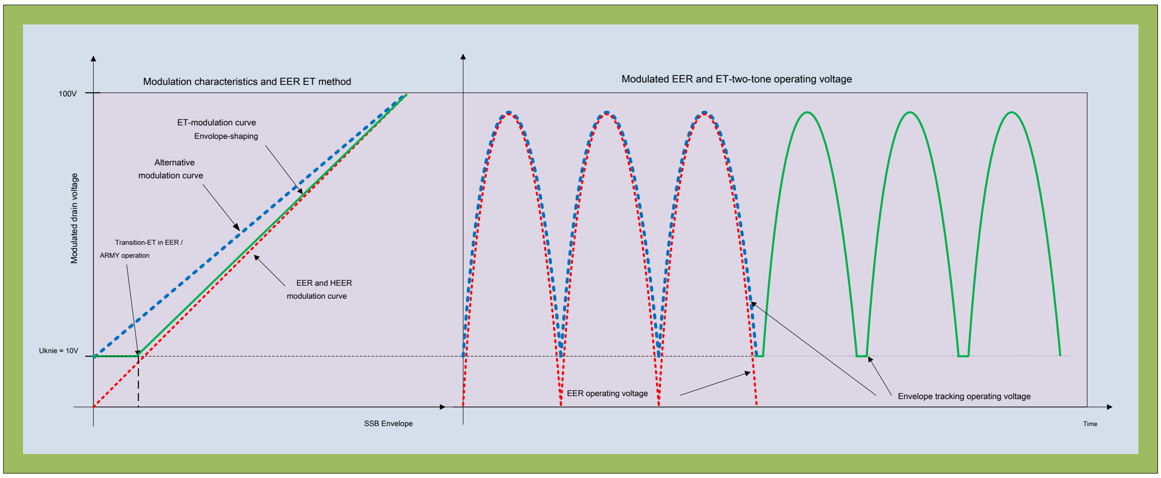


Figure 1: modulation characteristics of EER, HEER and ET-operation

You must ensure that there is always sufficient operating voltage available to provide the required instantaneous power in each control range of the PA. is known, this mode of an output stage of the audio range. It is referred to there as a class H mode. If the operating voltage is switched in two to three discrete stages, one speaks of the Class G operation.

A comparison of the efficiency between the power amplifier classes, shown in Figure 2, shows very clearly that substantial increases in efficiency can be achieved through the modulation of the operating voltage with respect to a normal class AB output stage, in particular for small and medium modulations. The best efficiency achieve Class D and their subgroups E, F and EF output stages.

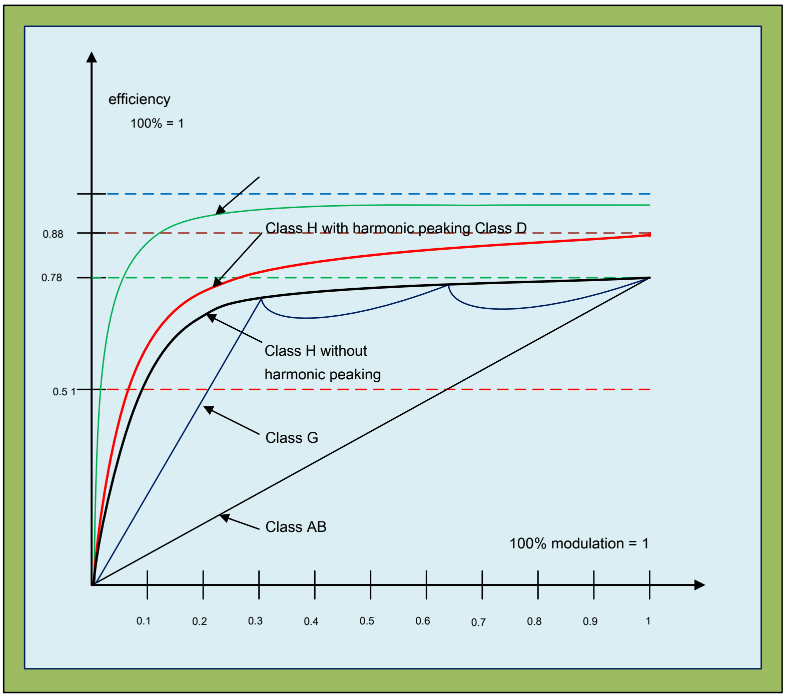


Figure 2: efficiency curves of different amplifier classes

Use of power-SDR software for the envelope modulator (PWM)

For users of power SDR software is available to allow direct control of Hermes transceiver the possibility the PWM and thus the shape modulation operating voltage under the tab DSP / EER. Figure 3 shows these possibilities. can with the value in the PWM Control "minimum" to set the minimum operating voltage value (eg, value of the knee voltage of Endstufenmosfets, here about 10 volts) and a maximum field the maximum value that should be achieved, the operating voltage at full load (in this case 100 volts).

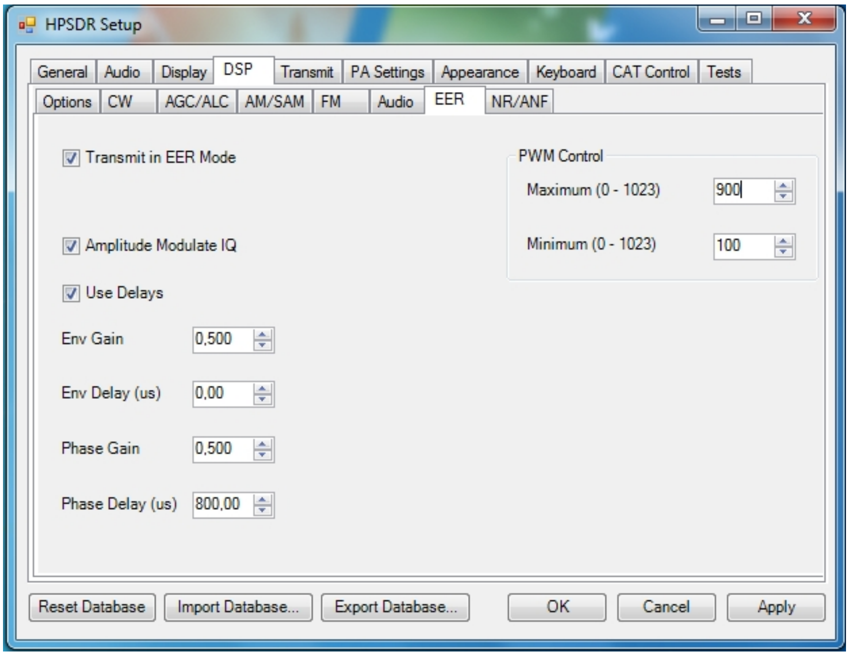


Figure 3: adjustment of the PWM modulation curve using power SDR software

When ET method, it is, like all HK method (EER, Army) important that the envelope of the SSB signal (modulated operating voltage) just in time to the phase signal is applied to the output stage. Delays of the envelope with respect to the phase signal are tolerable for the ET method to about 10 microseconds. The more accurate the match is, the better IMD3 values are reached. Larger deviations can be recognized by asymmetric intermodulation spectra. That is, the individual IMD carrier (3, 5, 7, 9, etc.) have on both sides of Zweitonspektrums different amplitude values. In the power SDR software this time relationship between two signals with the input fields "phase delay" and "Env Delay" now is very finely adjusted. This property is equivalent to a programmable delay line. OM goods C. Pratt, NR0V, the developer of the EER software accomplishes this by multiple spending towards Altera FPGA of Hermes transceiver. For the employed in this project system components such as PC Power SDR software and Hermes transceiver of the determined phase delay is value at about 800 microseconds. The value of 800 microseconds does not mean that a delay of 800 microseconds is produced by the TP of the PWM power unit, but that the Phasensignal- and Hüllkurvensignalbereitstellung for the PA due to software apart by approximately 800 microseconds. It is therefore essentially due to the system processing times in the PC and the FPGA of Hermes transceiver. The existing in the PWM low pass additionally generated about 7 microseconds delay time between envelope phase signal at a switching frequency of 250 KHz. Figure 4 shows in the left part,

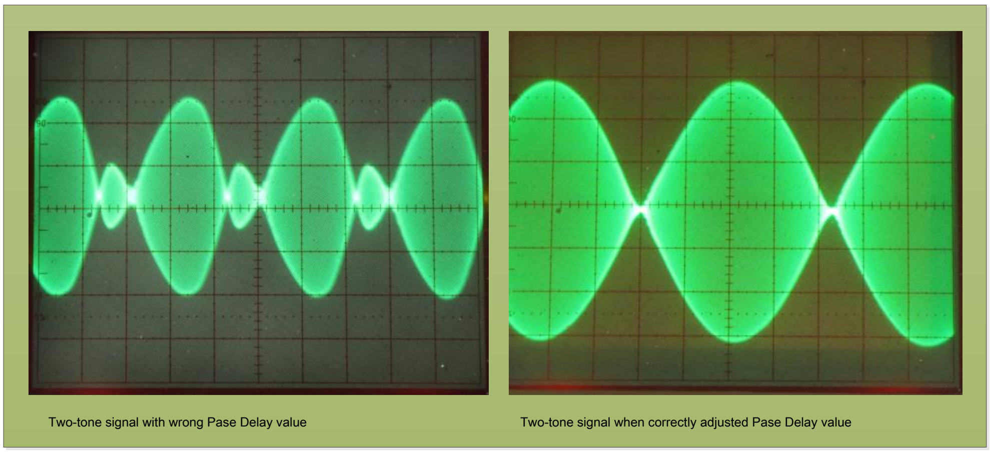


Figure 4: two-tone signal at the output of the PA at ET wrong and properly adjusted phase delay value.

This test should be carried out for Zweitonfrequenzen of 200 Hz, 1.2 kHz and 2.9 kHz. In all Zweitonfrequenzen the two-tone RF output signal of the PA is required to have a correct course. The variation of Zweitontestfrequenzen can be very comfortable and easily performed by the Power SDR software under the "tests".

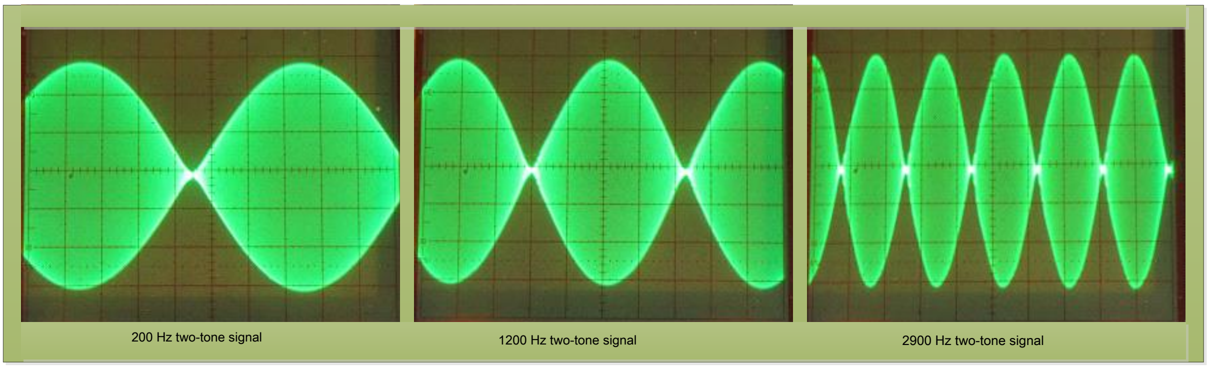


Figure 5: two-tone signal throughout the NF-SSB band at a correctly adjusted phase delay value of about 800µs

You can check the found delay value with a two-beam. Figure 6 shows the a low pass with a cutoff frequency of approximately 35 KHz recorded PWM output signal from the Hermes-transceiver (below) for a two-tone and the associated HF SSB two-tone signal to the TX output of the Hermes transceiver. In Figure 6 it is clearly seen that the SSB envelope is delayed from the SSB input signal.

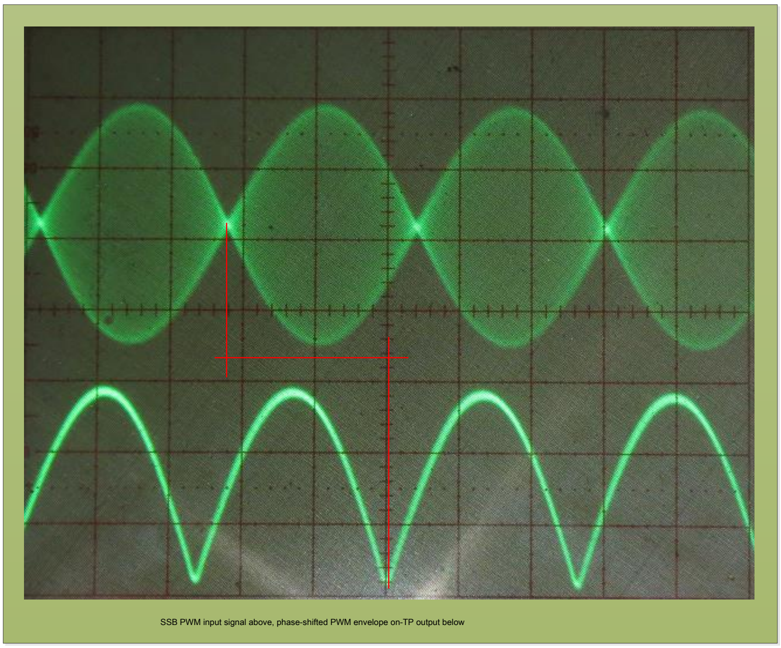


Figure 6: time delay between the PWM input signal and generated PWM envelope of about 800 microseconds at a Zweitonfrequenz of 1.2 KHz

PWM Control Settings

In this project, because that will ET procedures for the PA to be used, the author of the application at Figure 1 in green shown modulation curve. With the set PWM Control minimum to set the starting voltage and for the final stage. You should as already mentioned are just above the knee voltage of Endstufenmosfets used.

Figure 7 shows the "minimum" modulated with the PWM of the author operating voltages for the ET final stage in SSBZweitonaussteuerung for three different settings in the PWM Control.

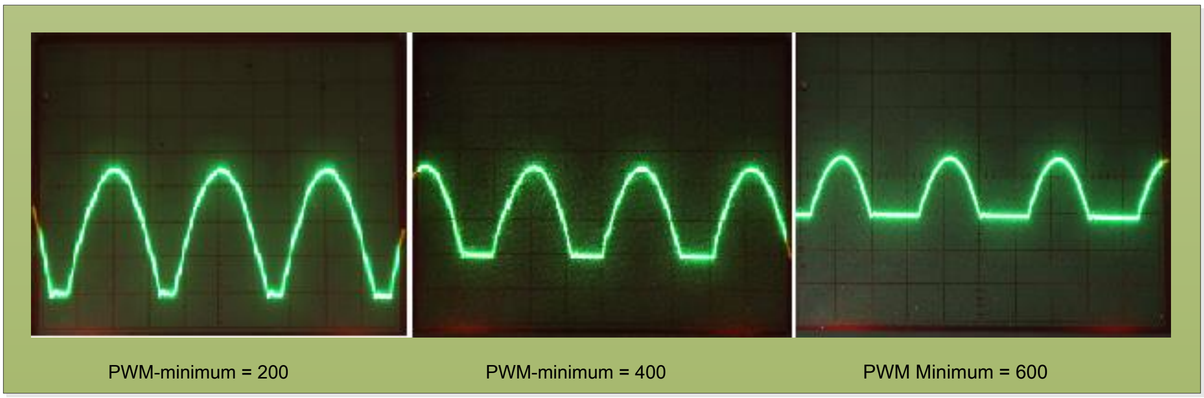


Figure 7: modulated operating voltage in dependence on the PWM Control (20 volts / tick)

For the described power amplifier, the values of 10 volts to the minimum value in the field and at 100 volts with the maximum value in the field to be set. Are used in this project two series-connected 48-volt switched mode power supplies, said first power supply is set at 50 volts and the second power supply to 55 volts, so that a total of 105 volt operating voltage for the PWM yield. 5 volts drop at full in the PWM modulator from the residual stress, so that the maximum operating voltage value is 100 V for the output stage. Figure 8 shows three examples of the operating voltage waveforms when is modulated instead of the two-tone modulation with the human voice. It is clearly seen that the integral over the time course of voltage fails substantially smaller than at a constant operating voltage.

the transistors decreases enormously and the fan for cooling the power stage are almost superfluous. In particular, during the speech pauses the transistors are charged significantly less while holding the PTT switch, as the operating voltage drops to about 10 volts. The quiescent power dissipation falls characterized in that intervals of 200 Watt (100Vx2A quiescent current) to about 20 watts (10Vx2A) from and is opposite amplifiers with fixed operating voltage only 1/10.

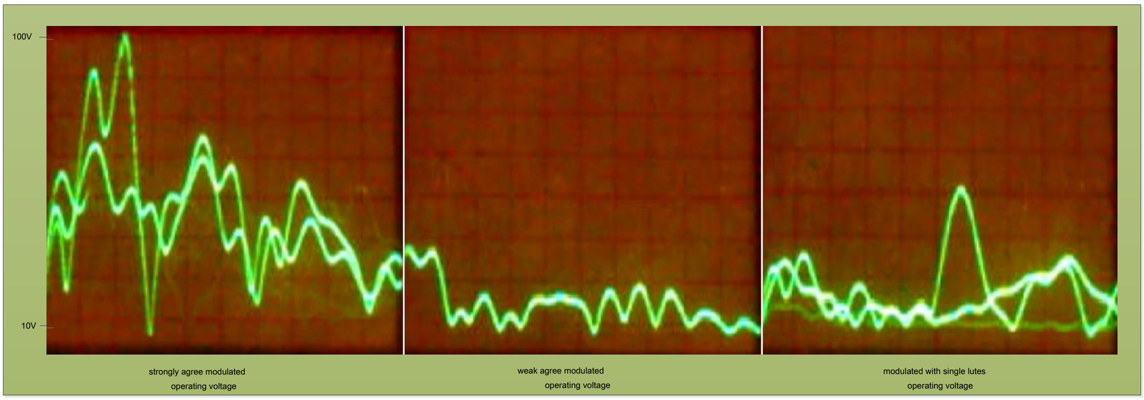


Figure 8: Time course of modulated with a human voice operating voltage of the PA for the envelope tracking operation.

All other settings in the SDR software should be made as shown in Figure. 3 These include in particular setting the hook "Transmit in EER Mode", "amplitudes Modulate IQ" and "Use delay" to turn on the Software Delay Line. The entry field for "Modulate IQ" ensures that the SSB signal at the TX output the Hermes transceiver reserves the amplitude information, which is essential for the ET-operation. If one takes the hook out the SSB output signal having the TX output a constant amplitude and is suitable amplifiers for the control of EER. the value in the "Envelope gain "affects the amplitude level of the modulated operating voltage and should be set at the beginning of the adjustment to values between 0.5 and 0.8. It is important to know, that the PWM output value of the Hermes board is independent of the drive controller setting the power SDR software. The value in "Phase Gain" field is of no importance for this application and can be set to the value 0.5. The software also allows to set the value "Env Delay", which would lead to a digital delay of the envelope with respect to the phase signal. but this is an unlikely application in practice.

Connecting the PWM to the Hermes transceiver

The firmware of OM Phil Harman, VK6APH developed Hermes in the Altera FPGA provides the digital PWM signal to jumpers J14, Pin 2 of the Hermes board. The author has accompanied the development of FPGA firmware and software EER in numerous tests. The EER-end in the Power SDR software itself has OM Warren C. Pratt, NR0V developed. Also with him was made a lively exchange of test results. The heart of the EER-ends in the power SDR software provides the programmable digital delay line for the SSB phase signal and SSB Envelopesignal. The logic level at the output FPGA be between 0 and 3.3 volts. a level of + 3.3V (operating voltage of the Altera FPGAs) and to pin 5 is the "ground" reference potential at pin 1 of J14.

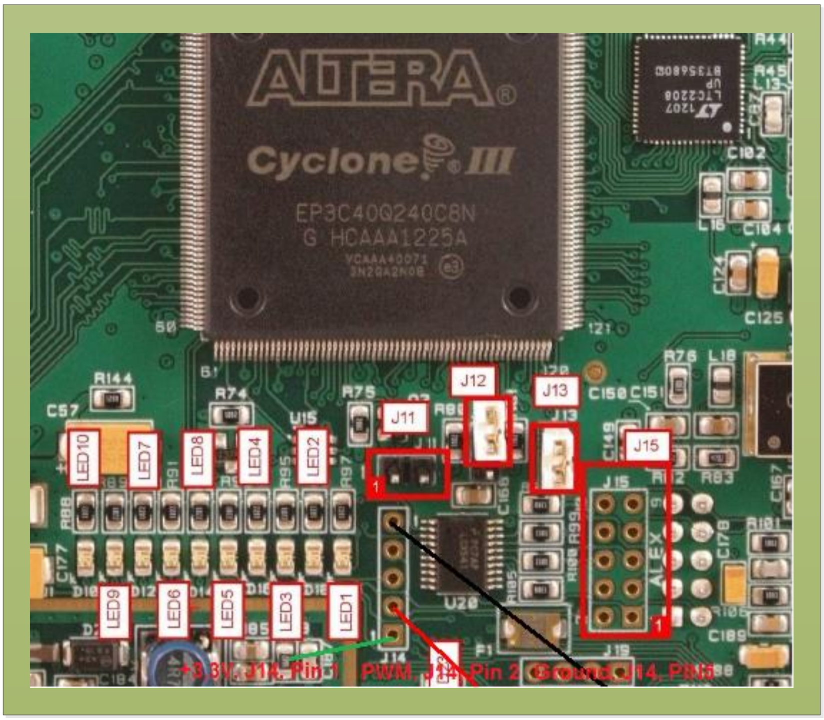


Figure 9: jumpers J14 Hermes board

The author has soldered a 5-pin plug connector in 2.54 mm grid on the Hermes board for J14, which is relatively safe to do so. Then, the terminal panel for the digital PWM signal is then plugged. In order to avoid noise and couplings between the transceiver and the Hermes-PWM, for the galvanic decoupling of the transceiver and PWM fast CMOS optocoupler Hewlett Packard HCPL type is used 0721st Figure 10 shows the plugged on J14 PWM connection board.

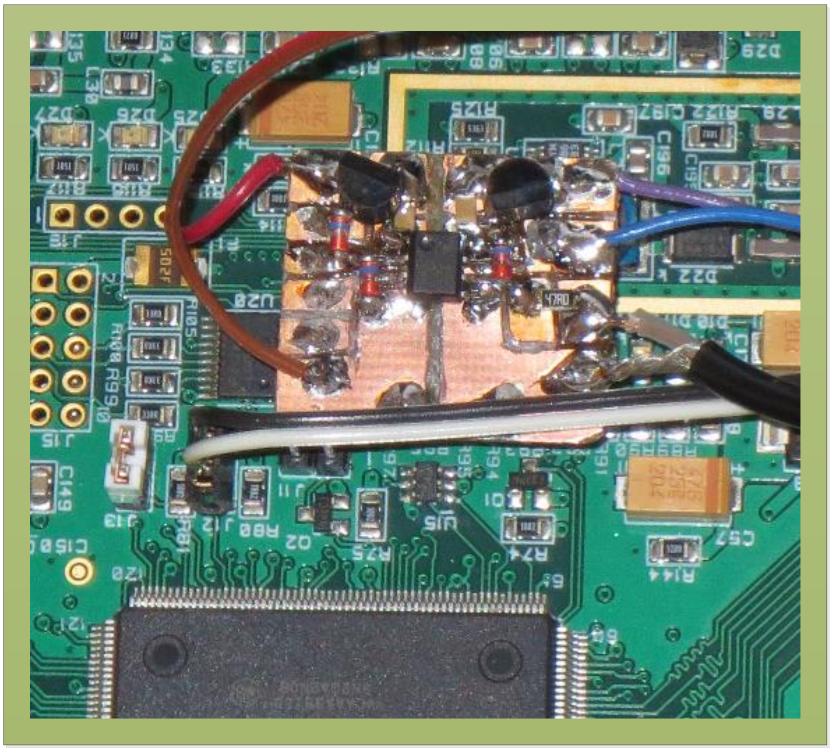
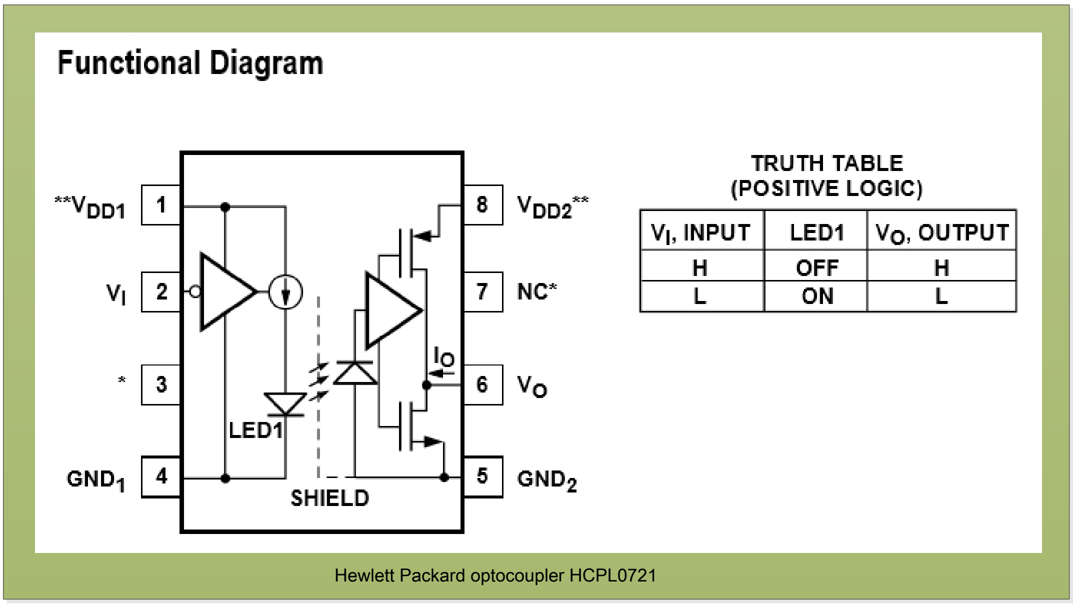


Figure 10: Plugged connection board with the HP Optocouplers HCPL 0721

It was initially designed as a universal board for testing purposes. In Figure 11, the internal circuit diagram of the opto-coupler is illustrated. Both supply voltages VDD1 and VDD2 are stabilized by means 78L05 voltage regulator on each of 5 volts. Blocking capacitors of 100 nF at the inputs and outputs of the voltage regulator are necessary for suppressing voltage peaks. To protect the inputs and outputs of the optocoupler from spikes two fast Schottky diodes are used. The input Vi, Pin 2 of the HCPL0721, is on the underside of the daughterboard arranged 5-pole female connector connected directly to pin 2 of J14. The PWM output signal is applied to pin 6 (Vo) of the HCPL0721 removed over a small protection resistor of 4.7 Ohm and switched to the PWM through a shielded about 2 meters long four-pole USB cable. This cable is also the voltage supply for the voltage regulator 78L05 is provided on the secondary side of the terminal board from the PWM. As connectors for the USB cable between Hermes transceiver and PWM, USBEinbaubuchsen own. Hermes transceiver this socket should be installed insulated to avoid unnecessary couplings between transceiver and the PWM.



Hewlett Packard optocoupler HCPL0721

Figure 11: internal circuit of the optocoupler HCPL 721 (source [11])

Figure 12 shows the circuit of the small daughterboard for galvanically isolated provision of the digital PWM output signal.

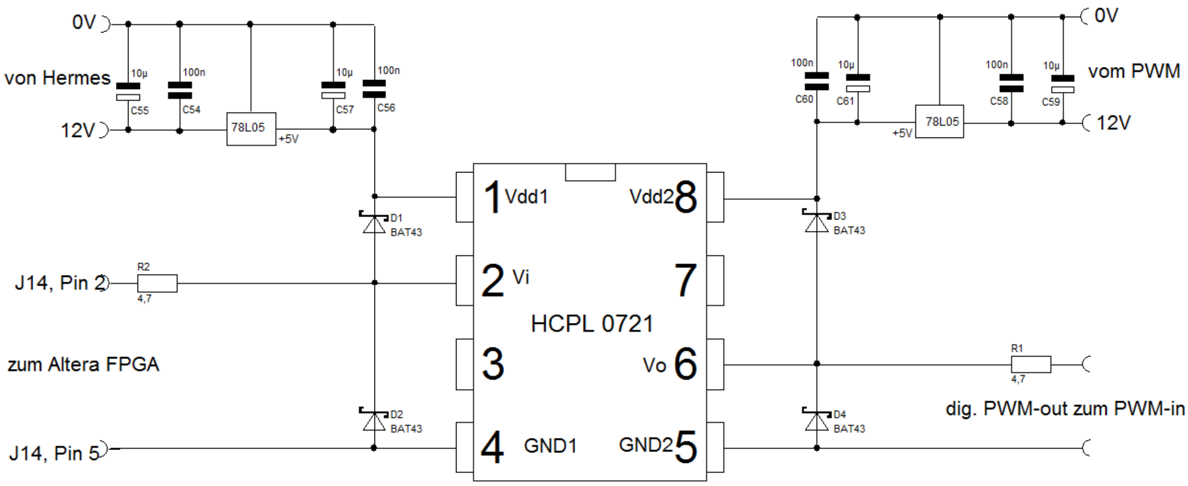


Figure 12: PWM circuit of the daughterboard

The output pulses of HCPL0721 are very steep flanks. Therefore it is essential to use a shielded cable. Figure 13 shows the PWM signals from the Hermes transceiver at the output Vo of the optocoupler. a two-tone signal with different PWM Control minimum settings. The amplitude height is almost 5 volts, for safe driving the PWM driver input of the type MCP14E11 by [3] is sufficient.

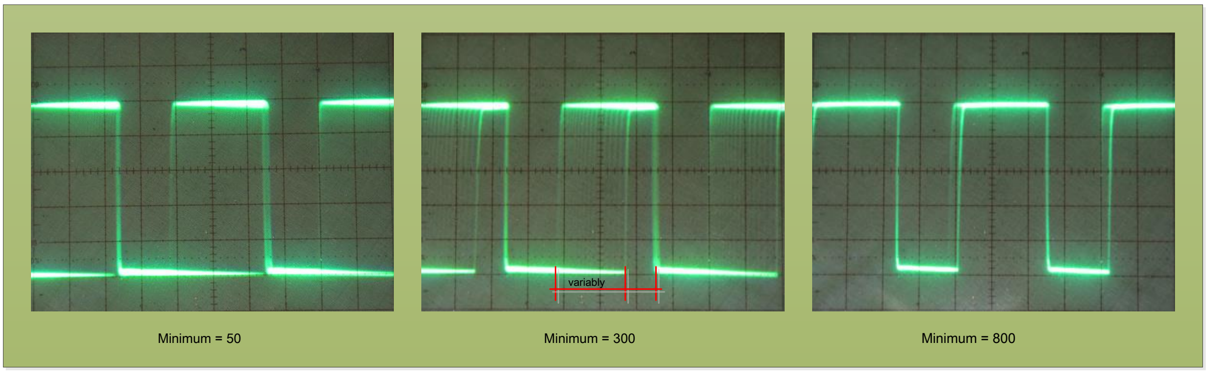


Figure 13: Digital PWM output signals for a two-tone signal with different PWM Control minimum settings

From Figure 13 one that values greater than zero, always a triggering of the PWM is carried out for minimum, the minimum operating voltage for the PA output stage must be greater than zero so recognizes. In the power PWM of the author by [3], the SSB envelope is filtered again through a low-pass according to block diagram in Figure fourteenth At the same time the maximum output amplitude is determined by the choice of + UDD, which indeed should be 100 volts in this project.

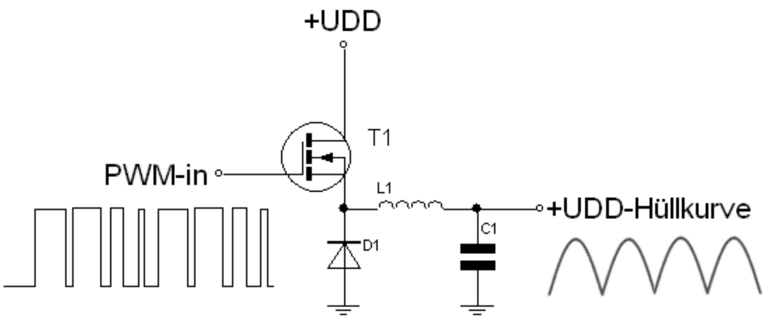


Figure 14: Block diagram of the power PWM according to the buck converter principle

The digital PWM output signal having a switching frequency of approximately 250 KHz from the Hermes transceiver also includes a factor of 8 to 10 broadened to approximately 25 to 30 KHz SSB envelope (see Marker 2 in Figure 15) in its spectrum. This can be demonstrated very well with a spectrum analyzer. Figure 15 shows the spectrum of the digital PWM, taken with a VNWA according DG8SAQ. The SSB spectrum ends just above 26.5 KHz (marker 2) at a 3 kHz SSB bandwidth. In addition, carriers (marker 7) and its harmonics are grouped around the 250 KHz more sidebands around with decreasing amplitude.

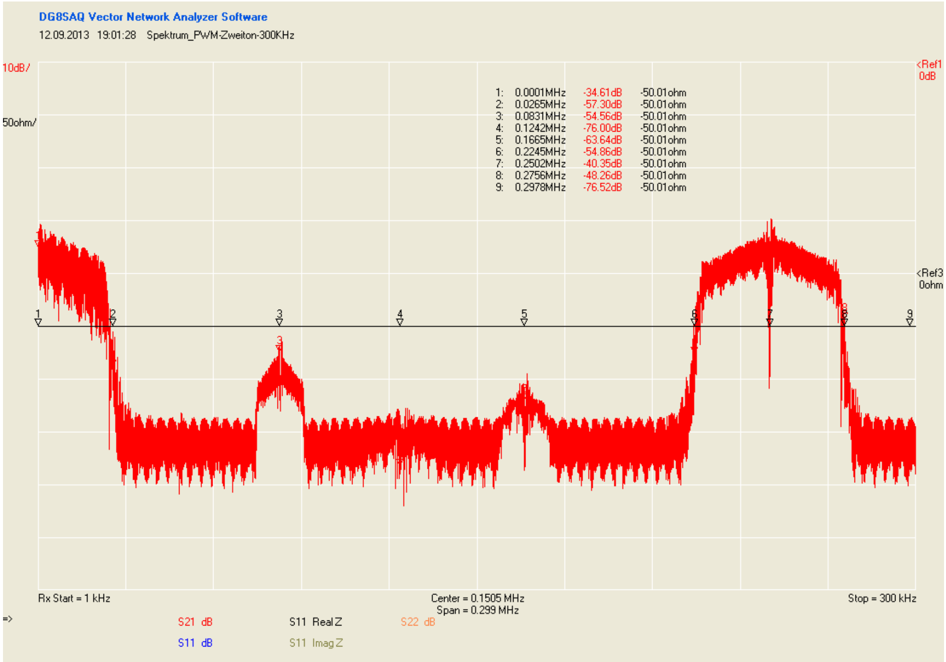


Figure 15: frequency spectrum of a digital dual-tone PWM

The cutoff frequency of the PWM low-pass filter should therefore be at least about 30 KHz to regain the original signal of the SSB envelope "undistorted". In addition, the harmonics must be adequately filtered out, which requires a higher order at the output of low pass PWMs. Further details on the dimensioning of the power PWMs can be taken from [3].

Envelope tracking power amplifier concept

There were developed schematics and PCB layout for a two-stage and one-stage PA.

Option 1 in two stages

- with 4xVRF3933 and 2x MRF 148A in the driver amplifier
- Total gain 38 dB, 160 milliwatt input power of 1000 watts output power

Option 2 stage

- with 4xVRF3933
- 22 dB gain, 6.3 watt input power of 1000 watts output power

For the one- and two-stage variants layout designs are provided in the download area of the radio amateur. In the download area are still the schematics in
,spl format.

driver amplifier

In order to achieve the goals set by linear frequency response and high IMA 3 to 6-meter band, the driver amplifier must be very good next to the power amplifier
have transmission characteristics. Bipolar transistors used by the author for years the type MRF 426 Motorola have since discontinued and only difficult to obtain. Chinese patterns have now been tested, but not nearly reached the properties of the original type. After a long search, much to the author, the MOSFET types VRF 148A by the company Microsemi and the MRF148A by the company MA-COM of VRF148A on. They are up to the gate voltage level almost identical. According to information in the data sheets, these two guys would at a driver output of about 6 watts, the targeted 50 dBc IMD3

Distance to the upper bands can do well. Another advantage over the bipolar transistor type MRF 426 is that they can be operated at 50 volts. Since the 100 Volt power amplifier power supply should be made of two series 48-volt switching power supplies, fall in the middle of the series, the 50 volts for the driver amplifier with the way from. A separate 24 volt power supply is no longer needed.

Circuit design driver stage

The driver stage is designed as a push-A amplifier with twice MRF148A. Figure 16 shows the circuit diagram of the driver amplifier.

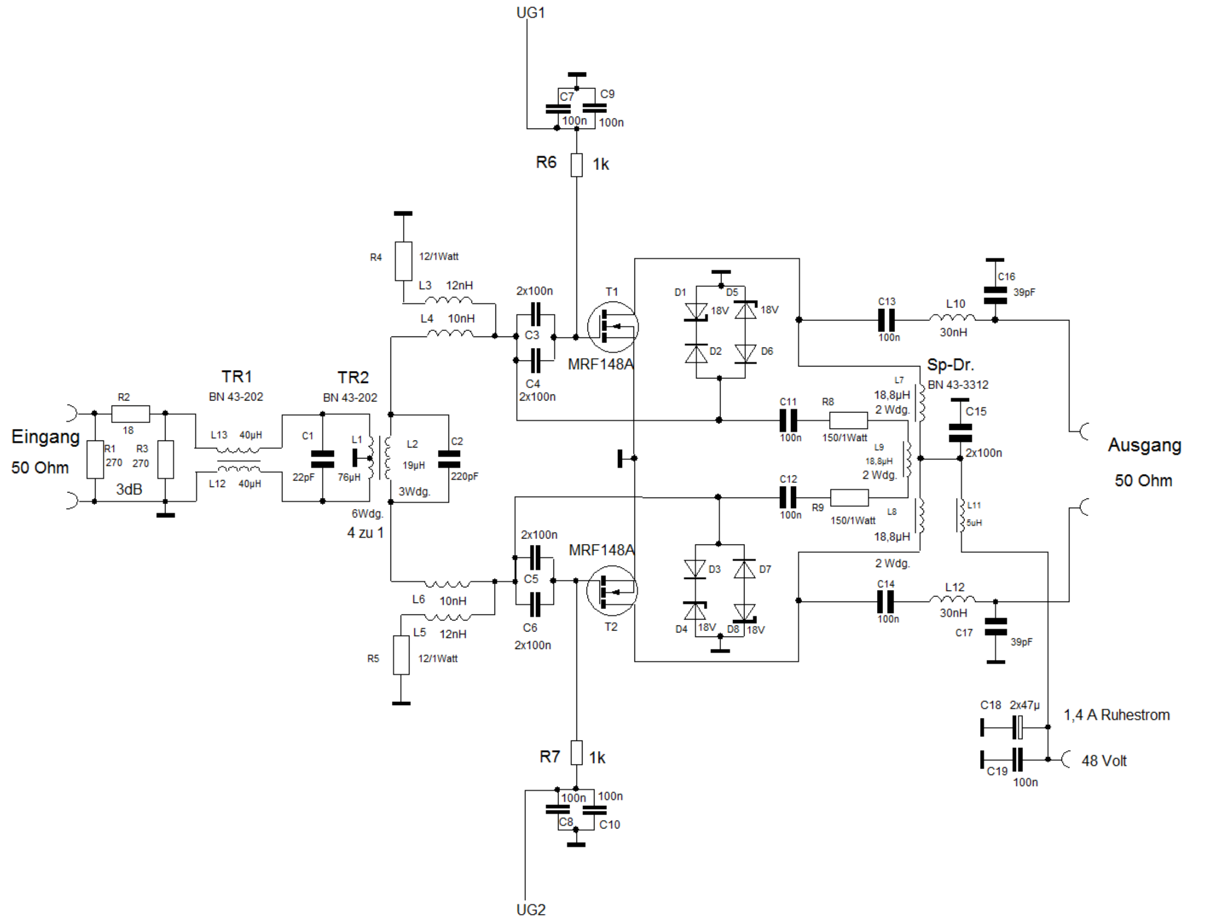


Figure 16: driver amplifier with 2x MRF148A in push-pull operation-A

The two series-connected input transformer can be realized by a 1 to 1 Guanella transformer and a 4 to 1 Faraday balun in each case to a double-hole core type BN43-202. TR1 converts the single-ended to a balanced input signal, and TR2 shall adapt the input resistance of the Mosfettreiberstufe to the value of 50 ohms before. At slightly lower demands on the symmetry of the circuit can be dispensed TR1. The capacitors C1 and C2 are used to compensate the leakage inductance. This is also absolutely necessary for operation up to 6-meter band. R1 to R5 and L3 to L6 form a further part of the input matching. They compensate for the input capacitance of the MOSFET. The two MRF 148A MOSFETs are operated at a quiescent current of about 700 milliamps and 50 volts. The supply of the operating voltage takes place via a common feed throttle in a twin-hole core type Amidon BN43-3312. An additional coil (L9) on the feed choke and the resistors R8 and R9 and capacitors C11 and C12, the negative feedback has been made. This reduces the gain of the driver to approximately 18.5 dB. The diodes D1 to D8 are used for voltage limitation at the gates. Another important advantage of the MRF148A and VRF148A is in its advanced withstand voltage at the gate of plus / minus 40 volts. This reduces the gain of the driver to approximately 18.5 dB. The diodes D1 to D8 are used for voltage limitation at the gates. Another important advantage of the MRF148A and VRF148A is in its advanced withstand voltage at the gate of plus / minus 40 volts. This reduces the gain of the driver to approximately 18.5 dB. The diodes D1 to D8 are used for voltage limitation at the gates. Another important advantage of the MRF148A and VRF148A is in its advanced withstand voltage at the gate of plus / minus 40 volts.

readings

Figure 17 shows the frequency response achieved (S21 red curve) and the input matching as VSWR (S11 green curve) of the driver stage. The VSWR varies from 160 up to 6 meters band between 1.0 and 1.4. The frequency response curve is up to 50 MHz excellent linear (S21 red curve). The gain variance is up to 50 MHz of less than 0.3 dB. This is partly due to the compensation measures at the entry and exit of the MOSFET. This is described in detail in his articles in [9 and 10] the author. If we add the 3 dB attenuator at the entrance, then the gain of the driver stage is ca.15,5 dB.

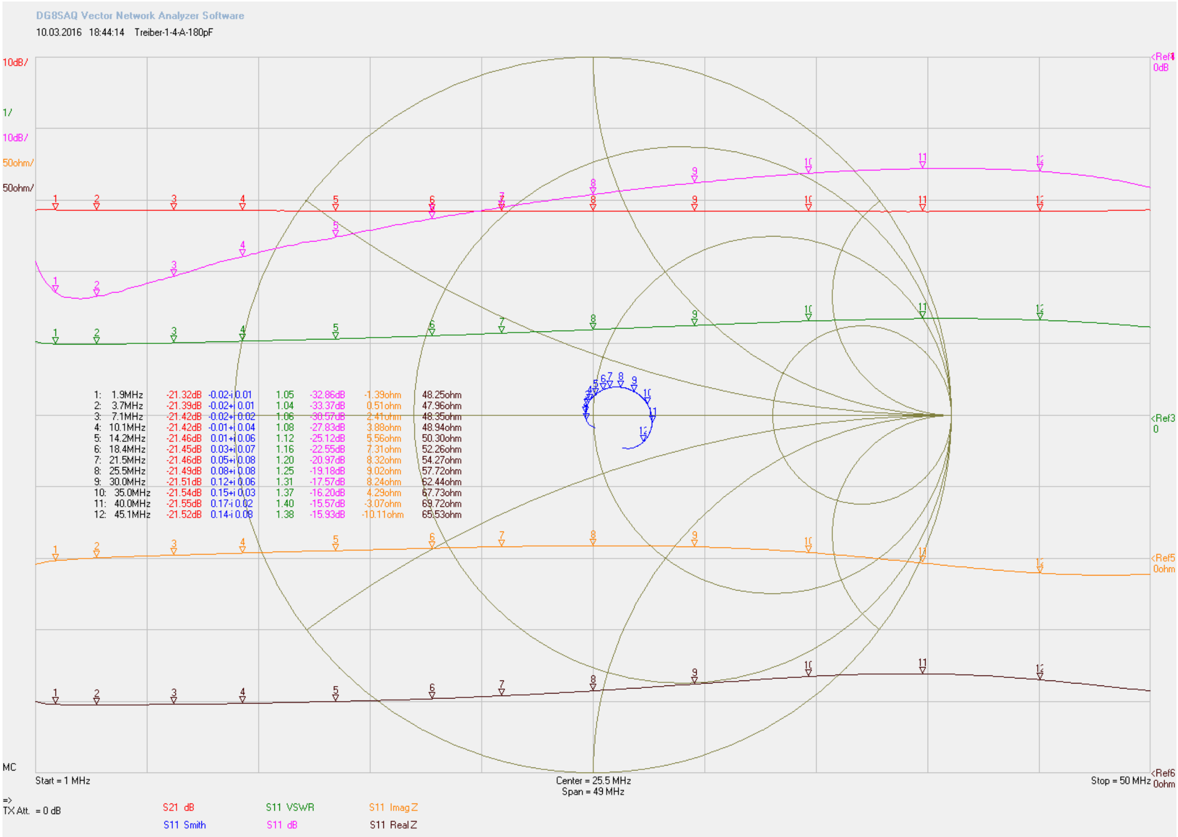


Figure 17: Frequency response and input VSWR of the driver stage, 18.5 dB gain without 3dB attenuator, otherwise 15.5 dB

With a quiescent current of 700 mA per Mosfet about 55 dBc IMD3 distance at 6 watts to achieve output power. Figure 18 shows the achieved IMD3 distance in the 80-meter band.

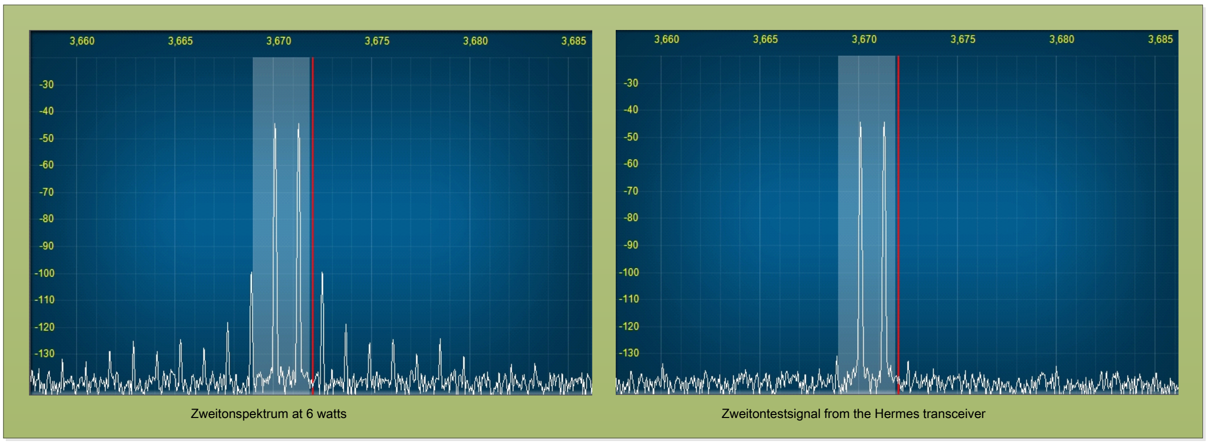


Figure 18: IMD3 spectrum of the driver amplifier and the test signal in the 80-meter band

It takes a very clean IMD3 free test signal for this measurement. This has started to win from his Hermes transceiver. By predistortion of IMD3 distance of the test signal was better than 85 dBc.

Gate voltage generation circuit and PTT

The Gatespannungsversorgungs- and PTT circuit has been compared to previous solutions the author very simplified. Figure 19 shows the circuit details.

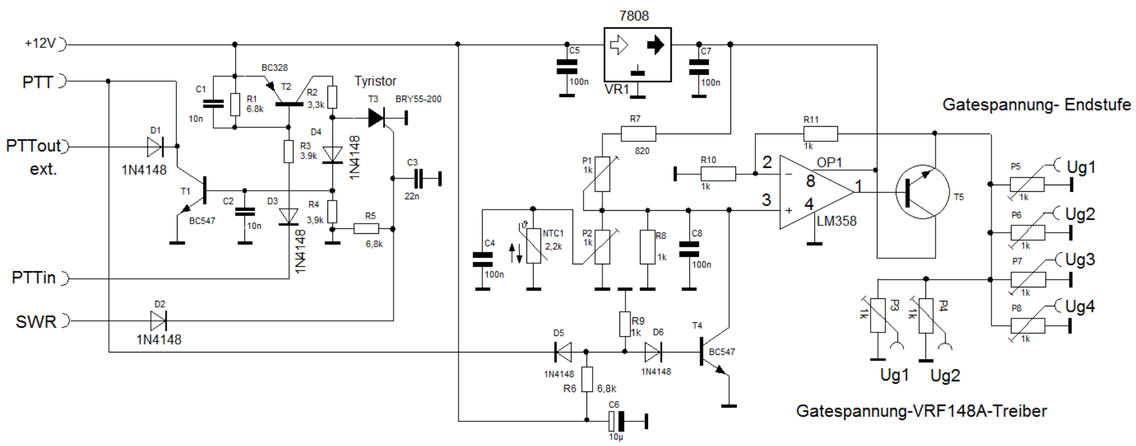


Figure 19: PTT circuit with gate voltage generation and control

T1, T2 and T4 take over the input diode D3 to turn on the quiescent current for both the Treibermosfets and for the Endstufenmosfets.

the desired bias currents for the driver amplifier through P3 and P4 can be set as soft as silk. The thermistor NTC1 of 2.2kOhm controls in cooperation with OP1 and T5, the gate voltage in dependence on the temperature. P1 and P2 can be Set the off steepness of the circuit according to his needs and cooling conditions very well, so that the quiescent currents of Treibermosfets and Endstufenmosfets be kept very constant over a wide range. P1 and P2 are to be rotated at the beginning of the adjustment in middle position. At the emitter of T5 then stand about 5 volts. It is with P2 then the exact value of 5.00 volts at about 20 ° C at the heat sink. P1 and P2 should be designed high quality and at least a 10-turn potentiometer. The 5 volt value will always be in this case represents the initial reference for further comparisons. As a failure protection a 5.1 volts zener diode can be placed in parallel to the six potentiometers. This can, under certain circumstances the failure of P2 or 8 volts voltage stabilizer, the final stage save them from destruction. P3 to P8, the four gate voltages required for the total Endstufenmosfets can be set separately. In the circuit 25-speed potentiometer were used to make this very fine. The MRF148A need about 2.1 to 2.2 volts and the VRF3933 the final stage for 500 mA approximately 3.5V gate voltage for 700 mA quiescent current. Be used in the driver VRF148A, then the necessary gate voltage increased to about 3.5 volts. So it is almost identical to the gate voltage of the Leistungsmosfets in the final stage. The VRF148A type would therefore be preferable to the MRF148A.

The thyristor T3 is used to quickly switch off the PA in the case of high SWR values. Voltages of + 1.6 to 2 volts at the input switch SWR the thyristor into a conductive state.

Circuit description of the final stage

In developing the Eingangsanpassnetzwerkes the Philips model [1], Figure 5 was taken as a basis. There is the task of compensating the input capacitances of the two parallel-connected MOSFETs of approximately 1600 pF. When Anpassnetzwerkschaltung is a TGlied with **Cin** as input capacitance of the parallel-connected MOSFETs.

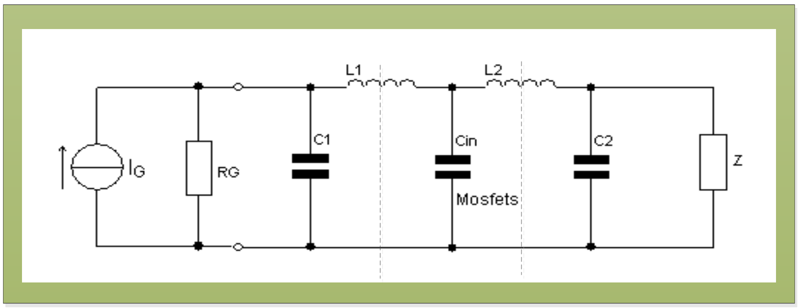


Figure 20: Eingangsanpassnetzwerk suitable according to [1], Fig. 5

The program RFSim99 for [8], the components of the T-gate can be determined very quickly. Figure 21 shows the calculated with the program RFSim99 values of the components up to 40 MHz. Since the frequency reduction of the simple T network is very shallow, even up to 50 MHz can be expected with reasonable gain. can be dispensed with the front inductor L1, since the 9 to 1 transformer having sufficient stray inductance. The inductor L2 is formed by a half turn aus1,5 mm enamelled copper wire having a diameter of 7 mm and the conductor tracks.

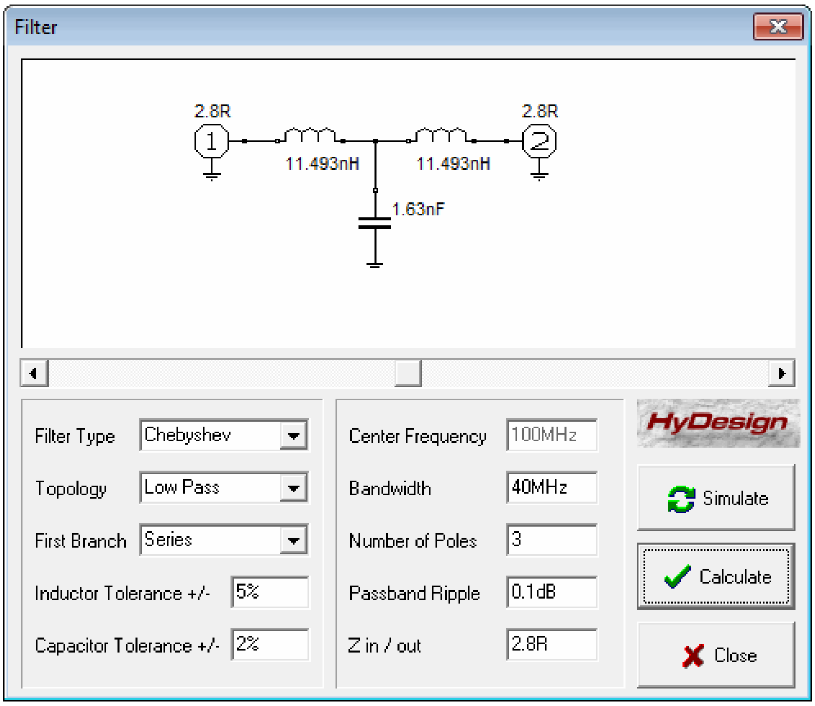


Figure 21: Calculated Eingangsanpassnetzwerk for Mosfetendstufe

The total input resistance of Mosfetendstufe is because of the input-side series connection of R1-3 to R4-6 and R7 and R8 approximately 5.6 ohms. In the circuit for the output stage (see Figure 24), the two T-elements with the six resistors R1 to R6 to be completed. This must be able to accommodate a total of 6.3 watts. Therefore, any resistance is a two-watt type. With the 9: 1 transformer Tr1 then reaches an input Z value of the power amplifier of 50 ohms. Tr1 must be very carefully carried out on the secondary side at a load of 5.6 ohms and compensated. To produce the transformers you take approx 10 cm silver-plated screening made a doppeltgeschirmten piece of RG400 coax cable and pulls three insulated wire strands into this shielding braid. It is sufficient to take the inner sheath of the braided shield.

3312. The three wires are connected in series and form the primary side of the transformer. The braided shield constitutes the winding for the secondary side. The compensation of the stray inductances succeeds quite effectively as Figure 22 shows to 50 MHz.

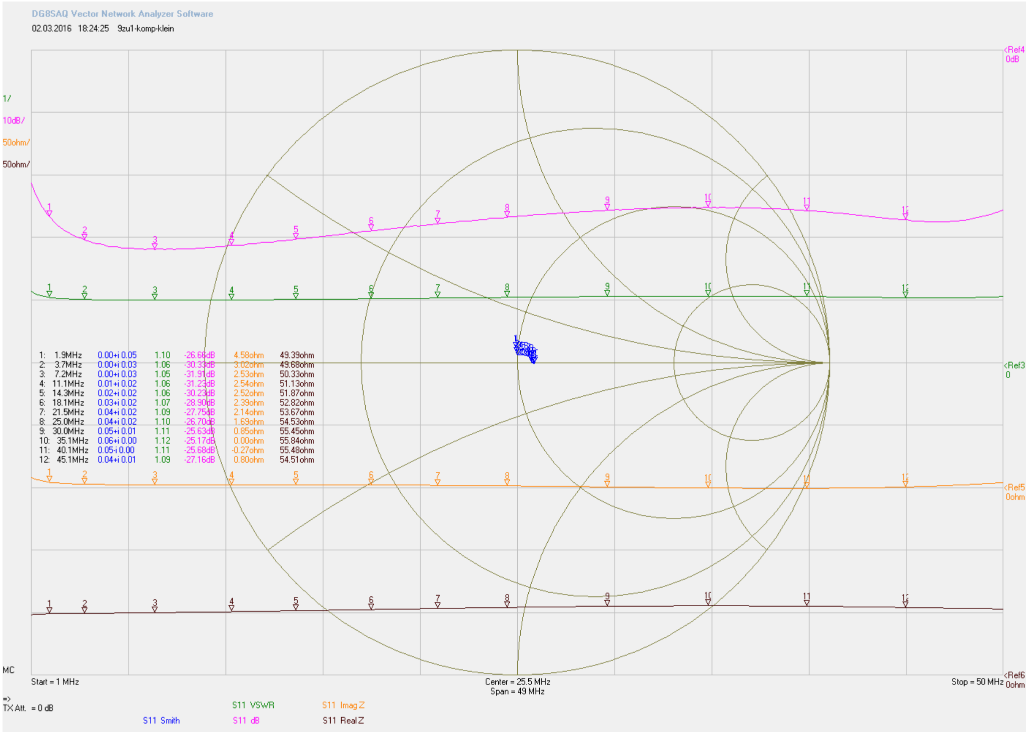


Figure 22: 9 to compensated 1Trafo (27pF primary and secondary 5.6 ohm resistor in parallel with 330 pF)

Short connecting wires and a good coupling factor to the primary winding conditions are absolutely necessary. An additional capacitor of 27pF on the primary side of the transformer Tr1 is how the measurements showed itself not necessarily needed in the two-stage PA variant. Secondary results in connection with the driver amplifier, a value from 420 to 470 pF optimal adjustment values. The pre-driver decouples the output stage of the entrance. However, anyone who wishes to operate in the single-stage variant, the PA should definitely the 27 pF on the primary side and 330 pF to 470 pF provide (Syndicate trimmer) on the secondary side of the transformer Tr1 of the amplifier. The optimal capacitance value depends on the quality of the prepared 9 to 1 transformers.

Determining the output impedance values of the output stage for P $_{OUTMAX}$ = 1KW

For a given operating voltage of 100 V the maximum output power should be about 1KW. The remaining residual stresses should not be less than in the state of the transistors controlled by the knee voltage threshold of approximately 10 volts. This then requires (due to the feed throttle 180 volts) at a stroke of 90 volts a load resistor RL of 12.5 ohms. A 1: 4 transformer at the output is required at 100 volts operating voltage. Each push-pull side then provides 6.25 Ohm (due to the voltage doubling at the feed choke has the conductive transistor side muster more power).

Since up to 6 meters band emphasis was placed on an operation, the output capacities of the two parallel-connected MOSFETs of about 600 pF had to be compensated. A suggestion, it was found in [2], Fig.3-21. The selected half load resistance of 6.25 ohms determines the impedance of the Ausgangsanpassnetzwerkes. The program RFSim99 the matching was determined. Figure 23 shows the values found.

The input capacitance of the Pi-Ausgangsanpassnetzwerkes is formed by the Drainausgangskapaziäten the Mosfets (2x300pF). The Ausgangskapaziät is realized by parallel connection of 3 x 180 pF and mica capacitors having a voltage of 500 volts. The 25 nH inductance of the Pi-member is wound on a 13.5 mm round body. It consists of 2 mm copper magnet wire.

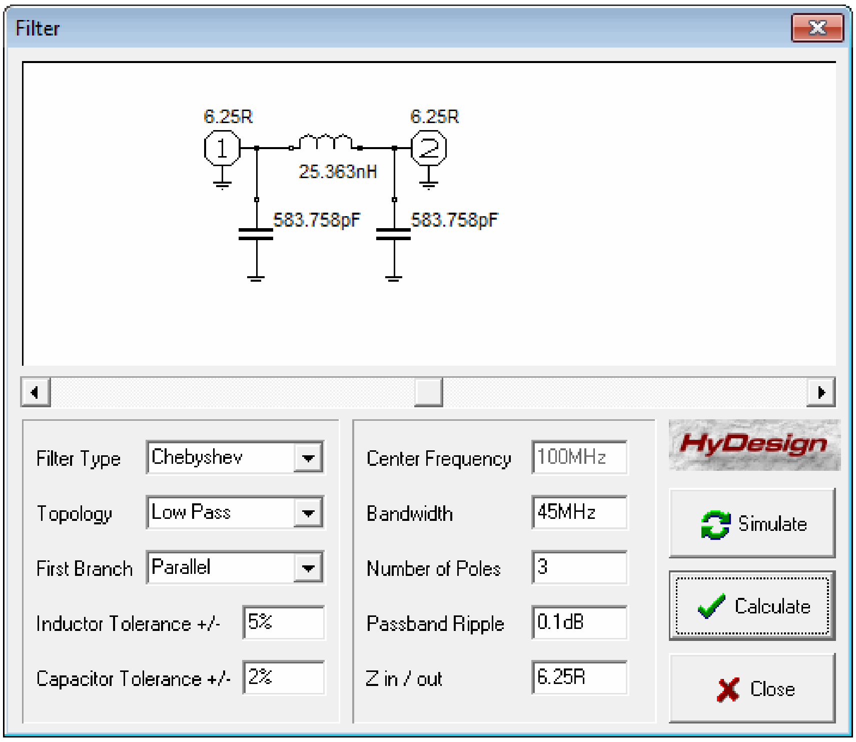


Figure 23: compensation network for the drain capacity up to 45 MHz.

Based on the foregoing considerations, the output stage versions were developed. The following Figure 24 shows the circuit diagram of the output stage. About L7 and R13, R14 and C20 / 21, the output stage is fed back. L7 is formed of one turn on the feed throttle. The feeder reactance coil itself, consists of 2 x 2 windings which are arranged in bifilar fashion. so that is 1/4 of the output voltage available for the negative feedback. This reduction reduces the power dissipation in the resistors R13 and R14. This voltage is again R4 to R6 reduced by the resistance ratios R13 / R1 to R3, and R14 /. The negative feedback is approximately 3 dB in the lower bands, and about 2 dB on the upper belts. This is partly also because the high input capacitances of the MOSFET cancel the negative feedback effect to some extent. The diodes D1 to D8 serve to protect the gates of Leistungsmosfets. Voltages higher than +/-

18.6 volts are cut off. This measure the gates protect against high input voltages. The Mosfettyp VRF3933 used is safe to operate up to voltage values of +/- 40 volts.

The connectors X1 to X4 allow the two different modes of operation mentioned above. X1 and X3 closed, the amplifier can be operated with modulated operating voltage (ET). X2 and X4 are closed, you can work with a fixed operating voltage. The ET mode offers the significant advantage that no cooling fan are no longer required.

The output transformer is constituted by the series connection of a 1 to 4 Faraday transformer with a 1: 1 current transformer (after Guanella). The advantage of this solution is that no selection of capacity are required and the inductance of the supply throttle can be somewhat lower. Moreover, the 1: 1 are prepared Guanella transformer means 50 Ohm coaxial cable, which is easily procured. Somewhat disadvantageous in this solution is the opposite of 1 to 4 Guanella transformer solution lower broadband the Faraday transformers affects. This can be minimized but the fact that it moves into a shielding braid two wire strands and these connected in series, and thus achieves a good magnetic coupling. These two strands then form the secondary winding of the Faraday transformers. The primary winding is then composed of the braided shield. In this way, the best magnetic coupling between two windings is achieved.

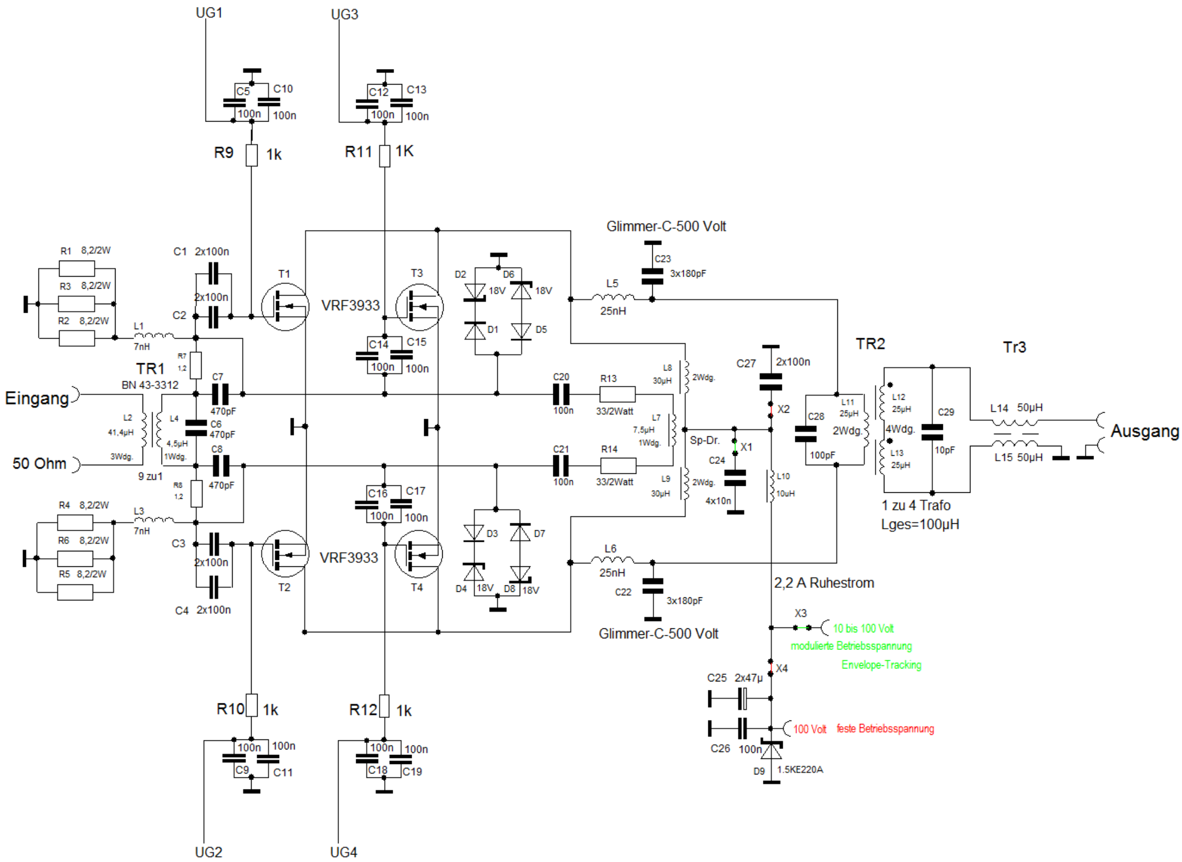


Figure 24: output stage with 1 to 4 and 1 to Faraday 1Guanella transformer

As core materials, ferrite sleeves Company AMIDON FB43-1020 own. In the figure, 25 which reached the frequency response of the power amplifier and the driver as the overall arrangement can be seen. In the measurement, a 40 dB attenuator was used to protect the VNWA input. The overall gain of the two-stage PA is located at 470 pF for C7 and C8 to 30 MHz between about 38 and 39dB. At 50 MHz, the gain is about 30 dB. The input VSWR is located in the entire frequency range from 1.9 MHz to 30 MHz between 1.0 and 1.3 and in the 6-meter band at 1.08.

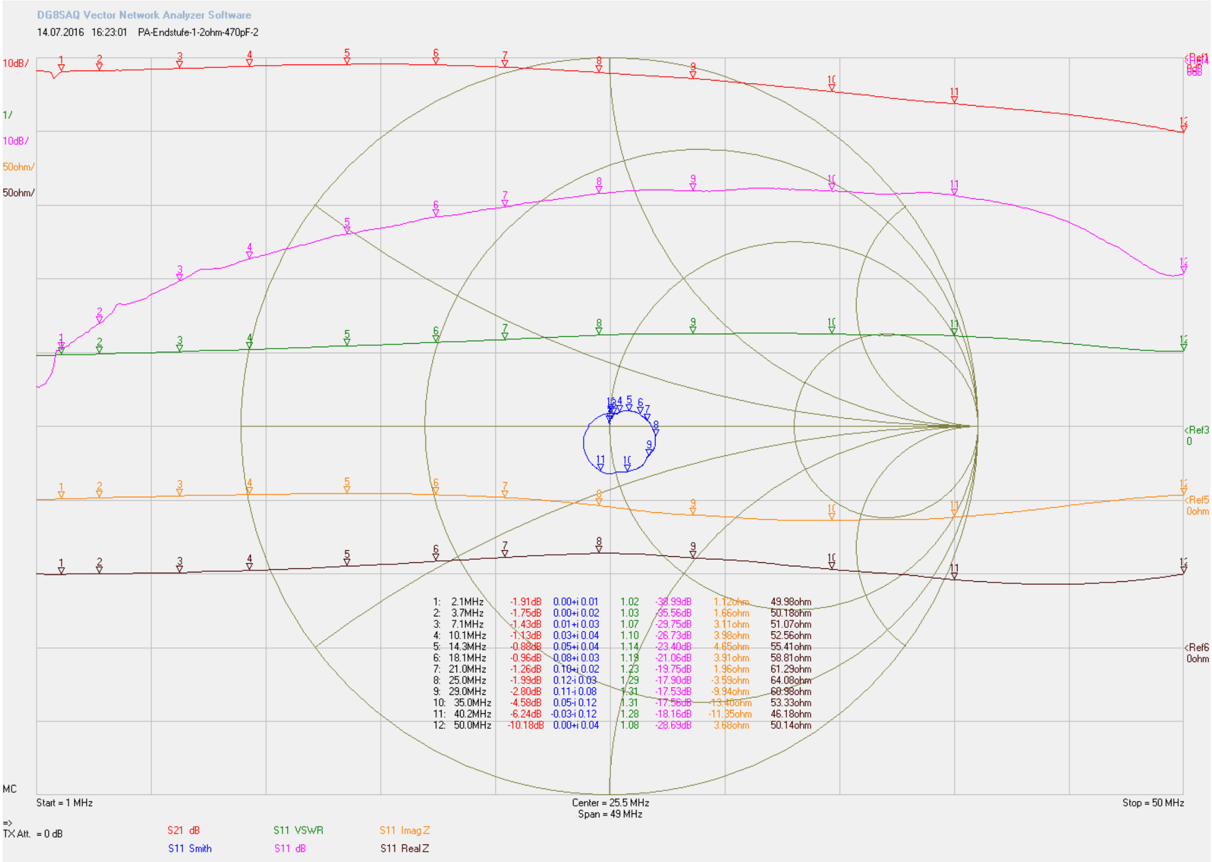


Figure 25: frequency response and input matching of the entire power amplifier having 1 to 4 Faraday transformer and 470pF for C7 and C8

Increased to C7 and C8 to, for example 4.7 nF then the frequency response up to 50 MHz is clearly linearized. The gain in 6-meter band then increases by about 7 dB to 37 dB. On the lower bands it is about 39 to 40dB. The power amplifier is then good shield because it (bad decoupling in the PTT circuit, for example) can also lead to tendency to oscillate under unfavorable circumstances. Figure 26 shows the linearized frequency response.

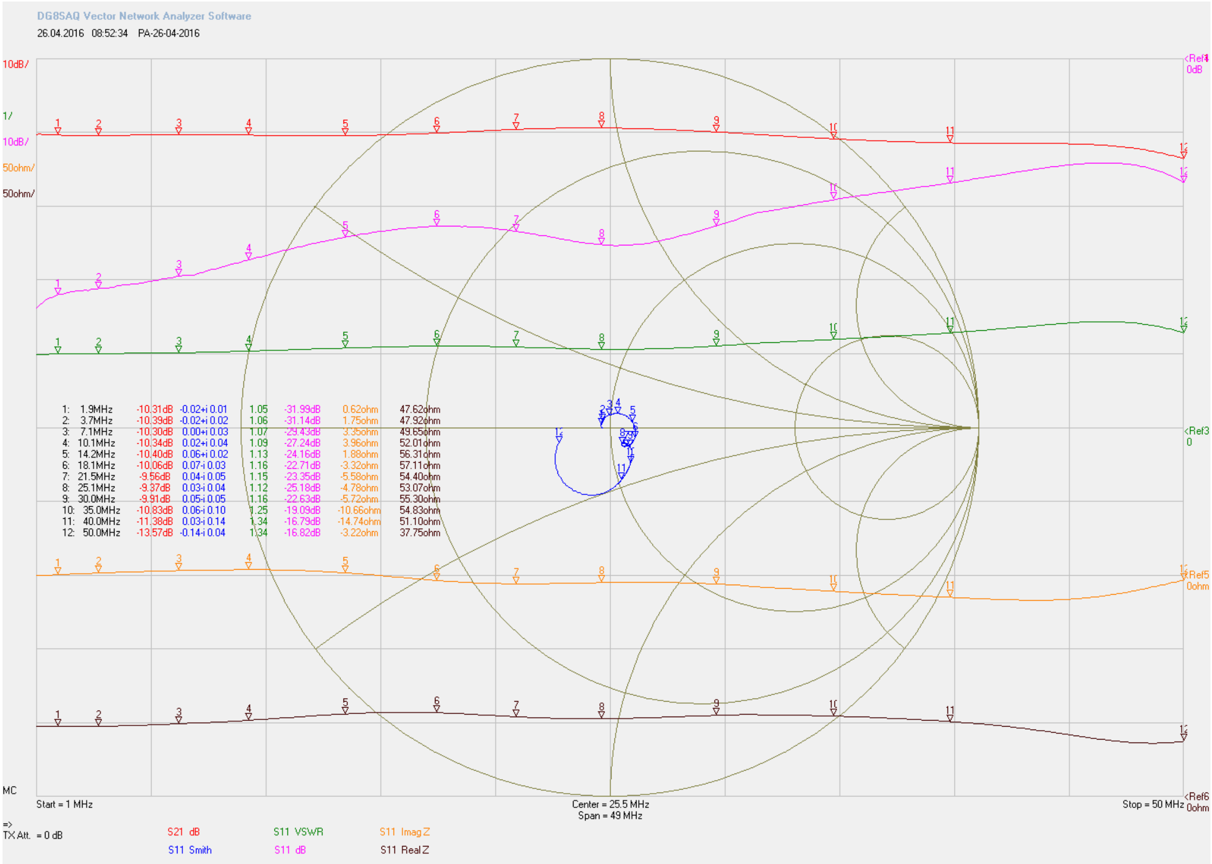


Figure 26: linearized frequency response at 4.7 nF for C7 and C8

layout development

The following figures show the layout and PCB layout of the individual variants. There are mainly SMD components of the 1206 series in the low voltage section. These are still easy to handle for the replica. Anyone who has an illuminated ring magnifier available and a variable in temperature soldering station should have no problems building. The following figures show the layout of the two-stage and single-stage PA variant.

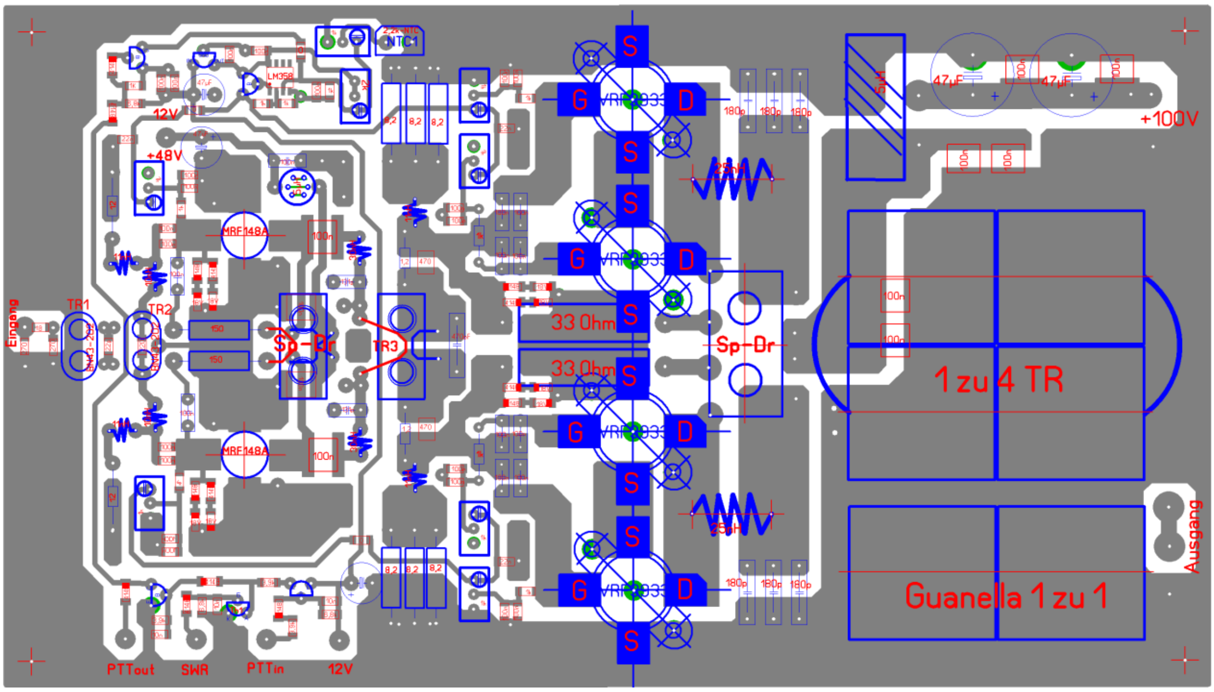


Figure 27: Layout and assembly diagram of the two-stage PA.

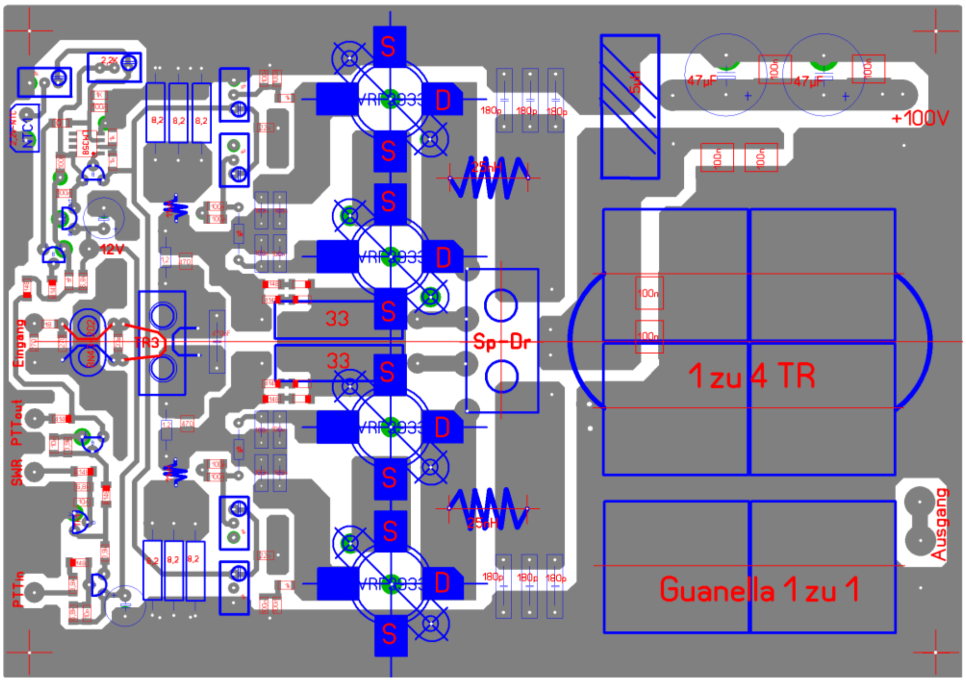


Figure 28: Layout and assembly diagram of the single-stage PA

Who already has a driver-PA for about 10 watts, can use the layout of the stage PA variant. This variant has about 22 dB of gain. The advantage of the single-stage variant is that they can very easily "combination partners" to 2 KW output stage. The author himself has not tested this myself.

PCB manufacturing and assembly

The layouts of the various PA variants can be downloaded from the download area of the radio amateur. They were created with the program Sprint layout of the company ABACOM. The back of the board (to the heat sink showing) forms a ground plane substantially. The author can be prepared two sample boards for the two-stage variant in a small factory. They are drilled but not contacted. Furthermore, one has the recesses for the

Leistungsmosfets establish itself. but this is not very complicated. The figure 29 shows the thus prepared prototype board.

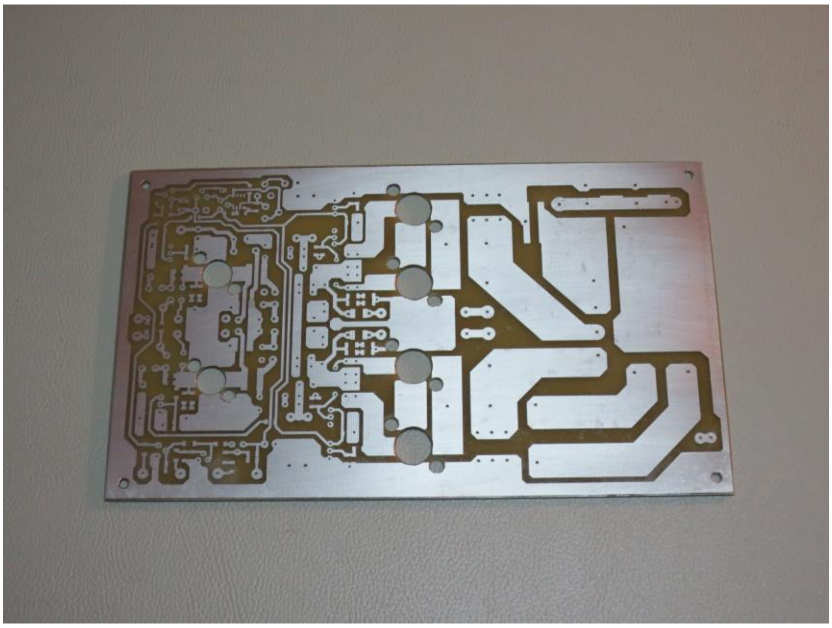


Figure 29: PA board for the two-stage variant

It has been optimized for all measurements. In the download section of the ham radio operator on this article are the corresponding revised Sprint-Layout-Files.

The assembly begins with the realization of the vias for ground connections. For this purpose, a 1 mm wire having already tin-plated surface, which is soldered on both sides is suitable. If all vias introduced, it is expedient way with the soldering of the two driver transistors MRF148A starts. After that, the rest of SMD components follow in any order.

After the assembly of SMD components, all other components are mounted. If all components are fitted in the front part of the board, the transformers, inductors, mica capacitors and inductors of the Mosfetendstufe can be fitted. The Figure 30 shows the completely assembled and put into operation amplifier.

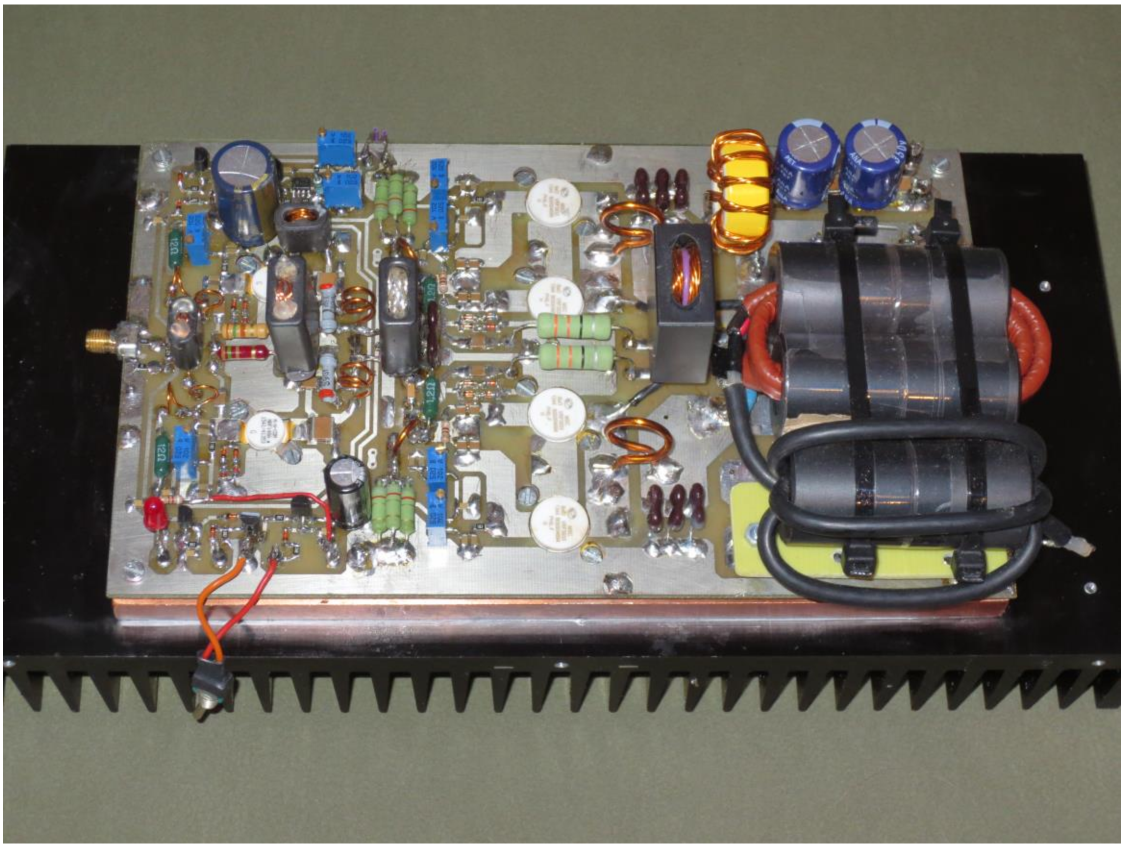


Figure 30: ET-power amplifier having 1 to 4 Faraday transformer and 1 to1 Guanella transformer

The four Leistungsmosfets the final stage are fitted at the end. In the run you have to have provided the necessary heat dissipation for the heatsink and the copper plate ready. For this, a series of holes and threads to print. The author himself cuts the thread for the screw connections of the transistors and MOSFETs and for the circuit board is always in the copper plate located under the aluminum heatsink. If you have enough experience, can cut the threads in the 10 mm thick copper cooling plate. But this can lead very quickly to cancel the tap, and then the not quite cheap copper cooling plate is no longer usable in general. Overall, a precise work is required at this point so that all screw can be tightened slightly.

Before screwing the copper plate to the aluminum heat sink it is polished on both sides. The side of the copper plate that is pointing to the aluminum heat sink, coated evenly with high-quality cooling paste. After the final screwing the copper plate with the heat sink out the swelling thermal paste is repeatedly removed (it swells by the contact pressure is always some paste out).

IMD 3 measurements in the 80-meter band without predistortion at 750 watts out

The presented PA with the four piece VRF3933 at the final stage reaches approximately 35-36 dBc (41 to 42 dB PEP) at an output power of 750 watts PEP in the 80-meter band. The locally performed measurements were also tape by OM Hermann, DJ5RV verified (see also Figure
32). So that it lines up with regard to the currently achievable with vmos PAs IMD3 values seamlessly. Better values would then only be reached with overcapacity (combi partners from two or more modules).

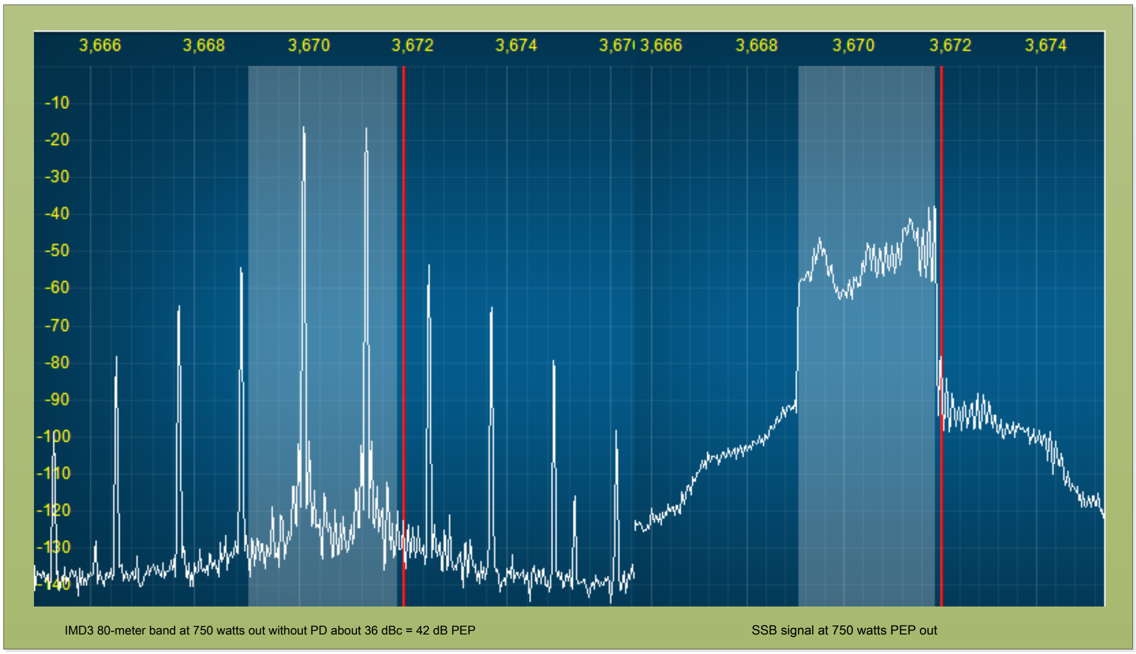


Figure 31: IMD3 behavior and SSB signal on 80 meters about 36 dBc at 750 Watts out (without predistortion)

Figure 32: IMD3 on tape at 250 km recorded without PD OM Hermann, DJ5RV

IN IMD 3 measurements in the 80-meter band with predistortion at 750 watts out

Figure 33 shows the IMD3 values and the SSB signal is activated predistortion. This gives again a IMD3 distance gain of about 25 dBc and ultimately achieved so IMD3 values above 60 dBc. These values can then be nothing to be desired for higher IMD3 distance more.

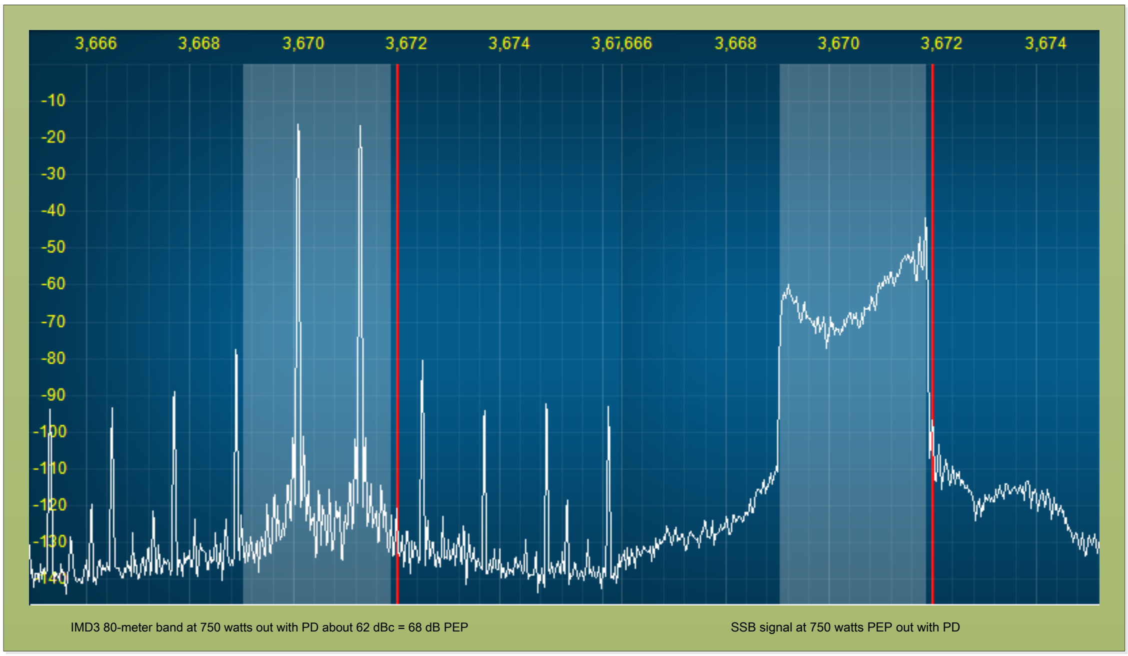


Figure 33: IMD3 behavior and SSB signal with activated predistortion to 80 meters out about 62 dBc at 750 watts out

The shown IMD3 properties have been added when using a fixed operating voltage. In modulated operating voltage in the ET process about 52 dBc be achieved with "predistortion", which also can be considered a very good IMD3 distance.
The built in Power SDR software function "Linearity" can selectively activate and deactivate. The software function "AmpView" allows a view of the correction values for phase and amplitude. Figure 34 shows this at about 750 watts of power.

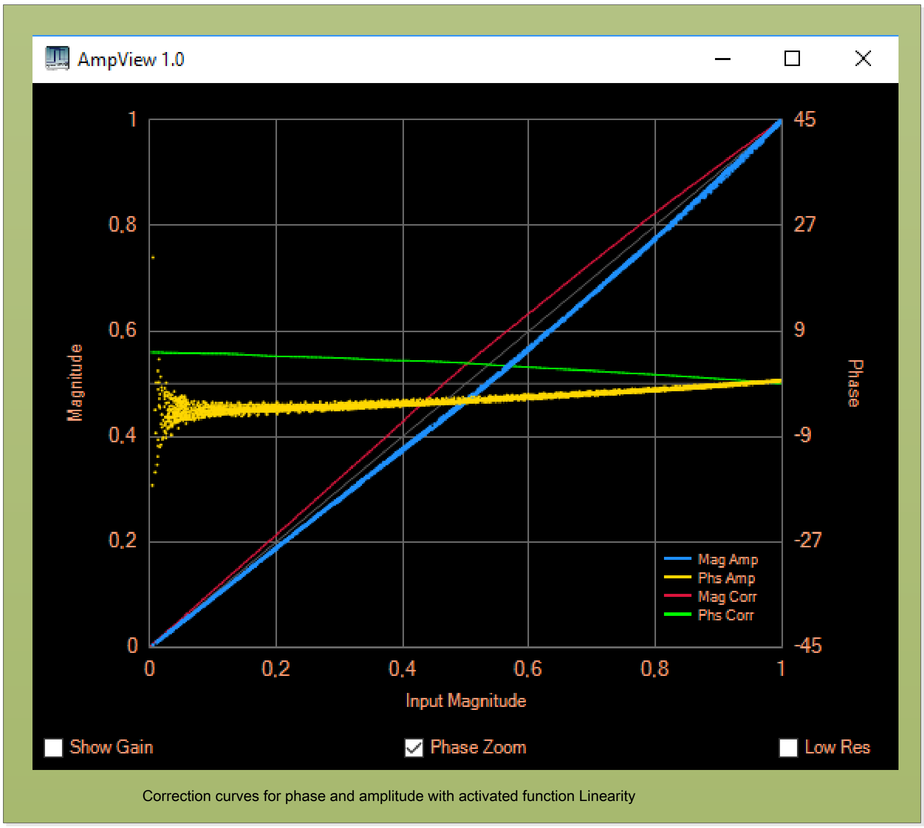


Figure 34: correction characteristics for phase and amplitude of the RF signal SSB with activated function Linearity

Both phase and amplitude values must be corrected in the positive direction by the predistortion software. This is not surprising on, because as the modulation of the influence of Mosfetkapazitäten not linear increases. However, the inserted compensation networks reduce the necessary correction amount. Otherwise you would not be able to achieve a IMD3Abstandsgewinn of 25 dBc.

output filters

The results in the spectra measurements have led the author to a Diplexfilter by OM
to refrain W. Sabin and instead use a five-pole double-T output filter. This can be extended to a diplex filter, if necessary by means of an additional high-pass filter. The Figure 35 shows the output filter for the 80-meter band. Its attenuation characteristic above the cutoff frequency of 4 MHz is sufficiently steep. Characterized in that the T-element begins with an inductance as an input element, an excessively large output current at the third harmonic is avoided.

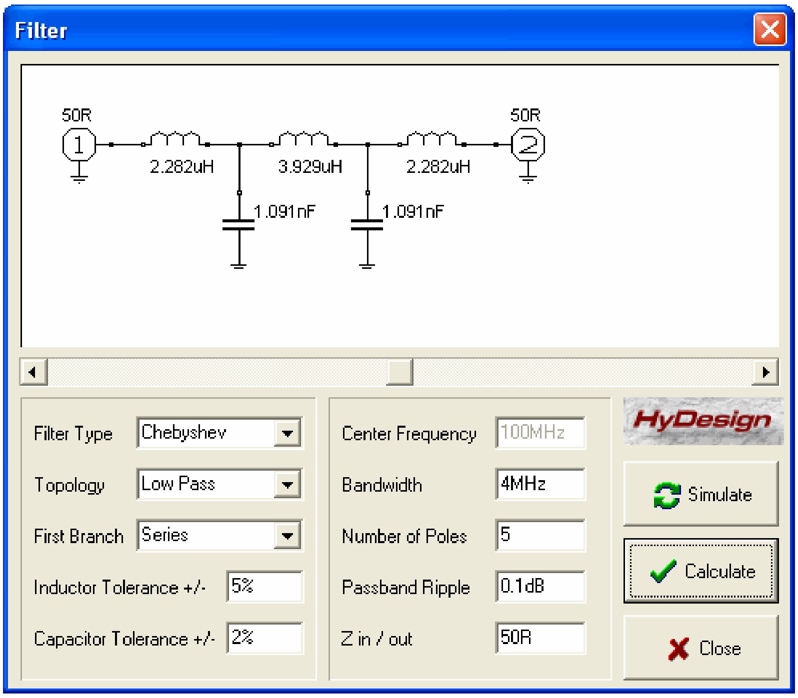


Figure 35: 5-pole low-pass output filter in double-T shape for the 80-meter band

The input inductance of about 2.3 .mu.H has an impedance of about 156 ohms at 08.10 MHz. The input capacitor of 1.1 nF has an impedance of about 13.4 ohms. In order for the present in the third harmonic energy can be "tamed" through both dummy elements flow out to ground without jeopardizing the MOSFET transistors. The resonant frequency of the two input reactive elements that form a series resonant circuit is approximately 3.18 MHz, which is well on the third harmonic of 10.8 MHz. The excess voltages at the drains of Endstufenmosfets by the reflections of the third harmonic can be tolerated. Those who want to improve this, can switch a high-pass part of OM Sabin according to [7] at the entrance of the low pass it. Figure 36 shows the finished output filter board.

Figure 36: Finished output filter board on the basis of Amidon T130 seeds for the bands 160-40 meters

The Figure 37 shows the revised layout of the output filter board in the dimensions 180x170 mm for four filter blocks and is easily extendable to other filter blocks. The component side is designed as a continuous ground plane.

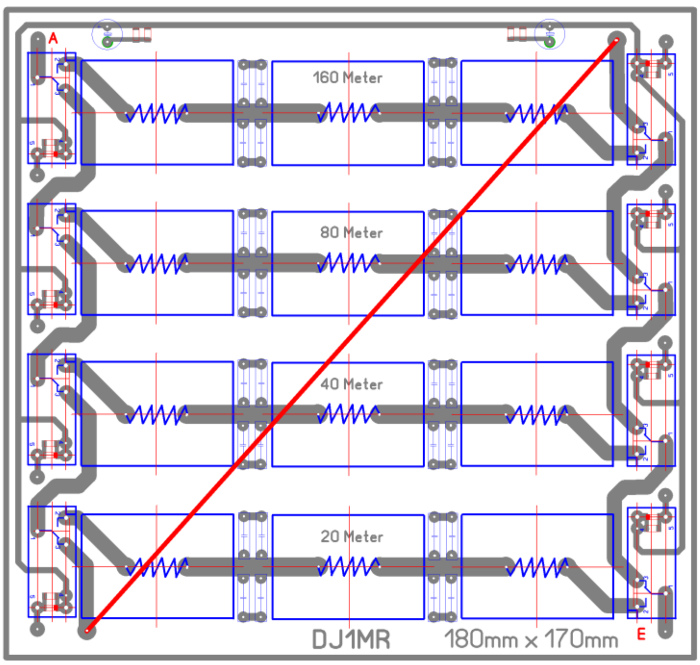


Figure 37: circuit board layout for the output low-pass filters

Block diagram and the sequence diagram of the transceiver and PA-assembly

The Figure 38 shows the time courses of the transceiver and PA arrangement. It has been considered important that the PTT circuit, the PA is (PTTin / BIAS-PA) only after the switching of the relay RE1 to RE3. The PTT circuit must have a high crosstalk attenuation due to the high gain of the PA of about 37 to 40 dB. Therefore, the relay RE1 to RE3 have been introduced and additionally accommodated on separate boards. When switching off the PTT signal for the PA is deactivated first. This prevents undue stress peaks at the various points of the circuit.

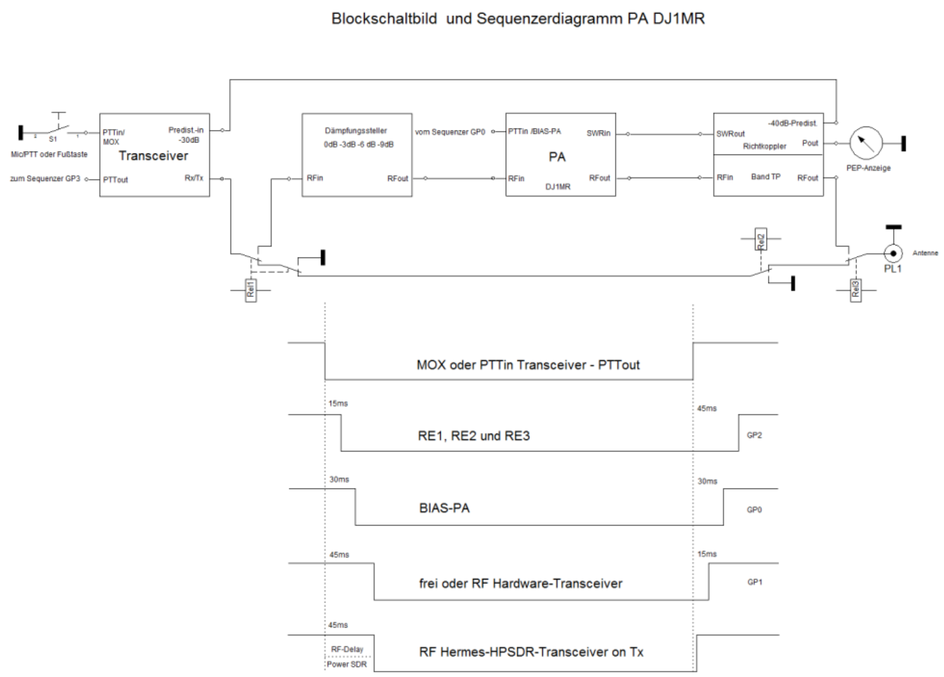


Figure 38: Block diagram and the sequence diagram of the transceiver and PA-assembly

Sequencer PA

Since even the PA amplifier by the power SDR software is controlled, one based on software solution was provided for the sequencer. It is based on the one developed by Bernhard Hochstätter, DL6NBS solution with a PIC 12F683 type. Bernhard has approved a kindly re-use and publication of this article. Here goes a special thanks to the author Bernhard. The temporal switching sequence has been adapted to the present project and behaves as described below:

- One Direction
  - RE1 to RE3 one
  - BIAS amplifier a (PA)
  - Transceiver or a RF of a HERMES (TX)
- Direction from
  - Transceiver from RF or alternatively by HERMES from (TX) (optional)
  - BIAS final stage of (PA)
  - RE1 to RE3 from (reception)

The sequencer to DL6NBS has the following properties:

- The delay can also be programmed freely (default = 50 ms)
- The CW-holding time can be set with the potentiometer in a wide range stepless.
- The outputs are galvanically isolated with fast-acting miniature relay

- is located on the circuit board layout in addition, a three-stage attenuator (attenuator, 3x3 dB steps) and three SMA connectors on the back of the board for the HF inputs and outputs.

- The dimension of the board is 50 mm x 110 mm.

Programming the delay:

If the inputs PTT and CW when turning on the sequencer simultaneously operated and maintained, the sequencer initially remain in setup mode. Now, the delay time between 10 ms and 250 ms can be set with the potentiometer P1. The control can be carried out with the help of LEDs at the individual outputs. the PTT and / or CW_Eingänge are now released again (high potential), the processor assumes the value set in its EEPROM and the sequencer immediately switches to normal operating mode.

The HEX file for the PIC can be loaded with permission from OM DL6NBS from the download directory of the ham radio operator for this post down. There are two versions to choose from. The difference is only in the negation of the output GP2. The circuit of OM DL6NBS was slightly modified at the outputs. Switching elements make quick miniature relay type OMRON G6K-2F as used herein variant. In the original Bernhard uses for galvanic isolation optocouplers. The Figure 39 shows the circuit diagram of the sequencer and Figure 40, the circuit board layout. In Figure 41 the construction of the finished assembled board is seen.

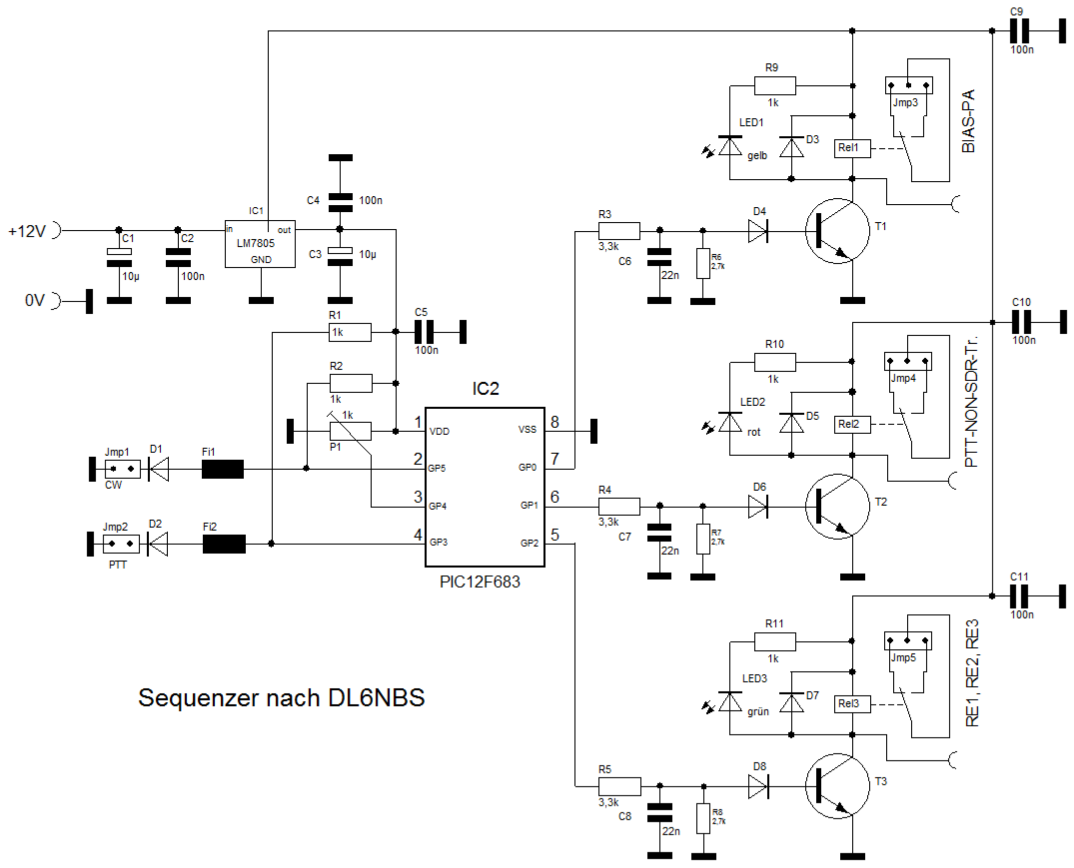


Figure 39: PTT sequencer

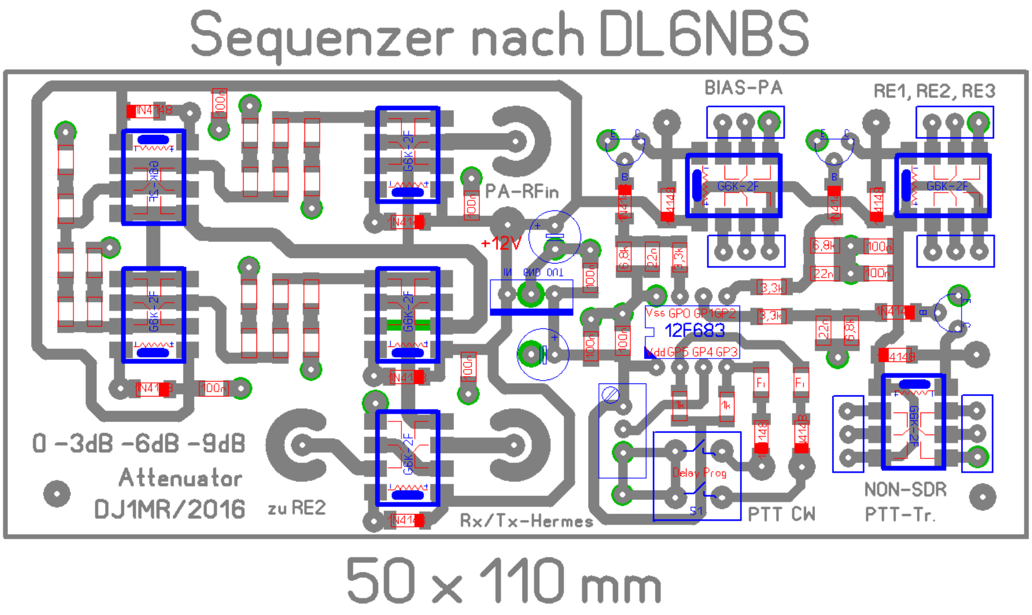


Figure 40: PCB layout for the sequencer and for the attenuator of the power stage

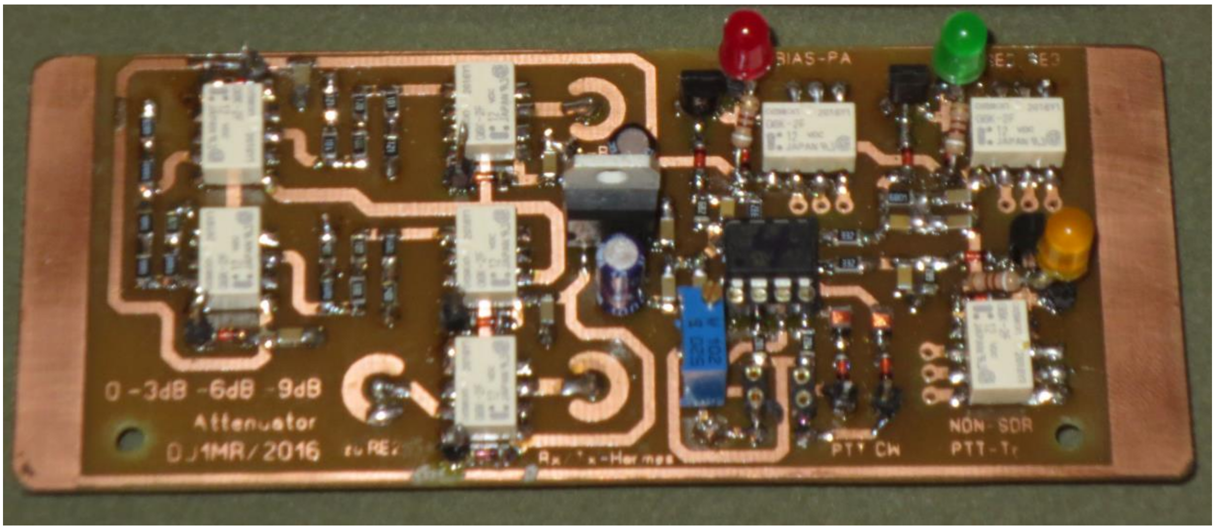


Figure 41: stocked sequencer and attenuator board

directional coupling

The directional coupling was carried out according to the in [6] of Josef Hisch, DJ7AW, presented solution. It is here a "Eintrafo" solution used, which has about 23 dB directivity. This value is sufficient for a cross pointer instrument. A second transformer to the coaxial cable of the directional coupler with 30 turns and an additional 10 dB attenuator filters to the total of 40 dB attenuated output signal for the predistortion functionality of the power SDR software. This signal is attenuated in Hermes transceiver further 30 dB. The means of Shottky diodes 43 of the type Bat rectified RF signals of both directions of flow are a fourfold OPV supplied from the type LM324, which is also the "Sample and Hold" driving members for a real PEP and SWR display. On the board, the two relays RE2 and RE3 (PA output relay and antenna relays) were accommodated. The RF input and output is (2 to 3 pF) compensated to 50 MHz respectively with a small capacitor. Figure 42 shows the circuit board layout in the dimensions 50 x 110 mm, and Figure 43, the completely assembled board. The SMD components are located on the bottom of the board.

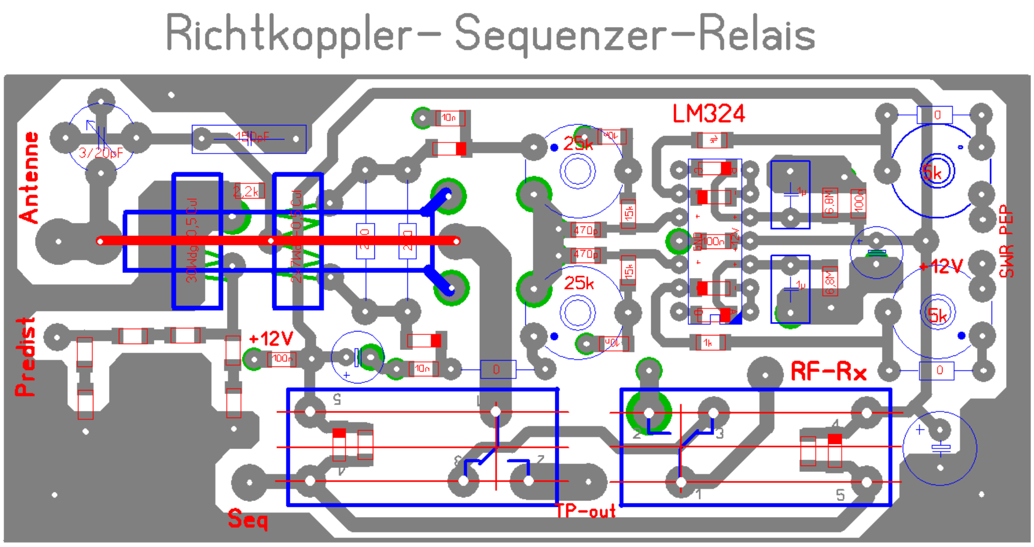


Figure 42: circuit board layout of the directional coupler and the PEP / SWR circuit

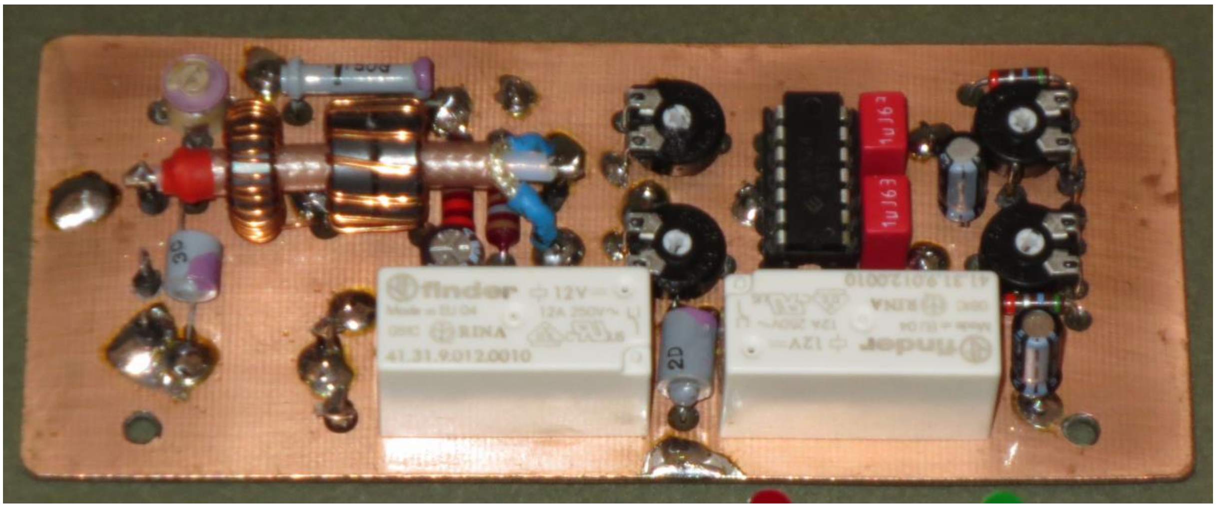


Figure 43: directional coupler, and PEP / SWR circuit according DJ7AW [x]

conclusion

The presented PA systems require the interested Nachbauer-depth knowledge of the functioning of RF circuits and their examination by means of suitable measurement technology. Many years of experience with RF circuits are necessary. It is not a beginner project.

Special thanks goes to the author of the OM Phil Harman, VK6APH, Warren C. Pratt, NR0V, Josef Hisch, DJ7AW and Bernhard Hochstätter, DL6NBS who have significantly contributed to the success of this Article.

references

[1] Philips Semiconductors A wideband linear power amplifier (1.6 - 28 MHz) 300 W for PEP with 2 MOS transistors BLF177Application Note NC08703

[2] Philips Semiconductors, RF Transmitting transistor and power amplifier fundamentals, power amplifier design

[3] pulse width modulator for linear amplifier stages, DJ1MR, FA No. 10 and 11 2014

[4] Bernhard sequencer Hochstätter,
https://dl6nbs.homepage.tonline.de/html/sequenzer.html
[5] Josef Hisch, DJ7AW, CQ DL Heft 4, 2001 envelopes PA 80-15 meters [6] Josef Hisch, DJ7AW, CQ DL Heft 10, 2004, performance is not the same power [7] QEX, diplexer filter for to RF MOSFET Power Amplifier, by William E. Sabin, W0IYH, [8] Bolch, P .: RFSim 99, program for RF circuit simulation. FA 2001 issue H. 1 H. 2, [9] 300 and 600 Watt PA with IXYS Z-Mosfets, DJ1MR, FA No. 7 and 8 in 2012 [10] Mosfet PA for 1000 watts DJ1MR, CQ DL special QRO [eleven] Datasheet HCPL 0721, www.agilent.com/semiconductors