RCA
Solid State
Division

Digital Integrated Circuits

Application Note
ICAN-6539

Micropower Crystal-Controlled Oscillator Design Using RCA COS/MOS Inverters

by S. S. Eaton

RCA COS/MOS inverters have nanowatt standby power dissipation and microwatt operational power dissipation. This note describes in depth, the design of crystal-controlled oscillators, using the RCA CD4007 and RCA Developmental type TA5987 COS/MOS inverters as design examples. The CD4007 is identical to the TA5987 except for the range of supply voltages over which it will operate in crystal oscillator circuits. The CD4007 should be used in oscillator circuits operating at supply voltages from 5 V to 15 V; the TA5987, in oscillator circuits operating at supply voltages from 1.5 V to 5 V.

The design analysis presented in this note applies equally to both types of COS/MOS Inverters.

Quartz crystal oscillators have long been popular because of their excellent frequency stability and the wide range of frequencies over which they can be used. COS/MOS crystal oscillator circuits provide the additional advantages of low power consumption and stable operation over a wide range of supply voltages with no change in circuit component values required.

The design of COS/MOS crystal oscillator circuits, as in the design of any crystal oscillator circuit, involves the design of a feedback and an amplifying section. The basic circuit configuration is shown in Fig. 1.

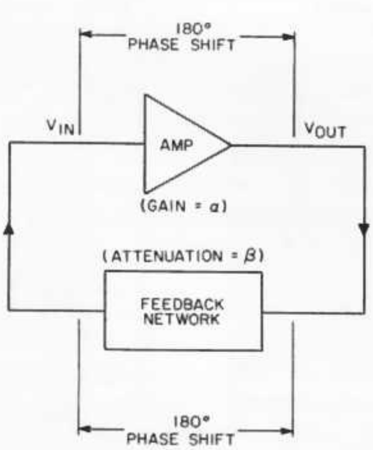


Fig. 1 - Basic feedback circuit.

To determine the conditions for oscillation, assume a small falling input (V_{in1}) to the amplifier with an inherent 180° phase shift between its input and output. The output of the amplifier (V_{o1}) will then be a rising waveform of amplitude αV_{in1}. If this signal is then applied to a feedback circuit which itself causes an additional 180° phase shift, the amplifier input (V_{in2}) will be an attenuated rising signal of amplitude βV_{o1} whose phase lags V_{o1} by 180°. This rising signal will in turn cause an amplified falling signal (V_{o2}) of magnitude αV_{in2} to appear at the amplifier output. If $V_{o2} \geq V_{o1}$ this cycle will continue and sustain oscillation. But $V_{in2} = \beta V_{o1}$ and $V_{o2} = \alpha V_{in2}$, therefore, $V_{o2} = \alpha\beta V_{o1}$ and since oscillation requires $V_{o2} \geq V_{o1}$, one of the conditions for oscillation is that $\alpha\beta \geq 1$. For oscillation to begin, however, $\alpha\beta$ must be greater than and not equal to 1, hence oscillators must be designed to satisfy this criterion. The other criterion for oscillation, as noted above, is that the phase shift around the loop be n360°. These two design considerations are known as the Barkhausen criteria for oscillation.

An understanding of crystal oscillator circuits requires an understanding of the crystal itself, or more specifically the equivalent electrical circuit of a quartz crystal shown in Fig. 2. This circuit is valid at

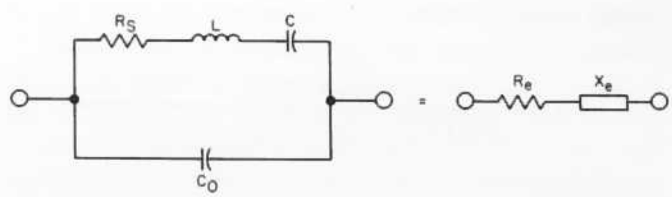


Fig. 2 - Equivalent circuit for a crystal.

frequencies near mechanical resonance and, with a change of values, at overtone frequencies. C_o is the actual electrical capacitance due to the plates enclosing the quartz and may be measured with a capacitance bridge. The other values are best measured with a C.I. (crystal impedance) meter. Table I lists typical values of the circuit elements at various resonant frequencies.

Printed in USA/1-71

TABLE I - TYPICAL CRYSTAL PARAMETER VALUES

Parameter	Frequency			
	90 kHz	280 kHz	525 kHz	2 MHz
R_s (Ω)	15 k	1.35 k	220	150
L (H)	137	27.7	7.8	0.785
C (pF)	0.0235	0.0117	0.0115	0.00135
Co (pF)	3.5	6.18	6.3	3.95

Assume for a first analysis of the equivalent circuit that $R_s = 0$. The complex impedance may then be expressed as:

$$Z = \frac{j(1 - \omega^2 LC)}{\omega^3 LCC_o - \omega(C + C_o)}$$

The series resonant frequency f_s is defined at the zero impedance point when $\omega^2 LC = 1$ or:

$$f_s = \frac{1}{2\pi\sqrt{LC}} \qquad (1)$$

The parallel resonant frequency f_p occurs at the infinite impedance point where $\omega^3 LCC_o = \omega(C+C_o)$ or:

$$f_p = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{1}{C} + \frac{1}{C_o}\right)} \qquad (2)$$

The impedance then becomes:

$$Z = \frac{-j}{\omega C_o} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

The addition of R_s to the equivalent circuit results in a crystal impedance of:

$$Z = \frac{(1 - \omega^2 LC) + j\omega R_s C}{-\omega^2 R_s CCo - j[\omega^3 LCC_o - \omega(C + C_o)]} \qquad (3)$$

Fig. 3a shows a graph of the magnitude of the impedance expressed by Eq. 3 as a function of frequency. The crystal parameter values used were those of a crystal having a series resonant frequency of 279.569 kHz. (280 kHz column in Table I). Fig. 3 also shows graphs of the impedance angle (ϕ_c) vs. frequency and the equivalent resistive (R_e) and reactive (X_e) components of the impedance obtained by multiplying both the numerator and denominator of Eq. 3 by the complex conjugate of the denominator. The magnitude of the impedance is then equal to $\sqrt{R_e^2 + X_e^2}$ and $\phi_c = \tan^{-1}(X_e/R_e)$.

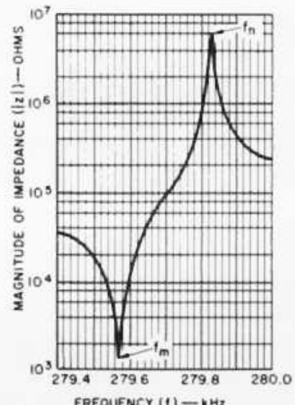
The reactance curve (X_e) of Fig. 3d, shows that the crystal appears purely resistive at two points where $X_e = 0$. These two points are defined as the resonance (f_r) and antiresonance (f_a) frequencies. Fig. 3d, shows f_r to be approximately 279.569 kHz, equal, at first glance, to the frequency of minimum impedance f_m (Fig. 3a) and to the series resonant frequency. This would indeed be true with $R_s = 0$. Actually, $f_m < f_s < f_r$, but may be considered equal for this discussion because for typical values of R_s, the difference between these frequencies is within a few parts per million. Similarly, consider $f_a = f_p = f_n$.

Fig. 3a shows that only a small frequency difference exists between the maximum and minimum impedance points. The ratio of f_n to f_m may be expressed as:

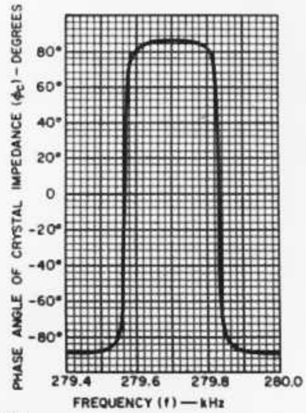
$$\frac{f_n}{f_m} \approx \frac{\omega_p}{\omega_s} = \frac{\sqrt{\frac{1}{L}\left(\frac{1}{C} + \frac{1}{C_o}\right)}}{\sqrt{\frac{1}{LC}}} = \left(1 + \frac{C}{C_o}\right)^{1/2}$$

therefore:

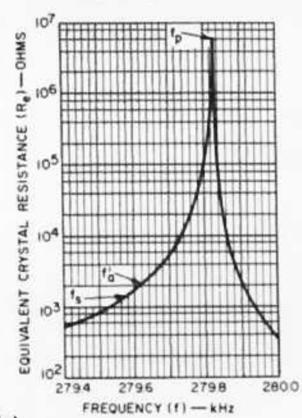
$$f_a \approx f_s \left(1 + \frac{C}{C_o}\right)^{1/2}$$



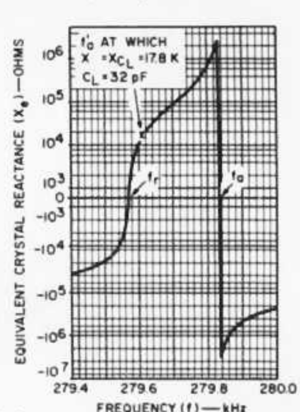
(a)
Fig. 3a - Magnitude of crystal impedance - vs - frequency.



(b)
Fig. 3b - Phase angle of crystal impedance - vs - frequency.



(c)
Fig. 3c - Equivalent crystal resistance - vs - frequency.



(d)
Fig. 3d - Equivalent crystal reactance - vs - frequency.

The ratio C/C_o is typically about 0.003, then $f_a \approx 1.0015 f_s$. Virtually all crystal oscillators are designed to operate between f_s and f_a hence the frequency difference is important.

Values of R_e and X_e are important considerations when designing for maximum oscillator stability. At the resonance and antiresonance frequencies, $/Z/ = R_e$ because $/Z/ = \sqrt{R_e^2 + X_e^2}$ and $X_e = 0$. The impedance at $f_s \approx f_r$ is equal to the impedance of R_s in parallel with C_o and since $X_{C_o} \gg R_s$ in a good crystal, $/Z/ \approx R_s$, hence at series resonance, $R_e \approx R_s$ are shown by Figs. 3a and 3c.

Another important consideration in a stable oscillator design is the rate of change of feedback network phase angle ϕ with frequency. One of the conditions for oscillation is that the phase angle around the loop be equal to n360°. If the amplifier phase shift is 180°, the feedback network must provide an additional 180° of phase shift. Because of inherent propagation delays, however, the amplifier phase shift is not precisely 180°. Furthermore, the propagation delay in the amplifier is variable e.g., due to supply voltage variations and/or variations in semiconductor performance with temperature changes. To maintain a 360° loop phase shift the feedback network must provide a phase change to compensate for any change in amplifier phase shift. The result is a frequency shift, which as in the case of a stable oscillator, will be small if $d\phi/df$ is maximized.

The rate of change of feedback network phase angle with frequency is directly related to the phase changing properties of the crystal. Fig. 3b, shows that a high rate of change of impedance angle with frequency occurs at the resonance and antiresonance frequencies. The high $d\phi/df$ is a result of the high $Q = \omega_0 L/R_s$ of the equivalent circuit. Maximum $d\phi/df$ will occur with maximum Q or when R_s is a minimum. With $R_s = 0$, Fig. 3b will appear as two vertical lines at f_r and f_a indicating infinite $d\phi/df$. For maximum frequency stability, then, it is desired that R_s be minimum.

Fig. 3a shows that the impedance of the crystal rapidly increases as f_a is approached. For this reason, most crystal oscillator circuits are designed to operate at or near series resonance. Operation at antiresonance is impractical not only because of the extremely high input impedance, but also because of the frequency dependence on C_o (Eq. 2). Stray capacitance in the circuit layout is usually significant when compared with C_o, hence wide variations in frequency can occur with various circuit layouts. The frequency becomes less dependent on C_o as f_s is approached and is completely independent of C_o at f_s.

A method of reducing the frequency dependence on C_o is to manufacture the crystal to resonate at the design frequency with a specified value of external loading capacitance. A load capacitor C_L could be placed in parallel with the crystal thereby effectively increasing C_o and greatly reducing the effect of circuit stray capacitance if C_L is sufficiently large. The presence of C_L will also decrease the impedance viewed across the crystal terminals. Both considerations make operation at antiresonance more practical.

Another method of operation is to place the loading capacitor in series with the crystal. The effective resistance R_e of the series circuit will not change, however, the reactance becomes $X_e - X_{C_L}$. The frequency of minimum impedance will again occur when the total reactance is zero or when $X_e = X_{C_L}$. Fig. 3d shows a frequency f'_a of about 279.611 kHz at which $X_e = X_{C_L}$ for C_L = 32 pF. Because $X_e - X_{C_L} = 0$ at this frequency, the magnitude of $Z = \sqrt{R_e^2 + (X_e - X_{C_L})^2} = R_e$. To keep R_e small, then, f'_a should be close to f_s. C_L, however, becomes infinite as f_s is approached. Hence one cannot choose a point too close to f_s such that the large values of C_L required cannot satisfy the gain and phase requirements of the oscillator circuit. Values for C_L of 20 pF and 32 pF are typically used.

The frequency f'_a at which $X_e = X_{C_L}$ is approximately equal to the antiresonance frequency of the crystal with the same value of C_L as a parallel loading capacitor. The crystal impedance at f'_a, however, differs for the two cases. With a series loading capacitor it has been shown that $/Z/ = R_e \approx$ 1.9 kΩ at f'_a (Fig. 3c). The impedance (with a parallel loading capacitor of 32 pF) can be calculated using Eq. 3. With C_o = 32 +6.18 = 38.18 pF, /Z/ is found to be 155 kΩ at f'_a, or many times greater than 1.9 kΩ. The $d\phi/df$ is also found to be greater for a series loading capacitor than for a capacitor in parallel with the crystal. Hence a series loading capacitor is generally preferred.

Crystals manufactured to resonate at the stamped design frequency, then, will oscillate with a parallel loading capacitor at the antiresonant frequency f'_a of the combination and with a series loading capacitor at the series resonant frequency (again f'_a) of the combination. Such crystals are called antiresonant crystals for use in antiresonant oscillator circuits as distinguished from series resonant crystals designed to oscillate at f_s in series resonant oscillator circuits. The term "antiresonant oscillator circuit" is perhaps a misnomer. When operating with a series loading capacitor the circuit is oscillating somewhere between f_s and f_a and not at the true antiresonant frequency of the crystal.

Both types of oscillator circuits employ the general circuit configuration shown in Fig. 1. However, the design of the amplifying and feedback sections differ. Antiresonant oscillator circuits with a series loading capacitor are most applicable to COS/MOS crystal oscillator circuits and are the types discussed subsequently.

A good amplifier for the amplifying section of the oscillator is a COS/MOS inverter with a large resistor connected from the input of the inverter to the output as shown in Fig. 4a. The value of R_f should be large enough ($\geq$ 10 MΩ) such that the attentuation and phase of the feedback network are not appreciably affected. The resistor dc biases the output voltage at the point at which $V_O = V_I$. This point is typically at or near one-half of the supply voltage as noted from the typical COS/MOS inverter transfer characteristics shown in Fig. 4b. With V_{DD} = 10 V, a ±1 V swing around the bias point causes an output swing of

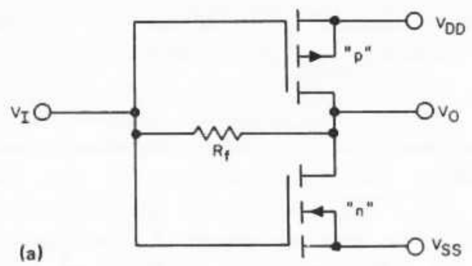


Fig. 4a - Typical COS/MOS inverter with feedback resistor.

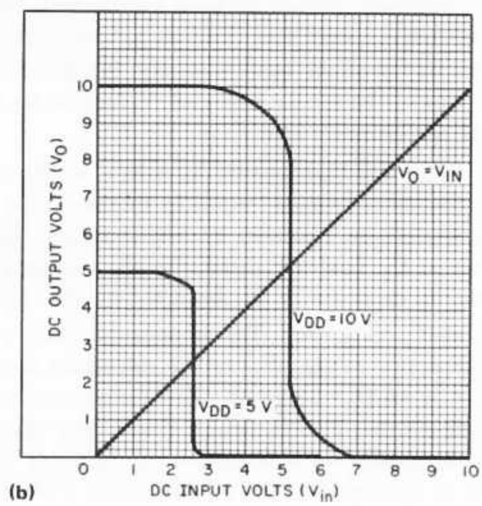


Fig. 4b - Typical COS/MOS inverter transfer characteristics.

approximately 10 V, hence the voltage gain (α) of the amplifier for a full swing is about 5. The transfer characteristics become sharper as the supply voltage is lowered and the gain at a V_{DD} = 5 V increases to about 10. An oscillator circuit, then, may be formed using this amplifier with a feedback network having an attenuation constant (β) greater than 1/5 ($\beta = 0.2$).

The feedback circuit should not only be capable of $\beta >$ 0.2 but should also maintain a high rate of change of phase angle with frequency ($d\phi/df$) and be designed such that interchanging any oscillator component will not cause a significant shift in the frequency of oscillation. Fig. 5 shows a crystal pi network circuit which will accomplish these objectives with the correct choice of component values.

The analysis of this circuit is best accomplished by referring to the circuit in Fig. 5 showing each element with its effective impedance. Because the input to the COS/MOS inverter appears almost purely capacitive, this input capacitance has been added to C_Y and designated as C_S. Similarly, the output impedance, almost purely resistive, is added to the value of R_X; with the total resistance designated as R.

Loop equations for this circuit are:

$$V_1 = I_1\,(R - jX_{C_T}) + I_2(jX_{C_T})$$
$$0 = I_1\,(jX_{C_T}) + I_2\,[R_e + j(X_e - X_{C_X} - X_{C_T} - X_{C_S})]$$
$$V_2 = -I_2(jX_{C_S}) \qquad (4)$$

V_2/V_1 is then found as shown below: *

Let:

$$X_{L(eff)} = X_e - X_{C_S} - X_{C_X} \qquad (5)$$

Then $X_{L(eff)}$ is the effective inductance of the circuit in parallel with C_T.

The phase angle between V_2 and V_1 is then given as:

$$\phi = 180^\circ - \tan^{-1}\left[\frac{R\left(X_{L(eff)} - X_{C_T}\right) - R_eX_{C_T}}{R_eR + X_{C_T}\;X_{L(eff)}}\right] \qquad (6)$$

The phase angle will equal 180° when:

$$R(X_{L(eff)} - X_{C_T}) - R_e\,X_{C_T} = 0 \qquad (7)$$

For an ideal crystal with zero series resistance, R_e will also equal 0 and Eq. 7 becomes:

$$X_{L(eff)} - X_{C_T} = 0$$

Substituting from Eq. 5 for $X_{L(eff)}$ and solving for X_e:

$$X_e = X_{C_S} + X_{C_X} + X_{C_T} \qquad (8)$$

$$* \;\; \frac{V_2}{V_1} = \frac{-X_{C_T} \bullet X_{C_s}}{R_e \bullet R + X_{C_T}\,(X_e - X_{C_s} - X_{C_X}) + j\,[R(X_e - X_{C_T} - X_{C_s} - X_{C_X}) - R_eX_{C_T}]}$$

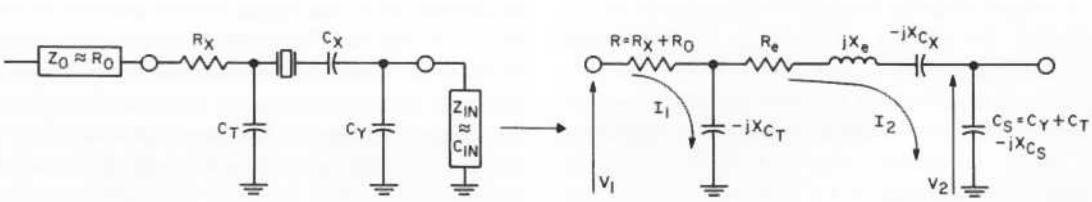


Fig. 5 - Crystal pi network.

The right-hand side of Eq. 8 is the capacitive reactance seen by the crystal at its terminals and is equal to X_{C_L}, where C_L is the value of the series loading capacitor mentioned previously. It was noted, then, that the minimum impedance point existed at the frequency f'_a at which $X_e = X_{C_L}$. Eq. 8 predicts that for a crystal pi network with an ideal crystal, the required phase angle of 180° necessary for oscillation will also occur at f'_a where $X_e = X_{C_L}$. Typical value of R_e will cause the phase angle at f'_a to be greater than 180°. However, the difference is usually within 10°, and is actually beneficial for design, because the feedback network is always required to have a phase shift greater than 180°, to compensate for an amplifier phase shift less than 180°.

When $\phi = 180°$ Eq. 4 shows that the magnitude of V_2/V_1 becomes:

$$\left|\frac{V_2}{V_1}\right| = \beta = \frac{X_{C_T} X_{C_S}}{R_e R + X_{C_T} X_{L(eff)}}$$

This may be rearranged as:

$$\beta = \frac{X_{C_S}}{X_{L(eff)}} \left[\frac{1}{1 + \left(\frac{R}{X_{C_T}}\right)\left(\frac{R_e}{X_{L(eff)}}\right)}\right] \tag{9}$$

Defining:

$$K_A = 1 + \left(\frac{R}{X_{C_T}}\right)\left(\frac{R_e}{X_{L(eff)}}\right) \tag{10}$$

Eq. 9 becomes:

$$\beta \text{ at } \phi = 180° = \frac{X_{C_S}}{X_{L(eff)} K_A} \tag{11}$$

This equation is important when choosing component values which must satisfy the loop gain requirement.

Another important requirement is that $d\phi/df$ must be large for stable oscillation. The phase change around the 180° point is found from Eq.'s 5 and 6 as:

$$\tan(\Delta\phi) = \frac{R(X_e - X_{C_s} - X_{C_x} - X_{C_T}) - R_e X_{C_T}}{R_e R + X_{C_T}(X_e - X_{C_s} - X_{C_x})} \tag{12}$$

To find $d(\Delta\phi)/df$, note that:

$$\frac{d(\Delta\phi)}{df} = \frac{dX_e}{df} \cdot \frac{d(\Delta\phi)}{dX_e} \approx K \frac{d(\Delta\phi)}{dX_e}$$

because dX_e/df can be regarded as the constant in the small frequency range around f'_a. X_{C_S}, X_{C_x}, and X_{C_T} in Eq. 12 can also be considered constant, and X_e is the only frequency dependent term. For stability calculations, then, it is sufficient to find $d(\Delta\phi)/dX_e$.

$d(\Delta\phi)/dX_e$ can be calculated by differentiating Eq. 12 as:

$$\frac{d\,[\tan(\Delta\phi)]}{dX_e} = \frac{d(\Delta\phi)}{dX_e} \cdot \frac{d\,[\tan(\Delta\phi)]}{d(\Delta\phi)} = \frac{d(\Delta\phi)}{dX_e} \cdot \sec^2(\Delta\phi)$$

then,

$$\frac{d(\Delta\phi)}{dX_e} = \cos^2(\Delta\phi)\,\frac{d\,[\tan(\Delta\phi)]}{dX_e}$$

and:

$$\frac{d(\Delta\phi)}{dX_e} = \frac{\cos^2(\Delta\phi)}{R_e}\left[\frac{1}{1 + \frac{X_{C_T}}{R}\cdot\frac{X_{L(eff)}}{R_e}}\right]\left[1 - \frac{X_{C_T}}{R}\left[\frac{R(X_e - X_{C_T} - X_{C_S} - X_{C_x}) - R_e X_{C_T}}{R_e R + X_{C_T} X_{L(eff)}}\right]\right] \tag{13}$$

Using Eq's 10 and 12, this may be simplified as:

$$\frac{d(\Delta\phi)}{dX_e} = \frac{\cos^2(\Delta\phi)}{R_e}\left[\frac{K_A - 1}{K_A}\right]\left[1 - \frac{X_{C_T}}{R}\tan(\Delta\phi)\right] \tag{14}$$

The maximum value of $d\Delta\phi/df$ (referring to Eq.13) is obtained when $R = \infty$. Then:

$$\left[\frac{d(\Delta\phi)}{dX_e}\right]_{MAX} = \frac{\cos^2(\Delta\phi)}{R_e} \tag{15}$$

A stability factor S_F for an oscillator circuit is:

$$S_F = \frac{\frac{d(\Delta\phi)}{dX_e}}{\left[\frac{d(\Delta\phi)}{dX_e}\right]_{MAX}}$$

S_F is then given by Eq.'s 14 and 15 as:

$$S_F = \left(\frac{K_A - 1}{K_A}\right)\left(1 - \frac{X_{C_T}}{R}\tan(\Delta\phi)\right) \tag{16}$$

Solving Eq. 10 for X_{C_T}/R and substituting into Eq. 16 results in:

$$S_F = \frac{K_A - 1}{K_A} - \frac{\tan(\Delta\phi)}{K_A\left(\frac{X_{L(eff)}}{R_e}\right)} \tag{17}$$

Maximum stability, then, occurs with maximum K_A and minimum $\Delta\phi$.

With the information given, it is now possible to derive the design equations for any crystal oscillator and apply them directly to oscillator circuits using COS/MOS amplifiers.

One important design equation is derived noting that the f'_a:

$$X_{C_T} = X_{L(eff)} \tag{18}$$

This result was obtained in the derivation of Eq. 8.

Another design equation may be derived by solving Eq. 11 for X_{C_S}, substituting into Eq. 5, and solving for $X_{L(eff)}$ as:

$$X_{L(eff)} = \frac{X_e - X_{C_X}}{1 + \beta K_A} \tag{19}$$

β in this equation should be chosen such that $\alpha\beta > 1$. For minimum power consumption β should be large because a large voltage swing at the amplifier input will minimize the operating time near the bias point when both "N" and "P" MOS transistors are "ON". Experimentally, $\beta = 0.75$ has proven to be a satisfactory value. The product $\alpha\beta$ will then always be greater than 1 because the gain of a COS/MOS amplifier is always greater than $1/.75 = 1.33$.

A suitable value of K_A may be chosen by solving Eq. 17 for K_A as:

$$K_A = \frac{1}{1 - S_F} + \frac{\tan(\Delta\phi)}{(1 - S_F)\left(\frac{X_{L(eff)}}{R_e}\right)} \tag{20}$$

Values of S_F and $\Delta\phi$ must now be determined.

In general, the power consumption of a crystal oscillator increases with increasing S_F, hence it is not always desirable to maximize S_F. It has been determined experimentally, that a value of $S_F = 0.75$ provides excellent stability with low power consumption.

The value of $\Delta\phi$ is experimentally determined by noting the phase shift through the COS/MOS amplifier at a particular frequency and supply voltage and subtracting this value from 180°. $\Delta\phi$ typically is less than 5° at frequencies up to approximately 300 kHz (V_{DD} = 8 V). A maximum value of 15° is a safe assumption for frequencies below 2.5 MHz.

Substituting $S_F = 0.75$ and $\Delta\phi = 15°$ in Eq. 20 results in:

$$K_A = 4 + \frac{1.07}{\left(\frac{X_{L(eff)}}{R_e}\right)} \tag{21}$$

Eq.'s 21 and 19 may now be solved simultaneously for K_A as:

$$K_A = \frac{4(X_e - X_{C_X}) + 1.07\ R_e}{X_e - X_{C_X} - 1.07\ R_e\beta} \tag{22}$$

With Eq.'s 10, 11, 18, 19, and 22, a COS/MOS crystal oscillator circuit may easily be designed for any crystal with only a known value of its maximum equivalent resistance at a specified value of loading capacitance C_L.

As a design example, consider a crystal which resonates in antiresonant oscillator circuits at 279.611 kHz with C_L = 32 pF. The data for this crystal were presented in Fig. 3 and an equivalent resistance of 1.9 kΩ was found at f'_a = 279.611 kHz. If this value is used for R_e, however, the results obtained would apply only to this particular crystal. Equivalent resistances of crystals manufactured to resonate at the same frequency can vary by an order of magnitude. The important value of R_e is the maximum value of equivalent resistance. Using this value will insure $S_F \geq 0.75$ and $\beta \geq 0.75$ at the design frequency.

One begins the design by calculating K_A from Eq. 22. In COS/MOS oscillator circuits C_X can usually be eliminated, then $X_{C_X} = 0$ in Eq. 22. It may, however, be desirable to include C_X in some cases, because this allows an increase in the value of C_S, which decreases the frequency dependence on the input capacitance of the COS/MOS inverter. With $X_{C_X} = 0$, though, the values of C_S obtained are usually much larger than the individual variations in inverter input capacitance.

The value of $R_{e_{max}}$ to be used in Eq. 22 is usually supplied by the crystal manufacturer and is specified as 2.5 kΩ for the 279.611 kHz crystal type used in this example. $X_e = X_{C_L}$ for C_L = 32 pF, was found previously as 17.8 kΩ. With R_e = 2.5 kΩ, $X_{C_X} = 0$ and $\beta = 0.75$, K_A then is calculated as 4.67. Substituting this value in Eq. 19 gives $X_{L(eff)}$ = 3.96 kΩ. From Eq. 18, X_{C_T} is also equal to 3.96 kΩ. X_{C_S} is found from Eq. 11 as 13.9 kΩ. The value of R is found from Eq. 10 to be 23 kΩ. Values of C_S and C_T may be found from:

$$C = \frac{X_e\ C_L}{X_C}$$

With C_S = 41 pF. and C_T = 142 pF one should check to insure that $1/C_L = 1/C_T + 1/C_S$, and in this case, $1/31 \approx 1/41 + 1/142$. The circuit then, should oscillate at or near 279.611 kHz with R = 23 kΩ, C_S = 41 pF and C_T = 142 pF, assuming that the amplifier phase lag is equal to or near the phase lead of the feedback circuit at f'_a.

Because the output impedance of a COS/MOS inverter is typically 1 kΩ, a value of 22 kΩ should be used for R_X (Fig. 5). To obtain the value for C_y, the value of C_S should be lowered by the value of the wiring and input capacitance including the increase in C_{in} due to the Miller effect. Assume:

$$C_y = C_S - 10\ \text{pF} \quad 1.5\ \text{V} \leq V_{DD} < 5\ \text{V}$$
$$C_y = C_S - 15\ \text{pF} \quad 5\ \text{V} \leq V_{DD} \leq 15\ \text{V}$$

In addition, a small trimmer capacitor for trimming to the design frequency should be added in parallel with C_T. The trimmer capacitor should have a maximum value of about 30% of the calculated value for C_T and the actual value of C_T chosen such that C_T plus the midrange value of the trimmer capacitor equals the calculated value of C_T. The complete COS/MOS crystal oscillator circuit for the 279.611 kHz crystal is shown in Fig. 6. Standard component values close to those calculated are used.

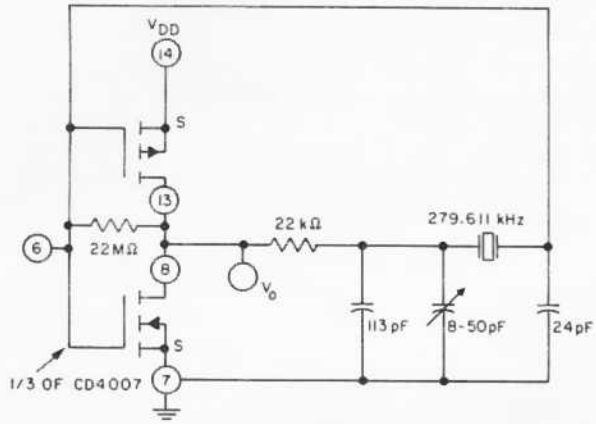


Fig. 6 - Crystal oscillator circuit using RCA type CD4007.

Fig. 7 shows results calculated from Eq. 4 for the phase shift vs. frequency (7a) and for β vs. frequency (7b.) for the 279.611 kHz oscillator. Note that $d\phi/df$ and β are greatest at 279.611 kHz or when $X_e = X_{C_L}$. From Fig. 7a, the frequency is seen to change by about 1.2 cycles for $\Delta\phi = 15°$. The stability of the oscillator may then be predicted at $1.2/279.611 = 4.3$ ppm assuming only a phase change in the amplifier. The actual stability, of course, will be somewhat less due to variations in crystal parameters and component values with temperature changes.

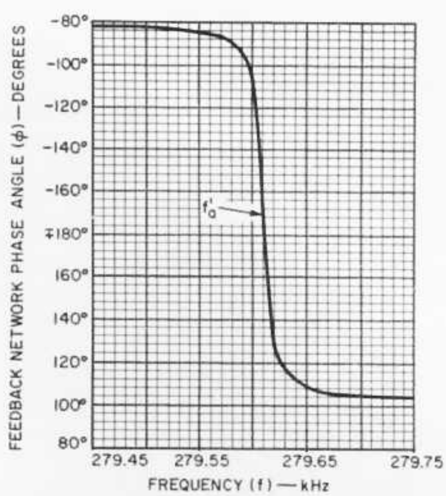


Fig. 7a - Feedback network phase angle - vs - frequency for circuit of Fig. 6, $V_{DD} = 15$ V.

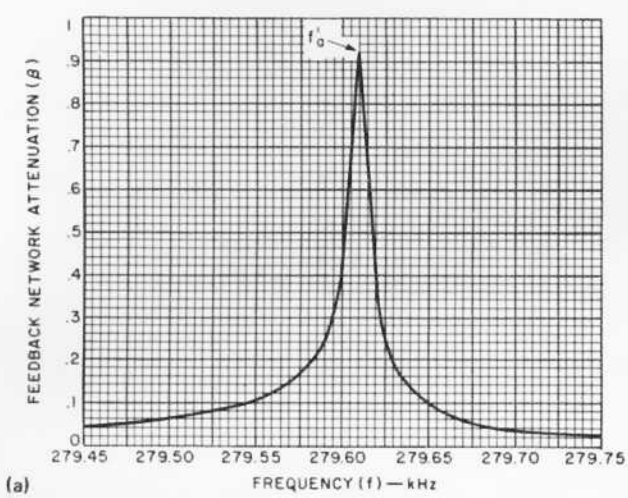


Fig. 7b - Feedback network attenuation - vs - frequency for circuit of Fig. 6.

The values of components in Fig. 6 only apply to the 279.611 kHz crystal used. Values of C_S and C_T, however, will remain close to 41 pF. and 142 pF, if $C_L = 32$ pF., and K_A is chosen from Eq. 20 with $\beta = 0.75$ and $X_{C_X} = 0$. The value of R, though, will change according to the maximum equivalent resistance of the crystal used. The number of different component values satisfying the design equations for different oscillator specifications is virtually infinite and the component values here are only presented for a typical case. The design equations have been derived to allow freedom of design for desired characteristics.

The COS/MOS crystal oscillator circuit shown in Fig. 6 may be operated at supply voltages from 5 V to 15 V using the CD4007 and as low as 2.5 V with the TA5987. For lower current drain, the circuit may be modified (Fig. 8) by adding resistors in the supply and ground lines when a full V_{SS} to V_{DD} output voltage swing is not required. The value of R_X in this circuit should be lowered by the added resistance.

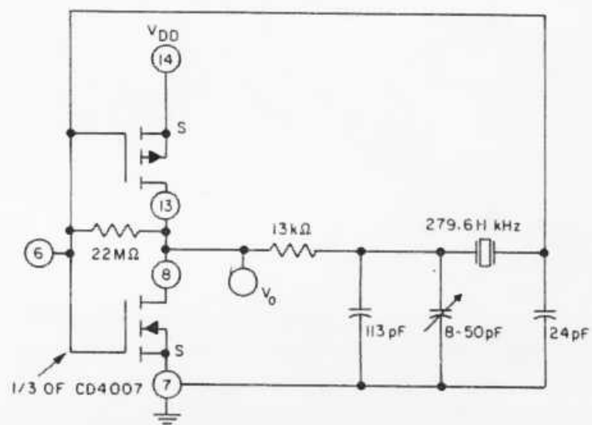


Fig. 8 - Crystal oscillator circuit using RCA type CD4007, $V_{DD} < 15$ V.

Operation at 1.5 V is possible using the TA5987 with the circuit shown in Fig. 9. The maximum operating frequency of this circuit is about 200 kHz. Beyond this frequency, inverter switching becomes difficult. The circuit of Fig. 9 uses a 65.536 kHz crystal with $C_L = 20$ pF., for reduced inverter loading. The 10 MΩ resistor should be connected to point A (Fig. 9) for "N" $I_{DS} = 10\ \mu A$ threshold voltages between 1.1 V and 1.4 V and to point B for "N" threshold voltages less than 1.1 V. Experimental data taken on all three oscillator circuits is listed in Tables II and III.

A wide range of frequencies are possible with COS/MOS crystal oscillator circuits. Frequencies up to about 10 MHz are possible at a V_{DD} of 15 V. Beyond 10 MHz $\Delta\phi$ becomes too large and stability decreases accordingly. The lowest frequency of operation depends only on the equivalent

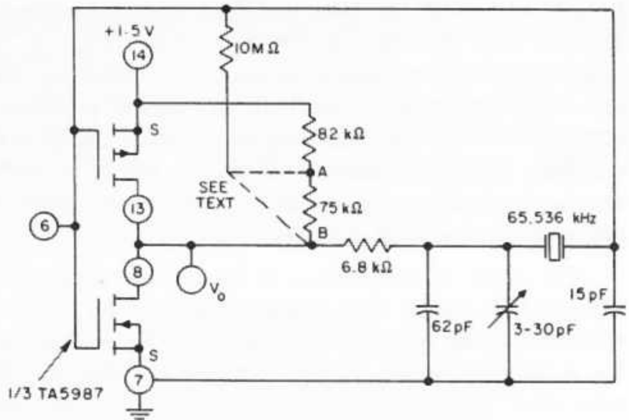


Fig. 9 - Crystal oscillator circuit using the RCA developmental type TA5987, V_{DD} = 1.5 V.

resistance of the crystal. Values of R_s and R_e increase rapidly at the lower frequencies and require amplifiers with high input impedance to minimize the attentuation (β) across the feedback network. Because COS/MOS amplifiers have high input impedances of approximately $10^{11}\Omega$, much lower frequencies are possible in COS/MOS antiresonant oscillator circuits than in bipolar transistor antiresonant circuits. Frequencies down to 2 kHz have been achieved with three inverters (one CD4007) connected in parallel to provide the greater current drive required by the crystal at this frequency.

Frequencies lower than 2 kHz are easily obtained by counting down the oscillator frequency. For example, a 16.384 kHz oscillator could be used with the RCA Dev. No. TA5939 14-stage binary counter with the fourteenth stage counting at one pulse per second. An inverter to be used as the âmplifier is already integrated into the TA5939, hence, only the feedback circuit needs to be added. Using the circuit shown in Fig. 9, the entire oscillator and counter can be operated at 1.5 V for single battery operation at an average current drain of less than 10 μA. A functional diagram of the TA5939 is shown in Fig. 10.

With the information presented on the crystal itself and from the design equations derived herein, it should now be possible to design COS/MOS crystal oscillator circuits for any specific application. A wide variety of applications can advantageously profit from the use of COS/MOS crystal oscillators, which offer exceptionally low power consumption and the ability to operate at supply voltages of 1.5 V to 15 V over a wide range of frequencies.

TABLE II – FREQUENCY CHANGE FOR CIRCUIT OF FIG. 6, AS A RESULT OF TEMPERATURE AND V_{DD} VARIATIONS

CONDITION	FREQUENCY CHANGE PARTS/MILLION	CIRCUIT
−40° to +85° change in ambient temperature:		Fig. 6
on the COS/MOS unit alone	4	
on the complete oscillator (mica capacitors, carbon resistors)	55	
+25% change in V_{DD} T_A = 25°C	+3.5	
−25% change in V_{DD} T_A = 25°C	−3.5	

TABLE III – SUPPLY VOLTAGE AND CORRESPONDING AVERAGE SUPPLY CURRENT FOR VARIOUS COS/MOS CRYSTAL OSCILLATOR CIRCUITS

SUPPLY VOLTAGE VOLTS	AVERAGE SUPPLY CURRENT MICROAMPERES	CIRCUIT
1.5	8	Fig. 9
2.5	23	Fig. 6
3.5	47	
5.0	105	
6.0	86	Fig. 8
10.0	200	

REFERENCES

(1) D. Firth, "Quartz Crystal Oscillator Circuits Design Handbook", The Magnavox Co., 1965.

(2) E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

(3) D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

(4) P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

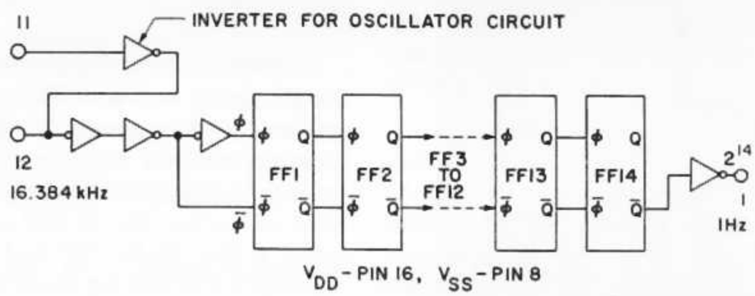


Fig. 10 - Functional diagram of RCA developmental type TA5939.