VINAY S

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Summary

Electronics and Communication Engineering graduate with internship experience at ISRO and a trained Design Verification Engineer. Strong foundation in digital electronics and skilled in debugging, analyzing functional correctness,and developing test strategies. Seeking opportunities in design verification roles in the semiconductor industry

Skills

Languages: Verilog, System Verilog, C, Python*,Perl*

Methodology:UVM.Constraint Random Coverage Driven Verification, Assertion Based Verification (SVA),Static Timing Analysis

Verification Tools: Siemens EDA(ModelSim),Synopsys VCS,MATLAB

Design Tools: Xilinx (ISE,Vivado),Intel Quartus,Synopsys Design Compiler,Cadence Virtuoso

Linting Tools: Synopsys SpyGlass

Verification Skills: RTL Simulation, Testbench Development

Protocols: AHB,APB,UART,SPI

Projects

•**AHB to APB Bridge Verification (UVM-based)**   *Technology Used: Synopsys VCS, Mentor's Questa*
Verification   Maven Silicon,2025

- Implemented a UVM environment for verifying an AMBA AHB-to-APB Bridge.
- Developed master (AHB) and slave (APB) agents including drivers, sequencers, monitors, and transaction-level objects and verified using Scoreboard.
- Generated and randomized AHB write/read transactions with constraints on address, size, burst, and length.

•**Implementation of Router 1x3**   *Technology Used: Xilinx ISE,Synopsys VCS*
RTL Design,Verification   Maven silicon,2025

- Designed and implemented a 1x3 packet router in Verilog with FSM-based control, FIFO buffering, synchronizer and register blocks for header, payload, and parity storage.
- Developed modular architecture ensuring reliable packet-based data transfer with address-based routing across three output ports.
- Developed a UVM based Testbench with sequence items, driver, monitor, scoreboard.

•**Implementation of Ethernet Switch**   *Technology Used: ModelSim, Quartus Prime*
RTL Design   Academic Project,2025

- Designed and verified a 2x2 packet router using Verilog HDL, integrating CRC (Cyclic Redundancy Check) error detection for enhanced data integrity and error correction in packet-switched networks.
- Implemented destination address-based routing logic to accurately process and forward incoming packets from two input ports to the appropriate output port
- Performed comprehensive RTL simulation using ModelSim and synthesis using Quartus Prime.

Experience

ISRO, U R Rao Space CenterProject: SRRC Filter with Variable Roll-Off Factor   **Oct 2024 - Jan 2025**

- Designed and implemented a Square Root Raised Cosine (SRRC) digital filter with a dynamic roll-off factor to improve digital communication system performance and spectral efficiency.
- Applied adaptive signal processing techniques to optimize filter response under varying channel conditions.
- Developed and simulated the filter architecture using MATLAB, Simulink, and polyphase filter structures for efficient realization

Certifications

Advanced VLSI Design and Verification course Pursuing at Maven Silicon (January 2025 - Present)

Explore Electrical Engineering Job Simulation GE Aerospace

System Verilog Udemy

ESP 32 and IOT Workshop IEEE Bangalore

IEEE SPS seasonal school on AI trends in Signal Processing IEEE Bangalore

Education

•**Bachelor of Technology in Electronics and Communication Engineering**   *2021-2025*
RNSIT,Visvesvaraya Technological University   CGPA: 8.3