Semiconductor Memory Organization & Addressing

Organización de Computadoras 2020

Dr. Agustin M. Laprovitta (alaprovitta@famaf.unc.edu.ar)

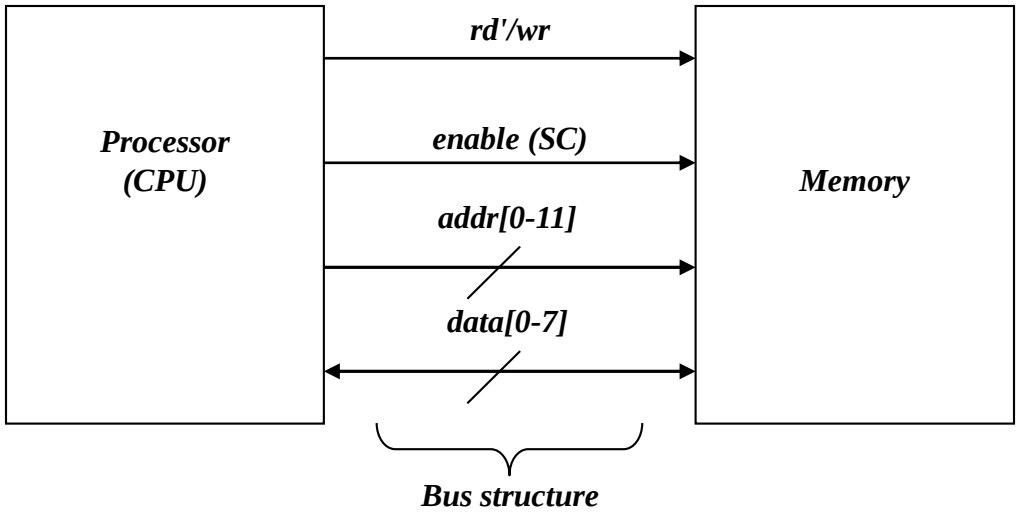
UNC Universidad Nacional de Córdoba

FAMAF Facultad de Matemática, Astronomía, Física y Computación

Introduction

- Computer systems functionality aspects
  - Processing
    - Transformation of data
    - Implemented using processors
  - Storage
    - Retention of data
    - Implemented using memory
  - Communication
    - Transfer of data between processors and memories
    - Implemented using buses
    - Called *interfacing*

A simple bus



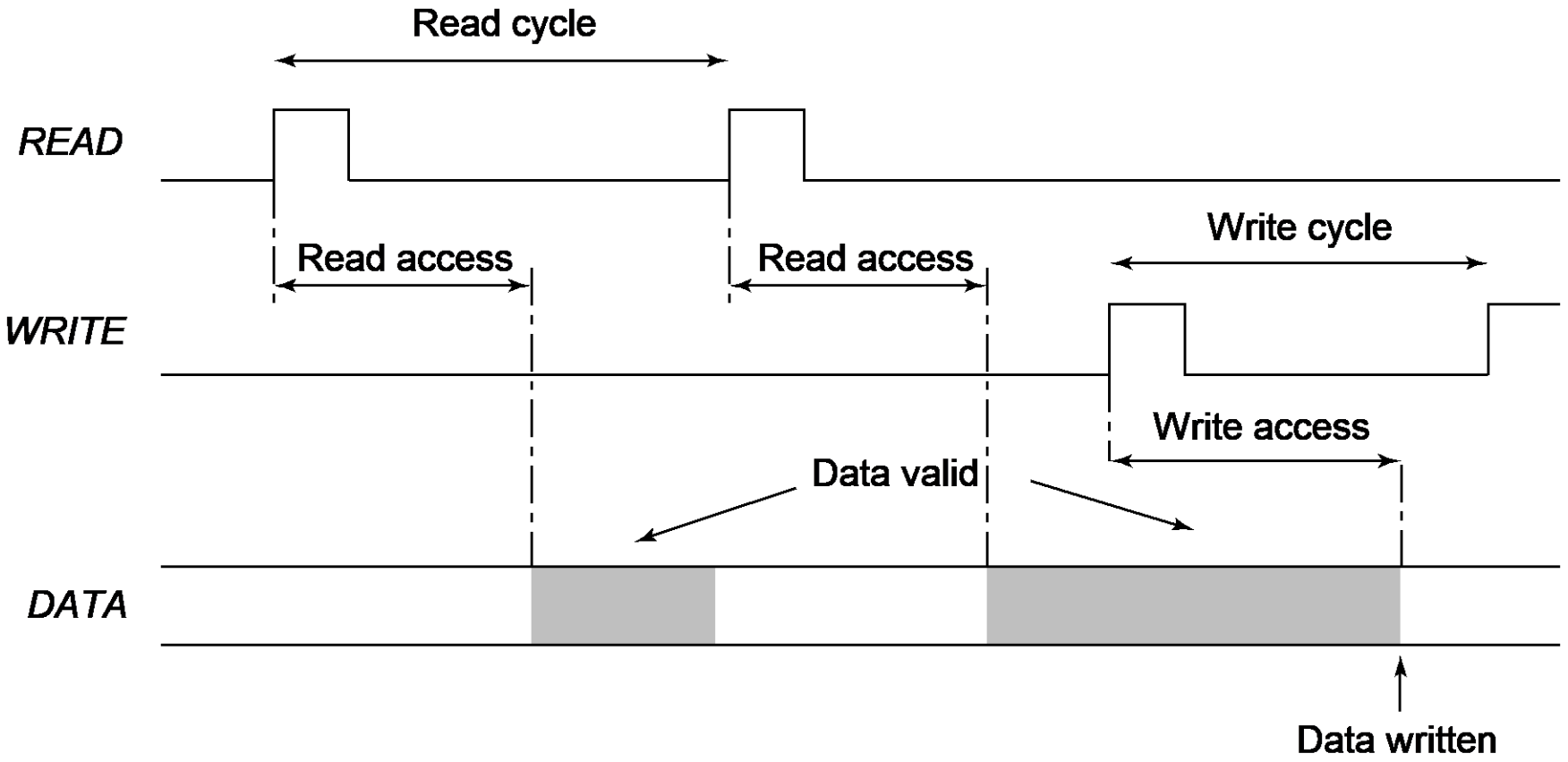
- Wires:
  - Uni-directional or bi-directional
  - One line may represent multiple wires
- Bus
  - Set of wires with a single function
    - Address bus, data bus
  - Or, entire collection of wires
    - Address, data and control
    - Associated protocol: rules for communication

Semiconductor Memory Classification

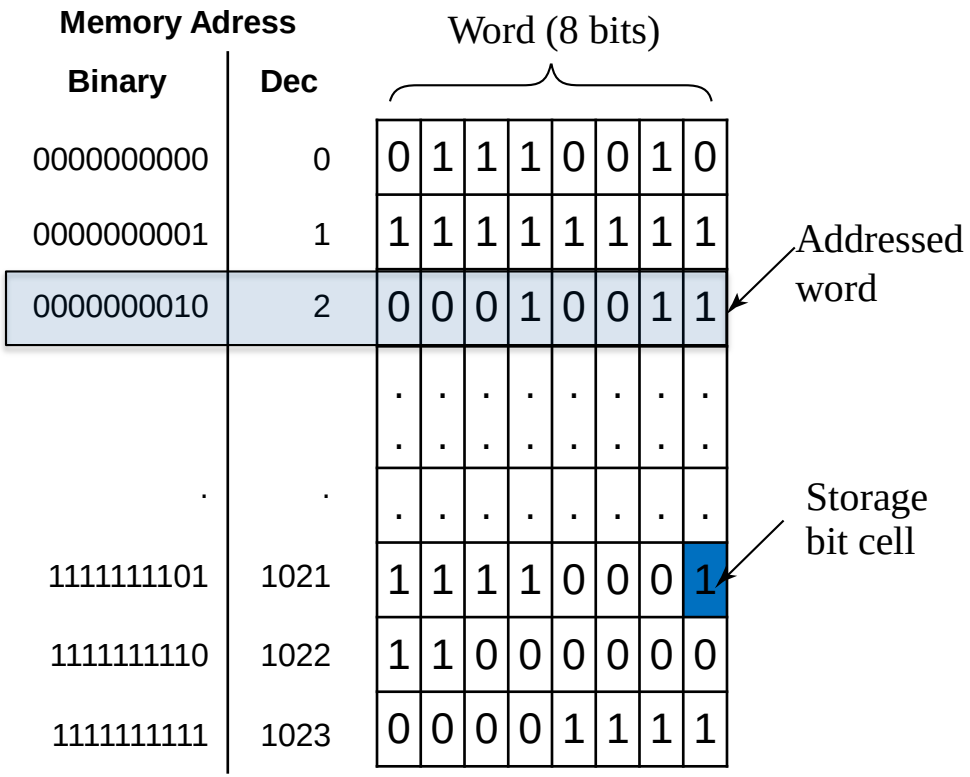
Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CACHE		

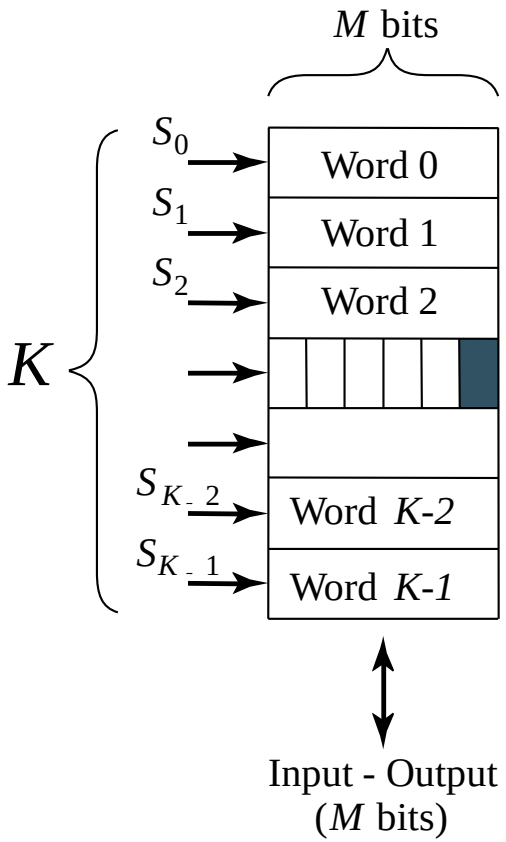
** Digital Integrated Circuits 2dn – Memories (SCU 2011, PhD Shoba Krishnan)*

Memory Timing: Definitions



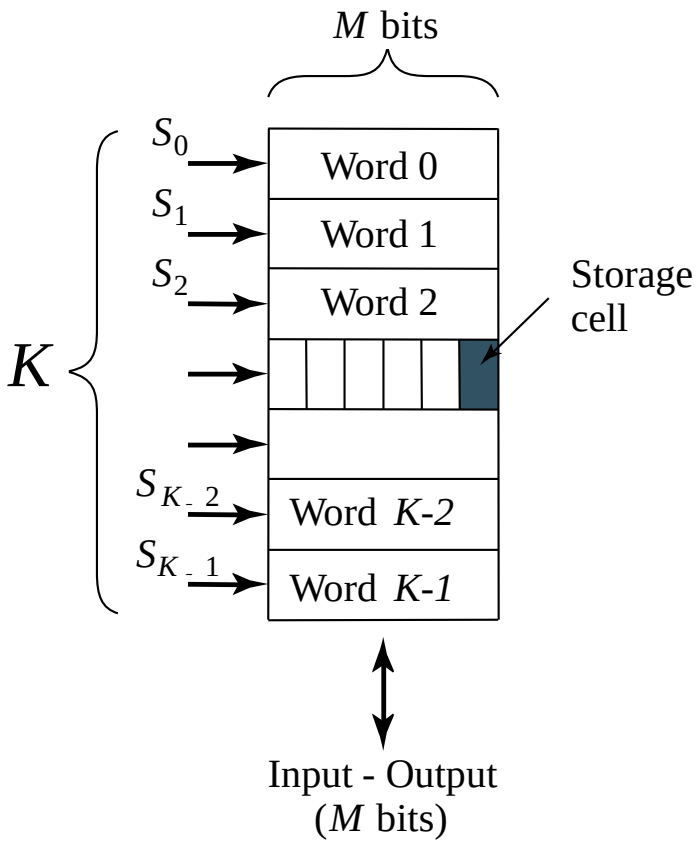
Memory Organization



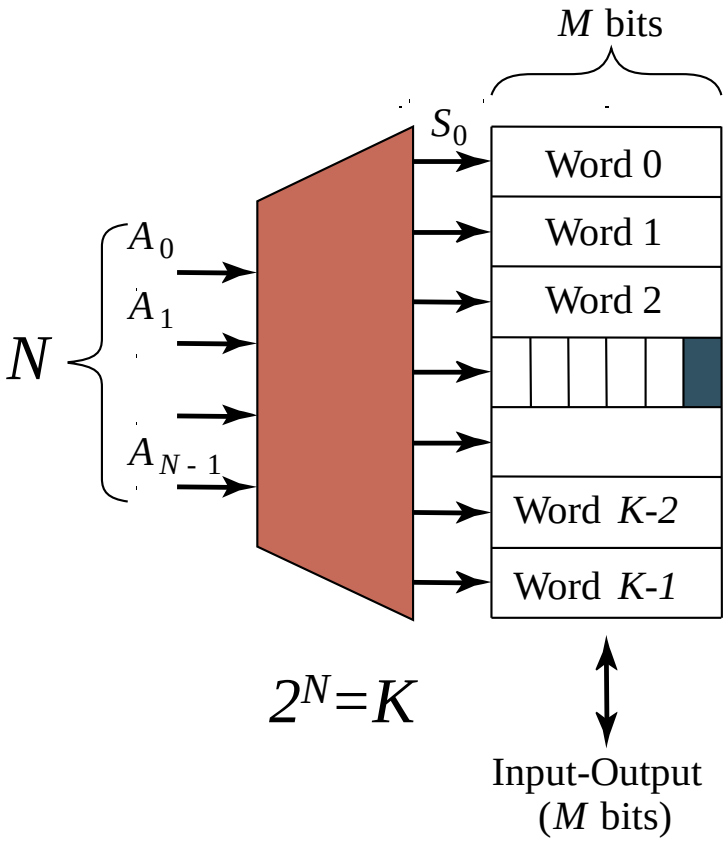


Example organization for
1Kword x 8 bits = 8K bits memory

Memory Architecture: Decoders



Intuitive architecture for K x M memory
Too many select signals:
K words == K select signals

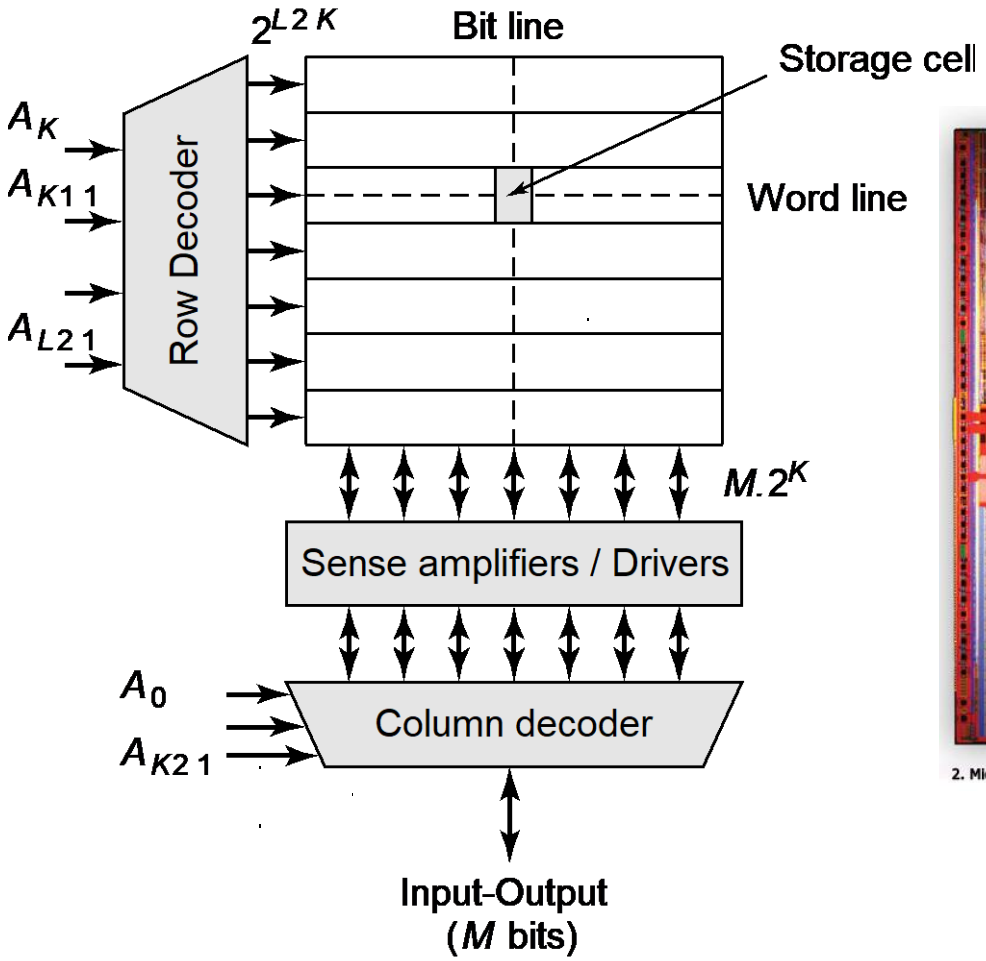


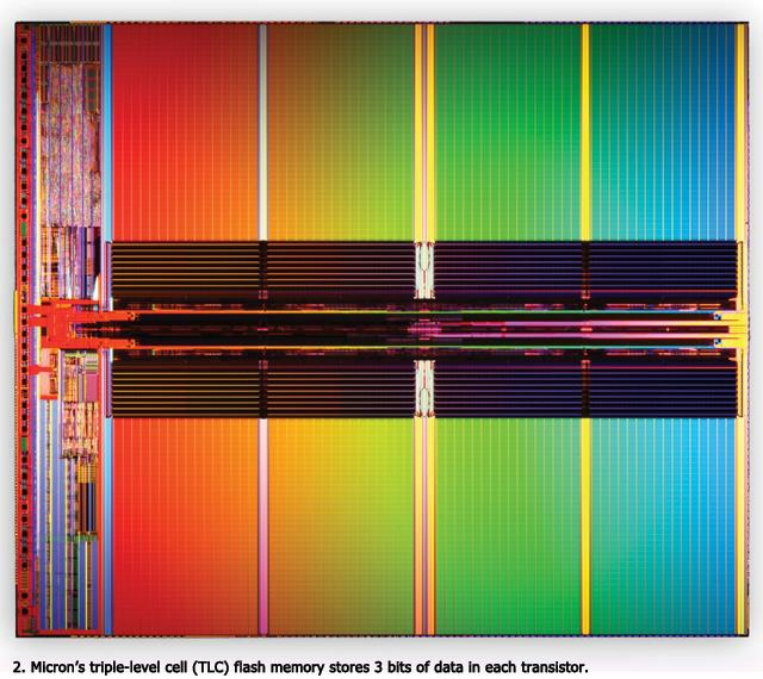
Decoder reduces the number of select signals

$N = log_2 K$

Array-Structured Memory Architecture

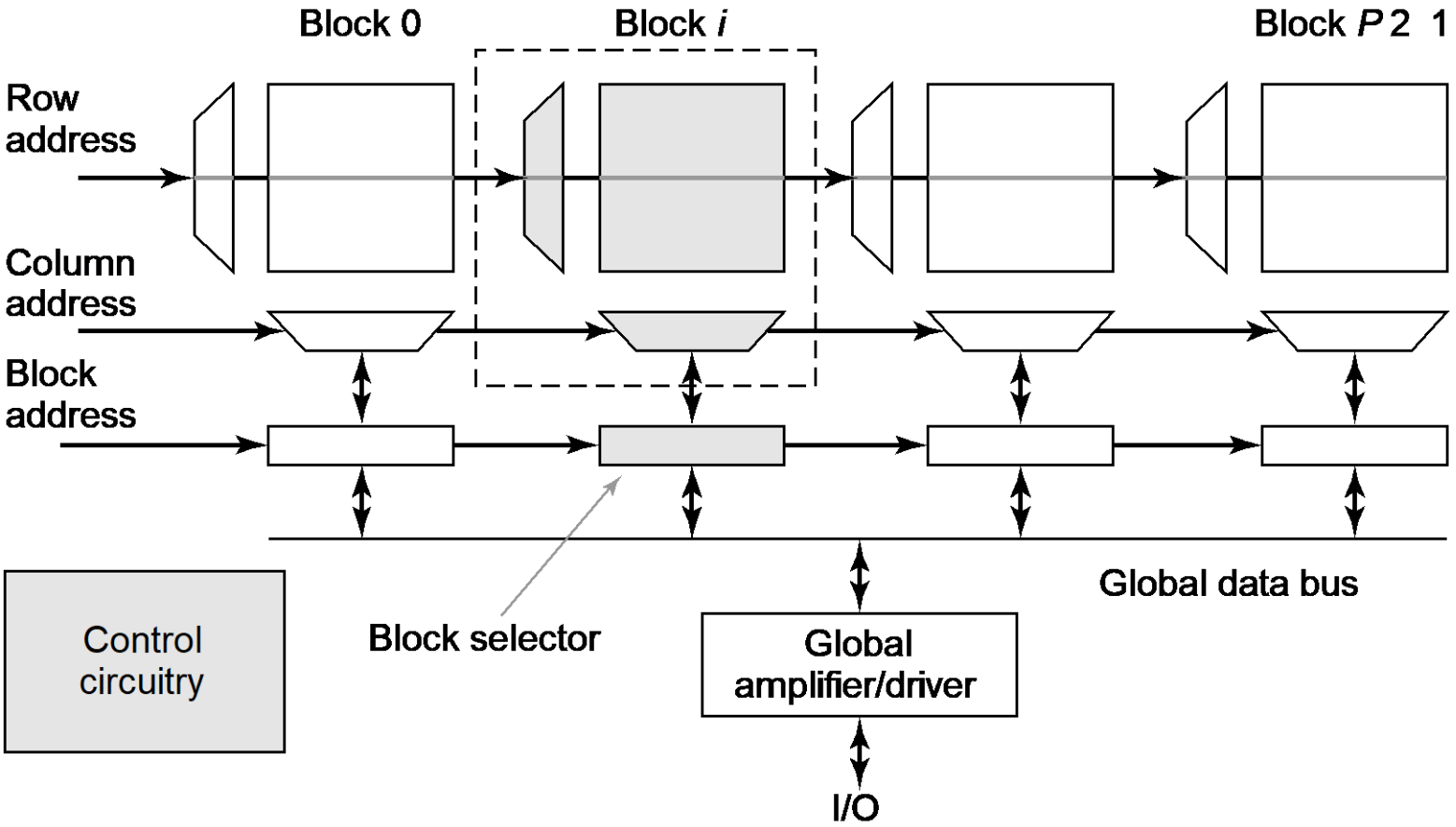
Problem: ASPECT RATIO or HEIGHT >> WIDTH





2. Micron's triple-level cell (TLC) flash memory stores 3 bits of data in each transistor.

Hierarchical Memory Architecture



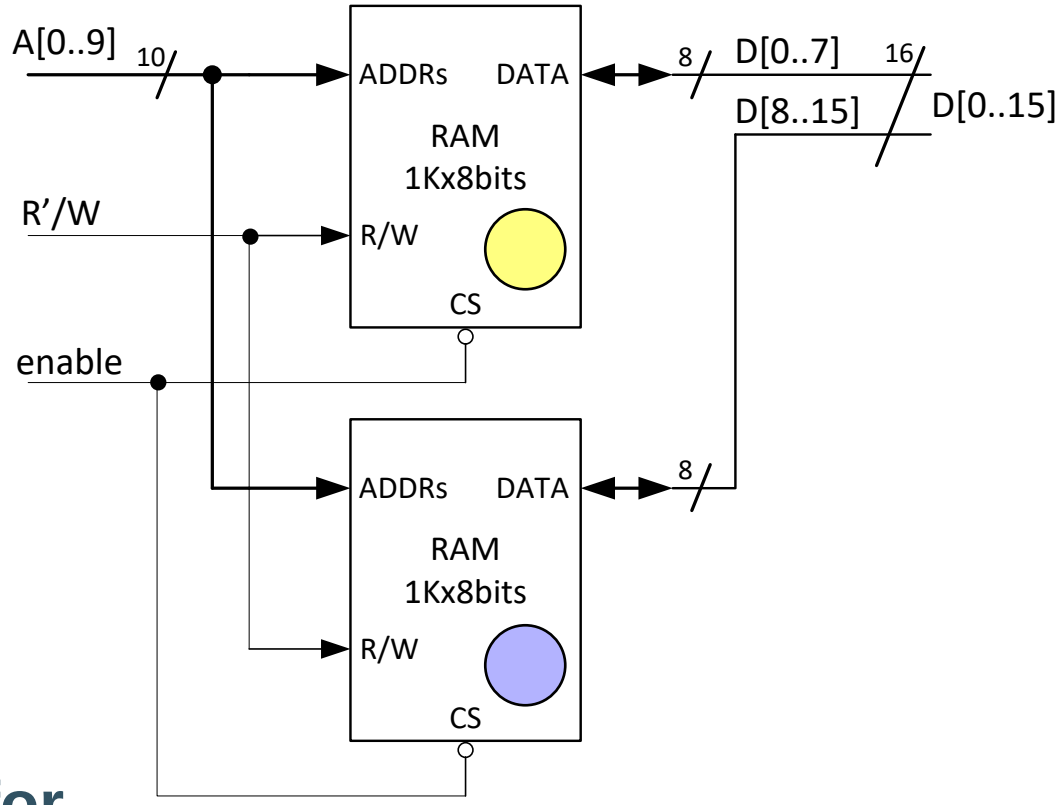
Advantages:

1. Shorter wires within blocks

2. Block address activates only 1 block => power savings

Memory Addressing (parallel)

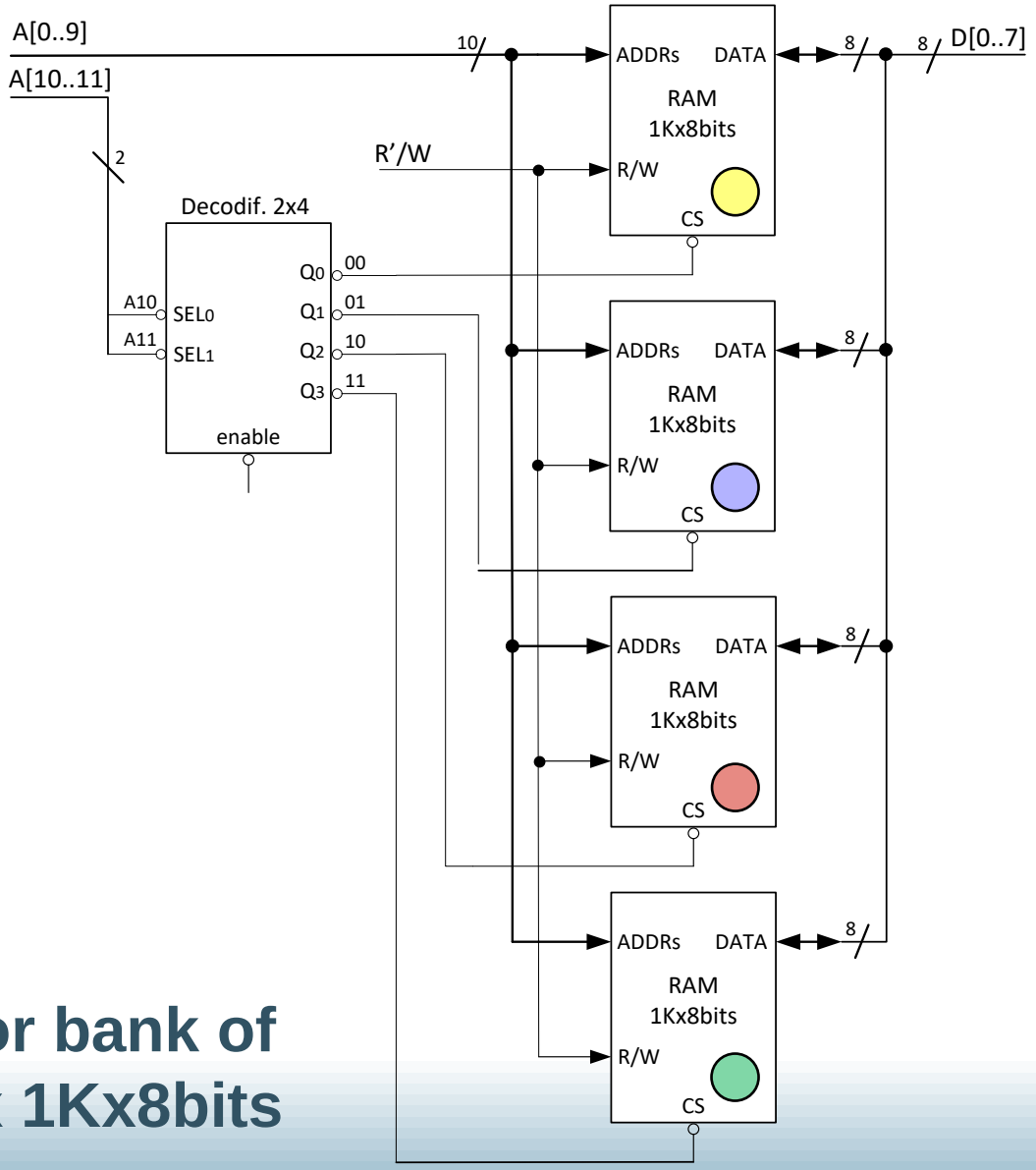
$A_9 \ldots A_0$	$D_{15} \ldots D_8$				$D_7 \ldots D_0$			
0000000000	0	1	.	1	0	.	1	0
0000000001	1	1	.	1	1	.	1	1
0000000010	0	0	.	1	0	.	1	1
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
1111111101	1	1	.	1	0	.	0	1
1111111110	1	1	.	0	0	.	0	0
1111111111	0	0	.	0	1	.	1	1



Example organization for bank of 1Kword x 16 bits from 2 x 1Kx8bits

Memory Addressing (serial)

A_{11} A_{10}	A_9 . . . A_0	D_7 . . . D_0
0 0	0000000000	0 1 1 1 0 0 1 0
		. . . .
0 0	1111111111	0 0 0 1 0 1 1 1
0 1	0000000000	0 1 1 1 0 0 1 0
		. . . .
0 1	1111111111	0 0 0 1 0 1 1 1
1 0	0000000000	0 1 1 1 0 0 1 0
		. . . .
1 0	1111111111	0 0 0 1 0 1 1 1
1 1	0000000000	0 1 1 1 0 0 1 0
		. . . .
1 1	1111111111	0 0 0 1 0 1 1 1



Example organization for bank of 4Kword x 8 bits from 4 x 1Kx8bits

Example: Conventional PC Memory map