Semiconductor Memory Organization & Addressing

Organización de Computadoras 2018

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Introduction

❑ Computer systems functionality aspects

- ▪ Processing
  - – Transformation of data
  - – Implemented using processors

- ▪ Storage
  - – Retention of data
  - – Implemented using memory

- ▪ Communication
  - – Transfer of data between processors and memories
  - – Implemented using buses
  - – Called *interfacing*

A simple bus

Processor (CPU) — Memory

rd'/wr
enable (SC)
addr[0-11]
data[0-7]

Bus structure
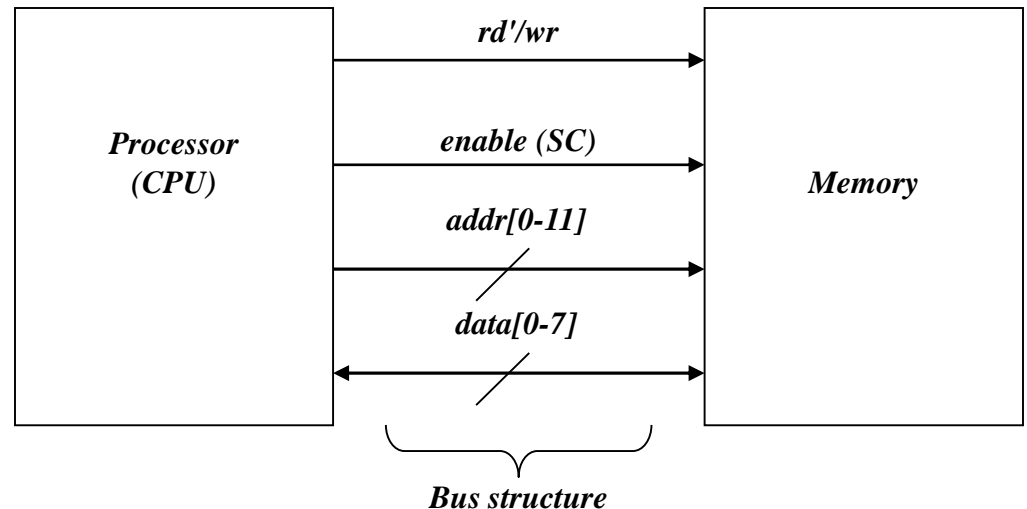
❑ Wires:
- Uni-directional or bi-directional
- One line may represent multiple wires

❑ Bus
- Set of wires with a single function
  - Address bus, data bus
- Or, entire collection of wires
  - Address, data and control
  - Associated protocol: rules for communication

Semiconductor Memory Classification

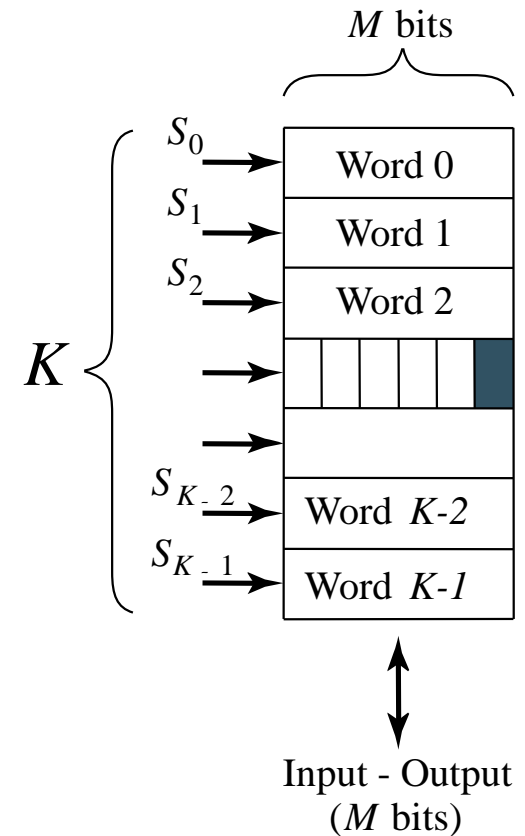| Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	Non-Random Access	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CACHE		

Memory Timing: Definitions
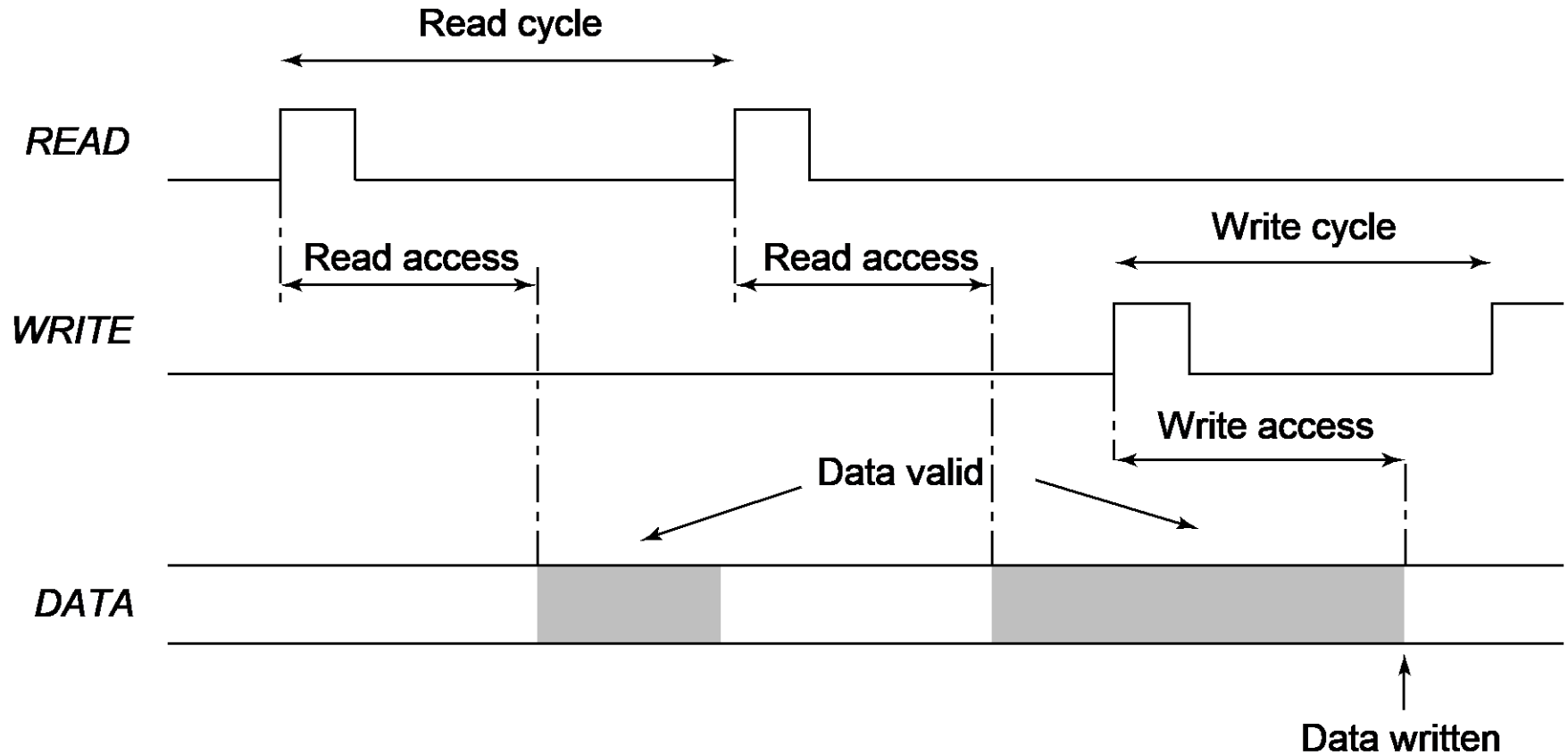
Memory Organization

Memory Adress		Word (8 bits)							
Binary	**Dec**								
0000000000	0	0	1	1	1	0	0	1	0
0000000001	1	1	1	1	1	1	1	1	1
0000000010	2	0	0	0	1	0	0	1	1
		.	.	.	.	.	.	.	.
		.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1111111101	1021	1	1	1	1	0	0	0	1
1111111110	1022	1	1	0	0	0	0	0	0
1111111111	1023	0	0	0	0	1	1	1	1

Addressed word

Storage bit cell

M bits

$S_0 \rightarrow$ Word 0
$S_1 \rightarrow$ Word 1
$S_2 \rightarrow$ Word 2
K
$S_{K-2} \rightarrow$ Word $K-2$
$S_{K-1} \rightarrow$ Word $K-1$

Input - Output (M bits)

Example organization for 1Kword x 8 bits = 8K bits memory

Memory Architecture: Decoders

M bits

S_0 → Word 0
S_1 → Word 1
S_2 → Word 2

K {

Storage cell

S_{K-2} → Word K-2
S_{K-1} → Word K-1

Input - Output
(M bits)

M bits

S_0 → Word 0
→ Word 1
→ Word 2

N {
A_0
A_1
A_{N-1}
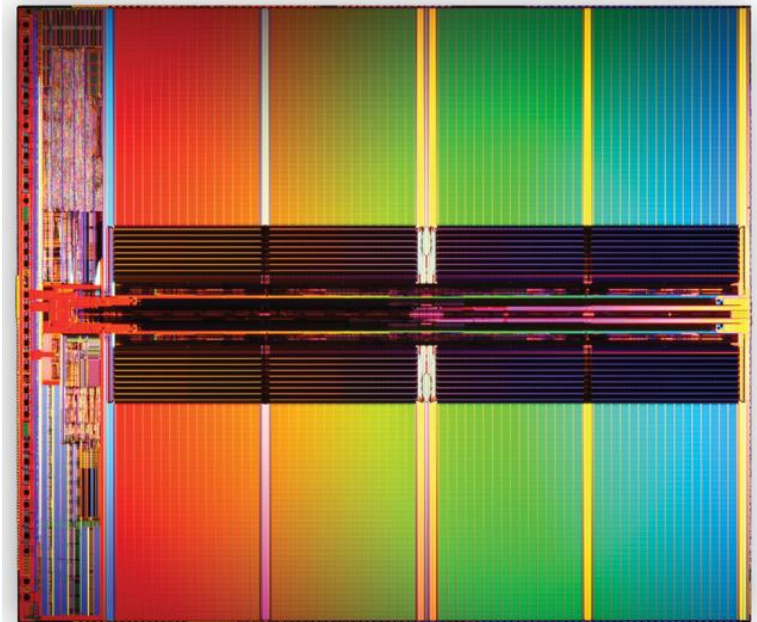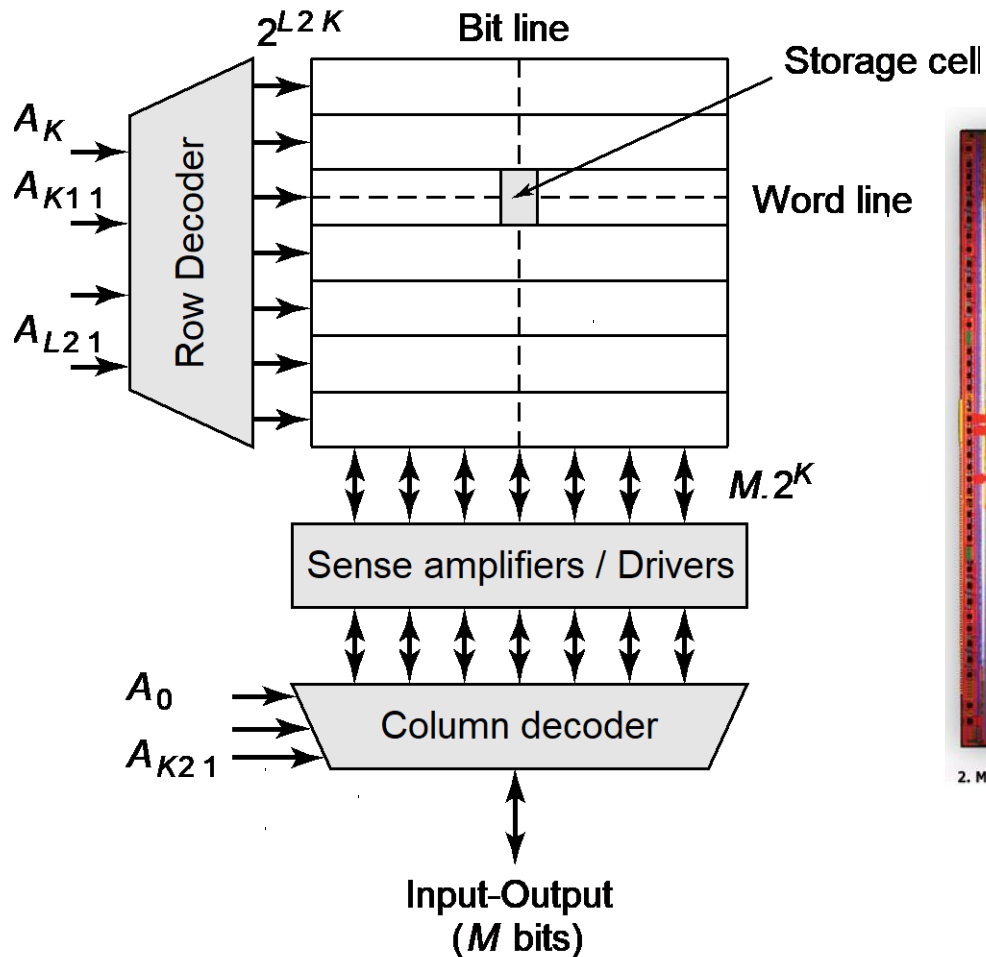
Word K-2
Word K-1

$2^N = K$

Input-Output
(M bits)
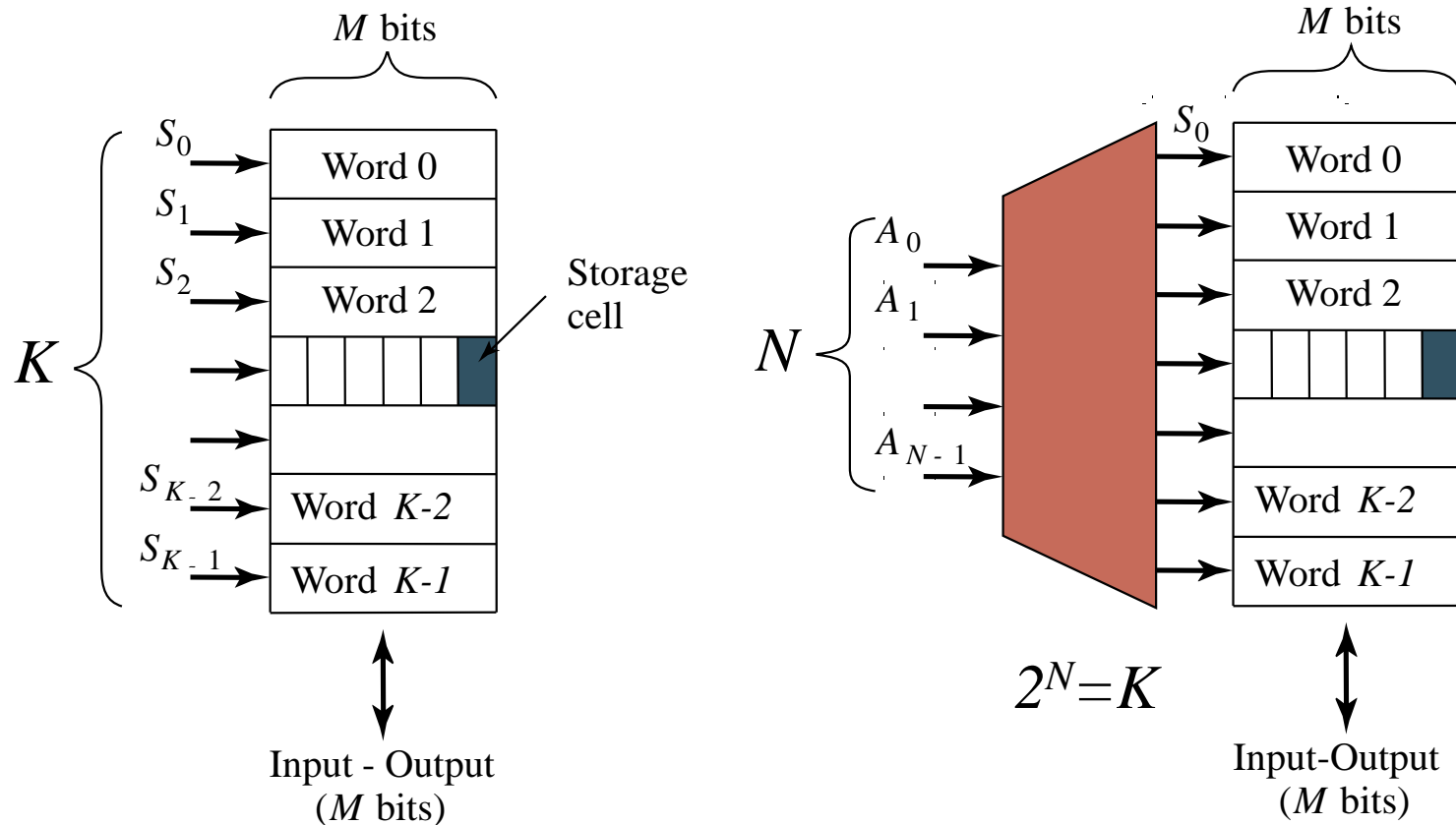
Intuitive architecture for K x M memory
Too many select signals:
K words == K select signals

Decoder reduces the number of select signals
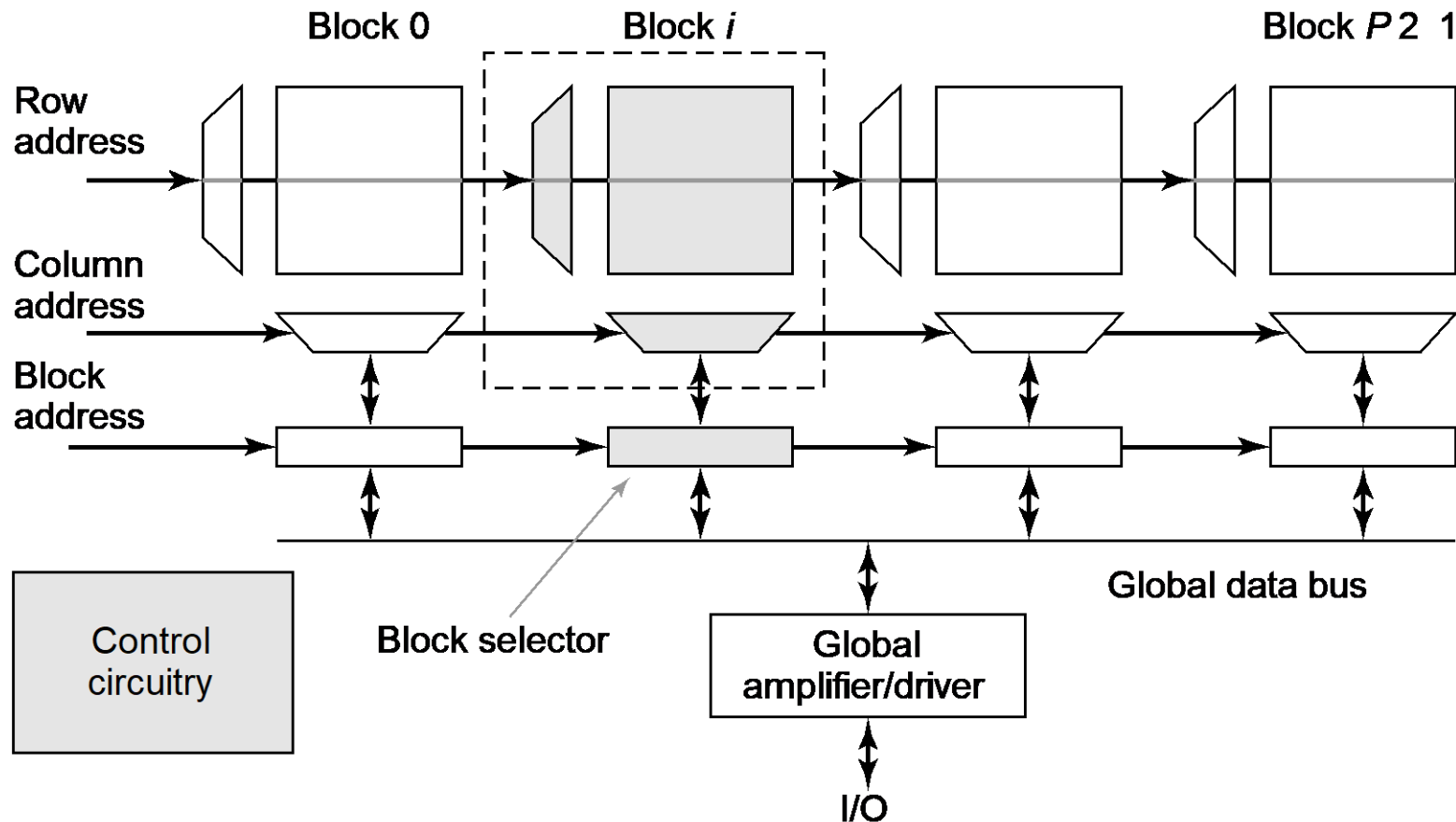$N = log_2 K$

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH

2. Micron's triple-level cell (TLC) flash memory stores 3 bits of data in each transistor.
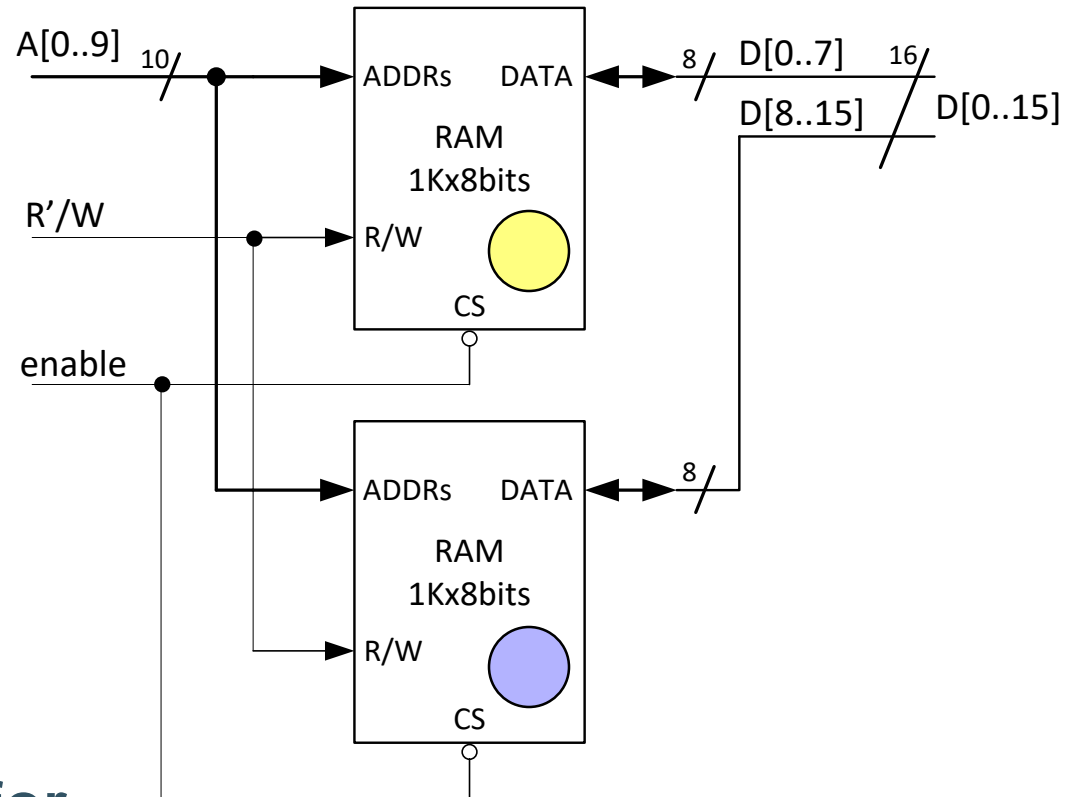
Hierarchical Memory Architecture

Advantages:
1. **Shorter wires within blocks**
2. **Block address activates only 1 block => power savings**

Memory Addressing (parallel)

Example organization for bank of 1Kword x 16 bits from 2 x 1Kx8bits

Memory Addressing (serial)

Example organization for bank of 4Kword x 8 bits from 4 x 1Kx8bits
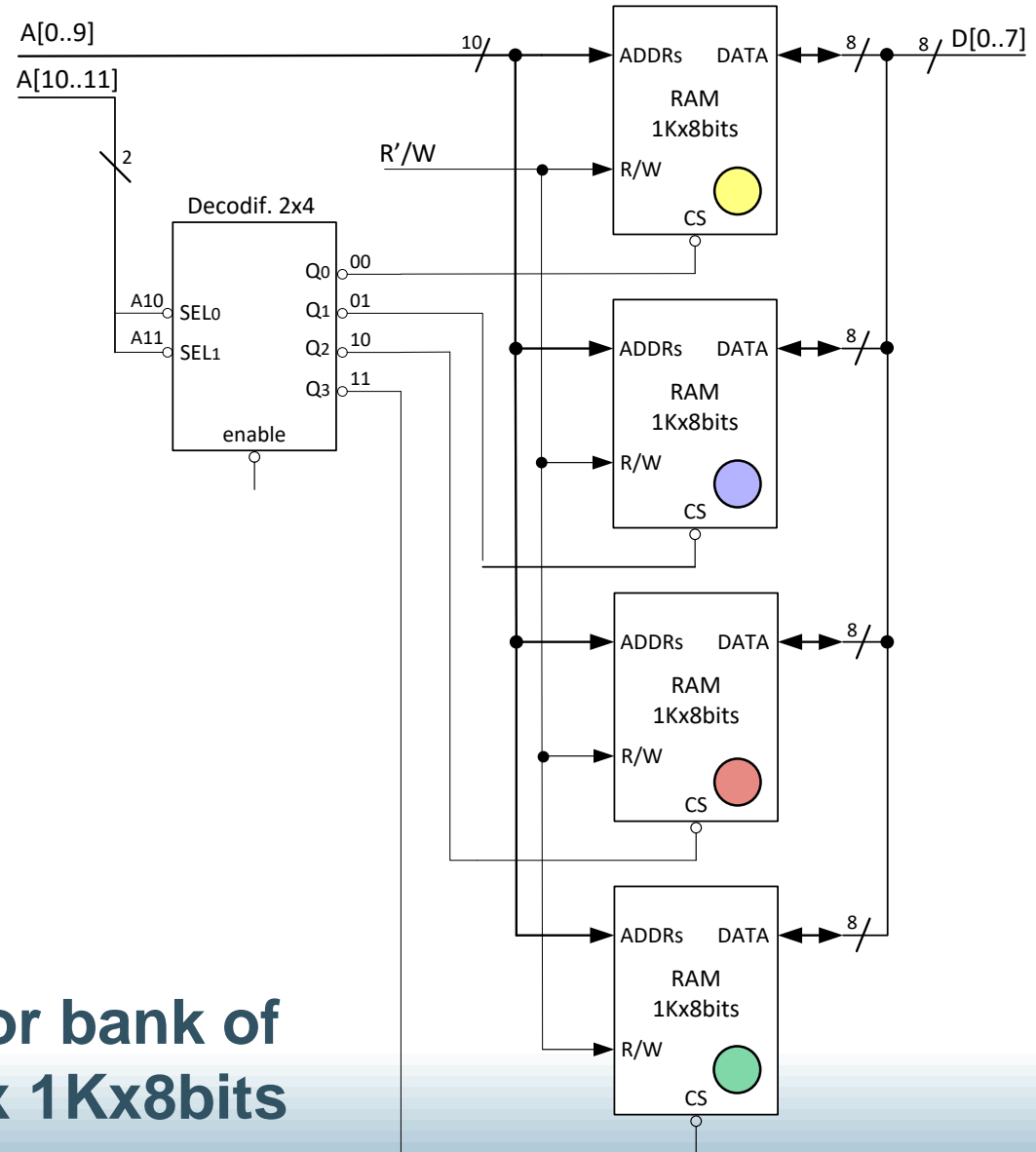
Example: Conventional PC Memory map

Address	Region
0xFFFFFFFF	Interrupt Vector
	(unused)
	Special Funct. Reg.
	Reserved
512M Slot	RAM slot #3
	RAM slot #2
	RAM slot #1
256M	**DRAM**
	RAM slot #0
256M	**DRAM**
0x00000000	Flash (BIOS)