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History of CISC Microprocessor

Intel 4004

- World's first first commercial microprocessor, advertised on November 15, 1971
- 4004 had the first application, a printing calculator called the Busicom 141-PF by manufacturer Nippon Calculating Machine Corp.
- 4-bit 16 pin microprocessor
- Consists of 2300 transistors
- Execute 92,600 instructions/sec and 1,200 calculations/ second
- Addressable memory: 640 bytes

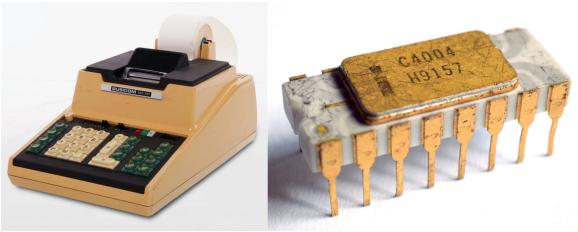

Figure 1: Intel 4004

History of CISC Microprocessor

Intel 8080

- The 8080 is a complete 8-bit parallel, central processor unit (CPU)
- It is a 40 pin processor
- It has 8-bit Data Bus and 16-bit address bus
- Addressable memory: 64 KB
- Consistes of 4,500 transistors

Intel 8085

- It is a 8-bit processor
- It is a 40 pin processor
- It has 8-bit Data Bus and 16-bit address bus
- Addressable memory: $2^16 = 64$ KB
- Consistes of 6200 transistors
- It has 8-bit input/output address lines to address $2^8 = 256$ input and output ports.

History of CISC Microprocessor

Intel 8086

- The 8086 is a 16-bit microprocessor. The term "16-bit" means that its arithmetic logic unit, internal registers and most of its instructions are designed to work with 16-bit binary words.
- It has a 16-bit data bus, and 20-bit address bus, so it can directly access $2^20 = 1MB$ memory locations. Each of the 1 MB memory locations is byte , means a sixteen-bit words are stored in two consecutive memory locations.
- It supports pipelining.
- Consistes of 29000 transistors

Intel 80186, 80286

- It is a 16-bit processor
- It has 16-bit Data Bus and 20/24-bit address bus
- Addressable memory: $2^24 = 16$ MB physical memory and 1 GB of virtual memory by using memory management system
- Consists of 55,000/13400 transistors

History of CISC Microprocessor

Intel 80386

- It is an advanced 32-bit microprocessor optimized for multitasking operating systems .
- It has a data and address bus of 32-bit each. Thus has the ability to address $2^32= 4$ GB of physical memory and and $2^46=64$ TB of virtual memory
- The on-chip memory-management facilities include
  -
  - Address translation registers
  - Advanced multitasking hardware
  - Protection mechanism
  - Paged virtual memory
- Consists of 275000 transistors

History of CISC Microprocessor

Intel Pentium

- It is an advanced superscalar 32-bit microprocessor
- It has a 64-bit data bus and a 32-bit address bus that offers 4 GB of physical memory space.
- Separate data and instruction caches: 8 KB for instruction and 8KB for data
- It has dual integer processors, means it can execute two instructions, which are not dependent on each other, simultaneously because it contains two independent internal integer processors called superscaler technology, allows the Pentium to often execute two instructions per clocking period.
- It introduced jump prediction technology that speeds the execution of program loops.
- It employs an internal floating-point coprocessor to handle floating-point data, albeit at a five times speed improvement.
- Consists of around 3.1 million transistors

History of CISC Microprocessor

Intel® Core™ i9-13900KS Processor

- It is an 64-bit microprocessor
- 24 cores
- total number of Performance-cores: 8
- total number of Efficient -cores: 16
- Total threads: 32
- It has 36 MB Intel Smart Cache. CPU Cache is an area of fast memory located on the processor. Intel® Smart Cache refers to the architecture that allows all cores to dynamically share access to the last level cache.
- L2 Cache: 32 MB
- GPU: Intel® UHD Graphics 770
- Instruction set: 64 bits
- Consists of around 25.9 Billion transistors

History of CISC Microprocessor

Features	**Intel 4004**	12^{th} **Generation Intel Core Processor Family**
Number of Transistors	2300	Billions
How many bits processor	4 bits	64 bits
Number of Pins	16 -pin dual-in-line on a package	1700 pin on a single socket
Frequency	750 Hz	Upto 5.2 GHz
Number of Cores	1	Upto 16 (8 Performance-Cores, 8 Efficient-Cores)
Addressable Memory	640 Bytes	256 GB

History of RISC Microprocessor

Three research projects:

- The first RISC projects came from IBM, Stanford, and UC-Berkeley in the late 70s and early 80s.
  IBM 801: not widely known or discussed Berkeley RISC processor UC Berkeley worked with DARPA two machine: RISC I and RISC II : Stanford MIPS processor under DARPA project to design a single chip simple machine within university : MIPS R200 1986, computer industry began to announce production 32 bit system based RISC architecture Sun microsystem SPARC 1987 derivative of Berkeley RISC II

History of RISC microprocessor

- Three research projects
  - IBM 801: not widely known or discussed
  - Berkeley RISC processor
    - UC Berkeley worked with DARPA
    - two machine: RISC I and RISC II

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  - Stanford MIPS processor
    - under DARPA
    - project to design a single chip simple machine within university

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  - MIPS R200
    - 1986, computer industry began to announce production
    - 32 bit system based RISC architecture
  - Sun microsystem SPARC
    - 1987
    - derivative of Berkeley RISC II

History of RISC microprocessor

- ARMv9: Cortex A 64 bit processor
- RISC -V 64, 128 bits

RISC vs CISC

- RISC (Reduced Instruction Set Computer), which focuses on having simple, fixed-size instructions that can execute in a clock cycle
- CISC (Complex Instruction Set Computer), which has instructions of different sizes that perform multiple operations and that can execute for more than a single clock cycle.

RISC vs CISC

- RISC architectures require memory access to be performed through either a load (copy from memory) or a store instruction
- CISC architectures may have a single instruction to access memory and, for example, perform some arithmetic operation on its contents.

RISC vs CISC

- RISC processors have a reduced number of instruction classes. These classes provide simple operations that can each execute in a single cycle. The compiler or programmer synthesizes complicated operations (for example, a divide operation) by combining several simple instructions. Each instruction is a fixed length to allow the pipeline to fetch future instructions before decoding the current instruction.
- CISC processors the instructions are often of variable size and take many cycles to execute.

RISC vs CISC

- RISC processors have a large general-purpose register set. Any register can contain either data or an address..
- CISC processors have dedicated registers for specific purposes.

RISC vs CISC

- RISC processor operates on data held in registers. Separate load and store instructions transfer data between the register bank and external memory
- CISC processors design the data processing operations can act on memory directly.
- Memory accesses are costly, so separating memory accesses from data processing provides an advantage because you can use data items held in the register bank multiple times without needing multiple memory accesses.

RISC vs CISC

- Multiplying Two Numbers in Memory: one stored in location 2:3 and another stored in location 5:2 - and then store the product back in the location 2:3.

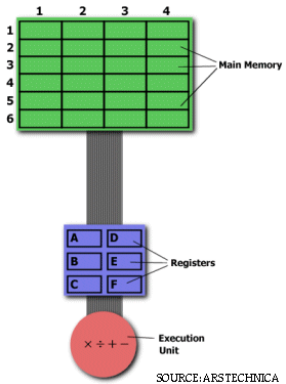

Figure 2

- For CISC: **MULT 2:3, 5:2**
  - One of the primary advantages is that the compiler has to do very little work to translate a high-level language statement into assembly.
  - Because the length of the code is relatively short, very little RAM is required to store instructions.
  - The emphasis is put on building complex instructions directly into the hardware.
- For RISC: **LOAD A, 2:3 ; LOAD B, 5:2 ; PROD A, B ; STORE 2:3, A**
  - Because there are more lines of code, more RAM is needed to store the assembly level instructions.
  - The compiler must also perform more work to convert a high-level language statement into code of this form.