Prototyping Silicon Detectors for the FAZIA and the LAMPS Experiments

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Presenter:
Phil Yoon, PhD
Research Professor
Korea University

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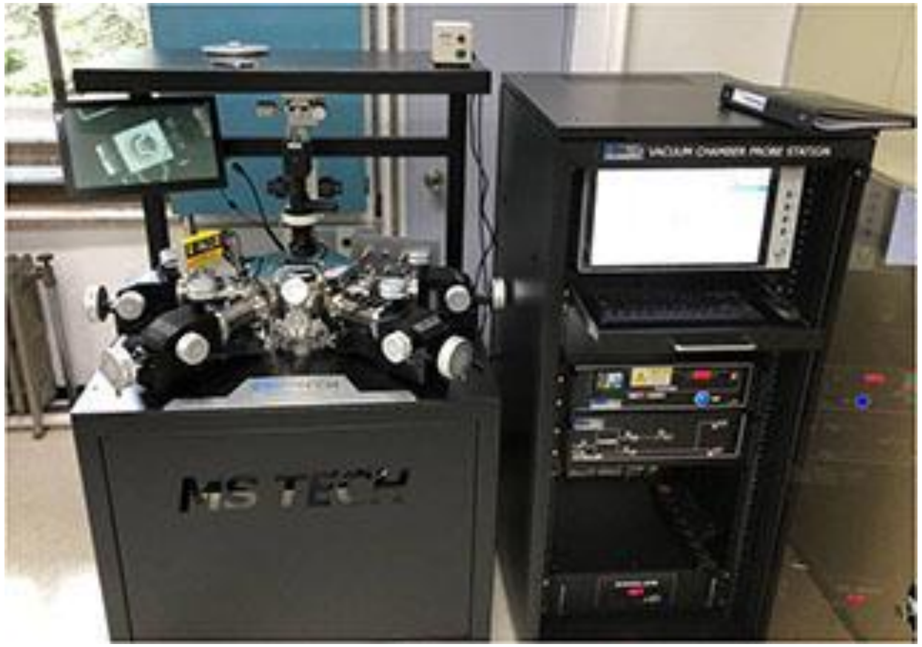
Research Capability and Vision

01 Introduction to the University Facility

- Laboratory for Semiconductor-based Detectors (LSD) is under preparation at Korea University.
- Sep. 2020: (Class-100) Clean Booth installed.
- Dec. 2020: In-vacuum probe station with a wide range of temperature variation.

  high-voltage DC sweep, in-vacuum (10^{-3} ~ 10^{-5} torr) characterization under temperature-varying environment.
- Dec. 2020: HV Parameter Analyzer system installed.

  → enabling J-V/C-V measurements and follow-up extraction of full semiconductor parameters.



02 Key Accomplishments of the Project Scientist

- International patent granted under the patent cooperation treaty (PCT): **WO 2012/138792**

  Annular-array Type Beam-Position Monitor with Sub-Micron Resolution and a Parametric Method for Optimizing Photo-Detectors.

- Relevant journal publications:

  (1) **Scientific Reports 8, 15926 (2018)**

  Customisable X-ray fluorescence photodetector with submicron sensitivity using a ring array of silicon p-i-n diodes.

  (2) **JINST 8 P06005 (2013)**

  A photometric Approach to Parametric Modelling for Optimising Multisegmented Photodetector Rings.

- Technology transfer and commercialization is underway under the auspice of the US Department of Energy.

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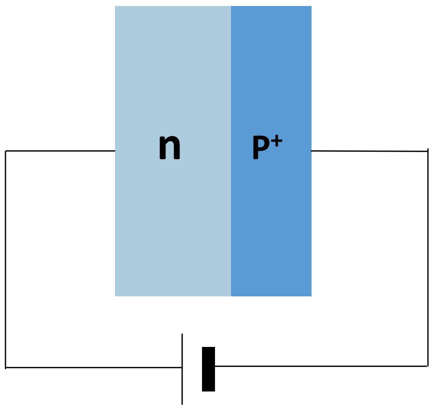
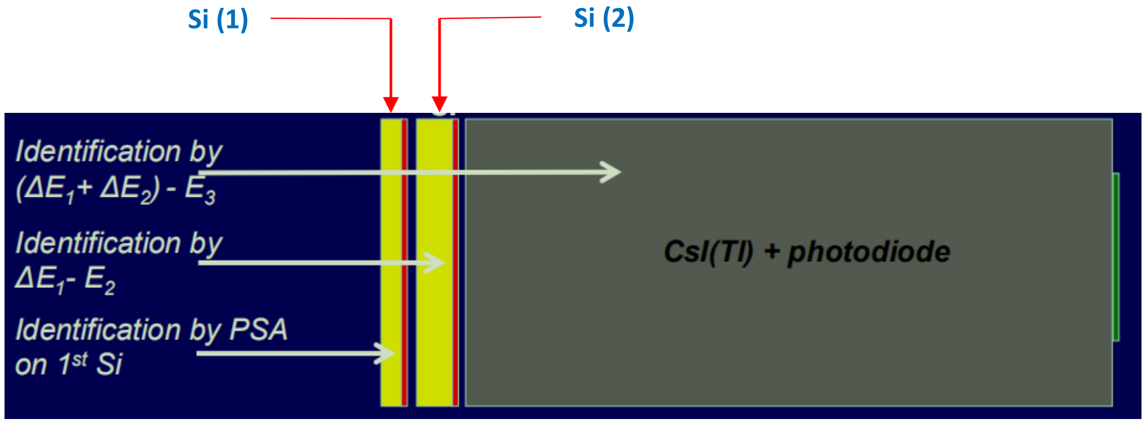
Technology Merits

01 Detector Overview





- Each two-stage (Si-Si) telescope comprises thin/thick Si detectors and a slab of CsI(Tl) scintillator. In order to identify heavy ions and nuclear fragments emerging from collisions of proton beams and the target, a tandem of thin (Si(1)) and thick (Si(2)) Si pads are positioned in front of the CsI(Tl) scintillator within the telescope.

- *Depletion volume* and *mass/charge resolutions* of the (p^+)n-junction Si detector can be determined by applying DC reverse bias.

- Conventional ΔE-E method and the Pulse-Shape Analysis (PSA) method are to be employed.

02 Technology Maturity

- The FAZIA (Four ∏ Z and A identification Array) collaboration led by INFN/Italy and CNRS/France had successfully developed Si energy-residual detectors in partnership with Si-processing companies. The first phase of the heavy-ion experiments were conducted in Italy and in France and came to end.
- The aftermath of COVID-19 halted research efforts at developing Si detectors throughout Europe.
- Presently, the second phase of experiments with upgraded Si detectors are under plan.
- Two types of Si detectors under design: **ultra-thin** (**150 microns)** and **thick** (**1000 microns)** pads.
- Korea University is currently spearheading the R&D endeavor on upgrading Si detectors in partnership with NINT (National Institute for Nanomaterials Technology)/POSTECH for the next experiments.
- The custom-design Si detectors are to be developed in full spectrum that includes layout design, processing, and prototyping.
- Making the most of the NINT facility--with an array of specialized processing equipment—will enable us to develop our own recipes for fabricating *low-noise Si sensors* with optimized processing.
- The Phase-0 is slated for Sep. 2020.

03 Technology Merits

Goal:

- Achieving or surpassing the mass/charge resolutions that the European collaboration had demonstrated through the first phase of the heavy-ion physics experiments.

How to Achieve the Goal:

- Developing methods of a dozen of Si processing in full spectrum with the aid of modeling and simulation.
- Designing ultralow-noise versions of the Si detectors.

- Devising our own recipes for Si processing.
- Suppressing leakage currents.
- Maximizing the signal-to-noise ratio (SNR) of the detector.
- In partnership with the nanoFab, we can realize the new ideas and processing technology for the Si detectors.

04 Marketability of the Technology

- Semiconductor detector market is growing at a faster pace with substantial growth rates worldwide.
- Global market by geography:

North America	Europe	Asia and Oceanic Countries
U.S.	UK	Japan
Canada	Germany	Australia
	France	
	Switzerland	
	Norway	

- Key Heavy-Ion Nuclear Physics Experiments worldwide:
  - IBS (Institute of Basic Science)/Korea: RAON/Large Acceptance MultiPurpose Spectrometer (LAMPS).
  - GANIL/France: FAZIA (4Π A and Z Identification Array) collaboration.
  - US Michigan State University: FRIB (Facility for Rare Isotope Beam) experiments.
  - CERN: ISOLDE (Isotope mass Separator On-Line facility) experiments.
  - Heavy-ion physics experiments are being planned in Russia and Poland.

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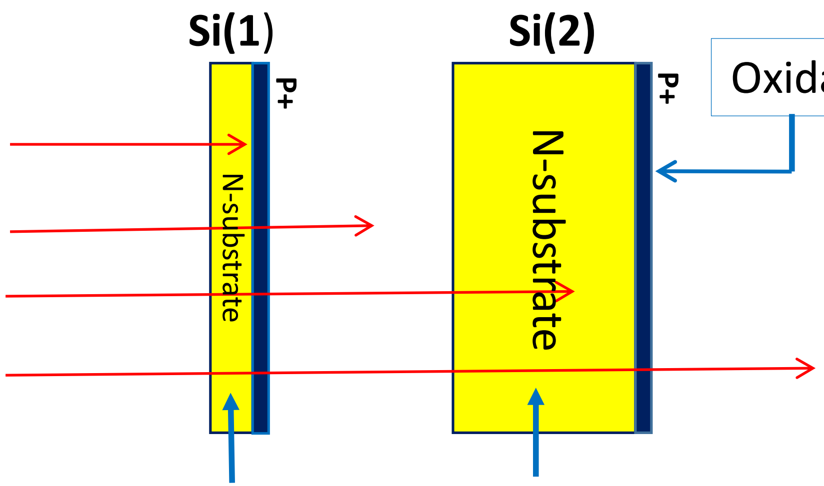
Eligibility for Grant Proposal

01 Overview of Prototyping

- The aftermath of COVID-10 halted most of the semiconductor foundries and processing facilities worldwide.
- Presently, the local nanoFab that we are partnering with is fully operational. Thus, the facility can carry out by itself a stream of complex and delicate processes on the Si wafers.

- **Phase-0**: Preparation phase; test run of the Si processing using test-grade bare wafers.
- **Phase-I:** Reverse engineering of Si pads produced by the FAZIA collaboration at the national facility.
- **Phase-II**: Enhancing the performance of the Si detectors. As a result, independent recipes for developing detectors are created.

not to scale



Oxidation, doping, metallization on the p^+n-junction side of the Si wafers.

Proton beams sourced from the linear accelerator are set on course to make collisions with a target. As a result, heavy ions and nuclear fragments are produced. Subsequently, those fragments traversing two-stage Si pads lose energy (ΔE) via ionization. And analyzing ΔE registered at each Si pad allows us to identify various kinds of heavy ions and isotopes under study.

Ultrathin type: 150 microns (20mm x 20mm x 0.150mm)

Ultrathick type: 1000 microns (20mm x 20mm x 1mm)

02 Production and Development Cost and Time

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Si-Processing WorkFlow

1. wafer cleaning
2. oxidation
3. Doping
4. Thermal Treatments
5. Photolithography (I)
6. Al Metallization
7. Photolithography (II)
8. Al Metallization
9. Passivation
10. Photolithography (III)
11. Dicing
12. wafer thinning
13. oxidation
14. Al Metallization
15. packaging

Electronic readout circuit

- **3 ~ 5 weeks** to complete the entire cycle of processing.
- Phase-0, Phase-1, and Phase-2: **3 ~ 4 months** for each phase.
- Estimated processing cost: ~ USD 37,500
- Design and fabrication of associated readout circuits: ~ USD 5000
- Total sum: USD 42,500

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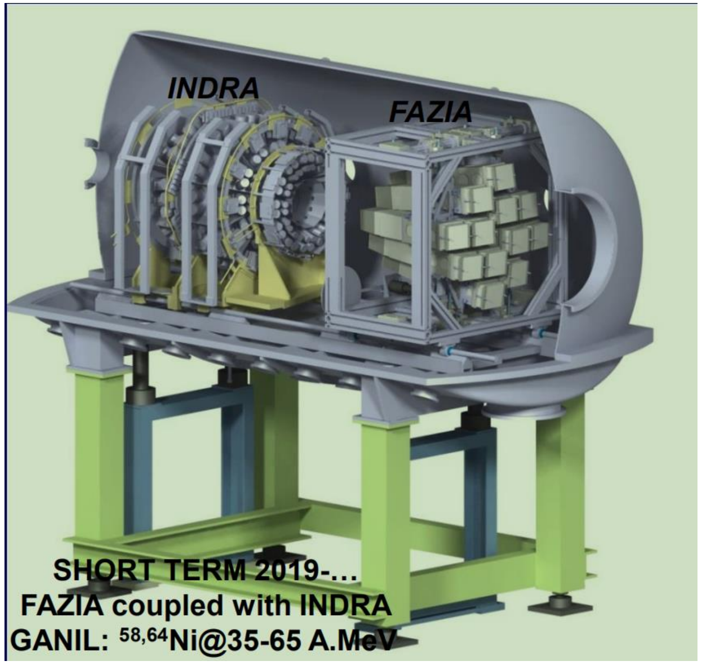
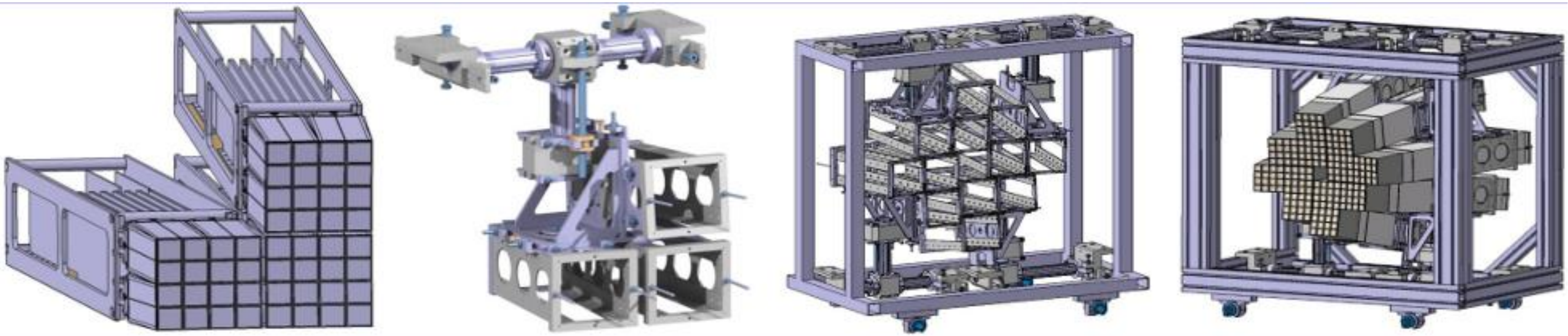
Future Prospects

01 Application of Prototype Detectors



- A total of 1 000 Si chips will be employed at the next round of FAZIA experiments at GANIL/France after a successful round of prototyping by Korea University.
- In addition, 500 ~ 1 000 units of Si detectors are in demand for making ready the low-energy LAMPS experiments at RAON/Korea.

Graphic courtesy of the FAZIA collaboration



Thank you for Watching!