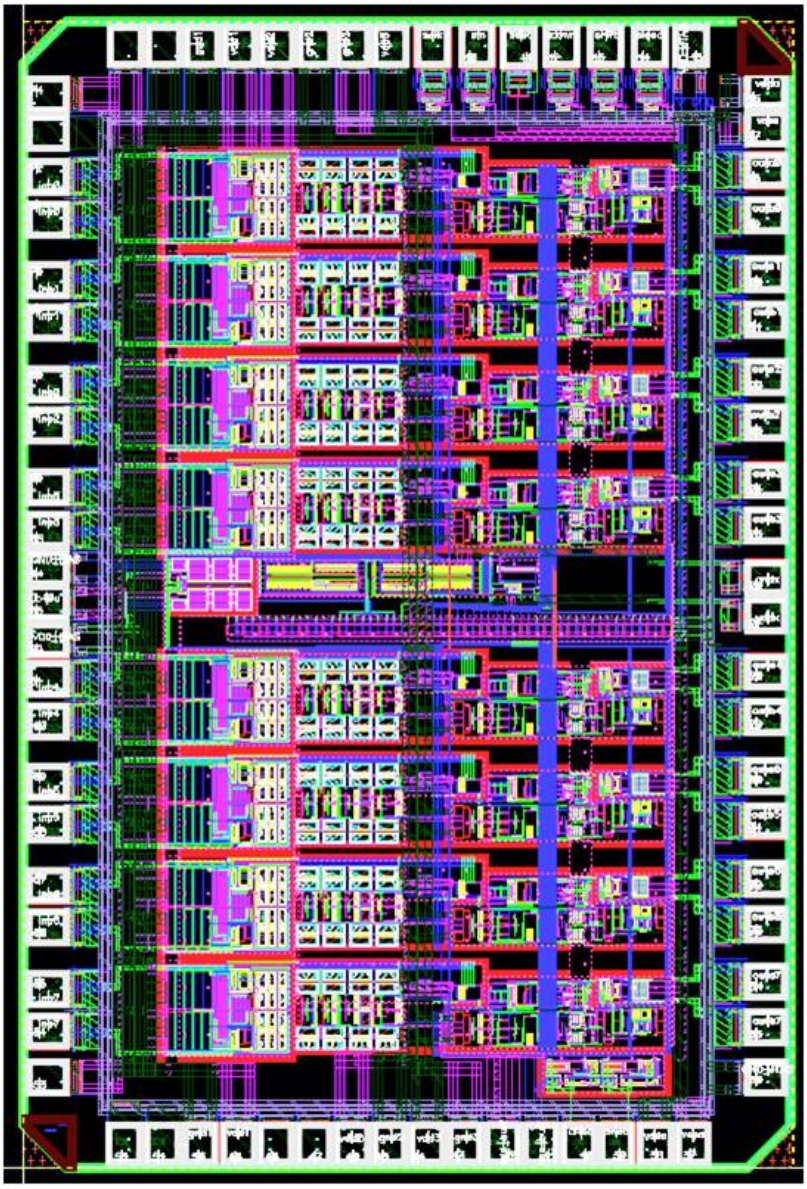
MDT ASD2 User Manual



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Sergey Abovyan[+], Andrea Baschirotto[*], Varuzhan Danielyan[+], Markus Fras[+], Oliver Kortner[+], Sandra Kortner[+], Hubert Kroha[+], Marcello De Matteis[*], Federica Resta[*], Robert Richter[+], Yazhou Zhao[+]

[*]) University of Milano-Bicocca [+]) Max-Planck-Institut for Physics, Munich

Contacts: Marcello de Matteis, marcello.dematteis@unimib.it, Robert Richter, richterr@mpg.mpp.de

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1 Introduction

1.1 MDT system overview

1.1.1 The MDT precision tracking Chambers

The Monitored Drift Tube (MDT) spectrometer represents the outermost shell of the ATLAS experiment at the LHC collider at CERN. It is segmented in 1084 rectangular and trapezoidal chambers made out of 370000 drift tubes and covers an area of about 5500 m^2. Shape and size of the chambers follow the projective geometry of the spectrometer and contain between 192 and 432 individual tubes. The early concept of the Muon Spectrometer is described in the TDR from 1997 [1], while an up-to-date description of the present ATLAS detector and of MDT readout electronics is given in [2] and [3], respectively. The LHC collider will go into a new mode of high-luminosity operation in 2025, providing about 7 times higher luminosity ("Phase-II"). The corresponding higher particle rates require the complete replacement of the MDT readout electronics. A detailed description of this upgrade is presented in sect. 6.4 of [4].

The MDT chamber design is optimized for precision tracking. The MDT tubes are pressurized at 3 bar to reduce diffusion effects and increase the rate of primary electrons, while the position of each chamber inside the spectrometer – crucial for the accuracy of momentum measurement - is monitored by an optical alignment system. The main operating parameters of the MDT are summarized in Table 1.

A schematic diagram of the MDT tube supplies and readout is given in Figure 1, where HV supplies are located at the right and components for signal readout on the left. On the right side, the wire is terminated with the tube impedance of 380 Ω in order to avoid signal reflection. On the readout side, signals from 24 tubes are collected by a passive distribution board ("Hedgehog board") and channeled to a readout board ("mezzanine card"), containing three Amplifier/Shaper/Discriminator (ASD) chips, a single 24-channel TDC and control circuitry.

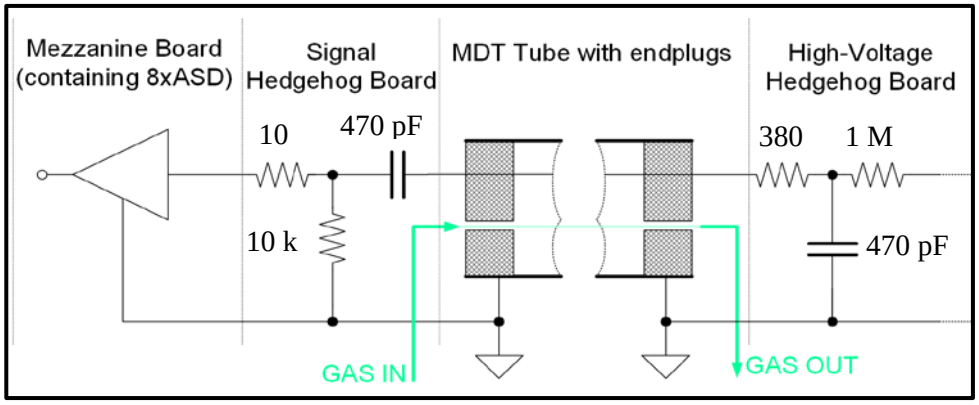


Figure 1 - Interface of the ASD with the MDT tube.

A single MDT chamber may have up to 432 drift tubes, serviced by 18 hedgehog/mezzanine board sets. Data are read out from each TDC via a 80 Mbit/s serial link[1] to a Chamber Service Module (CSM), multiplexing the (up to) 18 serial links into an optical fiber for transmission to the ATLAS DAQ.

A daisy-chain JTAG bus permits downloading of parameters to ASDs and TDCs. Each multilayer (3 or 4 tube layers) is shielded at both ends by a Faraday Cage. All AC signals exchanged with the CSM are low-level differential signals (lvds), while DC supplies are distributed from the CSM to each mezzanine board. MDT chambers are electrically isolated from support structures and (metallic) gas services, being grounded to a single common ground point to avoid ground loops. DC power supplies are "floating", i.e. their grounds are not connected among each other or to any other ground (e.g. safety ground).

While MDT tubes with a diameter of 30 mm are used in the largest part of the Muon detector, a special MDT type with half-diameter tubes is used in regions of high particle rates ("sMDT"). The smaller diameter leads to shorter drift time and lower acceptance for background hits (caused by converted γ's and neutrons), improving hit efficiency and accuracy at high rates. Details about the sMDT are given in [4] and [5]. Table 2 contains numbers for the main components of the MDT readout system.

[1] In the upgraded version of the readout electronics, the bandwidth of this link will be increased to 320 Mbit/s [4].

1.1.2 Characteristics of the MDT tube signals

An ionizing track crossing a MDT tube generates a string of primary electrons which subsequently drift towards the central anode wire, see Figure 2. Depending on the distance of the track from the wire, the drift time may extend up to 750 ns, leading to a sequence of signals at the input of the amplifier of corresponding duration. Depending on the spatial distribution of primary electron clusters along the path of the track, described by Poisson and Landau statistics, more than one crossing of the discriminator threshold may occur due to one single track, while only the first crossing (corresponding to the electrons closest to the wire) is relevant for the determination of the track-to-wire distance. Subsequent crossings do not contain useful information and lead to an unwanted increase of data flow and the corresponding load to the DAQ. To retain all but the first threshold crossing, a veto for the discriminator has been installed, the length of which can be programmed in the range of about 150 to 750 ns.

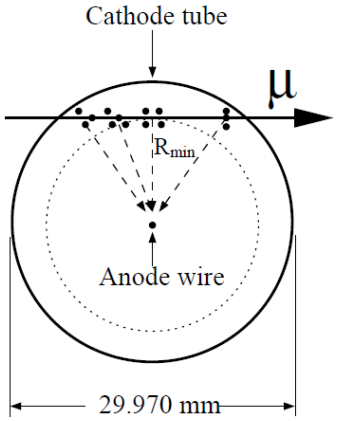


Figure 2 - The primary electrons at R_{min}, closest to the wire, determine the drift time measurement.

Table 1 - Operating parameters of MDT chambers with large and small tubes.

Parameter	Large tubes	Small tubes
Length	From 1.5 to 6 m	1.5 to 2.50 m
Diameter	30 mm	15 mm
Wire diameter	50 μm	idem
Wire resistance	44 Ω / m	idem
Impedance (Z_0)	380 Ω	340 Ω
Termination	380 Ω in series with 470 pF	340 Ω w. 470 pF
AC coupling capacitor	470 pF	idem
Drift gas	Ar/CO_2 (93%/7%)	idem
Maximum hit rate	500 Hz/cm^2	30 kHz/cm^2
Nominal operating voltage	3090 V	2730 V
Electron avg. drift velocity	20 μm/ns	42 μm/ns
Maximum drift time	750 ns	180 ns

1.1.3 On-chamber readout electronics

The ASD2 chip has been designed as a replacement of the ASD1, the amplifier which is currently used for the readout of the MDT ASD1 [12]. Architecture and functional structure of the ASD2 was adopted from the ASD1. Design aim was to match or exceed function and performance of ASD1, in particular the specifications for the analog performance as given in Table 3.

Table 2 - Component numbers in the MDT Readout for 30 mm and 15 mm tube chamber in Phase-II.

	Large tubes	Small tubes	Total
MDT Chambers	958	126	1.084
Tubes	305.952	63.514	369.466
ASDs	38.244	8.106	46.350
Mezz. cards	12.748	2.702	15.450
CSMs	958	240	1.198

The ASD1 was designed in the – now unavailable - Agilent 500 nm technology. For the design of ASD2, the 130 nm process by IBM (later Global Foundries) was selected. Due to progress in chip technology and process control, the design resulted in an improvement of several operational parameters, like risetime, gain, noise and threshold matching. The new design also allowed to correct a few minor bugs, discovered in ASD1. Performance measurements of the final chip are presented in section 3.

1.2 Performance requirements of the Front end electronics

For an accurate measurement of the drift time, the design of the ASD must address a number of critical requirements:

- With a gas gain of about 2×10^4, the expected average signal is 1500 electrons (0.25 fC) per primary electron. The standard trigger threshold is 5 primary electrons, equal to 1.25 fC at the input of the ASD. The noise contribution from the frontend should not exceed 1500 electrons. The frontend noise is depending on the performance of active elements in the ASD, but also by passive components in the MDT, like the terminating resistor and the total capacitive load of the tube.
- Due to high signal rates in a number of MDT chambers (up to 400 kHz/tube), bipolar shaping is chosen to avoid deterioration of efficiency due to baseline fluctuations.
- The channel to channel crosstalk is specified to be less than 1%.
- A pre-amp peak time of <15 ns is specified to minimize time slewing effects due to pulse height variations.
- To further reduce the error due to pulse height variations, an ADC is implemented in each of the 8 channels to measure the signal charge following the initial threshold crossing. The signal charge is encoded into the pulse width using the dual-slope "Wilkinson" technique (see section 2.4.7). This charge information allows to improve the accuracy of the time measurement by a charge dependent correction [8][9], thus improving the spatial resolution of the detector. The charge information is also used to monitor gas amplification and for other diagnostic purposes.
- Two modes of operation are provided:
  (a) Time over Threshold (ToT) mode: the length of the ASD output corresponds to the time of the input signal above threshold.
  (b) ADC mode: the length of the ASD output corresponds to the charge, contained in a time window of 8-16 ns after threshold crossing, thus representing an approximate measure of the peak amplitude of the incoming signal.
- To suppress multiple threshold crossings for a single track passing a tube, a “dead time” (DT) is introduced, disabling the discriminator for a programmable time after a threshold crossing. The DT can be selected in the range 150-750 ns.

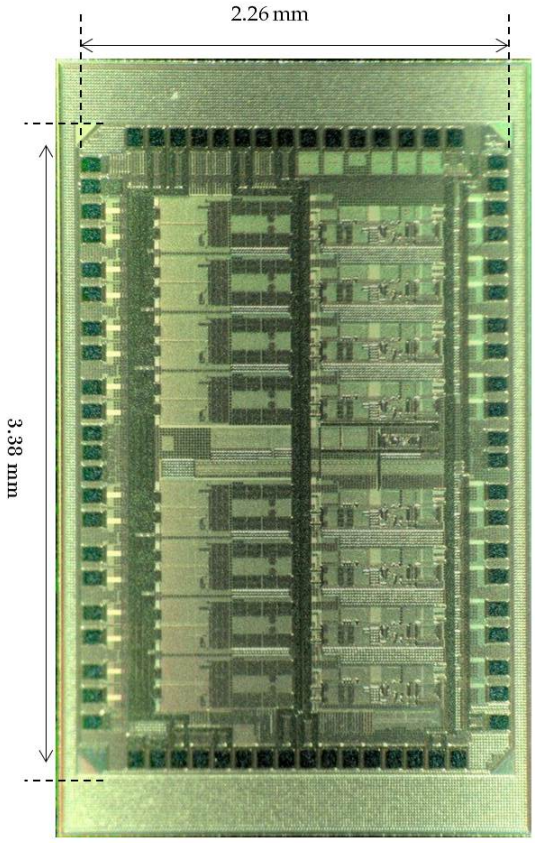


Figure 3 - Photo of the ASD die.

Accuracy of the TDC:

The ATLAS Muon Spectrometer aims for a resolution of the transverse momentum (p_T) of 10% for 1 TeV muons, which translates into a RMS-resolution requirement of < 80 μm for a single tube. The binning error of the TDC should be negligible besides errors due to physics effects, like diffusion, distribution of primary electrons along the track and statistics of gas amplification. Given the electron drift velocity of 20 and 42 μm/ns in large and small MDT tubes, the 0.78 ns binning error of the time measurement results in an error of 5 and 10 μm (RMS) for large and small tubes, respectively. (The least significant bit (lsb) of the TDC, used in the MDT readout, is defined by the LHC clock of 25 ns divided by 32.)

2 Design of the ASD2

The ASD2 is an octal CMOS Amplifier/Shaper/Discriminator, which has been optimized for the ATLAS MDT chambers. The MDT use the RC net shown in Figure 1 to suppress signal reflection from the "far end" of the tubes. The noise contribution from the terminating resistor is the dominant noise source in the ASD implementation [15][16]. For reasons of design flexibility and cost, implementation as an ASIC in a high quality analog CMOS process has been selected for this device (2.2).

2.1 Overview and specifications

The structure of one analog channel of the ASD is shown in Figure 4. It is a fully differential structure with a Charge Sensitive Preamplifier (CSP) and three shaping stages (DA1-DA3), followed by a discriminator and a leading edge charge integrator to be described later (section 2.4.6). The negative input of the CSP (Figure 5) is connected to the signal source of the MDT tube (i.e. the central wire), while the positive one is fixed with an internal resistor divider to a proper bias voltage. The capacitance formed by wire and tube corresponds to a parasitic capacitance of about 30 pF. At the same node, a 66 pF capacitor guarantees matching between the two differential inputs.

The main analog specifications for ASD1 [12], serving as reference for ASD2, are summarized in Table 3. Additional functional specifications are presented in section 2.5.

Table 3 - Specification of the Analog Parameters for ASD2.

Input impedance	Z_{IN} = 120 Ω
Noise	ENC = 6000 e^- rms or ~ 5 prim. e^- (~1 fC)
Shaping function	Bipolar
Shaper peaking time	t_p = 15 ns
Sensitivity at discriminator input	1.65 mV/e^- or 8.9 mV/fC (delta pulse injected into the ASD input)
Linear range[2]	1.5 V or 900 primary e^- (~170 fC)
Nominal threshold setting	40 mV or 24 primary e^- (~ 5 σ_{noise})

2.2 Fabrication Process

The ASD chip has been realized with the 130 nm process (CMRF8RF) by Global Foundry (previous IBM), using the option for eight metal layers. This implies a sheet resistance of 71 mΩ/□ for the first metal (M1) that reduces down to 7 mΩ/□ for the last one (MA). The selected transistors for the design are nfet33 and pfet33, which operate at 3.3 V of supply voltage and a nominal threshold voltage of 380 mV and -320 mV, respectively. The key electrical parameters of these devices are listed in Table 4.

Table 4 - Global Foundry 130nm Process Parameters of Field Effect Transistors (FETs).

Parameter	3.3V I/O nfet33/pfet33	Unit
Nominal supply voltage V_{DD}	3.3	*V*
Gate oxide thickness T_{OX}	5.2	*nm*
$L_{DES,MIN}$	0.40	*µm*
L_{EFF}	0.335	*µm*
Vt_{SAT}	380 / -320	*mV*
ON current I_{ON}	740 / -380	*µA/µm*
OFF current I_{OFF}	30 / -30	*pA/µm*
Max supply voltage	3.6	*V*

2.3 Topology and Architecture

The ASD2 was conceived to match or exceed the performance of the ASD1 [12]. It consists of a fully differential chain (Figure 4), optimized for the IBM 130 nm CMOS 8 RF-DM technology. A fully differential Charge Sensitive Preamplifier (CSP) is the best design for optimizing the immunity against external noise sources, in particular rejection against Common Mode on the signal inputs as well as

[2] This specification of a linear range in [12] is unrealistic. Simulation in section 2.4.8 and measurements in 3.2.3 show linearity at the level of 10% up to about 50 fC and a continued flat increase up to about 100 fC. For the accuracy of the time-of-arrival measurement, however, only linearity in the range of small signals around the threshold is relevant.

rejection of other noise on the power supply lines. The CSP and the three subsequent differential amplifier stages (DA1, DA2 and DA3) compose the analog part of the channel. The negative input (IN_{CSP}^{-}) of the CSP is connected to the MDT and the positive input (IN_{CSP}^{+}) is biased on-chip to about 783 mV for the purpose of input matching. The CSP amplifies the input charge, generating a proportional voltage signal which is amplified and shaped in the subsequent stages (DA1 to DA3).

The fully differential structure was chosen for noise immunity, while bipolar shaping was selected to reduce the effects of baseline shift at high signal rates [8][10][13]. For each of the eight channels, the output of the DA3 shaping stage is fed into the discriminator stage DA4 as well as into the Wilkinson Analog-to-Digital Converter (WADC). The DA4 stage compares the output of DA3 with a programmable threshold (DISC1 threshold). At the moment of threshold crossing, the (digital) outputs of DA4 change polarity, going, e.g. "from 0 to 1", thus defining the "leading edge" of the ASD output. At the same moment the WADC stage starts to perform a voltage-to-time conversion, based on the amount of input charge supplied to a capacitor during a short, programmable time span. The operation of the ADC proceeds in the following steps:

- Integration of the DA3 output on a holding capacitor for a programmable time span, defined by the 'Integration Gate Width' parameter (see section 2.5.1.2)
- Discharge of the holding capacitor at a constant, programmable current, defined by the 'Rundown Current' parameter (see section 2.5). Once the capacitor discharged, the output of DA4 changes polarity again, going back "from 1 to 0", thus defining the "trailing edge" of the ASD output.

The integration and discharge times determine the width of the Wilkinson ADC output (i.e. the delay between leading and trailing edge), encoding the charge in the first 10 to 30 ns of the incoming signal, which is an approximate measure of the signal amplitude. This information can be used to compensate for the effect that small pulses take longer to reach the discriminator threshold than large pulses, allowing for a pulse height dependent correction in data analysis ("time slewing correction").

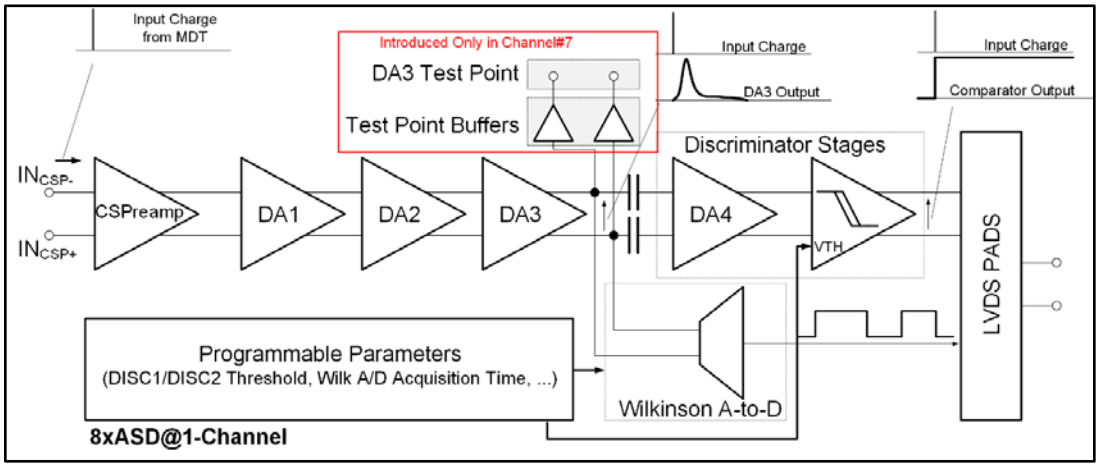


Figure 4 - Block Diagram of one ASD channel.

Differential logic controls the operation of the Wilkinson ADC, leading to good immunity against substrate coupling. Coupling between the digital and analog domains is strongly reduced by the implantation of a highly resistive BFMOAT[3] layer in the substrate. Further decoupling is obtained by strictly separating voltage and ground supplies among analog and digital domains.

The final output of the discriminator stage is sent to the LVDS PADS cell and converted to external low level signals (about +- 200mV signal swing into 50 Ω).

Each ASD channel draws approximately 15 mA from a 3.3 V supply, thus dissipating about 50 mW per channel (cf. Table 12 and Table 13). The operation of the ASD sub-cells is described in the following sections. The corresponding measurements of the analog behaviour of the finished chip are presented in section 3.2.

[3] „Moats" of insulating Boron-Fluorid (BF_2) implants are geometrically closed trenches in the substrate, preventing ohmic coupling across the trench.

2.4 The Analog Signal Chain

2.4.1 Charge Sensitive Preamplifier (CSP)

The design of the ASD was based on the following list of specifications (cf. Table 3).

- Power dissipation of the CSP: 12.87 mW (~ 3.9 mA @ 3.3 V)
- Z_{IN}: < 120 ohms (DC & AC/dynamic)
- Charge gain: ~ 1 mV/fC
- DC voltage gain: > 100 (40dB)
- Input noise density: 1.3 nV/√Hz
- ENC (with 380 Ω termination): 6000 e^- rms
- Peak time < 15 ns for a delta pulse, generated by a voltage step, capacitively injected into the ASD input.

The Charge Sensitive Preamplifier has been implemented with a cascode input differential stage and an optimized M4-RS-M5 source follower as shown in Figure 5. This is the key block of the chain and its performance strongly depends on the parasitic capacitance C_D of 60 pF connected to the negative input. The very large value of C_D is mainly due to the PCB parasitics and the long wires of connection between the ASD and the tubes (see Figure 1). In particular, it affects the closed-loop-gain bandwidth with a corresponding reduction of the voltage response rise-time and the sensitivity of the CSP.

The transistors of the input differential pair (M1A and M1B in Figure 5) are crucial for an optimum trade-off between noise, speed and power consumption. For this reason, they are very large (W = 2 mm and L = 400 nm), sink about 1.8 mA of current and have a transconductance g_m of about 34 mA/V. The values of currents, voltages, dimensions of passive/active components are reported in Figure 5 and in Table 5.

The positive input has been fixed by a resistor divider (RP1 and RP2) to 0.783 V and connected to an integrated capacitance C_P of 66 pF, reducing the mismatch introduced by C_D when the tube is connected. The currents I_A and I_B are implemented through low voltage cascode current mirrors ($M6_{A-B}$ and $M7_{A-B}$ in Figure 5). They mirror the current from a reference of 31 µA and contribute to determine an equivalent impedance at the node out_oa (R_{OUT}) of about 9.8 kΩ. It is given by the parallel between

- the load resistance (R_L) of 20 kΩ
- the M_{1B}-M_{2B} output impedance ($R_{M2B-M1B}$) of about 32kΩ and
- the mirror impedance (R_{IB}) of about 46 kΩ.

The resulting loop gain is 50 dB. The large input device sizes result in approximately 2 pF of gate-source parasitic capacitance, which, however, is negligible w.r.t. the detector parasitic capacitance C_D. The feedback network has been implemented with an equivalent resistor $R_F = R_{F1} + R_{F2}$ of 25 kΩ and a capacitance C_F of 600 fF. This way, the M_3 - R_{F2} - M_4 source-follower optimizes the common-mode voltage for the output node, leading to a better operation of the following DA1 stage, which has NMOS input transistors (and for thermal noise minimization).

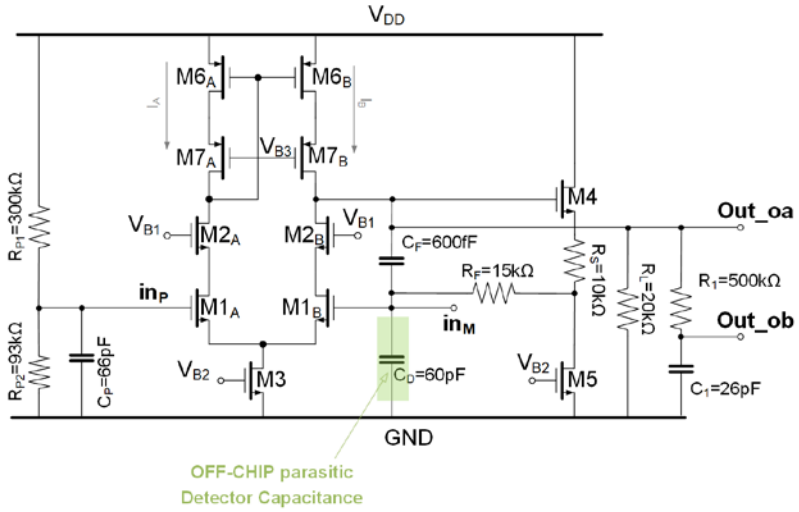


Figure 5- Simplified Scheme of the Charge Sensitive Preamplifier (CSP).

Table 5 - Parameters of the most important CSP transistors.

MOS	W/L	g_m – [mA/V]	r_{DS} – [kΩ]
$M1_A$	2mm/400nm	34.36	1.03
$M1_B$	2mm/400nm	33.36	0.978
$M2_A$	150µm/400nm	17.38	3.14
$M2_B$	150µm/400nm	16.74	2
M3	928µm/3µm	18.41	505.7
M4	80µm/500nm	1.187	118
M5	16µm/3µm	0.348	549

The CSP transfer function[4] depends on the feedback network (R_F and C_F), the transconductance of the input transistor (M_1), the output impedance (R_{OUT}) and the detector capacitance (C_D). It can be approximated by Eq. 1 (cf. ref [17]). This equation can be further approximated by Eq. 2, replacing the ratio R_{OUT}/R_F and neglecting the higher frequency zero (since $g_{m_{M1}} \gg 1/R_F$ and the zero is around 9 GHz).

$$T(s) \cong -R_F \frac{1 + s\frac{C_F}{g_{m_{M1}}}}{\left(1 + sC_F R_F\left(1 + \frac{C_D}{C_F}\left(1 + \frac{R_{OUT}}{R_F}\right)\frac{1}{1 + g_{m_{M1}} R_{OUT}}\right)\right)\left(1 + s\frac{C_D}{g_{m_{M1}}}\right)} \qquad \textit{Eq. 1}$$

$$T(s) \cong -R_F \frac{1}{\left(1 + sC_F R_F\left(1 + 1.39\ \frac{C_D}{C_F}\frac{1}{g_{m_{M1}} R_{OUT}}\right)\right)\left(1 + s\frac{C_D}{g_{m_{M1}}}\right)} \qquad \textit{Eq. 2}$$

The values of C_D, C_F, g_{mM1} and R_{OUT} determine the constant time of the dominant pole (τ_{P1}) and the sensitivity (S_{CSP}) according to Eq. 3 and Eq. 4, respectively. The variations from the ideal case depend mainly on a no-negligible parasitic detector capacitance (C_D). Moreover, the time constant of the non-dominant pole is fixed by the input transistor transconductance (to see Eq. 5) and guarantees a good time response.

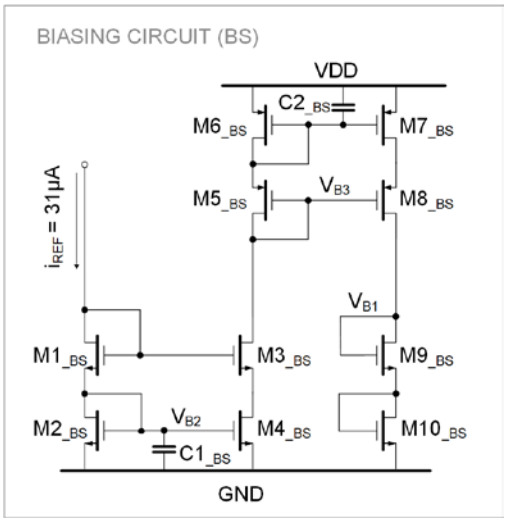


Figure 6 – Scheme of the CSP Biasing Circuit.

$$\tau_{P1} \cong \tau_{P1\_IDEAL}\left(1 + 1.39\ \frac{C_D}{C_F}\frac{1}{g_{m_{M1}} R_{OUT}}\right) \cong 1.4 \cdot C_F R_F \cong 21\ ns \qquad \textit{Eq. 3}$$

[4] A concise introduction to the concept of transfer functions and to the application of the Laplace transform for the analysis of electronics networks is given in [11].

$$S_{CSP} \cong S_{IDEAL}\left(\frac{1}{1+1.39\frac{C_D}{C_F}\frac{1}{g_{m_{M1}}R_{OUT}}}\right) \cong 0.7 \cdot \frac{1}{C_F} \cong 1.1\frac{mV}{fC} \qquad \textit{Eq. 4}$$

$$\tau_{P2} \cong \frac{C_D}{g_{m_{M1}}} \cong 1.7\ ns \qquad \textit{Eq. 5}$$

Similarly, the input impedance transfer function is approximately given by Eq. 6. It is almost constant ($Z_{IN}(0) \cong 57\ \Omega$) for all in-band frequencies since it is fixed by (R_F, R_{OUT}, g_{mM1}) at low frequencies and by (C_F, C_D) at higher frequencies.

$$Z_{IN}(s) \cong \frac{T(s)}{g_{m_{M1}}R_{OUT}} \qquad \textit{Eq. 6}$$

Out_oa and out_ob nodes in Figure 5 represent the CSP outputs and are biased at the same voltage through a proper R1 - C1 net. Instead, VB1 bias voltage is provided by a bias circuit (Figure 6) exploiting a cascode current mirror.

2.4.2 The Differential Amplifiers

The CSP preamp is followed by a chain of three differential amplifiers, DA1 through DA3, implemented with the identical circuit topology (Figure 7). The DA1 to DA3 chain amplifies and filters the CSP output [17][18]. The bipolar shaping at DA3 determines the fall-down time of the signal. This is achieved by replacing the ohmic impedances Z1 and Z2 in DA1 by a combination of resistors and capacitances. The $M4_A$ – $M4_B$ and $M5_A$ – $M5_B$ transistor pairs implement the common mode feedback of the stage and work in the linear region with about 40 mV of V_{DS}.

Shaping is implemented by the stages DA2 and DA3 using Z1-RC networks. All values are selected to cancel the very long time constant component of the positive ion MDT pulse [12].

Each stage has a gain given by the ratio between Z2 and Z1, while the bandwidth is fixed by the resistive and capacitive loads connected to the output nodes. The design values of Z1, Z2, I1 (equal to I2) in the stages DA! to DA3 are listed in Table 6 together with current and power consumption.

Figure 7 also shows the biasing circuit. A mirror current biases the gates of M3 and M2 transistors, mirroring the proper current to the input differential pair ($M1_A$ – $M1_B$).

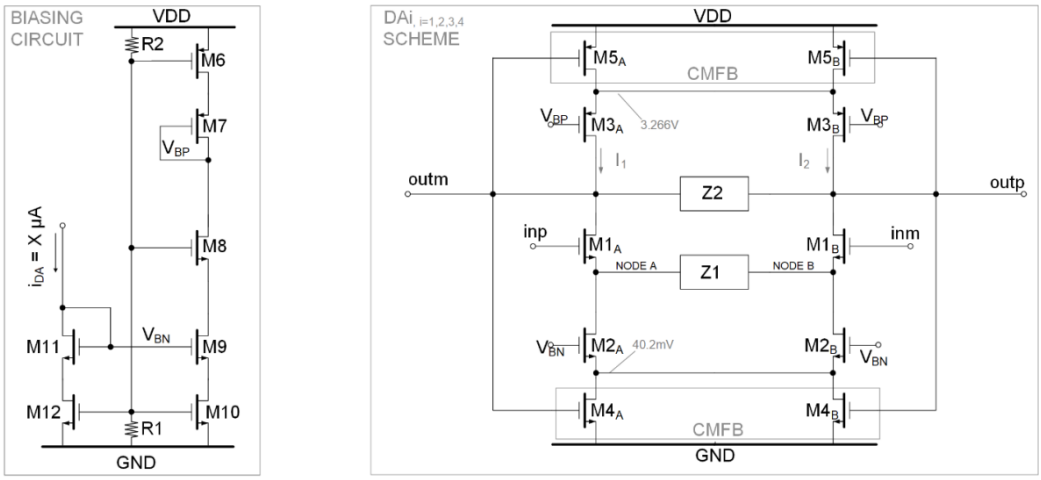


Figure 7 - Differential Amplifier Scheme (right) with its biasing circuit (left).

Table 6 - Component values for the amplifiers DA1 to DA3 in the circuit topology of Figure 7.

PARAMETER	DA1	DA2	DA3
Z1	1.33 kΩ	$2.44\ \text{k}\Omega \parallel \left(2.4\ \text{k}\Omega + \frac{1}{s \cdot 42.8\ \text{pF}}\right)$	$2.4\ \text{k}\Omega + \frac{1}{s \cdot 42.8\ \text{pF}}$
		The parallel of R=2.44 kΩ and the series R-C of 2.4 kΩ and 42.8 pF	Series of R=2.4 Ω and C= 42.8 pF
Z2	6.26 kΩ	6.26 kΩ	9.47 kΩ
I1 = I2	283 µA	295 µA	293 µA
I_{TOT}	746 µA	748 µA	745 µA
P_{TOT} @ V_{DD} = 3.3 V	2.46 mW	2.47 mW	2.45 mW

2.4.3 Pre-discriminator Gain Stage

The DA3 shaper output is AC coupled to one additional differential amplifier, DA4, referred to as pre-discriminator gain stage, which provides additional gain to the discriminator. The circuit topology of this stage is identical to the one of the previously presented differential amplifiers (Figure 7), with the Z1 and Z2 impedances equal to 0 Ω and 2.7 kΩ. NODE A and NODE B of Figure 7 are shorted to maximize gain and bandwidth at the expense of higher sensitivity of the gain to process variation. Since, however, the threshold is applied at its input, the gain sensitivity to process variation is irrelevant. Instead, the smaller load resistance (Z2) provides lower driving impedance to the subsequent discriminator stage.

2.4.4 The Discriminator

The discriminator (Figure 8), is a high DC-gain differential amplifier with symmetrical current-mirror loads and a main differential pair, M_{IN_A}/M_{IN_B}, biased at about 500 µA. Two current-mirror "loops" provide a differential gain of about 500 with no hysteresis.

Hysteresis is provided by the M1a/M1b pair, which unbalances the static current through the main differential pair by a variable external current. The main bias current is provided by R1 (poly-resistor) as shown in the yellow box of Figure 8.

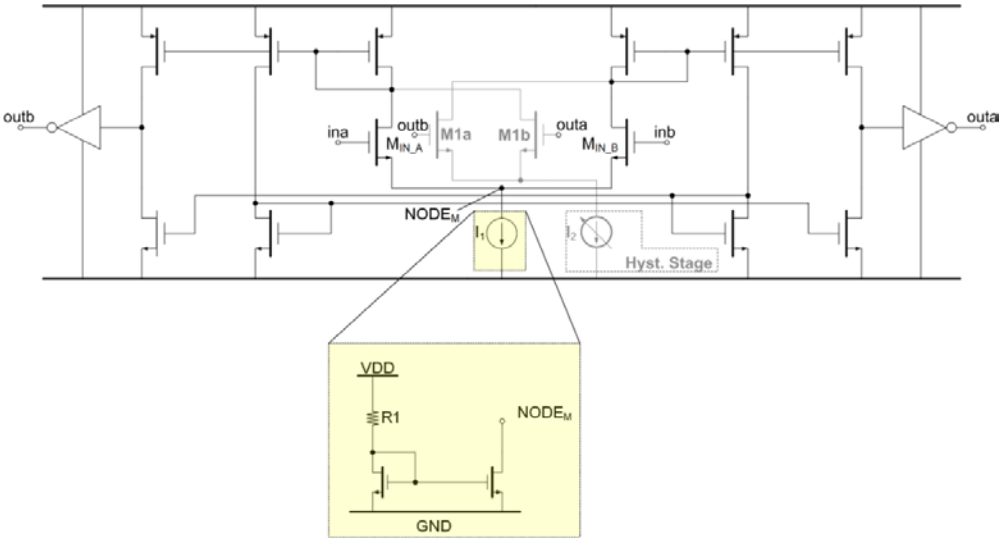


Figure 8 - Schematic of the Discriminator Stage.

2.4.5 The LVDS Output Cell

The output of the Low Voltage Differential Signals (LVDS) stage (Figure 9) can be selected by a multiplexer to be either the direct Discriminator output, i.e. the Time over Threshold (ToT) or else the output of the Wilkinson ADC, where the time difference between leading and trailing edge corresponds to the charge deposited on the Integration Gate, as described in section 2.3. Either option can be selected by the "ChipModeBit" in the shift register, see Table 8.

The LVDS output works with a nominal swing of 180 mV into 100 Ω centered at 1.23 V. This

range is compatible with the 'reduced range link' described in IEEE 1596.3 [19]. The input nodes (IN_A and IN_B) come from a previous MUX stage and go to a pair of moderate-sized inverters ($M5_A/M6_A$ and $M5_B/M6_B$). These inverters drive the output stage, which is essentially a pair of inverters ($M2_A/M3_A$ and $M2_B/M3_B$) with their output current limited by transistor pairs ($M1_A/M1_B$ and $M4_A/M4_B$) operating in their resistive region. $M1_A/M1_B$ and $M4_A/M4_B$ constitute the common mode feedback fixing the common mode output voltage. The DC characteristics are set entirely by transistor sizes.

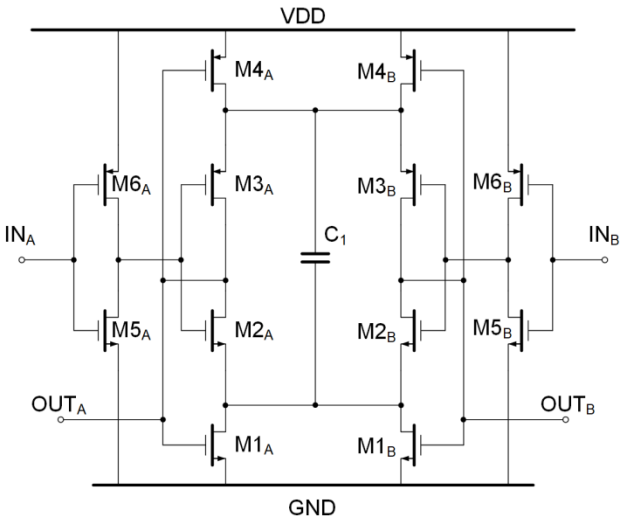


Figure 9 - Schematic of the LVDS stage.

2.4.6 The Analog Pad Driver

The last channel (CH7) has been implemented with an additional test function, making the output of DA3 available outside of the chip for diagnostic purposes. The driver for the DA3 output is called Test Point Buffers or Analog Pad Drivers (APD) as shown in Figure 4. The circuit (Figure 10) is based on a set of cascaded source followers [12]. The two switches, marked S_1, disable the stage when not in use to limit mismatch with other channels and to save power. Both switches are controlled by the same signal S1, shown in the figure.

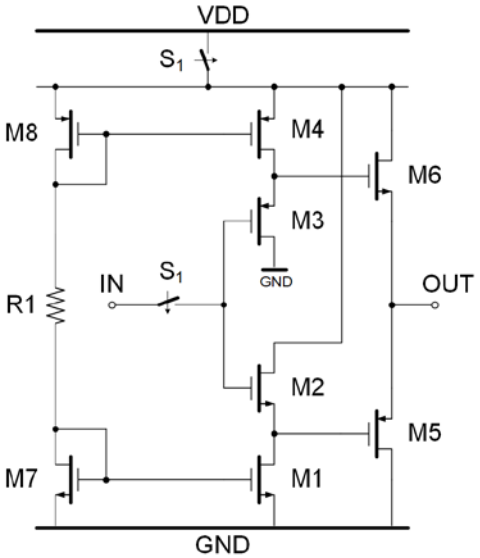


Figure 10 - Scheme of the Analog Pad Driver in CH7

2.4.7 The Wilkinson ADC

The Wilkinson ADC (WADC) [17][18] performs an approximate measurement of the amplitude of the incoming signal in the time window shortly after the signal was triggering the discriminator. Knowing this amplitude allows for a correction of the raw trigger time for time slewing (as already mentioned in section 2.3) and, in addition, provides diagnostics for monitoring the gas gain of the chamber.

The WADC performs a Voltage-to-Time conversion by charging and discharging the capacitor C_H shown in Figure 11. The conversion starts when an input signal is detected and the DISC1 stage provides the Start-of-Conversion signal. The rising edge of the DISC1 signal fires the FF1 flip-flop and the D_GATE delay element controlled by the Integration Gate Width bits, see Figure 12. The SG signal is output of FF1 and determines the charge on the sampling capacitor C_H for the time TGW, as defined by the D_GATE delay elements. In the same time, the V_A (t) – V_B (t) signal reaches the V_{AB_MAX} voltage, which is proportional to the input charge. Detection of the falling edge of SG fires the second flip flop (FF2), starting the discharge phase through the SW signal (FF2 output). The C_H discharge occurs with a constant current, controlled by the Rundown Current bits and finishes when V_A (t) – V_B (t) signal crosses zero, corresponding to the falling edge of the DISC2 output. The time of the C_H discharge is called T_{DISCH} and is proportional to V_{AB_MAX}. It results in a WADC output width given by TGW and T_{DISCH} and is controlled by the Φ_1 and Φ_2 signals, i.e. on ON–OFF phases.

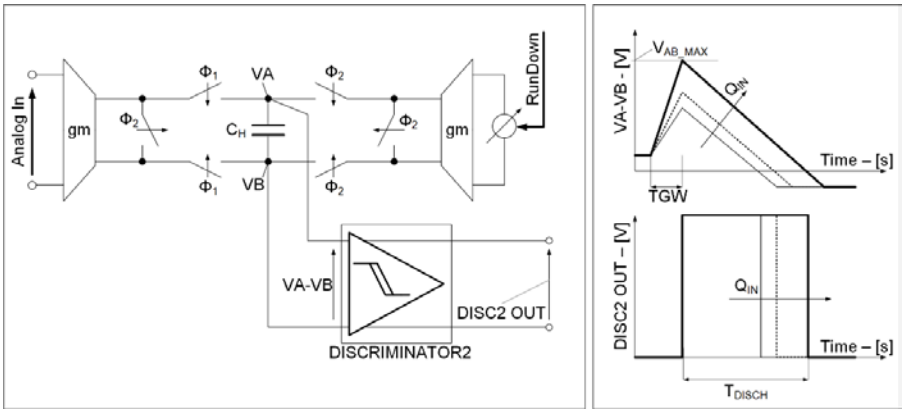


Figure 11 - Wilkinson Analog to Digital Converter (W-ADC) Scheme.

The timing depends on a specific set of programmable control bits for Integration Gate Width, Rundown Current and DeadTime. The corresponding data format is defined in section 2.5. The DeadTime (DT) signal is generated from the third flip flop (FF3) by the rising edge OUT when the delay elements (DT_1, DT_2 and DT_3) are activated. All delay elements are based on complementary current sources, charging appropriately sized capacitors, driving logic gates with hysteresis. The currents are programmable by a binary-weighted switched resistor string. The discriminator DISC1 is disabled for the time DT, such that incoming signals, crossing the threshold, will not create output towards the subsequent stage, the TDC. A proper differential logic (as described in [12]) controls the complementary phases Φ_1 and Φ_2 as well as the corresponding MOS switches.

The gm-transconductors are DA stages based on the scheme shown in Figure 7, where poly-silicon resistors replace Z1 and Z2. They are used like in the shaper stage as a floating current source, both for the integration current source and for the rundown current sink.

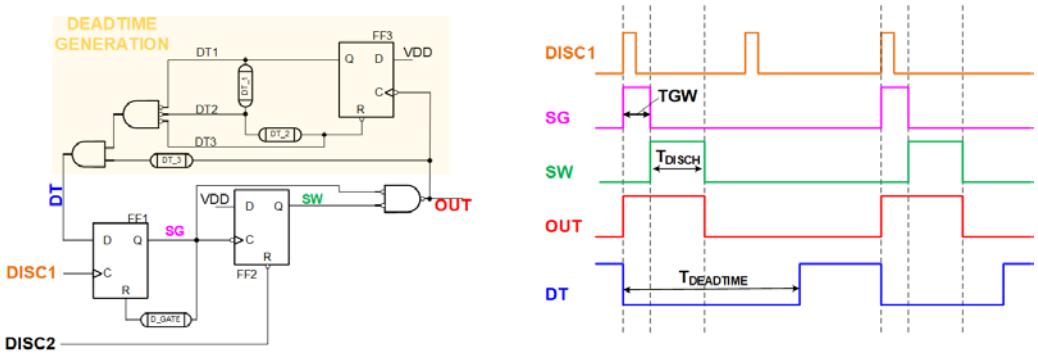


Figure 12- Control logic of ADC and Deadtime generator and corresponding signals.

2.4.8 Protection of the CSP Input against Overvoltage

The central wire in the standard MDT tubes is at 3090 V DC. The inputs of the preamplifiers must therefore be protected against spontaneous discharges of the wire, such that the amplitude at the ASD input does not exceed the allowed maximum of about 12 V.

As a standard design feature, all inputs in this technology are protected against accidental discharges, typically cause by Human Body Discharge (HBD). Crossed protective diodes are implemented as illustrated in Figure 13. Here the CSP inputs (IN_{CSP-} and IN_{CSP+} in Figure 4) are connected to each pad.

The two protection diodes esdvpnp (P+/NW ESD) and esdndsx (N+/PW ESD) are from the ESD library of IBM013. Their breakdown voltage is 11.5 –12 V with 1 µA of reverse current at 25° C. The diodes esdvpnp and esdndsx are robust, as the foundry guarantees sufficient hardness to high HBD (> 4 kV).

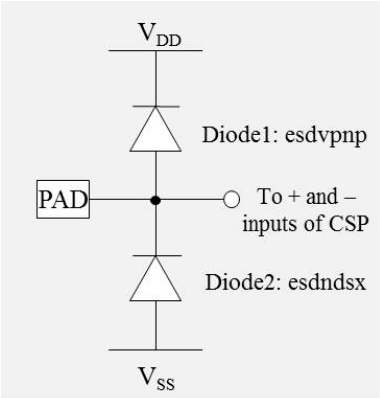


Figure 13 - Simplified Scheme of the Integrated Protection Circuit.

In addition to this internal protection, equivalent circuitry is implemented on the carrier PCB (“mezzanine”). Figure 14 shows the protective network as presently implemented on the frontend readout boards (“mezzanines”). The HV on the wire is decoupled from the readout by a 470 pF capacitor. AC-wise, the input of the ASD is protected by two sets of 20 Ω resistors followed by crossed diodes. A series of tests was done to assure this protection circuit also to be suffient for ASD2.

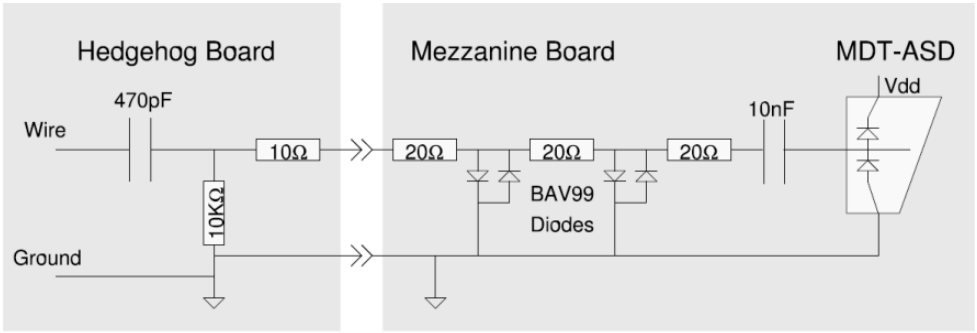


Figure 14 - Protective circuit against HV discharges applied to the input of the legacy ASD.

Figure 15 shows the circuit for the corresponding test. HV pulses with up to +/-3 kV amplitude were applied to the network, but did not lead to amplitudes at the AC output outside the specified voltage range.

In a first test, switch J2 was closed and resistor R_{IN} simulated the resistive load of the amplifier. Subsequently, ASD2 prototypes were connected to the AC output (TP) and a large number of HV pulses was applied to the network without any damage found in the tested devices.

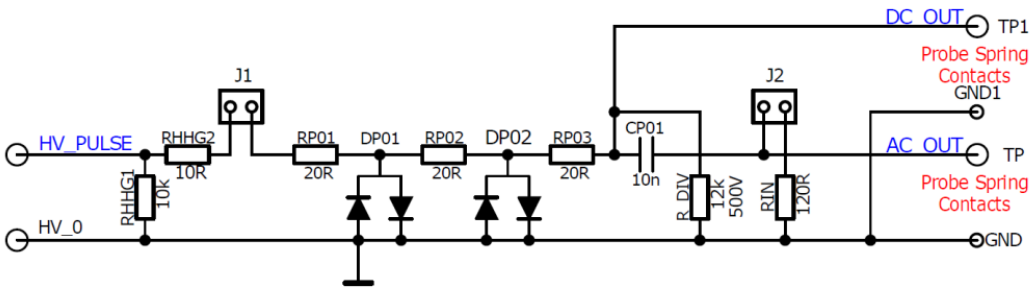


Figure 15 - HV circuit for tests of the protective network.

2.4.9 CSP and Shaping Stages in the Signal Processing Chain

2.4.9.1 Simulation in the Time Domain

The ASD2 signal processing chain (cf. chapter 2.3), was designed to detect input charges Q_{IN} up to 100 fC, but the range of simulation has been extended to 175 fC to also cover the saturation region. The input charge has been simulated with a parasitic capacitance of 60 pF in parallel to an ideal current pulse (I_{PULSE}). I_{PLUSE} has a fixed duration (T_{PULSE}) of 3 ns and an amplitude given by Q_{IN}/T_{PULSE}. For the sensitivity of the CSP, simulation predicts 1 mV/fC, for the peaking time about 7 ns, see Figure 16 (top).

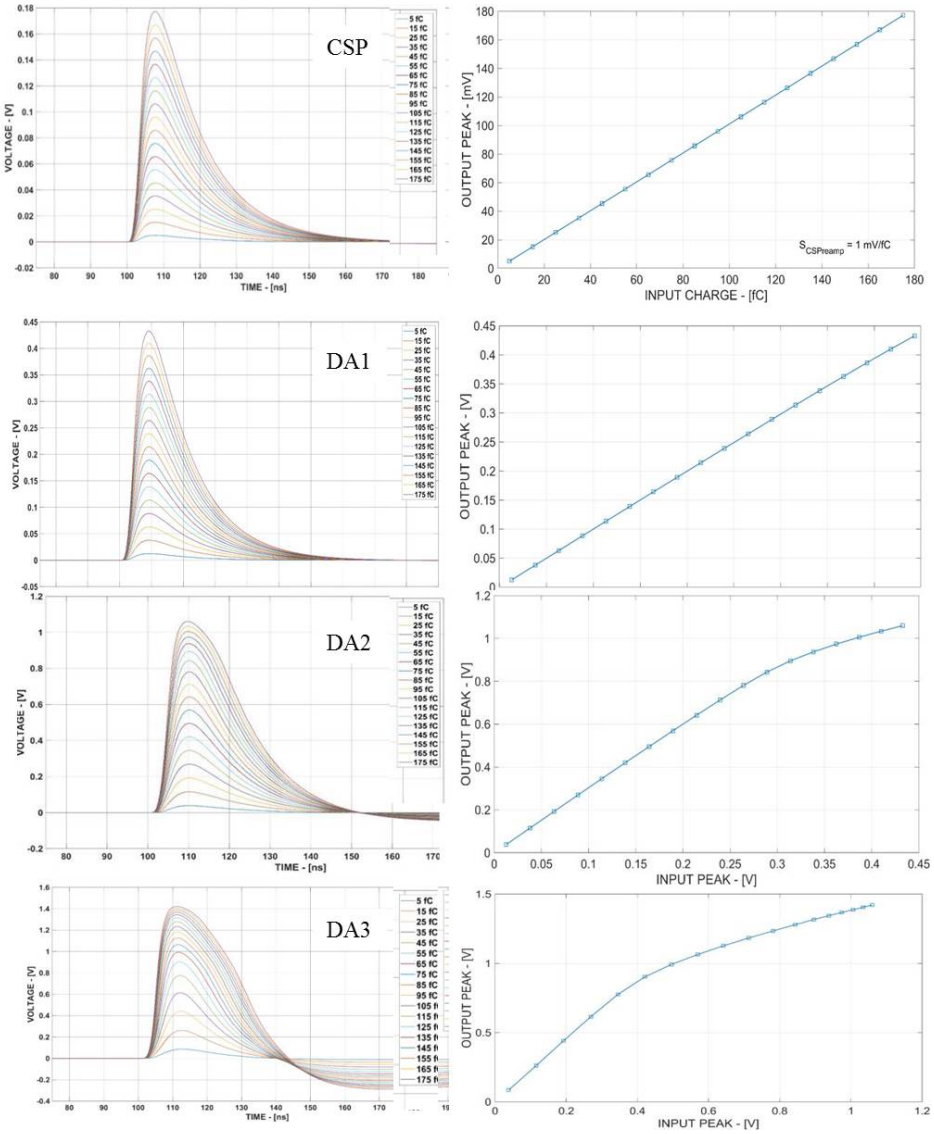


Figure 16 - Signal shape and gain of CSP and DA shaping stages vs. input charge 5 to 175 fC.

The differential stages DA1 to DA3 amplify and shape the output of the CSP, as shown in Figure 16. At the end of the analog chain, i.e. at the output of DA3, the peak amplitudes for input charges of 25, 50, 75 and 100 fC gain values are 17.6, 16.8, 14.2 and 12.2 mV/fC. The small-signal gain of about 18 mV/fC is thus considerably higher than the 8.9 mV/fC, specified in Table 3. Likewise, the peaking time of 12 ns is faster than the specified 15 ns.

A characterization in terms of peak input vs peak output has been done for each differential amplifier. DA1 has a purely resistive feedback and its output changes linearly with the input.The shaping stages, in contrast, show increasing non-linearity at high input charge (Figure 17). Measurements on the finished chip have verified the corresponding saturation effect of the DA3 output (Figure 28).

2.4.9.2 Simulation in the Frequency Domain

The AC characteristics of the CSP and the differential amplifiers DA1-DA3 are shown in Figure 17. The DA1-DA3 amplifiers serve both as gain and as shaping stages. The topology for all amplifiers is identical (Figure 7), while the feedback network differs according to the desired frequency characteristics and the corresponding values of the feedback elements Z1 and Z2 (Table 6).

- DA1 is a simple gain stage with purely resistive feedback. The gain is 8.3 dB with a 3dB bandwidth of 129.5 MHz (Figure 17).
- the DA2 and DA3 stages implement the intended bipolar shaping. Their frequency response is achieved replacing the impedance Z2 with the R-C nets specified in the table.

The maximum gain of DA2 is 9.9 dB between 750 kHz and 184 MHz, while the DA3 stage performs a gain of 8 dB in the range 1.1 MHz – 65 MHz.

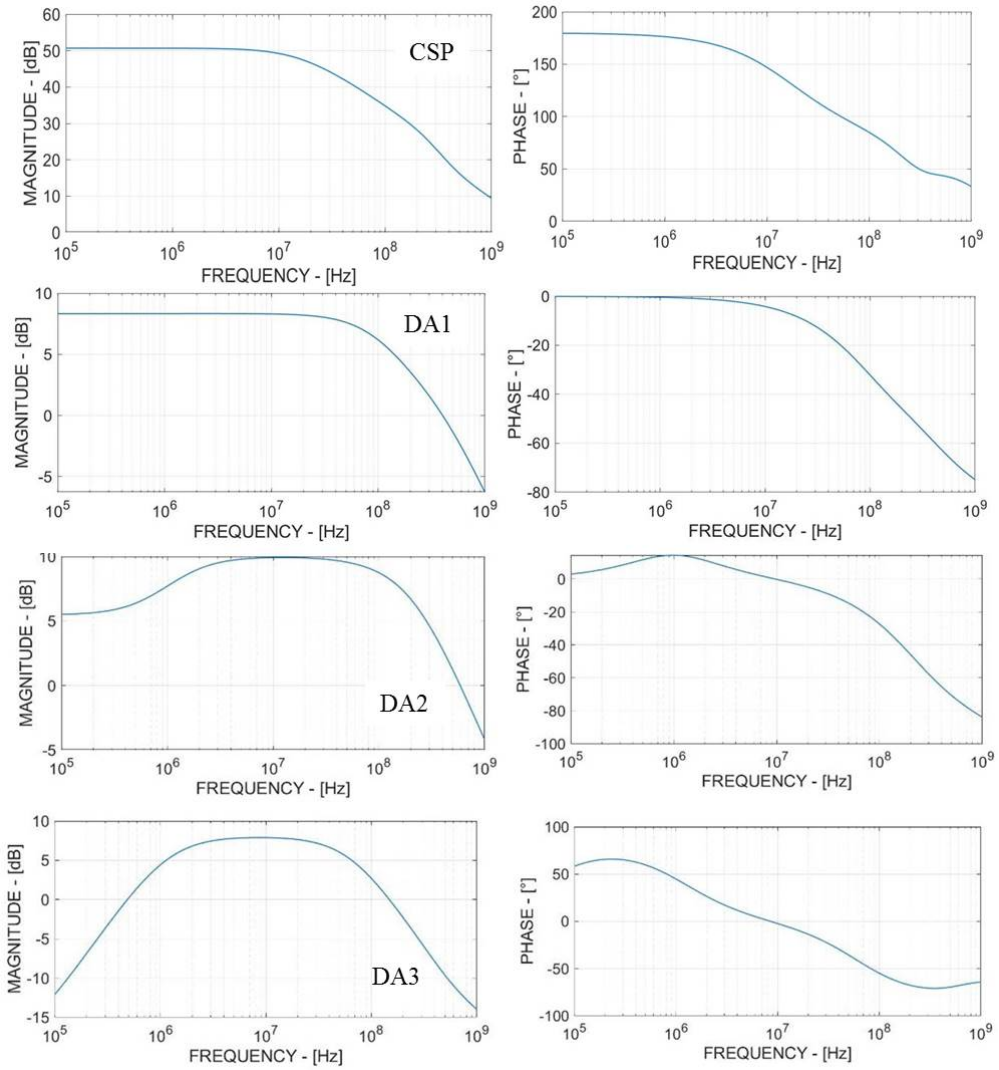


Figure 17 – Gain and Phase of the CSP and DA shaping stages vs. frequency.

Figure 17 shows gain vs. frequency for all four analog blocks as well as their superposition. The pass-band frequency response is characterised by a bandwidth of about 16 MHz (from 1.4 MHz to 17 MHz) with a maximum gain of 76 dB. The high-pass cutoff frequency (1.4 MHz) depends only on the frequency response of DA3, while all stages contribute to the low-pass cutoff (17 MHz), as DA3 is the only stage with AC coupling in the chain (see Table 6).

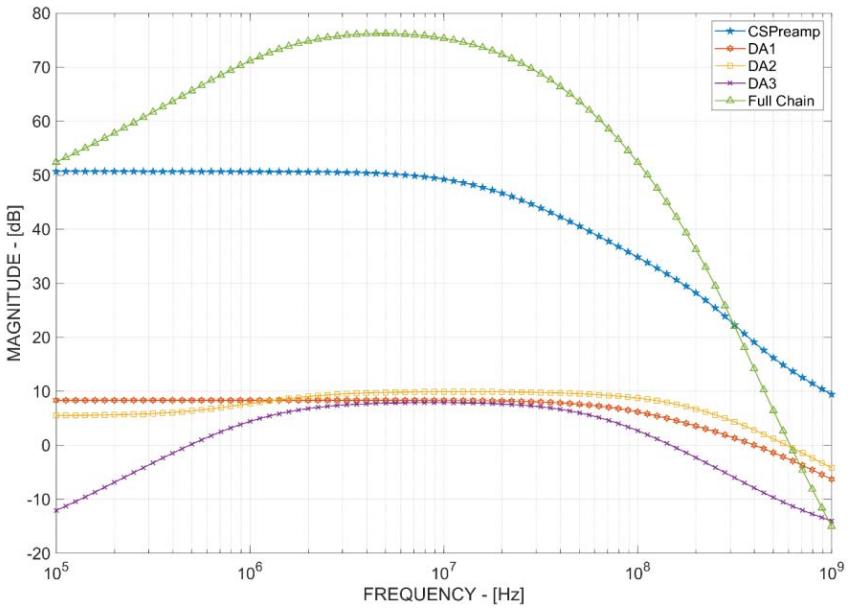


Figure 18 - Frequency response of the full analog chain and response of each single stage.

The Analog Pad Driver (Monitoring Buffer) is only implemented for channel 7. It allows to test the output of DA3, controling performance parameters like gain, peak time or pulse shape in overload conditions. It may also be used to detect digital-to-analog interference or crosstalk among adjacent channels. The data shown in section 3.2 were recorded at the monitoring buffer output, cf. Figure 4.

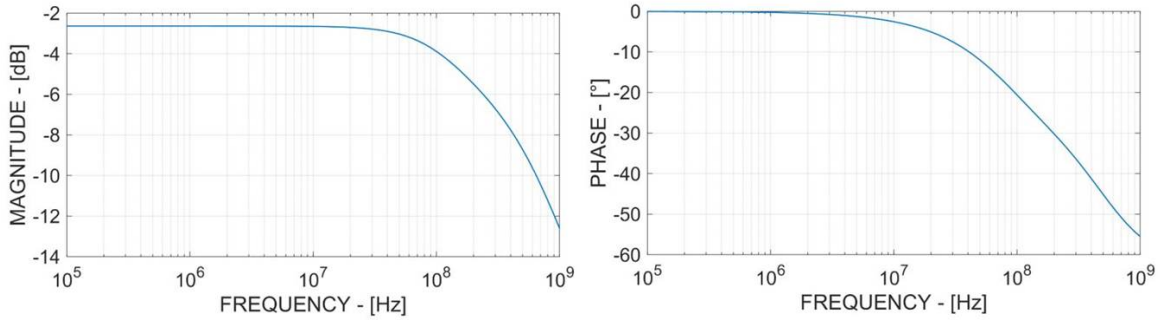


Figure 19 - Bode diagram of the Analog Pad Driver with a constant gain up 211 MHz (3 dB point).

The analog pad driver works with a gain of - 2.6 dB[5] and a bandwidth of 211 MHz (Figure 19), a bandwidth considerably wider than the one of the DA3 output in Figure 17. Consequently, it does not contribute to the shaping of the DA3 output at any significant level. Due to the -2.6 dB attenuation of the APD, readings must be multiplied by 1.35 to correspond to the DA3 output.
As this buffer represents a non-negligible load to the output of DA3 and also consumes significant power, signal input and supply voltage can be disconnected when the pad driver is not in use. This way, all 8 channels have the same electrical behaviour and operate under identical conditions.

[5] Corresponding to $V_{out}/V_{in} = 0.741$

2.4.10 The Wilkinson ADC

The WADC performs a voltage-to-time conversion, resulting in an approximate measurement of the input charge [12]. An example of the W-ADC output pulse generation is shown in Figure 20.

The width of the WADC output (Figure 20, bottom) is the sum of the charge and discharge time of the capacitor CH (Figure 11 in section 2.4.7). The signal at CH during charge and discharge is shown in Figure 20 (top). It is obtained with 32 mV of threshold voltage (VTH2), an integration gate time (i.e. charge phase) of about 26 ns and a rundown current of 3.4 µA. The integration gate and rundown signals are shown in the center of the same Figure.

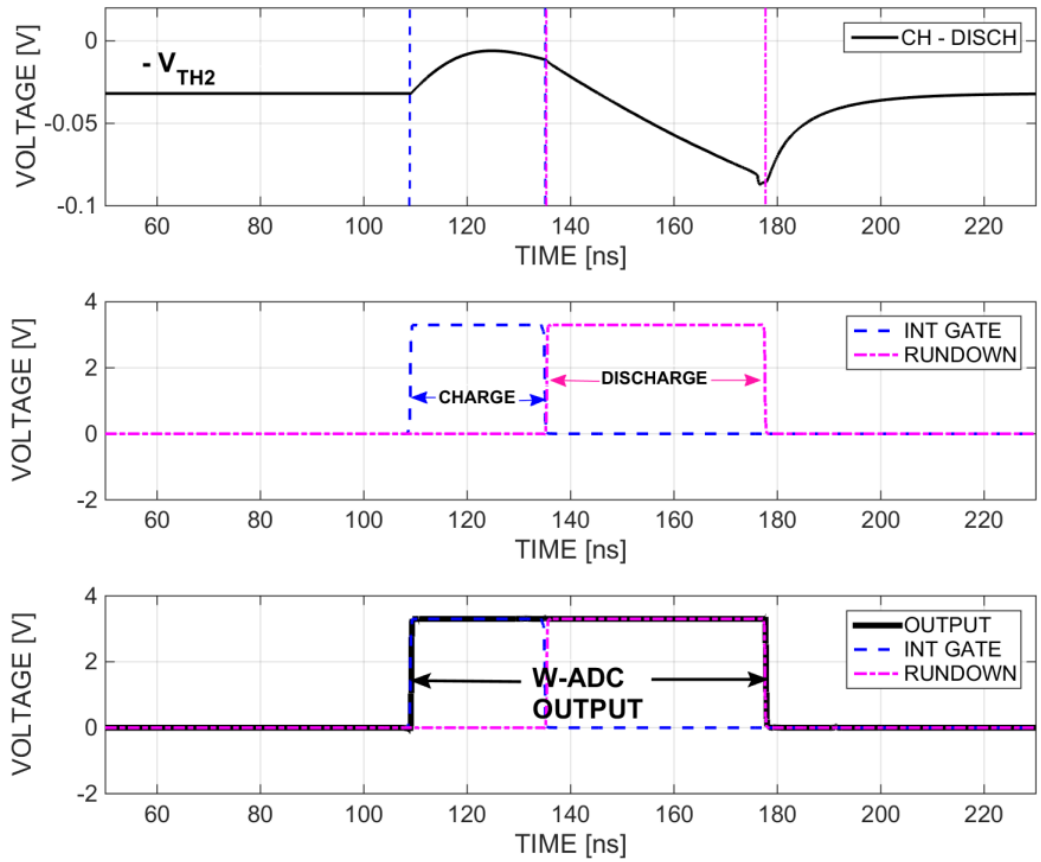


Figure 20 - WADC Output from its internal signals.

2.4.11 Simulation

The ASD2 chip has been simulated at the schematic level using Cadence Tools and the GF 130 nm (CMRF8RF_LM) Process Design Kit (PDK). The configuration used for simulation is presented in Figure 20, while Figure 21 shows the main input/output voltage signals of the Analog Pad Driver (see section 2.4.6).

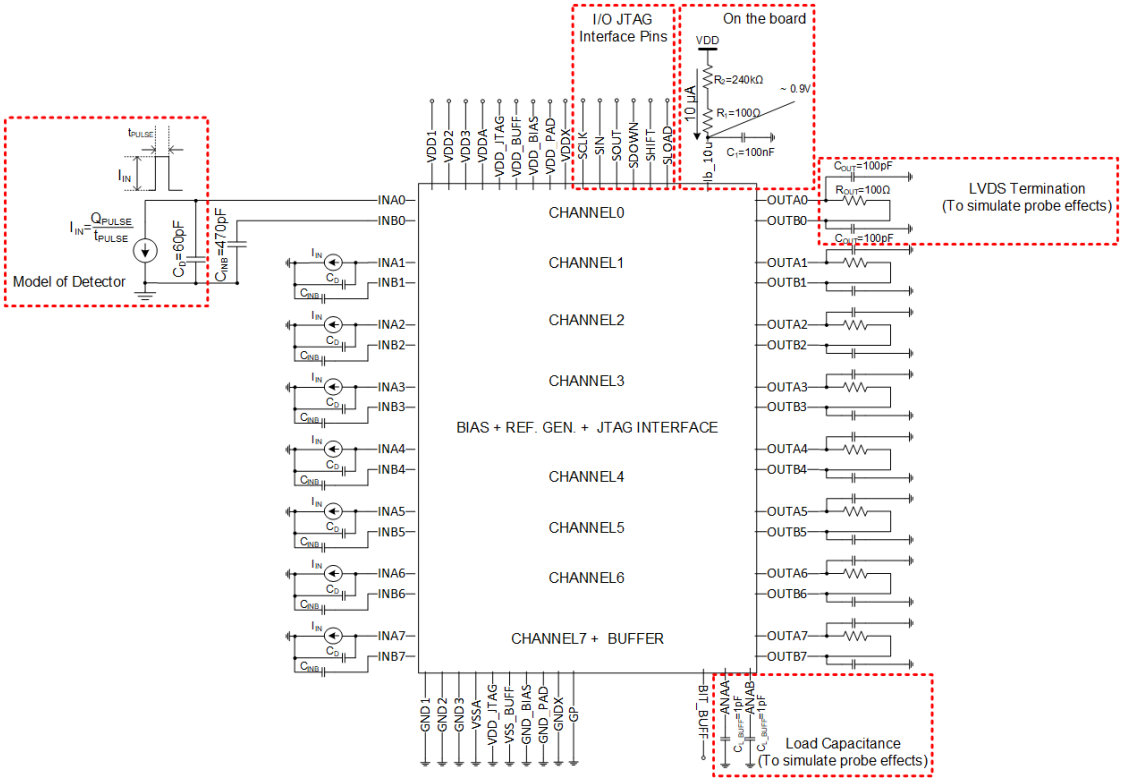


Figure 20 - ASD2 simplified Simulation Scheme.

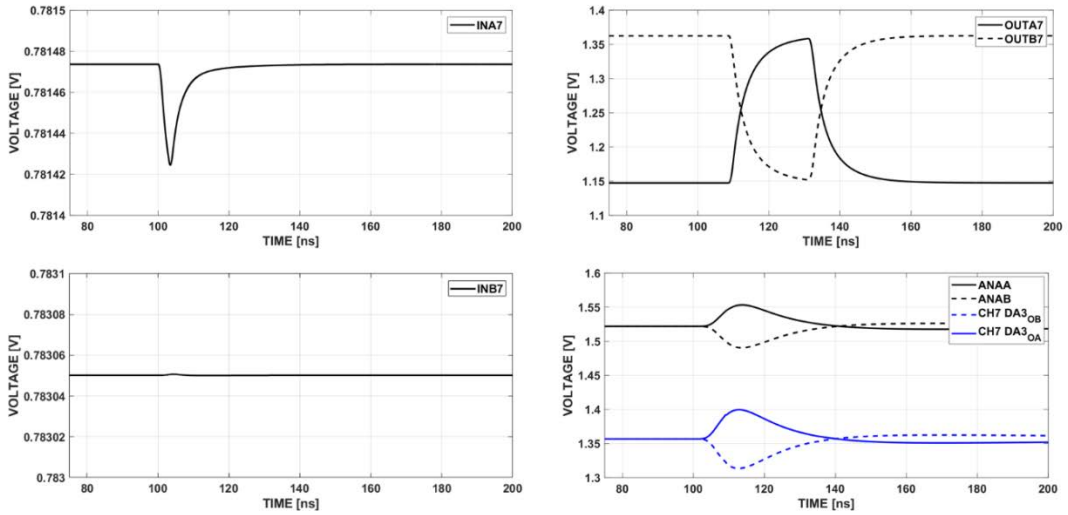


Figure 21 - Input and Output Voltage signals of test channel (CH7).

Cadence tools also allow to investigate the chip performance with respect to Process/Voltage/Temperature (PVT) variations with the aim to,detect potential mismatch among devices of identical design. Our result w.r.t. process variations was that the variation of transistor parameters (e.g. threshold voltage, transconductance, output impedance) and resistor and capacitor values may cause performance variations within ± 20 %. for parameters like peak voltage, peak time, width of the ADC output and deadtime.

Simulation was based on the following sets of parameters:

- a temperature range between – 40° and 120°
- five different processes of fabrication
  - typical – TT
  - slow slow – SS
  - fast fast – FF
  - slow fast – SF
  - fast slow – FS
- supply voltage variation of 10 %.

An example for the variation of device parameters is shown in Table 7. For this purpose four typical devices have been chosen: an input NMOS transistor (W/L = 220 µm / 400 nm), a PMOS load (W/L = 500 µm / 400 nm), a resistor (W = 600 nm, L = 16.42 µm) and a capacitor (W = 11.48 µm, L = 25 µm). Obviously, the variation of performance is given by a combination of all relevant parameters. This justifies the variation of the peak voltage and the peaking time delay at the DA3 output in the range 60 – 120 mV and 11 – 15 ns, respectively.

Table 7 - Range of parameter variation used in simulation for critical components.

PARAMETER	MIN	NOM	MAX	UNIT
NMOS Threshold Voltage	396.5	514.5	611.6	mV
NMOS Transconductance	3.744	4.504	5.248	mA/V
NMOS Output Impedance	3.468	6.971	11.01	kΩ
PMOS Threshold Voltage	371.9	363.9	447.6	mV
PMOS Transconductance	7.029	8.203	9.628	mA/V
PMOS Output Impedance	5.886	7.893	10.62	kΩ
Resistor	9.823	10	10.2	kΩ
Capacitor	599.2	599.8	600.7	fF

2.5 Programmable Parameters

As indicated in the block diagram of Figure 4, the Programmable Parameters (PPs) section on the chip controls the proper functioning of the ASD by defining parameters like threshold, gate width, run-down current and dead time. A 55-bit digital word is transmitted to the ASD using a simplified JTAG protocol, while an interface, based on a chain of register, transmits the word code associated to each parameter to Digital-to-Analog Converters (DACs).

Table 8 gives a summary of the PPs together with the number of bits, corresponding range, and resolution/LSB. Analog PPs control Discriminator (DISC1) and Wilkinson ADC (WADC) stages. The other PPs are functional and manage channel/chip operation mode.

Table 8 - Summary of the Programmable Parameters.

STAGE	PARAMETER	RANGE	LSB	UNIT	BITS
DISC1	DISC1 Threshold – V_{TH1}	-255 to 255	2	mV	8
	DISC1 Hysteresis	0 - 320	20	µA	4
WADC	Wilkins. Integration Gate	8 - 45	~ 2.5	ns	4
	DISC2 Threshold –V_{TH2}	32 - 256	32	mV	3
	Run-down current	2.4 – 7.3	~ 0.7	µA	3
	Dead Time	13.8 - 785	~ 100	ns	3
LVDS OUTPUT	Channel Mode	ON, HI, LO	-	-	2
	Chip Mode	ADC, ToT	-	-	1

2.5.1 Programmable analog Parameters

2.5.1.1 Discriminator control

The Discriminator Stage compares the analog DA3 output with a ***threshold voltage*** (V_{TH1}) and uses a ***hysteresis*** to avoid multiple threshold crossings due to noise.

V_{TH1} is applied at the AC coupled input of the pre-discriminator differential amplifier stage (DA4) and is generated by two complementary 8-bit dual resistor divider voltage DACs (ref.[12]). The final differential output threshold can vary from – 255 mV to + 255 mV with an LSB of 2 mV.

Hysteresis is applied through a scaled-transistor current source DAC with a resolution of 4 bits. The range of the DAC is 320 µA with a LSB of 20 µA, which is 0 - 85 mV at the discriminator input.

2.5.1.2 Wilkinson ADC Control

The WADC output pulse width depends on the following programmable parameters [12]:

- Integration Gate Width (IGW)
- Threshold (V_{TH2}) for the WADC comparator (DISC2)
- Rundown Current (RC)
- DeadTime (DT).

The ***Integration Gate Width*** PP determines the 16 different charge timings of the capacitor C_H (section 2.4.7) through 4-bit words. The settable value range is 8 ns – 45 ns, with steps of ~ 2.5 ns.

The ***DISC2 threshold*** (V_{TH2}) is applied to the differential threshold terminals of the WADC comparator by two coupled resistor divider voltage DACs with 3-bit resolution and a range of 32 mV to 256 mV.

The ***Rundown Current*** PP controls the discharge phase of the capacitor C_H. It is set by a binary-weighted switched resistor chain between 2.4 µA and 7.3 µA. The pulse width range of the ADC is jointly determined by the Integration Gate Width (IGW), the discriminator threshold V_{TH2} and the Rundown Current of the switched resistor chain.

The ***DeadTime*** PP defines an additional time window after each hit, during which the logic does not accept new input. The dead time can be selected in the range 13.8 ns to 785 ns.

To optimize matching among the 8 ASD channels, IGW, RC and DT are generated locally in each channel.

2.5.2 Programmable functional Parameters

2.5.2.1 Chip mode

The ASD2 can operate in ADC or Time-over-Threshold (ToT) mode, selectable by bit number 16. When bit 16 is zero (ADC mode) the LVDS output corresponds to the output of the WADC, otherwise (ToT mode) it corresponds to the output of the discriminator.

The bit assignments of the shift register are given in Table 9. The shift register operates as a FIFO, so bit 0 is the first to enter and the first to go out, as illustrated in Figure 22.

2.5.2.2 Channel mode

For diagnostic purpose it might be useful to force the LVDS output to a logic HIGH or LOW. One of the following channel operation modes can be selected:

- ON MODE: default working setting; the output depends on the Chip Mode bit.
- HI MODE: the output is forced to HIGH or ‘Logic 1’ (regardless of what happens in the analog part of this channel).
- LO MODE: the output is forced to LOW or ‘Logic 0’ (regardless of what happens in the analog part of this channel).

In HI or LO MODE the channel is disabled. This option may be used to disconnect noisy MDT tubes from the Readout, which otherwise might saturate the readout bandwidth with meaningless data.

2.6 Architecture and I/O operation

2.6.1 Shift register bit Assignment

The bit assignment of the shift register is given Table 9. The shift register operates as a FIFO: bit 0 is the first to enter and the first to go out, as illustrated in Figure 22.

Table 9 - Bit assignment in the shift register.

JTAG BIT #	DESCRIPTION	LSB/code
[0:1]	Channel Mode – Channel 0 (TOP) – [0:1]	00 → ON (ACTIVE) 10 → ON (ACTIVE) 01 → LO (FORCED) 11 → HI (FORCED)
[2:3]	Channel Mode – Channel 1 – [0:1]	
[4:5]	Channel Mode – Channel 2 – [0:1]	
[6:7]	Channel Mode – Channel 3 – [0:1]	
[8:9]	Channel Mode – Channel 4 – [0:1]	
[10:11]	Channel Mode – Channel 5 – [0:1]	
[12:13]	Channel Mode – Channel 6 – [0:1]	
[14:15]	Channel Mode – Channel 7 (BOTTOM – with Test Points) – [0:1]	
[16]	Chip Mode	0 → ADC Mode 1 → ToT Mode
[17:19]	DeadTime – [2:0]	Bit 19 LSB
[20:23]	WADC Integration Gate – [3:0]	Bit 23 LSB
[24:26]	WADC Rundown Current – [2:0]	Bit 26 LSB
[27:30]	Hysteresis DAC (DISC1) – [0:3]	Bit 27 LSB
[31:33]	WADC threshold 2 (DISC2) – [2:0]	Bit 33 LSB
[34:41]	Threshold 1 (DISC1) – [7:0]	Bit 41 LSB
[42:54]	NOT USED	–

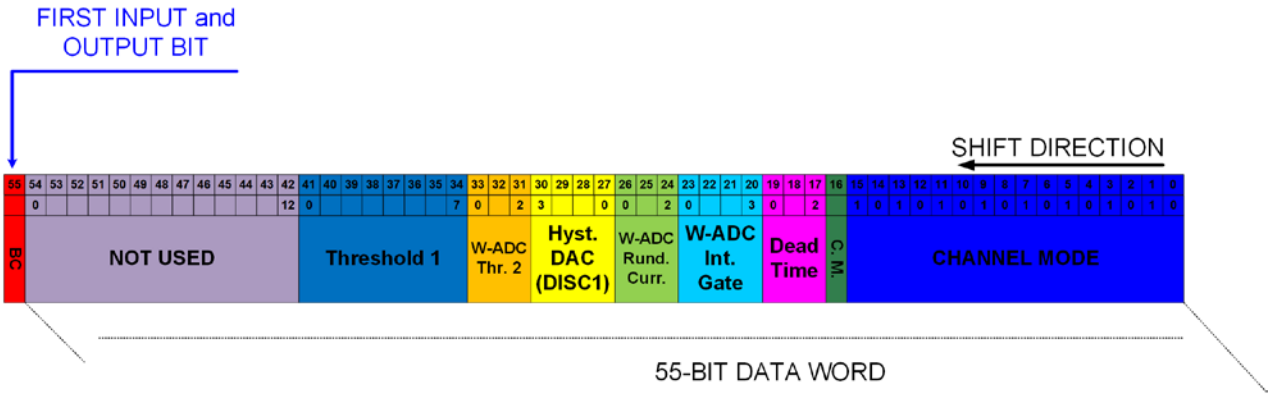


Figure 22 - Shift Register Image.

2.7 IC layout and I/O pad assignment

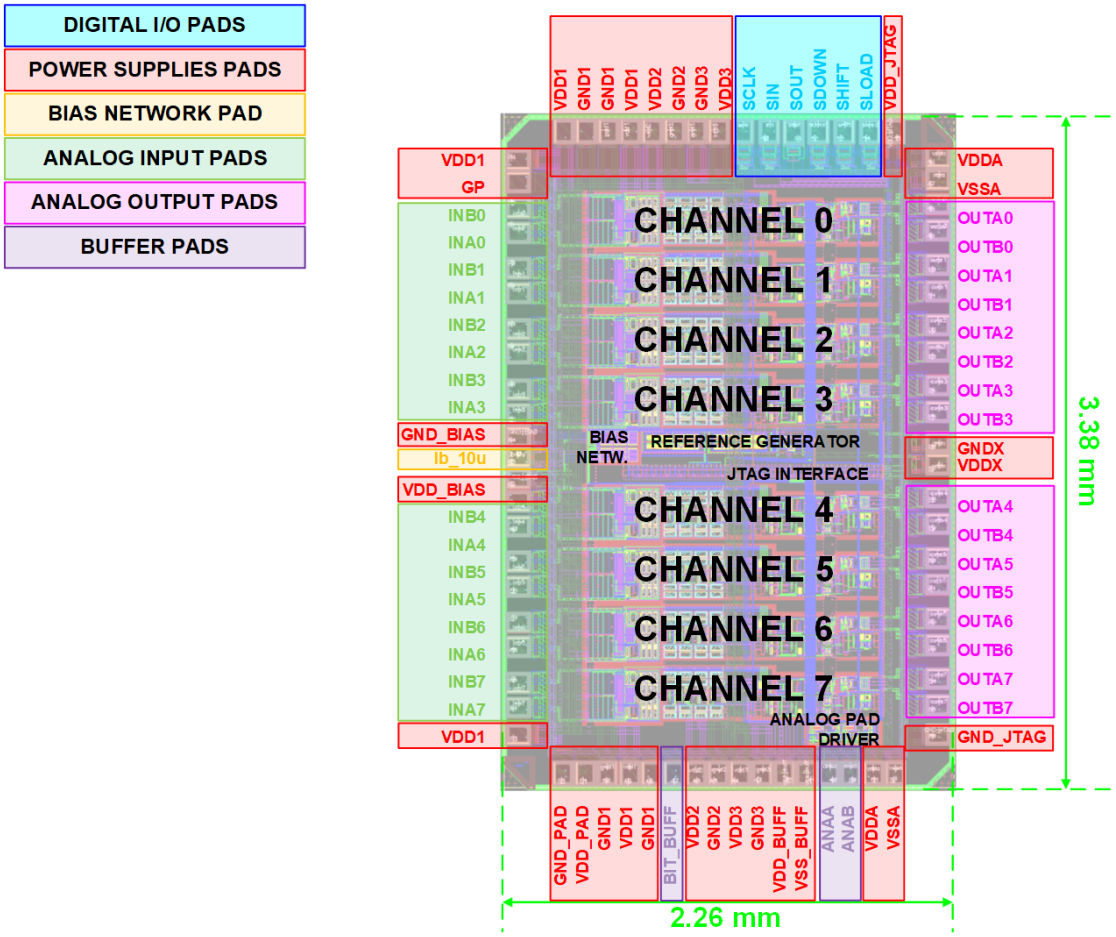


Figure 23 - Layout and floor plan of the ASD2 chip fabricated in IBM 130 nm technology.

ASD2 occupies an area of 3380 µm x 2260 µm. The overall structure is shown in Figure 23. The padring is composed by 74 pads, according to the following segmentation:

- DIGITAL I/O PADS
- POWER SUPPLIES PADS
- BIAS NETWORK PAD
- ANALOG INPUT PADS
- ANALOG OUTPUT PADS
- BUFFER (i.e. analog pad driver) PADS.

The individual function of the 74 signal and power pads is given in Table 10. The various VDD power domains, kept separate inside the chip, will remain separate on the carrier PCB in order to avoid supply voltage coupling between digital and analog circuitry. In contrast, the VDD_JTAG/GND_JTAG and VDD_PAD/GND_PAD domains will be connected to the power and ground planes of the PCB. One should note in this respect, that there will be no digital activity on JTAG related pads during normal ASD operation, discarding the possibility of signal interference during data taking.

The ASD2 core includes the eight channels arranged to preserve the matching. For the same reason, all shared reference (bias network and reference generators) are in the center, see Figure 23. Power supply pads are at top and bottom of the chip to guarantee an accurate supply for each channel, minimizing resistive voltage drop with distance from the supplied channel.

Table 10 - List and description of the I/O pad.

BLOCK	PAD NAME	DESCRIPTION	TYPE	#	I/O INTERFACE
JTAG (8 PADs)	SCLK	Clock Line	Digital Input	1	Vpulse Generator
	SIN	Load Control Line	Digital Input	1	Vbit Generator
	SDOWN	Down Control Line	Digital Input	1	Vpulse Generator
	SHIFT	Shift Control Line	Digital Input	1	Vpulse Generator
	SLOAD	Data Line	Digital Input	1	Vpulse Generator
	SOUT	Data Line	Digital Output	1	noConn Istance
	VDD_JTAG	JTAG Supply Voltage	Analog Input	1	DC-Volt. Generator of 3.3V±5%
	GND_JTAG	JTAG Ground Voltage	Analog Input	1	DC-Volt. Generator of 0V
ASD-MDT-Channel (55 PADs)	<ina0:ina7>	Positive Input of Channel	Analog Input	8	• 1nF Capacitance → if the channel is not used to detect an input charge • Current generator in parallel with 60pF capacitance → if the channel is used to detect an input charge
	<inb0:inb7>	Negative Input of Channel	Analog Input	8	• Capacitance of 470pF in simulation • Floating on the PCB
	<outa0:outa7>	Positive Output of Channel	Analog Output	8	Input 'A' of LVDS Termination
	<outb0:outb7>	Negative Output of Channel	Analog Output	8	Input 'B' of LVDS Termination
	VDD1	CSP Supply Voltage	Analog Input	5	DC-Volt. Generator of 3.3V±5%
	GND1	CSP Ground Voltage	Analog Input	4	DC-Volt. Generator of 0V
	VDD2	Analog Section Supply Voltage	Analog Input	2	DC-Volt. Generator of 3.3V±5%
	GND2	Analog Section Ground Voltage	Analog Input	2	DC-Volt. Generator of 0V
	VDD3	Digital Supply Voltage	Analog Input	2	DC-Volt. Generator of 3.3V±5%
	GND3	Digital Ground Voltage	Analog Input	2	DC-Volt. Generator of 0V
	VDDA	MUX-LVDS Supply Voltage	Analog Input	2	DC-Volt. Generator of 3.3V±5%
	VSSA	MUX-LVDS Ground Voltage	Analog Input	2	DC-Volt. Generator of 0V
	VDDX	Common Block Supply Voltage	Analog Input	1	DC-Volt. Generator of 3.3V±5%
	GNDX	Common Block Ground Voltage	Analog Input	1	DC-Volt. Generator of 0V
CH7 – Buffer (5 PADs)	VDD_BUFF	Buffer Supply Voltage	Analog Input	1	DC-Volt. Generator of 3.3V±5%
	VSS_BUFF	Buffer Ground Voltage	Analog Input	1	DC-Volt. Generator of 0V
	ANAA	da3_oa of CH7	Analog Output	1	1pF Capacitance
	ANAB	da3_ob of CH7	Analog Output	1	1pF Capacitance
	BIT_BUFF	Active High Enable for analog test output	Digital Input	1	Vpulse Generator
External Bias (3 PADs)	VDD_BIAS	External Bias Supply Voltage	Analog Input	1	DC-Volt. Generator of 3.3V±5%
	GND_BIAS	External Bias Ground Voltage	Analog Input	1	DC-Volt. Generator of 0V
	Ib_10u	Input Reference Current	Analog Input	1	Current generator of 10uA±5%
PadRing (3 PADs)	VDD_PAD	PadRing Supply Voltage	Analog Input	1	DC-Volt. Generator of 3.3V±5%
	GND_PAD	PadRing Ground Voltage	Analog Input	1	DC-Volt. Generator of 0V
	GP	PadRing Ground Plane	Analog Input	1	DC-Voltage Generator of 0V

3 Measured Performance of the ASD2

3.1 Description of the test setup

The automatic evaluation system for ASD chips testing is shown in Figure 24. The signal generator injects test pulses with variable repetition rate into any combination of the 8 channels of the ASD. The amplitude of the signal is controlled by a programmable attenuator. Test signals are voltage steps applied to a capacitor to generate charge injection into the ASD frontend (step function leading to a delta-charge). Optical insulation between the measuring setup and the PC is used to avoid injection of digital and/or switching noise into the ASD frontend.

The operating parameters of the ASD are controlled by the "ASD serial interface board", which defines, controlled by software, the shift register bits (cf. Table 8). This way, a programmed sequence of measurements can be obtained with minimal personal intervention. A threshold scan for all 8 channels, e.g., generates an important volume of data, so automatic operation of the test is a necessity.

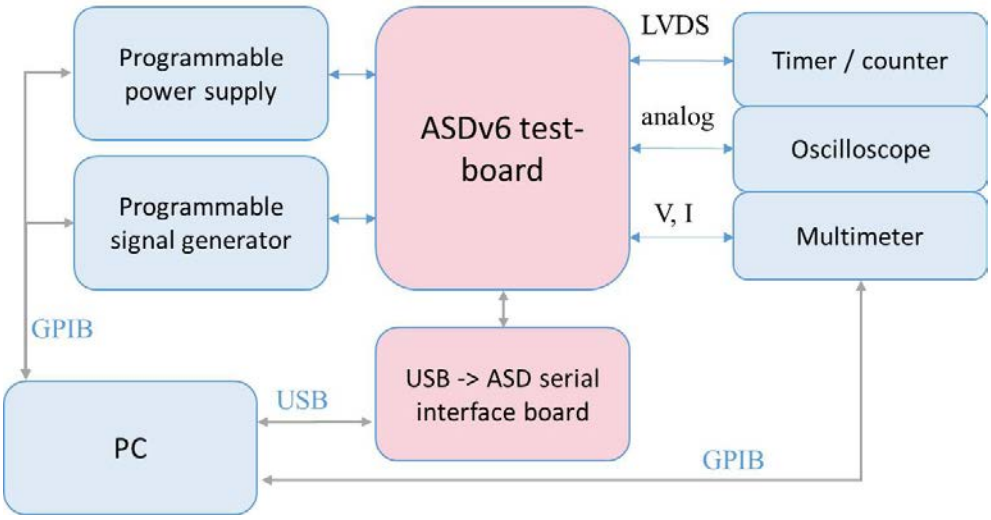


Figure 24 - The ASDv6 test environment.

While data from the timer unit, connected to the LVDS outputs of the ASD, can be stored and processed in the controlling PC, screenshots on the oscilloscope, recorded from the Analog Pad Driver on channel 7 (cf. section 2.4.6) can equally be stored on the PC for later analysis.

In the following sections we report on

- the performance of the linear chain CSP to DA3 (Figure 4), like peak time, gain, noise, linearity and operation in overload conditions
- performance of the digital part, i.e. rundown current control of the WADC, control of timing accuracy and range of the dead time generator
- equality of performance parameters among the 8 ASD channels. The equality of the 8 channels w.r.t. dead time and run-down current (which controls the length of the WADC output) is important, because all channels are controlled by one 3-bit word in the serial register, which does not allow correction for individual channels. The same is true for the equality of threshold settings, as the threshold for the 8 channels is controlled by one 7-bit word in the serial register. A detailed inquiry of this problem with the method of the S-curve scan is presented in section 0.

3.2 Measurement of the Linear Chain using the Monitor Output (APD)

3.2.1 Peak time, Linearity, Saturation behaviour at DA3

Figure 25 shows the response of the shaper stage DA3 to a delta charge injection into the CSP input. The signal shown is the differential output of the Analog Pad Driverr of channel 7 (cf. 1.2). The peak time of about 12 ns and the zero crossing time of 40 ns correspond to the results from simulation, see Figure 16.

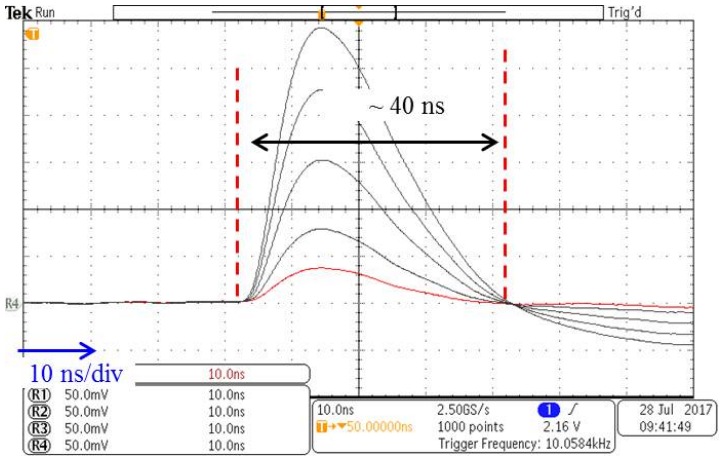


Figure 25 - Step response to injected charges of 5,10,20,30, 40 fC behind DA3. Peak time is 12 ns.

Figure 26 shows the corresponding results for the injection of much higher charges, which may occur due to heavily ionizing particles or converted neutrons. As the signal returns below the trigger threshold only after about 65 ns and reaches zero after about 400 ns, there is no significant loss of efficiency, as the amplifier is immediately ready to record the next signal.

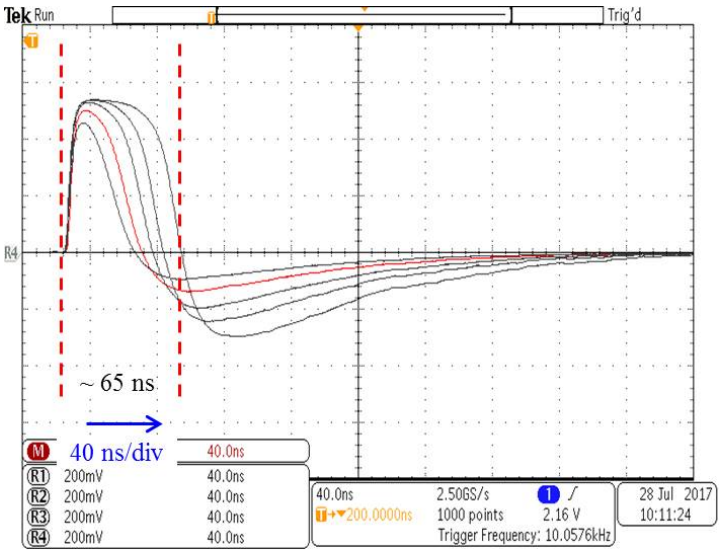


Figure 26 - Overload condition: step response to charges of 100, 200, 500, 1000 and 2000 fC.

3.2.2 Suppression of digital-to-analog Interference

The ASD chip is operating in “mixed mode”, i.e. sensitive analog amplifiers are operating close to digital circuitry. Coupling from the digital part into the analog part may happen via supply voltage lines and/or grounds, but also via the substrate of the chip. Separate external supply lines for voltages and local grounds have been foreseen in the design for the CSP stage, the DA1-DA3 amplification stages, the digital section and the LVDS output part, see Table 9. Substrate coupling has been suppressed by an implantation of highly insulating boron fluorid (“BF2 moat”), which separates the domains of analog and digital activity from each other.

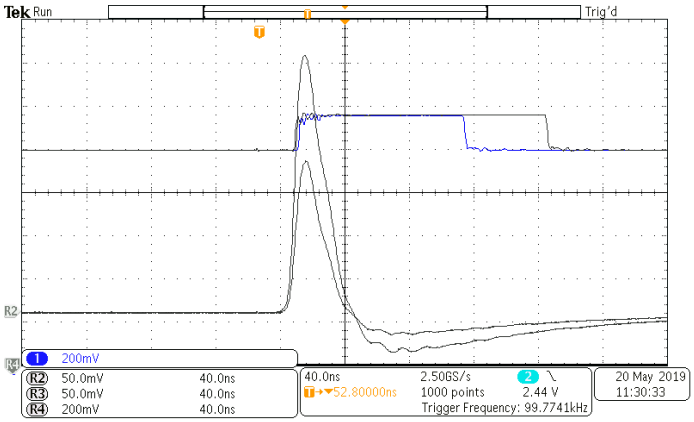


Figure 27 - Two signals at the DA3 output (bottom) and the corresponding LVDS outputs (top).

The absence of digital-to-analog coupling can be verified in the screen shot of Figure 27. It displays two analog signals at the DA3 and the corresponding digital output at the LVDS pads. As can be seen, the output of DA3 is not affected by the rising or falling edges of the digital output, demonstrating good separation of the analog and digital circuitry. The figure also illustrates the operation of the WADC: the length of the LVDS output signals corresponds to the amplitudes seen at the output of DA3. This measurement can, of course, only be done at the APD output of channel 7.

3.2.3 Gain of the ASD

Figure 28 shows the peak amplitudes[6] at the Analog Pad Driver (APD) versus input charge for two ASD2 chips and a legacy ASD1. The curves for the two ASD2 only show a small mismatch of up to 3 % at input charges > 50 fC, illustrating good process control of the 130 nm GF technology. The hatched line comes from simulation (at the schematic level), showing fair agreement with the measurements. The numeric values of amplitudes and gain are summarized in Table 11 (cf. 2.4.9.1).

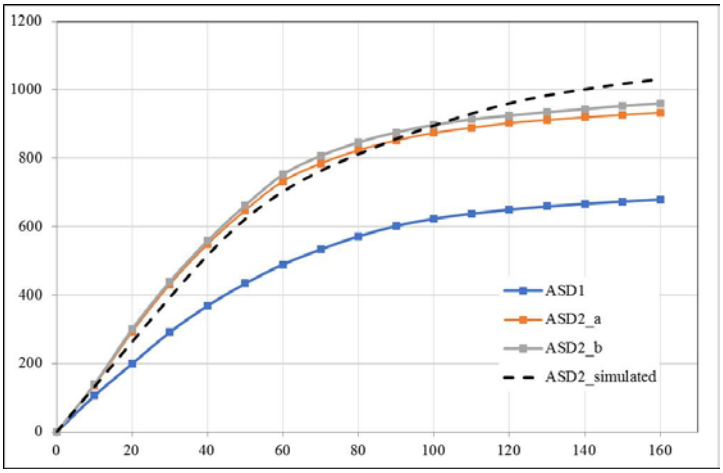


Figure 28 - Gain vs. Input Charge for two ASD2 (red, grey) and for an ASD1 chip.

[6] The peak amplitudes, as read from the APD output, are corrected for the APD gain of of -2.6 dB to present the amplitudes at the output of DA3.

Table 11 - Gain vs. input charge, measured at the DA3 output.

	measured		simulated		
Q	Peak voltage	Gain	Peak voltage	Gain	meas.-sim. gain
fC	*mV*	*mV/fC*	*mV*	*mV/fC*	
25	492	19.7	450	18.0	9.4%
50	877	17.5	850	17.0	3.2%
75	1079	14.4	1050	14.0	2.8%
100	1214	12.1	1250	12.5	-2.9%

3.2.4 Time Slewing versus Input Charge

The most relevant performance parameter for the determination of the MDT coordinates is the accuracy of the arrival time measurement of the electrons closest to the MDT wire, as discussed in sections1.2 and 2.4.9.1. The main error source does not come – by far – from the accuracy of the TDC, but from the fact that the amplitude of the signals, produced by the MDT tube, is vaying over a wide range, depending on the distribution of primary electrons along the track. Small signals take longer to reach the trigger threshold than larger ones. A short peak time and/or high gain of the DA3 output - at a given threshold - tend to mitigate this problem, the "time slewing effect".

As discussed in the previous section, the small-signal gain of ASD2 of 19.6 mV/fC, shown in Table 11, is in fair agreement with the simulated value of 18 mV/fC, presented in sect. 2.4.9.1 and exceeds the gain, specified in Table 3 of 8.9 mV/fC by a factor of two.

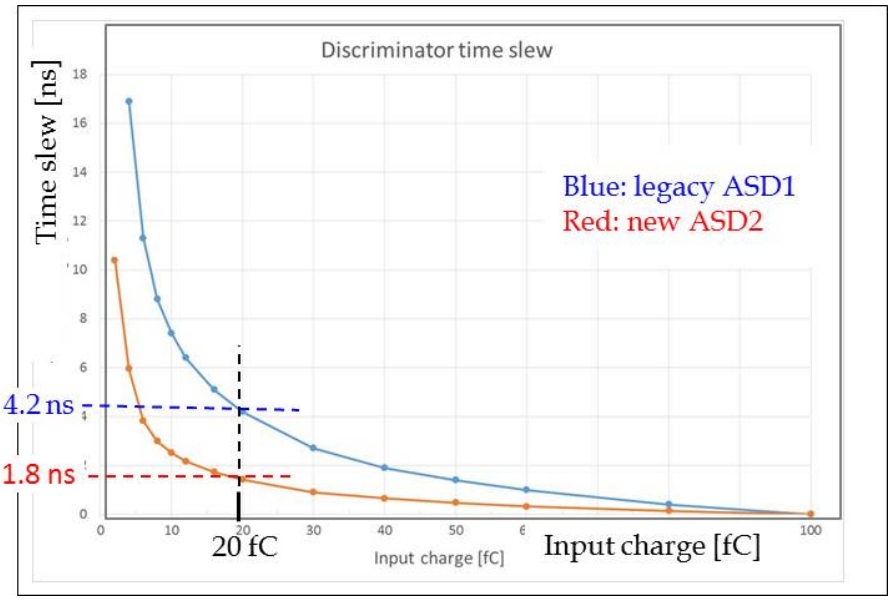


Figure 29 - Time slewing vs. Input Charge for ASD2 (red) and ASD1 (blue).

Figure 29 shows the measured time slewing for ASD2 (red) and for the "legacy" ASD1 (blue). Due to higher gain and shorter peak time, ASD2 provides less time slewing at a given input charge. At 20 fC, e.g., the slewing delay is about 2 ns compared to about 4 ns in ASD1. Given the average electron drift velocity of about 20 µm/ns, this corresponds to measuring errors of 40 µm and 80 µm for ASD2 and ASD1, respectively. Part of this effect can be corrected off-line, using the charge measurement of the WADC.

In summary, the data of Figure 29 indicate that offline corrections for "time-slewing" will be less important, once the new readout electronics with the ASD2 will be implemented in the Muon Spectrometer.

3.3 Length of the WADC Output versus Rundown Current Code

The charge detected by the WADC is translated into the time delay between leading and trailing edge of the discriminator output of the corresponding channel. The time delay is approximately proportional to the run-down current which, in turn, is inversely proportional to the resistance of the discharge resistor. This resistor can be selected to have 8 values, being controlled by a 3-bit code (bits [24:26] in Table 9.

Figure 30 (left) shows the width of the lvds output versus the 3-bit run-down current code for the 8 channels of an ASD2 chip. Ideally, all 8 trace would be on top of each other. Due to process variations there is a spread, increasing with increasing code (i.e. decreasing rundown current). At a typical operating code = 2 the spread among the 8 channels is 120 to 150 ns, which is acceptable for our application, as the measured charge is only used to correct for the slewing effect. Figure 30 (right) shows the same dependence for 3 different ASD2 chips. The spread among these 3 chips at operating code = 2 is again 120 to 150 ns.

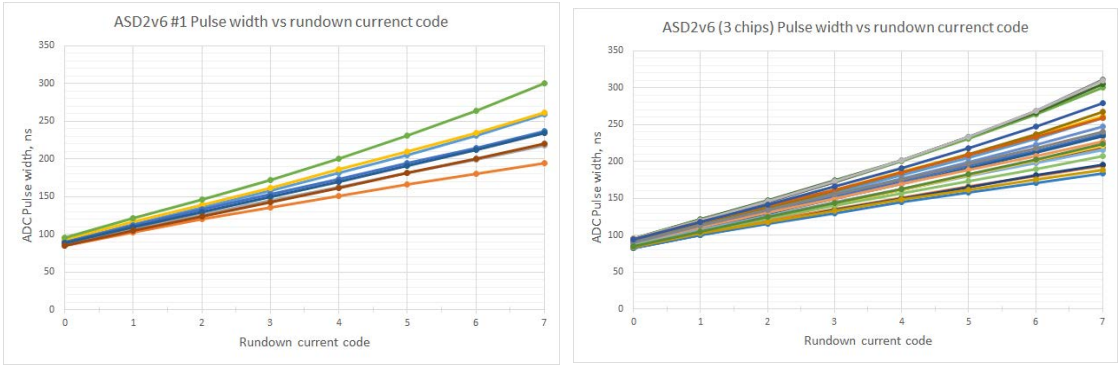


Figure 30 - Pulse width vs. Run-down code for the 8 channels of one (left) and of 3 chips (right).

3.4 The Programmable Deadtime versus Dead Time Code

As mentioned in Section 1.2, the discriminator can be disabled after a threshold crossing for a programmable time, which is controlled by a 3-bit code. This feature of the chip allows to supress multiple threshold crossings from the same track, leading to a reduction of the data load to the DAQ. Figure 31 presents the response of dead time vs. 3-bit code for the 8 channels of an ASD2 chip, showing a satisfactory match among the 8 channels. Depending on the code, the dead time can be selected between 40 and 800 ns in steps of 100 ns. As the maximum drift time of electrons in the MDT tubes (30 mm diameter) is about 750 ns, the programmable dead time covers the whole range of the drift time.

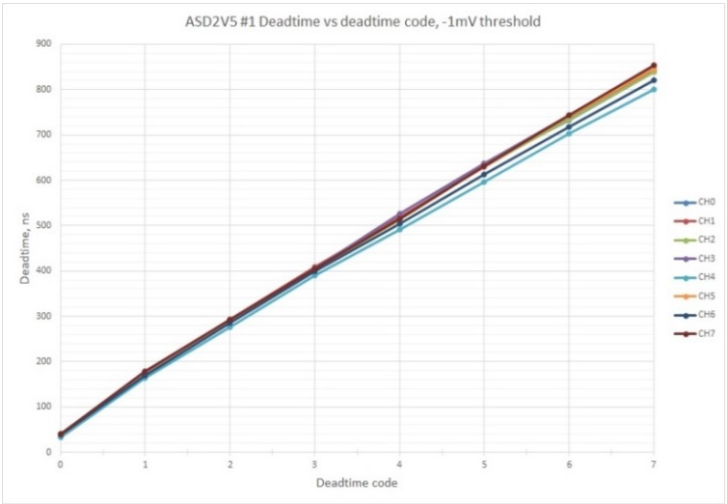


Figure 31 - Dead time vs. 3-bit code for the 8 channels of an ASD2 chip.

3.5 Threshold Scans

The following procedure was used to measure the noise of an ASD channel. A pulse with constant amplitude was injected into the *input* of the ASD with a constant frequency, like 10 kHz, while the frequency of the discriminator *output* was recorded as a function of the programmed threshold. Figure 32 shows results for one channel of the ASD2. Scanning the pulses by threshold steps from high to low, the output frequency is changing from zero to 10 kHz. At 5 kHz recorded rate, half of the hits is below and half above the applied threshold. The width of the S-curve corresponds to the noise on top of the test pulses, which is mainly due to the noise of the CSP and the rest of the analog chain[7].

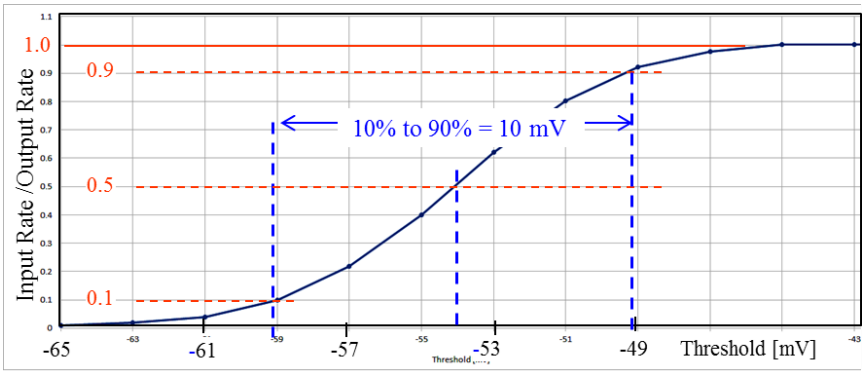


Figure 32 - Threshold scan for one channel of an ASD2 chip.

If the pulseheight distribution at the discriminator corresponds to a gaussian, the S-curve in Figure 32 represents the integral over its area. The FWHM of the gaussian is about 0.94 of the 10-90% range of the integral, and σ_{RMS} about 0.4 of this range. Looking at Figure 33, the 10-90% voltage range is 10 mV, leading to a FWHM of 9.4 mV and a σ_{RMS} of 4 mV. Based on the measured gain of 15 mV/fC, the σ_{noise} is about 0.27 fC, corresponding to 1700 e-, a factor of 3.5, better than specified in Table 3.

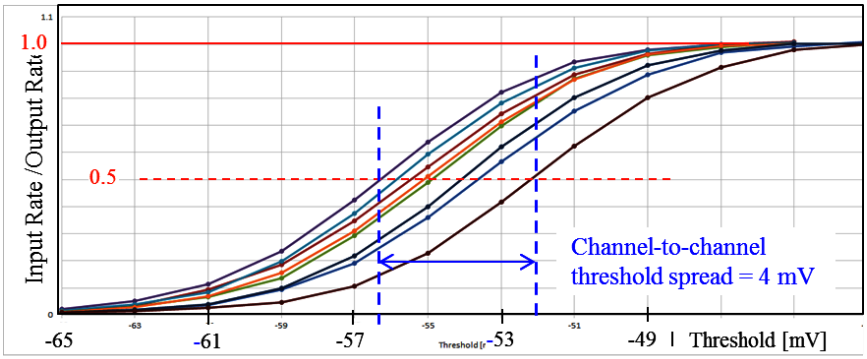


Figure 33- Threshold scan for all 8 channels of an ASD2 chip.

Ideally, all 8 channels of an ASD chip should produce an output signal, when more than 5 primary electrons (equivalent to a charge of about 1 fC) arrive at the wire of a MDT drift tube. As the discriminator thresholds, however, can not be adjusted individually for each channel, a sufficiently small threshold spread at a given theshold setting is essential for uniform detector operation. Threshold deviations to a higher value may reduce efficiency and increase slewing delays, while deviations in the opposite sense may increase the rate of noise hits.

Figure 33 shows the S-curves for 8 channels of an ASD2 chip. The maximum deviation between two channels is 4 mV, while the corresponding RMS-deviation of any channel from the average value is only about 1 mV, a factor 4 less than the RMS value of the noise.

The spread of the discriminator thresholds in the ASD2 is about a factor of 3-4 lower than in the case of the “legacy” ASD1. This improvement of the threshold matching is thought to be due to improvements of technology and process control in the 130 nm IBM/GF technology compared to the 500 nm Agilent technology, used for ASD1.

[7] If there was zero noise, the distribution would be a step, going from zero to one at the discriminator threshold.

3.6 Immunity against environmental effects

3.6.1 Radiation Background in the Experimental Hall: Tolerance vs. Total Ionizing Dose (TID)

The frontend electronics, containing the ASD2, is exposed to ionizing radiation caused by conversion of neutrons and γ-rays. The Total Ionizing Dose, accumulated in the Muon Spectrometer during 10 years of HL-LHC operation (i.e. for an event rate of about 4000/fb) is expected to be in the range 2-20 krad, depending on the location of the device in the detector. These numbers already contain "Safety factors" of about 15, representing uncertainties about effects like low dose rates, chip-to-chip variations and others (cf. appendix A in [4]).

To certify the ASD2 for sufficient tolerance against ionizing radiation, four chips were exposed in the CERN X-ray irradiation facility [20]. Two chips were irradiated up to 150 krad, while two others were irradiated up to 1 Mrad, the maximum dose available in this campain. Subsequent measurements did not reveal any changes w.r.t. pre-iradiation in any performance parameter, like peak time, gain, noise, ADC functionality or lvds output amplitudes.

As the tested dose of 1 Mrad exceeds the required TID level of 20 krad by a large factor, TID tolerance of the ASD2 for use in the Muon Spectrometer has been successfully demonstrated. This result is in accordance with predictions in a publication by F Faccio, CERN, about radiation damage in deep submicron CMOS [21].

3.6.2 Packaging, Power Dissipation and Junction Temperature

The ASD2 chip is packaged in a QFN-88 package with 10 * 10 mm^2 outer diameter and 0.4 mm pad pitch. Figure 34 presents the top and bottom view of the ASD2 package. A unique device number is attached to each chip, using a label with a 2D-bar. The rear side of the chip contains, inside the square of solder pads, a blank surface for good heat transmission through tight contact to the PCB. Figure 35 shows a readout card for the sMDT with three ASDs mounted.

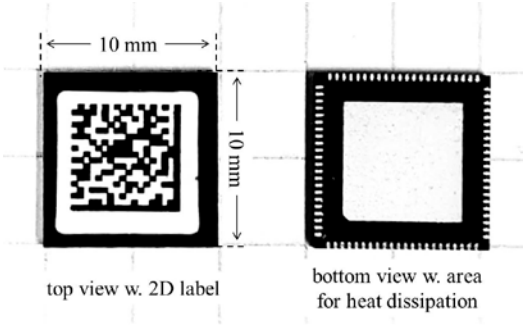


Figure 34 - Photo of the ASD2 package.

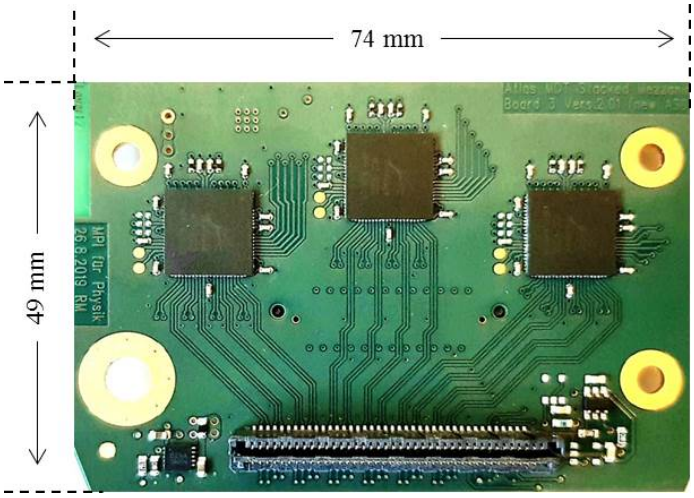


Figure 35 - 3 ASD2 mounted on a PCB for the sMDT readout.

Power consumption and expected junction temperature of the ASD2 were evaluated for supply voltages 3.3, 3.0 and 2.7 V. Figure 36 shows the corresponing temperatures of the QFN package and the dissipation of the heat in the PCB, measured with an IFR camera. Good heat dissipation in the PCB is essential for keeping a low junction temperature of the chip. It requires tight contact between package and PCB as well as sufficient copper inside the board. As seen in the Figure, temperatures of ASD case are around 45 °C. Conservatively, one can expect the real junction temperature to be below 50°C as the thermal resistance junction-to-case for this type of package is about 1 °C/W, see Ref. [22]. With the dissipated power of the ASD of 0.3 W this leads to a negligible difference of 0.3 °C between the measured case temperature and the junction temperature. With the maximum operating temperature of the chip being specified as 120°C, the measured values around 50°C provide sufficient safety margin and concerns about chip lifetime can be safely discarded.

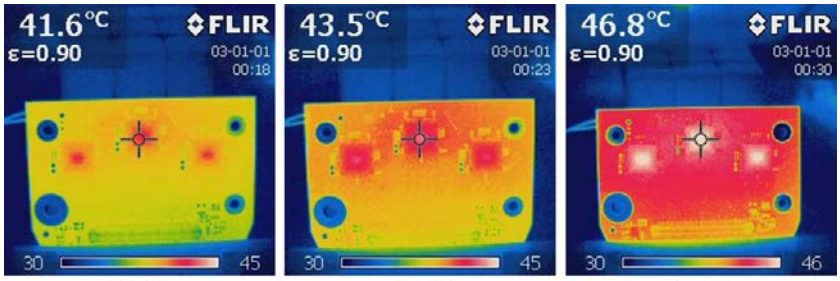


Figure 36 - Temperature distribution on the PCB of Figure 35, operated at 3 supply voltages.

Table 12 gives power consumption and temperatures measured on the QFN88 package as shown in Figure 36. The operating voltage of 3.0V has been selected for V_{cc}. Tests have shown that this reduction of the supply voltage does not result in any significant performance degradation compared to operation at 3.3 V.

Table 12 - Power consumption of the ASD2 vs. supply voltage V_{cc}.

Vcc	Current	Power/ASD		$T_{package}$
V	*mA*	*mW*	*%*	*°C*
3.3	116	382	49%	47
3	85	256	0%	43.5
2.7	70	189	-26%	41.5

The simulated power consumption of the ASD2 subsystems is listed in Table 13, showing good agreement with measurements.

Table 13 - Power consumption of the ASD components from simulation.

Function	Name	Operation @ 3.3 V		Operation @ 3.0 V	
		I / chip	N / chip	I / chip	N / chip
		mA	*mW*	*mA*	*mW*
Charge Sensing Preamp	I_{VDD1}	31.5	104.0	28.6	85.8
Shaping Stages DA1-DA3	I_{VDD2}	28.7	94.7	26.1	78.3
Discriminators & WADC	I_{VDD3}	43.1	142.2	39.2	117.6
MUX & LVDS Drivers	I_{VDDA}	17.1	56.4	15.6	46.8
Common Block	I_{VDDX}	1.1	3.6	1	3.0
External Bias	I_{BIAS}	0.09	0.3	0.08	0.2
Total Current & Power simulated		122	401	111	332
Total Current & Power measured		121	**399**	102	**306**

4 Summary

Design, implementation and measured performance of the new ASD2 have been presented in this manual. Compared to the previous version of this chip (ASD1), presently used for the readout of the MDT chambers, the ASD2 shows improved performance in critical analog parameters like gain and peak time. Noise and threshold spread, both limiting for efficiency and time resolution, could bereduced by factors of about 2 and 4, respectively. In combination with the shorter peak time, this leads to a reduction of the time slewing effect for detector signals with small amplitude, resulting in substantially improved spatial resolution campared to ASD1. Figure 37 shows the spatial resolution in MDT chambers as measured with muon tracks of 150 GeV as a function of …

The immunity of the chip against ionizing radiation has been verified at the CERN X-ray facility. While a TID of up to 20 krad is anticipated for the "hottest" regions of the muon spectrometer, tests up to 1 Mrad did not show performance degradation of the chip in any measured parameter.

The effectiveness of HV protection was tested with a pulser, injecting negative and positive going pulses with up to 3 kV into the protective network, implemented inside and outside the chip, but no damage to the tested devices could be detected.

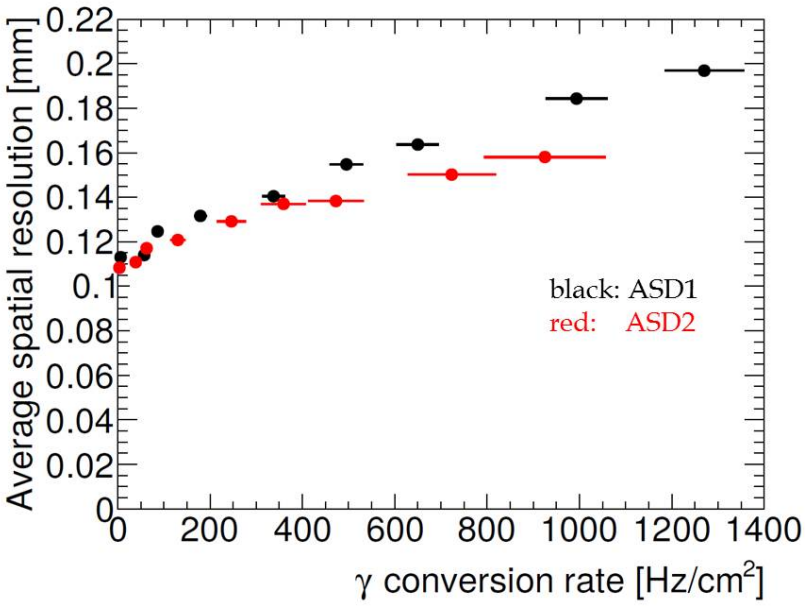


Figure 37 - Spatial resolution of ASD1 and ASD2 vs. background rate in a testbeam.

Known functional problems of ASD1, like amplitude instabilities of the LVDS outputs in response to small noise hits (causing the "pair mode problem" in the TDC) have been corrected.

Full production was ordered with GF in 2019, and three 12' wafers with about 3500 chips each were received as a preseries ("engineering run"). Presently, 7000 packaged chips are in the process of testing. Results from a sample of about 10% indicate a yield of > 99%.

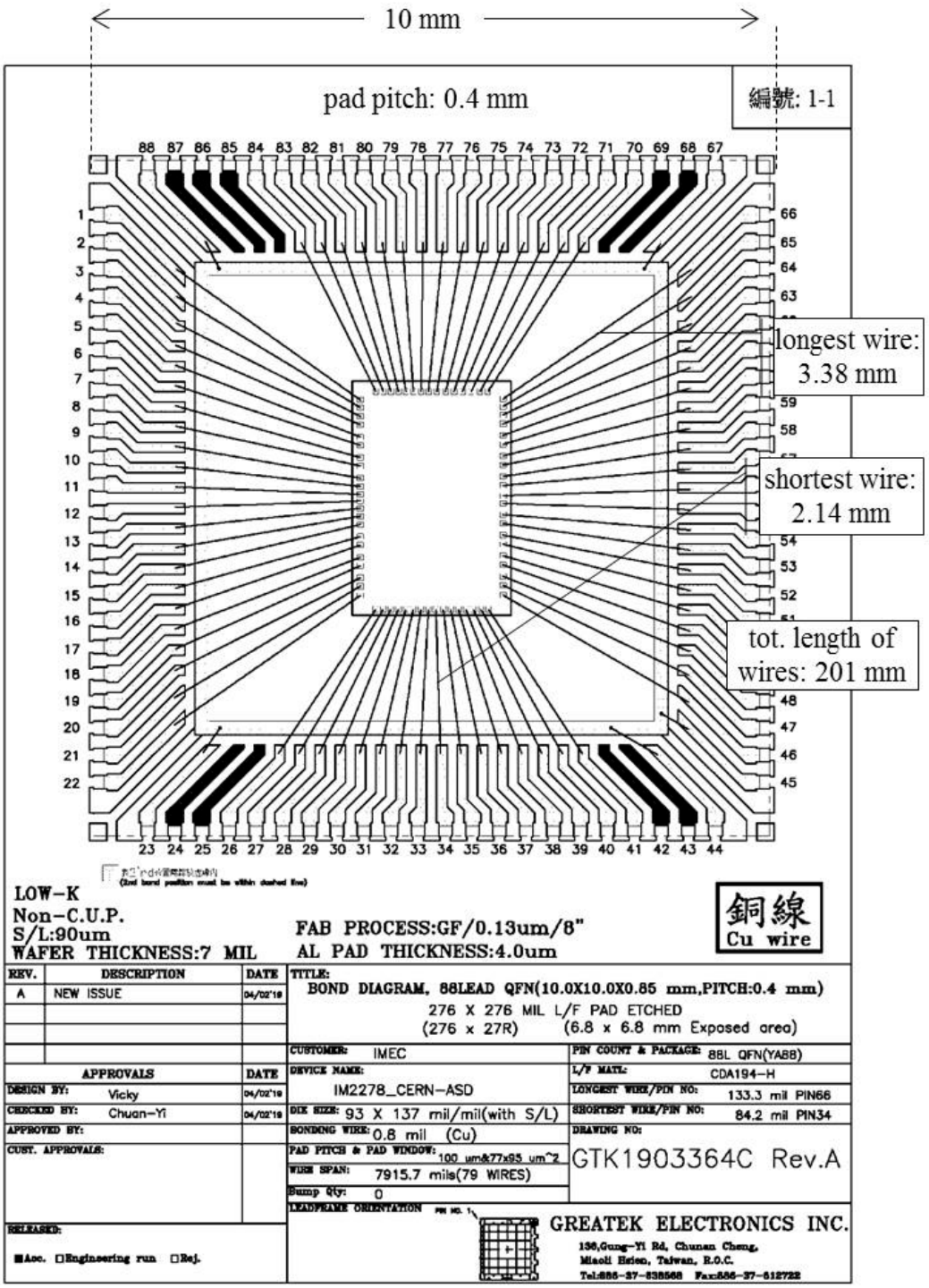
5 Appendix – Packaging Information

5.1 Pin out Diagram of ASD2

The different groups of supply voltages and corresponding grounds have been chosen to minimize coupling among the functional blocks of the chip (cf. Figure 4), in particular between the analog and the digital part. Thus VDD1 and GRND1 serve the CSP, while VDD2 supplies power to the amplification and shaping stages DA1, DA2 and DA3. VDD3, VDD_BUFF and VDD_JTAG serve the discriminator, the APD and the slow digital control system ("JTAG"). The pins ANAA and ANAB are the analog outputs of the APD, which allow to monitor the output of shaping stage DA3 (cf. section 2.4.6).

		THERMAL PAD	NO CONN	NO CONN	NO CONN	VDD1	GND1	GND1	VDD1	VDD2	GND2	GND3	VDD3	SCLK	SIN	SOUT	SDOWN	SHIFT	SLOAD	VDD_JTAG	NO CONN	NO CONN	THERMAL PAD
		88	87	86	85	84	83	82	18	80	79	78	77	76	75	74	73	72	71	70	69	68	67
VDD1	1																						66 VDDA
GP	2																						65 VSSA
NO CONN	3																						64 OUTA0
INA0	4																						63 OUTB0
NO CONN	5																						62 OUTA1
INA1	6																						61 OUTB1
NO CONN	7																						60 OUTA2
INA2	8																						59 OUTB2
NO CONN	9																						58 OUTA3
INA3	10																						57 OUTB3
GND_BIAS	11																						56 GNDX
Ib_10µ	12																						55 VDDX
VDD_BIAS	13																						54 OUTA4
NO CONN	14																						53 OUTB4
INA4	15																						52 OUTA5
NO CONN	16																						51 OUTB5
INA5	17																						50 OUTA6
NO CONN	18																						49 OUTB6
INA6	19																						48 OUTA7
NO CONN	20																						47 OUTB7
INA7	21																						46 GND_JTAG
VDD1	22																						45 THERMAL PAD
		23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
		THERMAL PAD	NO CONN	NO CONN	GND_PAD	VDD_PAD	GND1	VDD1	GND1	BIT_BUFF	VDD2	GND2	VDD3	GND3	VDD_BUFF	VSS_BUFF	ANAA	ANAB	VDDA	VSSA	NO CONN	NO CONN	THERMAL PAD

5.2 Bonding protocol for the ASD (supplied by the GREATEK company)



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