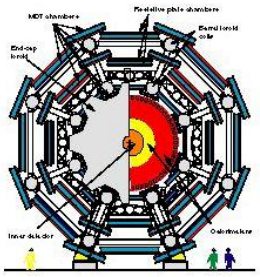

MiniDAQ04.1 Guide

University of Michigan

November 6, 2003

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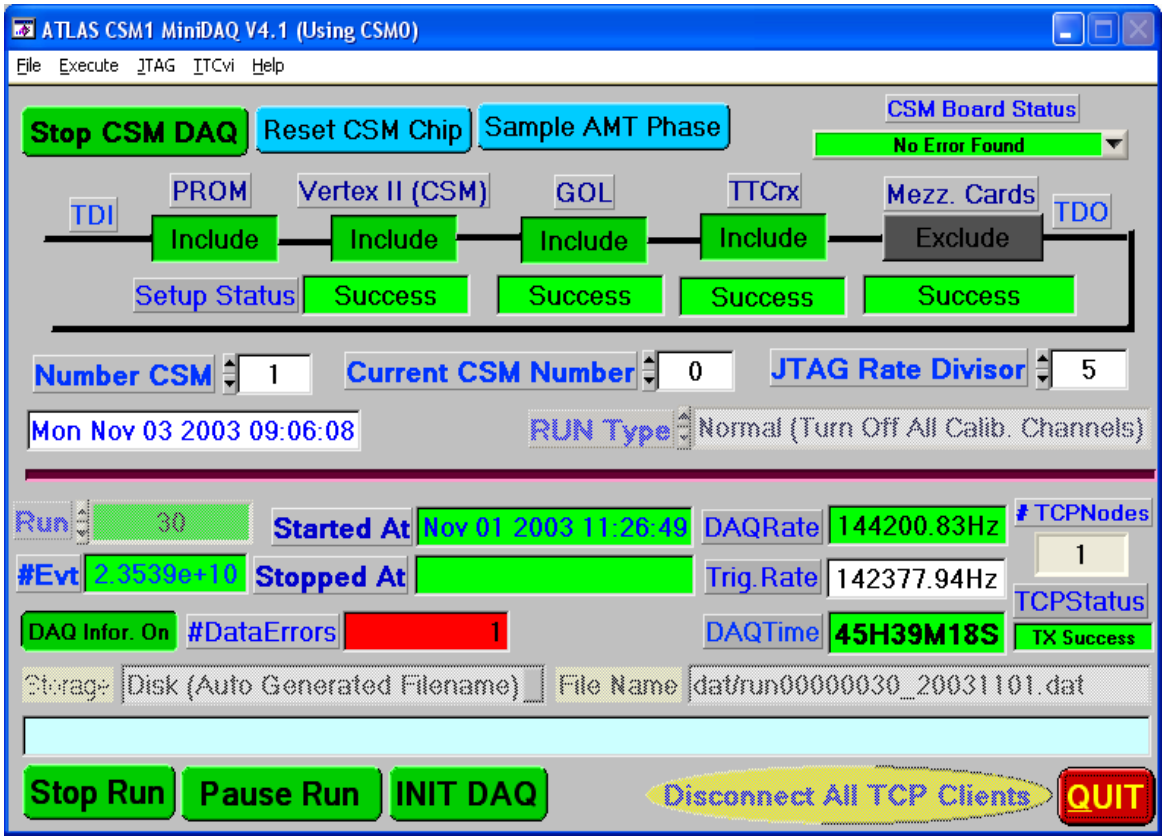


Contents

1 Introduction to the MiniDAQ04.1

MiniDAQ04.1 program is software developed at the University of Michigan using National Instruments LabWindows/CVI (part of Measurement Studio) for using with the CSM1 module. The purpose of the program is to provide an easy way for user by using windows interface for accessing to the CSM1 JTAG chain including the AMT mezzanine cards and to control TTCvi and for controlling data acquisition card (GOLA card) at Linux box via TCP/IP. This program has three major functions: DAQ control, JTAG programming and TTCvi control.

The MiniDAQ04.1 program is developed for CSM1 Card (including GOL and TTCrx) and Octal Mezzanine Card where AMT2/AMT3 is used. More detailed information on the CSM1, the GOL, the TTCrx, the AMT and the ASD can be found in their respective manuals[1] [2] [3] [4] [5] [6]. This guide is designed to be a guide to users new to the MiniDAQ04.1 program and combine the most commonly needed aspects of several sources into one concise guide.

This guide assumes you are using a National Instruments VME interface for the CSM0 module (JTAG Driver) and the TTCvi module. If you are not using a National Instruments compatible controller card, the JTAG controller (CSM0) and the TTCvi Control will not work from the standard MiniDAQ04.1 program distribution and the code will need to be modified to take into account the different driver.

Any suggestion and comment are welcome. Also if you have any problem, please contact T.S. Dai at daits@umich.edu.

Installation and Build Option:

To install the MiniDAQ04.1 program, first get the MiniDAQ04.1 program distribution kit from http://atlas.physics.lsa.umich.edu/docushare/dscgi/ds.py/View/Collection-299/ . Then run the **setup.exe** where user is able to modify the installation path.

Starting the MiniDAQ04.1:

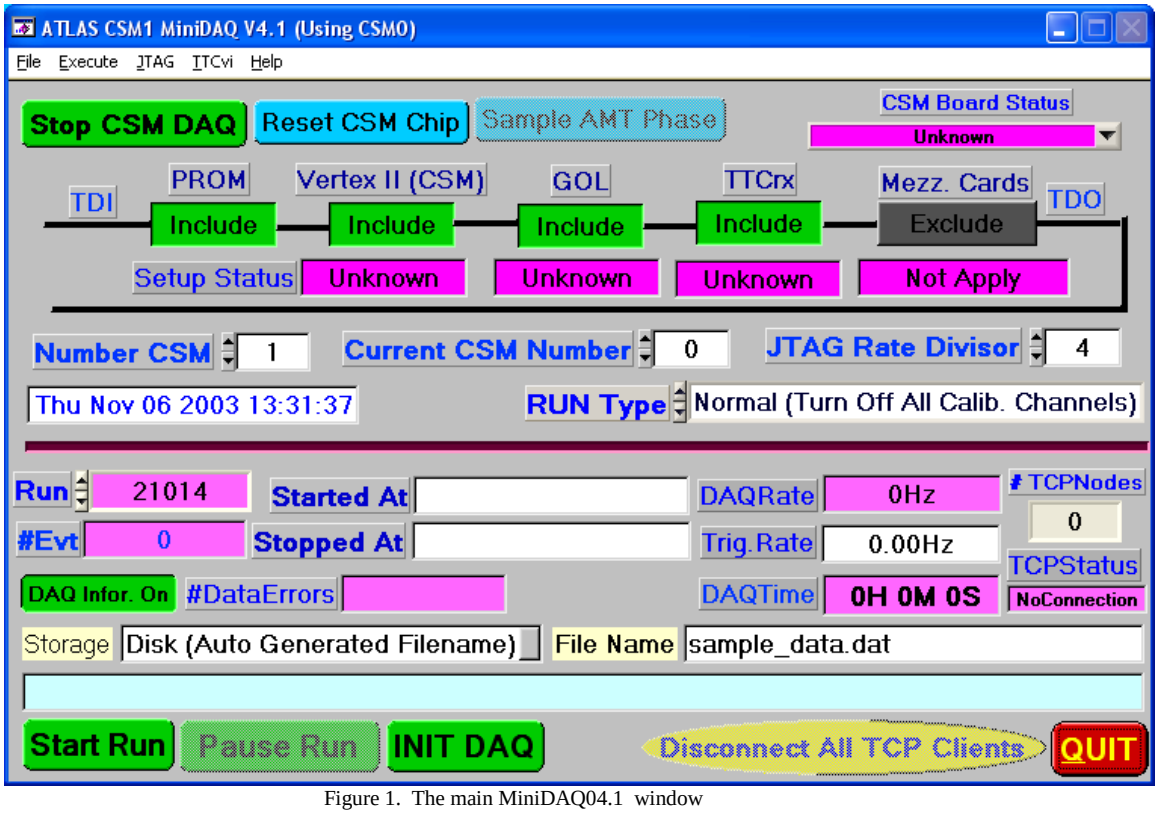
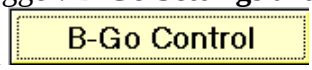


Figure 1. The main MiniDAQ04.1 window

The MiniDAQ04.1 program is started with the file DAQControl.exe, which will automatically locate the CSM0. If multiple CSM0 are found, user will be asked to select the CSM0. The main MiniDAQ04.1 window is shown in Figure 1. The program will automatically search known JTAG devices with different JTAG clock speed and setup the JTAG chain. If no valid JTAG device is found, the program will automatically recall previous JTAG chain from the parameter file <DAQControlpara.txt>. If default settings are saved by user, the default settings will be loaded.

The program will automatically scan all available TTCvi boards in the VME crate if one can not access TTCvi board by using previous TTCvi BASE address. If only one TTCvi board is found, the board will be used, otherwise user will be asked to provide additional information (i.e. TTCvi BASE address). If no valid TTCvi board is found, the DAQ system will not work.

All of the necessary commands to modify the settings for all devices in CSM1 JTAG chain (CSM1, TTCrx, GOL and AMT mezzanine card) are in the **JTAG** pull-down menu, including the JTAG diagnostic panel. The setups can be saved and be recalled from the **File** menu. DEFAULT setups could be saved or removed from the **File** menu. If a DEFAULT setups are saved, this DEFAULT setups will be recalled at startup of the program and user will be prompted to confirm downloading the settings to the hardware. Varies setting for DAQ are saved into action file with file extension "act" and JTAG operations are saved into sequence file with file extension "seq" by invoking **JTAG → Generate All Action/Sequence Files for DAQ.**

TTCvi module is controlled via pull-down menu **TTCvi.** It is user responsibility to setup TTCvi via **TTCvi → Status and Control** for varies operation, mainly to select run type and trigger. **B-Go Settings** and **B-Go FIFO** are invoked by **TTCvi → B-Go Control** or button 

in TTCvi Control window.

Use **Help** pull-down menu to obtain online help for command buttons and menu items. After select the menu item **Help on Buttons**, click on any wanted command button or menu item, where a brief description of the item functionality will be popped out for user to view.

3 JTAG Programming

3.1 Connecting the hardware

It is user responsibility that the VME hardware has been initialized with the NI Resource Manager and that all CSM0 and TTCvi modules are include in the device, where CSM0 module requires A32 address space and the TTCvi module requires A24 address space.

Following are the hardware list:

1. CSM1 board;
2. CSM motherboard;
3. 5 V power supplier for CSM1 and power cable;
4. CSM0 board;
5. JTAG adaptor board;
6. 5 V power supplier for JTAG adaptor and power cable;
7. TTCvi board;
8. TTCvx [8] board or TTCvi MiniCrate;
9. 2 RJ45 cables to connect CSM0 JTAG ports with JTAG adaptor JTAG ports;
10. 20 pin flat cable to connect JTAG adaptor JTAG signals with CSM1 JTAG signals (Connector HS1 at CSM motherboard);
11. Optical cables.

Assuming that TTCvx is used together with TTCvi, the hardware is arranged as:

- Install TTCvi, TTCvx and CSM0 into VME crate;
- Connect TTCvi and TTCvx using NIM cables: **a**) TTCvx Clock Out to TTCvi Clock In; **b**) TTCvi Channel Out A to TTCvx Channel In A; **c**) TTCvi Channel Out B to TTCvx Channel In B; **d**) Connecting necessary L1A In and B-Go In;
- Connecting CSM0 and JTAG adaptor by using 2 RJ45 cables (CSM0 JTAG OUT to JTAG adaptor JTAG IN, and CSM0 JTAG IN to JTAG adaptor JTAG OUT);
- Using 20 pin flat cable to connect JTAG adaptor U2 with CSM1 motherboard HS1;
- Install CSM1 on its motherboard;
- Fiber optical connections with CSM1: **a)** TTCvx Optics Output (anyone of 4) to CSM1 Optical Input; **b)** CSM1 Optical Output to GOLA card Optical Input;
- Supply 5V to JTAG adaptor and CSM1 motherboard.

The possible JTAG devices in the JTAG chain are PROM, Vertex-II, GOL, TTCrx and AMT Mezzanine Cards which could be selected from main CSM1 JTAG Control window as shown in Figure 1. The JTAG devices will be automatically searched at the starting phase of the program, if there is no valid JTAG device, previous JTAG chain will be used. Or user could include or exclude a device in the JTAG chain, simply by clicking at the include/exclude button for corresponding JTAG device at **TDI--TDO** line, where Exclude means that the device(s) is/are not in the JTAG chain and Include means that the device(s) is/are attached in the JTAG chain. If any JTAG device is

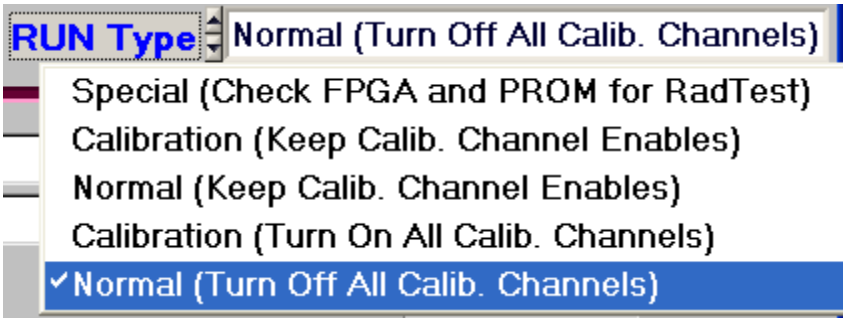
removed or added in the JTAG chain, it is user responsibility to set the JTAG chain in the main CSM1 JTAG Control window same as the hardware before the JTAG operation, otherwise the downloading setup will not work. The JTAG chain could be established via **JTAG → Setup JTAG Chain** and user is encouraged to use it.

Be sure the power is applied before starting JTAG programming.

*3.2 **DAQ** Control and **JTAG** Menu*

DAQ Control

The first step for DAQ control is to select the run type via **Run Type** button as shown in left figure. Four different run types have been defined:



1. **Normal (Turn Off All Calib. Channels):** normal DAQ run, where all calibration channels are disabled from ASDs (recommended for normal run);
2. **Calibration (Turn On All Calib. Channels):** calibration run, where all calibration channels are enabled from ASDs (recommended for calibration run);
3. **Normal (Keep Calib. Channel Enables):** normal DAQ run, it is user responsibility to turn on/off calibration channels;
4. **Calibration (Keep Calib. Channel Enables):** calibration run, it is user responsibility to turn on/off calibration channels;
5. **Special (Check FPGA and PROM for RadTest):** special case for radiation test, where the CSM status, FPGA and PROM will be checked continuously.

The initialization procedure for CSM1 and mezzanine cards should be as following:

1. Get CSM Status and Check the Status. If any CSM Error, perform Reset CSM Error or Reset CSM (Need wait at least 0.800 second);
2. Download CSM and TTCrx and Enable Mezzanine Card JTAG;
3. Download AMT (Clock On);
4. Download ASD;
5. Download CSM and GOL;
6. Sample AMT Phase;
7. Download AMT (Clock as user setting);
8. Download ASD;
9. Get CSM Status and Check the Status.
10. Initialize GOLA card at Linux Box if it connected;

The operation procedure for sampling AMT phase is defined as:

1. Download AMT (Clock On);
2. Download ASD;

3. Sample AMT Phase;
4. Download AMT (Clock as user setting);
5. Download ASD;
6. Get CSM Status and Check the Status.

And go through following steps to start CSM1 DAQ:

1. Turn Off Mezzanine Card JTAG Signals;
2. Start CSM DAQ;
3. Get CSM Status and Check the Status.

Similar operation procedure to stop CSM1 DAQ:

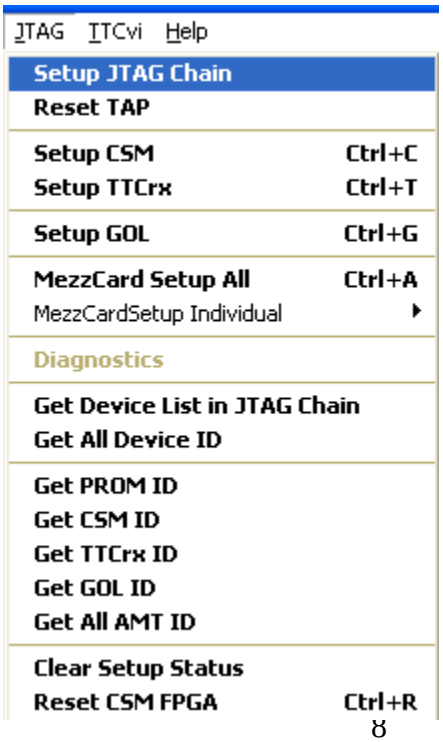
1. Stop CSM DAQ;
2. Get CSM Status and Check the Status.

To program individual JTAG device in the JTAG chain, the JTAG pull-down menu has to be used. If it is not needed to change the individual JTAG device settings, few predefined few control buttons in JTAG Control Main Window could be used to perform specified operation:

- INIT DAQ: initializes the DAQ and issues event counter reset and bunch counter reset if TTCvi is presented;
- Start CSM DAQ: enables CSM1 to collect data from mezzanine cards;
- Stop CSM DAQ: disables CSM1 to collect data from mezzanine cards;
- Sample AMT Phase: samples AMT Phase;
- Reset CSM Chip: performs a reset on CSM1 FPGA;

JTAG Menu

The JTAG devices are programmed through their JTAG port connections by using the **JTAG** pull-down menu as shown in the right picture. Also simple diagnostics tool has been provided. Loading an individual mezzanine card (**MezzCardSetup Individual)** is enabled only after mezzanine cards have been initialized with common settings.



- **Setup JTAG Chain** searches the JTAG devices and setup JTAG chain correspondingly.
- **Reset TAP** issues a TAP reset sequence (Test-Logic-Reset)
- **Setup CSM (CTRL-C)** brings up the CSM1 setup panel for user to program it.
- **Setup TTCrx (CTRL-T)** brings up the TTCrx setup panel for user to program it.

- **Setup GOL (CTRL-G)** brings up the GOL setup panel for user to program it.
- **MezzCard Setup All (Ctrl-A)** will call mezzanine card setup panel where user is allowed to modify the settings before they are downloaded to mezzanine cards. All mezzanine cards are programmed to the same settings.
- **MezzCardSetup Individual** will let user to select individual mezzanine card to be programmed.
- **Diagnostics** is not supported yet.
- **Get Device List in JTAG Chain** will automatically search for the JTAG devices in the JTAG chain.
- **Get All Device ID** will read out all JTAG device IDCODE according the JTAG chain settings.
- **Get PROM ID** will get PROM IDCODE.
- **Get CSM ID** will get Vertex-II IDCODE.
- **Get TTCrx ID** will get TTCrx IDCODE.
- **Get GOL ID** will get GOL IDCODE.
- **Get All AMT ID** will get all AMT IDCODE.
- **Clear Setup Status** clears setup status to "Unknown".
- **Reset CSM FPGA** performs a FPGA chip reset or reset CSM1 board.

Each JTAG device's setup status is shown in corresponding status window, there are three cases: "Unknown" means the settings are not downloaded through JTAG, and "Success" means that the JTAG setup bit stream is downloaded without error, and "Failed" means that the downloaded JTAG setup bit stream is not same comparing with returned bit stream. The CSM1 board status is also shown in the main JTAG control window.

JTAG clock period is determined by JTAG Rate Divisor, which could be set from 0 to 7 from JTAG Control Main Window as shown in Figure 1. Table 1 shows the corresponding JTAG clock period at varies JTAG rate divisor vale.

JTAG Rate Divisor	0	1	2	3	4	5	6	7
JTAG Clock Period(ns)	50	100	200	400	800	1600	3200	6400

Table 1. JTAG Rate Divisor vs JTAG Clock Period

If the JTAG rate divisor is smaller than default value of 4, the JTAG may not work properly.

In case there is a power outrage or any new JTAG device is added, for instance connecting a new mezzanine card, a "TAP Reset" should be issued, otherwise JTAG operation may get problem.

3.3 *Program CSM*

The CSM setup can be programmed via **JTAG → Setup CSM** which brings up the CSM setup panel as shown in Figure 2. The CSM setup panel includes two parts: CSM board status and settings. If the CSM board status is invalid due to JTAG error, no CSM status will be displayed, where the status background will be black. The green or white

background indicates normal CSM status and the red background indicates abnormal CSM status where user must be pay attention on it. It is very easy to change the CSM settings by clicking toggle button or selecting desired parameter. For normal DAQ operation, except the mezzanine card enable/disable and CSM DAQ enable/disable, unacceptable setting is indicated by red background, warning on setting is indicated with yellow background, and acceptable setting is indicated by green or white background.

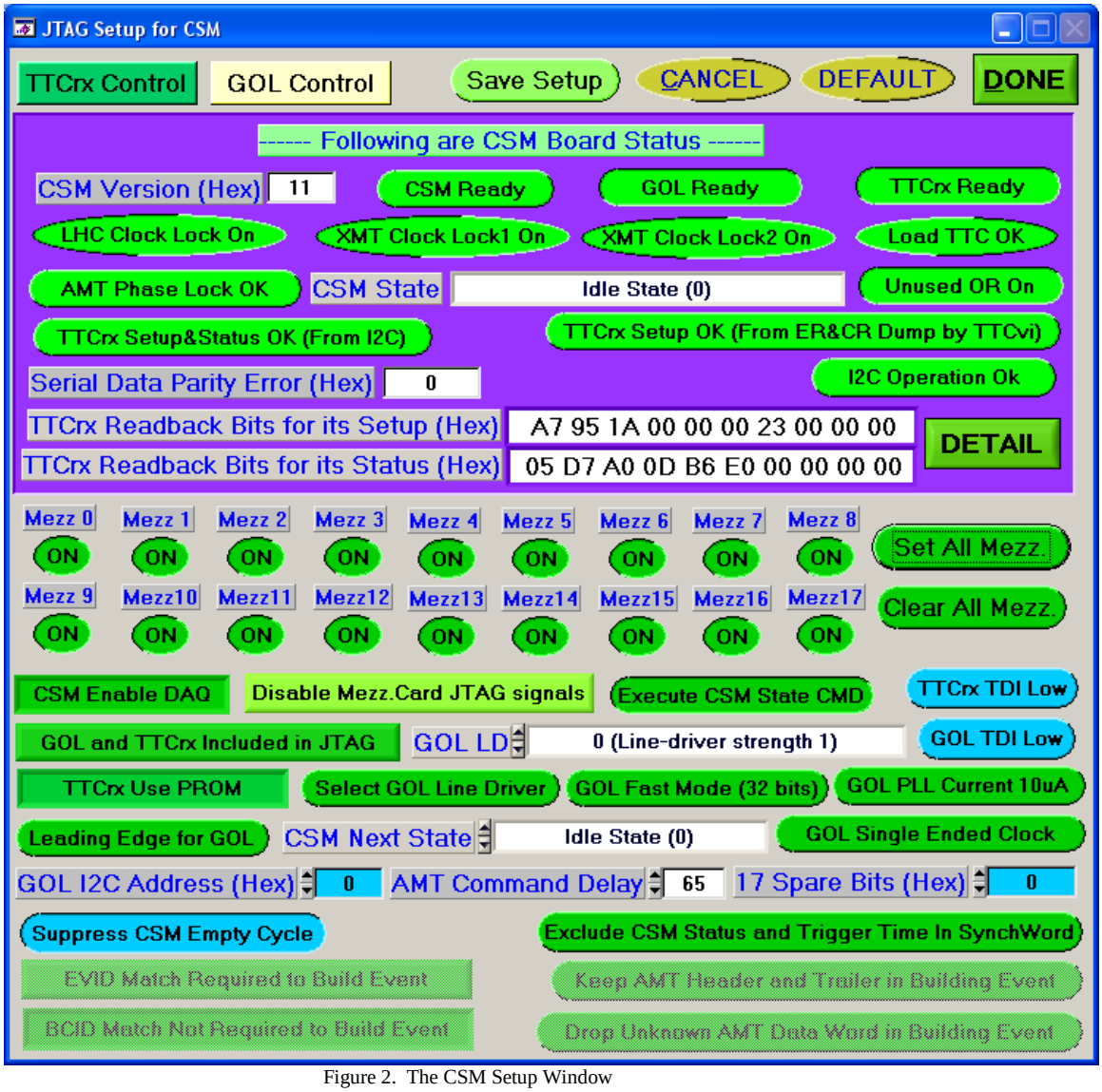


Figure 2. The CSM Setup Window

- DONE will download CSM1 and TTCrx setups to CSM1 (Vertex-II), where other JTAG devices are in BYPASS mode. The status of JTAG download is indicated at the main JTAG control window as shown in Figure 1;
- DEFAULT will bring the default settings;
- CANCEL will cancel any changes in CSM1 setup and quit from CSM setup panel;

- Save Setup will save CSM setup into a text file where user will be asked to give a file name;
- TTCrx Control will bring up the TTCrx setup panel;
- GOL Control will bring up the GOL setup panel which is only enabled when GOL is included in the JTAG chain.
- DETAIL will show the detail information of TTCrx read back bits for its setup and status, and bring up the TTCrx Internal Register Information Window as shown in Figure 3. There are 10 R/W registers and their results are displayed as binary format where the top binary number is the setting value and the bottom binary number is the read back value. It requires I2C to read back the TTCrx status and 3 configuration registers. For the 7 TTCrx internal registers shown in Figure 3, it also could be verified by using TTCrx Internal addressed commands ERDUMP (sub-address 4) and CRDUMP (sub-address 5) via TTCvi B Channel where the TTCrx parallel output bus must be enabled. The results are shown in Figure 3 from I2C.

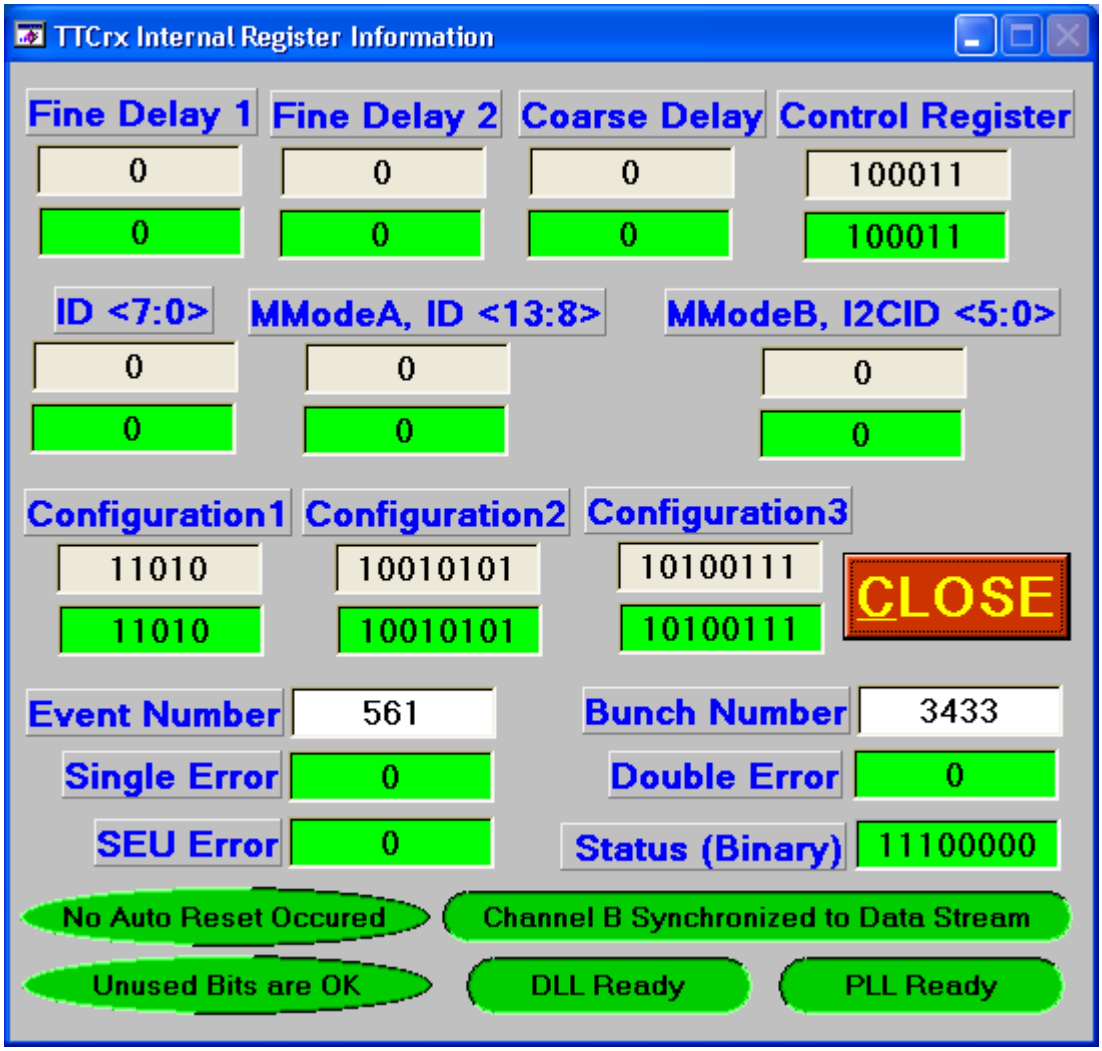


Figure 3. The TTCrx Internal Register Information Window

Maximum 18 mezzanine cards are allowed to connect to one CSM1, and each mezzanine card could be turned ON or turned OFF from CSM1. Any data from disabled mezzanine card(s) is ignored by CSM1, therefore wanted mezzanine card must be enabled. To program mezzanine card(s), the JTAG signals to mezzanine card must be turn on with Enable Mezz.Card JTAG signals. Enable/Disable DAQ at CSM1 is controlled by a toggle button, it is recommended to turn off mezzanine card JTAG signal Disable Mezz.Card JTAG signals if DAQ is enabled at CSM1. The CSM empty cycle could be included or excluded in the data transmission, it is recommended to suppress the CSM empty cycle by Suppress CSM Empty Cycle unless the CSM empty cycle is necessary. It is an option to include or exclude the CSM status and trigger timing information in the CSM synchronization word (so called D-word), see "*CSM1 User Manual* '' [1] for details. The AMT Command Delay is number of clock ticks (1 tick = 25ns), where the AMT commands include level 1 trigger, event counter reset, bunch counter reset and AMT global reset. The default value of the AMT Command Delay is set to 65 (=1625ns), it is necessary to adjust AMT settings and TTCrx settings (Clock 1 Coarse/Fine Delay) if the AMT Command Delay value is changed.

Specific CSM state could be selected from CSM Next State listing button as shown in Figure 4. To execute a selected CSM State Command, Execute CSM State CMD must be selected.

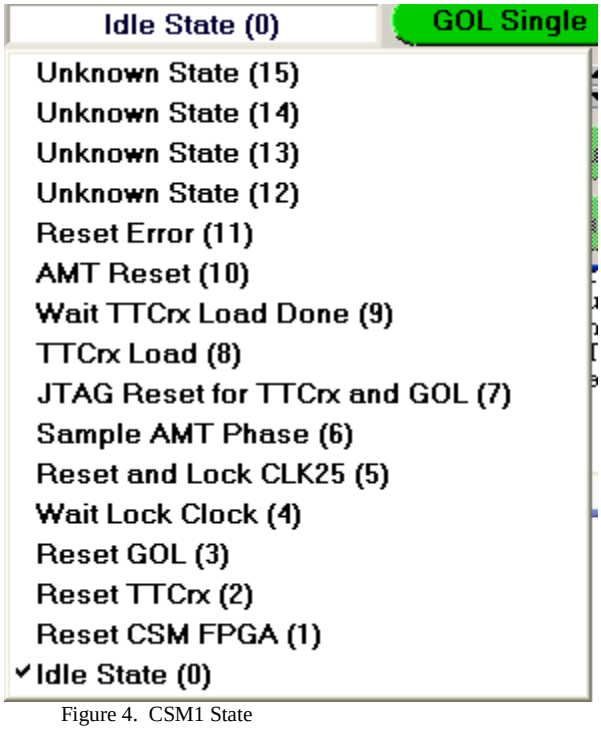


Figure 4. CSM1 State

GOL and TTCrx Included in JTAG must be set ff GOL and TTCrx chips are in JTAG chain. Since the CMS1 FPGA acts as a PROM for downloading TTCrx settings, it is better to turn on corresponding enable bit by selecting TTCrx Use PROM.

There are four buttons for EVENT builder version of CSM1:

- Enable/Disable EVID Matching;
- Enable/Disable BCID Matching;
- Keep/Discard TDC header and trailer;
- Keep/Discard Unknown AMT data word.

For rest CSM1 settings, it is recommended to select **GREEN** settings.

3.4 *Program TTCrx*

The TTCrx setup can be programmed via **JTAG → Setup TTCrx** which brings up the TTCrx setup panel as shown in Figure 5.

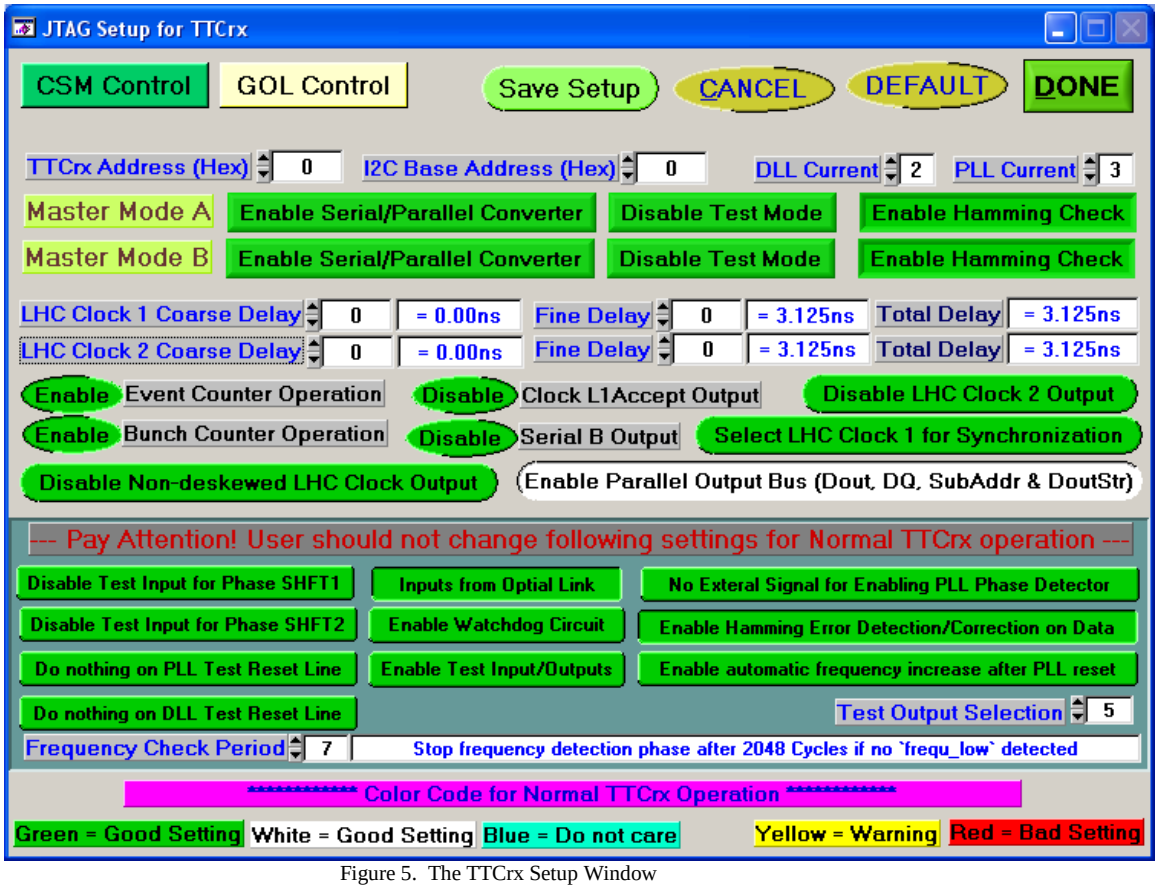


Figure 5. The TTCrx Setup Window

- DONE will download CSM1 and TTCrx setups to CSM1 (Vertex-II), where other JTAG devices are in BYPASS mode. The status of JTAG download is indicated at the main JTAG control window as shown in Figure 1;

- DEFAULT will bring the default settings;
- CANCEL will cancel any changes in TTCrx setup and quit from TTCrx setup panel;
- Save Setup will save TTCrx setup into a text file where user will be asked to give a file name;
- CSM Control will bring up the CSM setup panel;
- GOL Control will bring up the GOL setup panel which is only enabled when GOL is included in the JTAG chain.

Many TTCrx settings are for test only which are put together in TTCrx setup panel, user should not make any change on those settings at normal operation. The color code for normal TTCrx operation is following:

- Green or white background == good setting;
- Blue background == do not care;
- Yellow background == warning;
- Red background == Unacceptable setting.

For most normal TTCrx operation with CSM1, TTCrx settings as shown in Figure 5 are sufficient. If one wishes to individualize the TTCrx address must be set to none zero value (button TTCrx Address (Hex)). I2C base address could be set to any value. The Master Mode A/B must be set with disable test mode and enable serial/parallel converter and enable hamming check. For event builder version of CSM1, Event Counter Operation and Bunch Counter Operation must be enabled. For calibration run, Enable Parallel Output Bus (Dout, DQ, SubAddr & DoutStr) should be selected. If LHC Clock 1 Coarse Delay value is modified to none zero value, the AMT Command Delay value at CSM setup or AMT settings should be adjusted. The settings inside the "**Pay Attention! …**" box must not be changed for normal TTCrx operation.

3.5 *Program GOL*

The GOL setup can be programmed via **JTAG → Setup GOL** which brings up the GOL setup panel as shown in Figure 6.

The GOL setup panel includes two parts:

1. Hardwired GOL settings and GOL status. If the GOL status is invalid due to JTAG error, no GOL status will be displayed, where the status background will be black. The green or white background indicates normal GOL status and the red background indicates abnormal GOL status where user must be pay attention on it.

2. GOL settings: Unacceptable setting is indicated by red background, warning on setting is indicated with yellow background, and acceptable setting is indicated by green or white background.

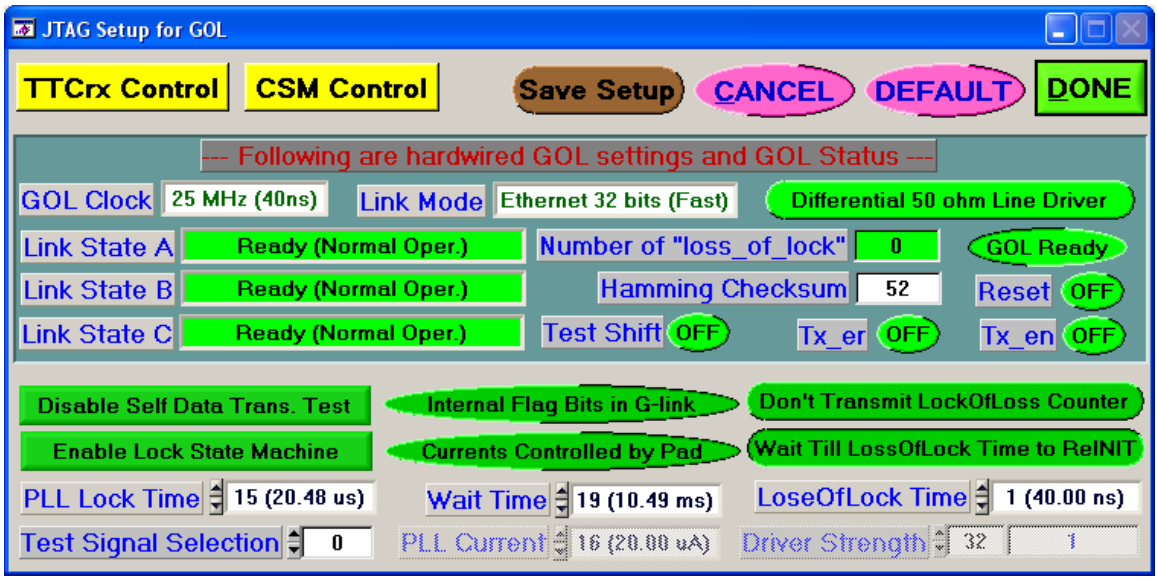


Figure 6. The GOL Setup Window

Only few parameters need to be set for GOL. For normal operation Self Data Transfer Test and Transmit Lock of Loss Counter must be disabled, and Lock State Machine must be enabled. Since the GOL is set as GBits Ethernet link in CSM1 board, the Flag Bits in G-link is not used. And PLL Current could be controlled by Pad or Configuration register as user's preference. The waiting time for GOL from Out-of-Lock to ready state is set by PLL Lock Time and Wait Time where the GOL default is chosen as shown in Figure 6. If one wishes to reduce the waiting time in a radiation environment, it is necessary to give enough waiting time for GOL to go back to ready state.

- DONE will download GOL setup, where other JTAG devices are in BYPASS mode. The status of JTAG download is indicated at the main JTAG control window as shown in Figure 1;
- DEFAULT will bring the default settings;
- CANCEL will cancel any changes in GOL setup and quit from GOL setup panel;
- Save Setup will save GOL setup into a text file where user will be asked to give a file name;
- TTCrx Control will bring up the TTCrx setup panel which is only enabled when CSM1 is included in the JTAG chain;;
- CSM Control will bring up the CSM1 setup panel which is only enabled when CSM1 is included in the JTAG chain.

3.6 *Program AMT Mezzanine Cards*

The AMT mezzanine cards settings can be programmed via **JTAG** menu, where **JTAG → MezzCard Setup All** is for common settings as shown in Figure 7 and **JTAG → MezzCardSetup Individual** is for individual settings. The AMT mezzanine card setup window contains switches, selection boxes and command buttons.

Applying individual setting to mezzanine card:
Once a common setup has been applied to the attached mezzanine cards, any given AMT card can be individualized. To program an individual mezzanine card, select **JTAG → MezzCardSetup Individual → Mezzanine *N***, where ***N*** is the assigned mezzanine card ID. The individual setup panel is virtually identical to the common setup panel. If a profile was loaded with an individualized setting for a card, the panel corresponding to that card will hold the saved values.

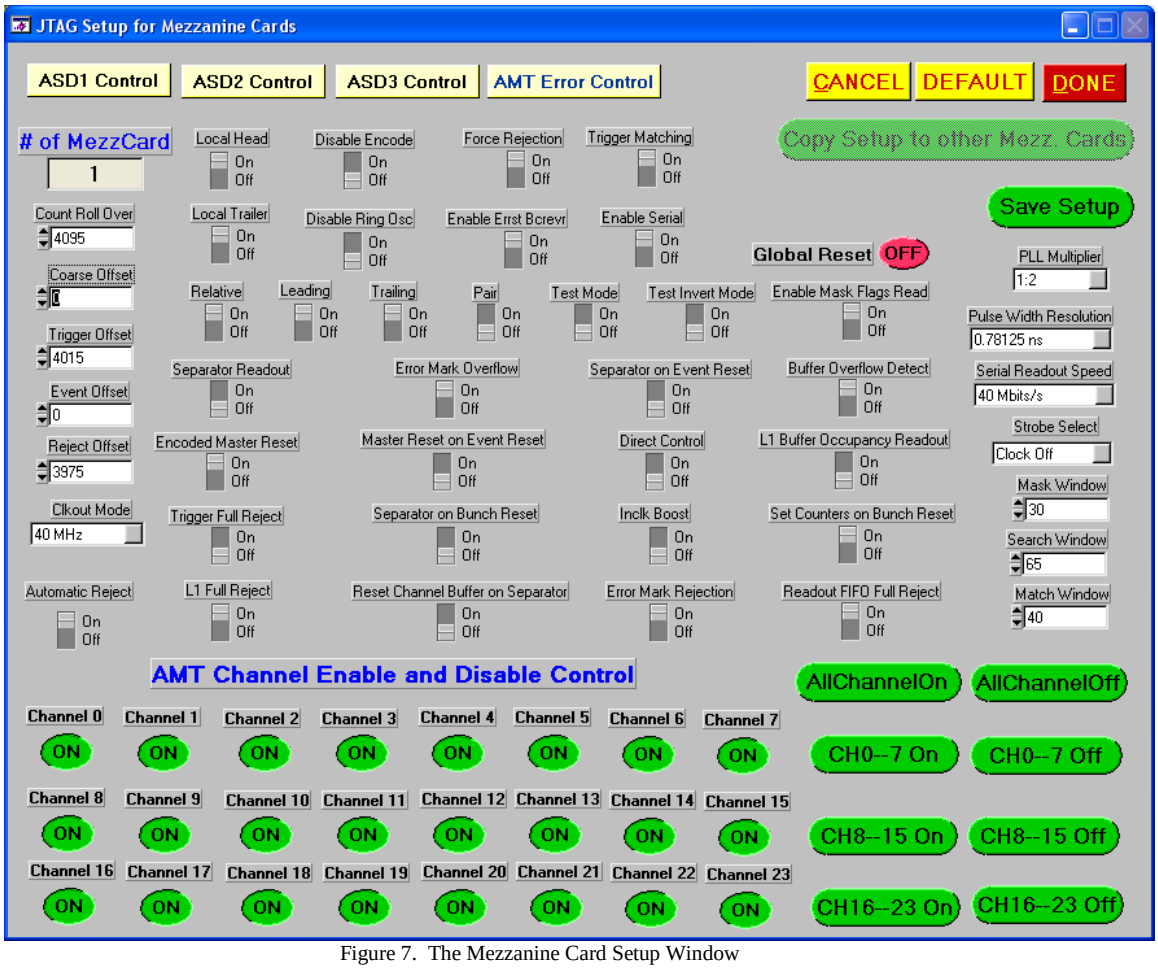


Figure 7. The Mezzanine Card Setup Window

Each mezzanine card has 24 channels which could be individually turn on/off by clicking on desired channel. The AMT Error Control Window (Figure 8) is invoked by clicking AMT Error Control.

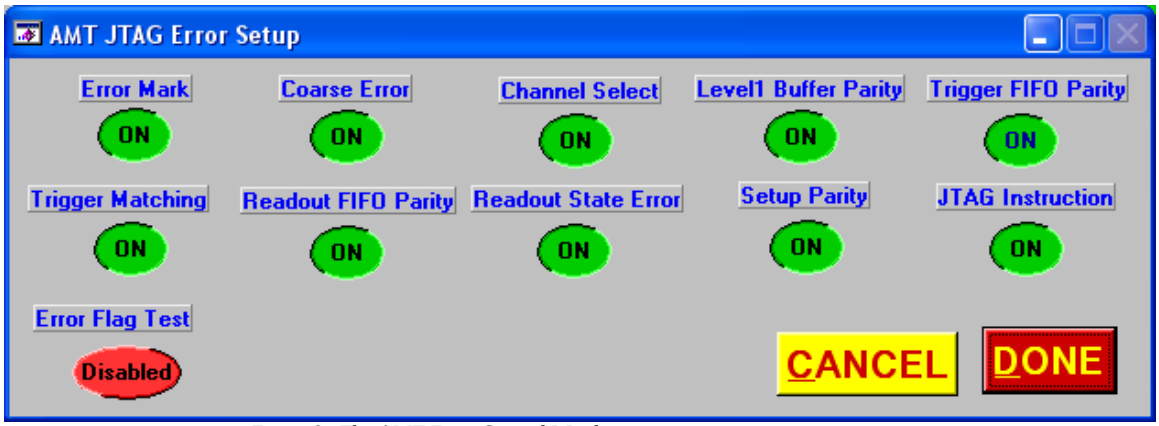


Figure 8. The AMT Error Control Window

Also each mezzanine card has three ASD chips which are programmable. The buttons of ASD1 Control, ASD2 Control and ASD3 Control access the corresponding ASD setup window as shown in Figure 9 (example for ASD1).

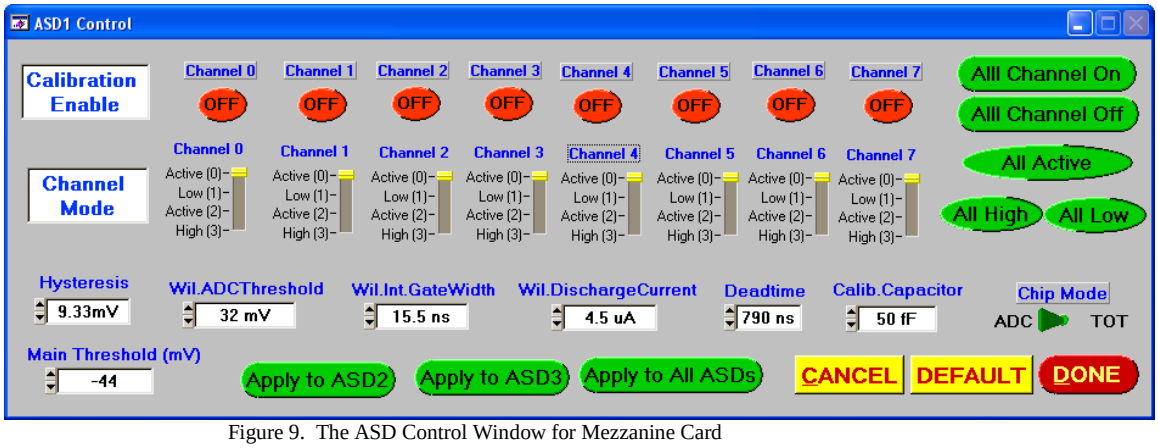


Figure 9. The ASD Control Window for Mezzanine Card

Each ASD controls 8 calibration channels which can be turned on/off individually. In normal DAQ runs, **ASD channel mode** should be turned to **Active** mode. For detailed ASD programmable parameters, please see reference[5].

Save Setup saves the current mezzanine card settings to a text file. DEFAULT recalls the mezzanine card default settings and CANCEL closes the setup windows and reverts to previous settings. The mezzanine card settings are applied after the DONE button on the Mezzanine Card Setup Window is selected.

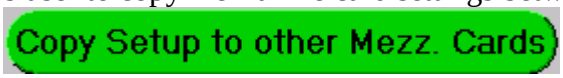
All the mezzanine card settings are read back via JTAG and are compared with original setup array. If any error is detected, programming information Panel will be popped out automatically where the failed mezzanine cards will be shown. Also the mezzanine card

setup status is shown in the main JTAG Control window as shown in Figure 1. All of the AMT and ASD settings are explained in Appendix B, for more detailed information please refer to the AMT manual [2] and ASD manual [5], [4]. For most applications, the default values should be sufficient. The values that will need the most tweaking are AMT Channel Control, Trigger Offset, the Mask Window, Search and Match Windows in Mezzanine Card Setup Panel, Main Threshold and Calibration Enable in ASD Control Panel.

3.7 *Copy Mezzanine Card Settings*

There is a command button 

in the mezzanine card setup window, which brings up the copy mezzanine card setup window as shown in Figure 10 and it allows user to copy mezzanine card settings between mezzanine cards.

The command button 

is disabled if there is only one on no mezzanine card for obvious reason.

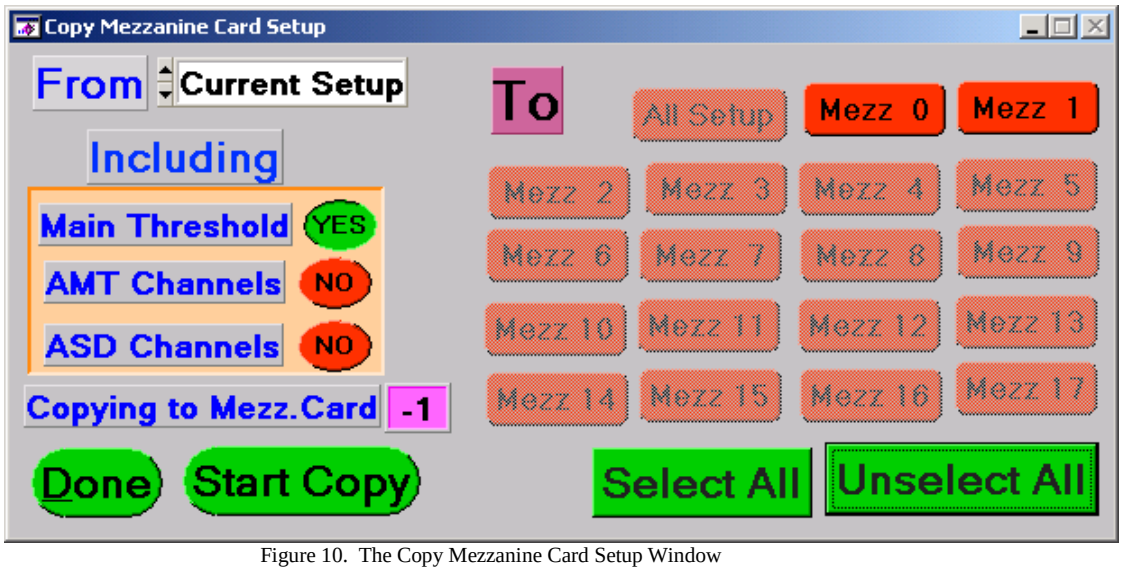


Figure 10. The Copy Mezzanine Card Setup Window

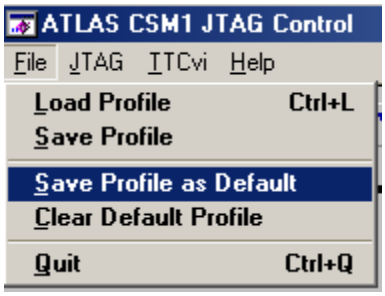
Be copied mezzanine card is selected from selection box of **From**, and destinations are a group toggle buttons. The main threshold, AMT channel mask and ASD channel mask are controllable, therefore user can decided whether to copy them. If the mezzanine card settings are copied, it is assumed that those mezzanine cards settings is individualized. To start copy mezzanine card settings, click on 

button and click on 

to exit from the copy mezzanine card setup window.

3.8 *Profile: Save and Download Setups*

The JTAG settings can be saved into a profile for future usage, and it can be done by using **File** pull-down menu. Select **File → Save Profile** to save current settings into a profile. This will bring up a file open dialog and display files with file extension .prf (**prof**ile), where user could provide a new file name or pick up an existing profile to overwrite it, and the current JTAG settings will be saved into the given file.



Similarly **File → Load Profile (Ctrl-L)** will allow user to load a saved profile by bringing up the file select dialog. After selected profile is loaded, user will be asked to select an action for loaded profile. There are three possible selections as shown in Figure 11: INIT DAQ will perform a DAQ initialization, Download Current Settings will download current settings into hardware and an answer of Do Nothing implies that user will download the JTAG settings into hardware later.

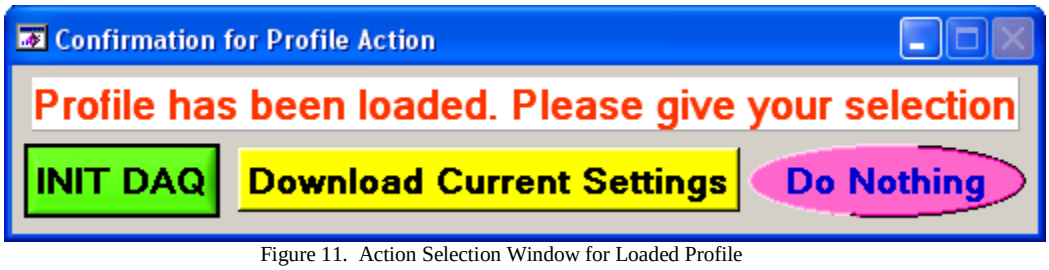


Figure 11. Action Selection Window for Loaded Profile

Also a default profile could be saved by using "**File → Save Profile as Default",** where the current JTAG settings are saved into a file <default.prf> and the file <default.prf> would be used as default JTAG settings in the future. To clear a default profile, it is better to do it through "**File → Clear Default Profile".**

3.9 *Generate Action and Sequence Files*

The JTAG control program is able to generate special formatted text files for varies JTAG operation. Those text files could be easily used by other JTAG control program to perform varies JTAG operation to CSM1. There are two type text files:

- **Action File:** contains JTAG instructions and JTAG bit stream;
- **Sequence File:** define JTAG operation.

To generate action and sequence files, two cases should be handled differently.

Case 1: Number of CSM has been defined and each CSM has been programmed.

1. If it is necessary to modify JTAG settings for a CSM, first select current CSM number (button Current CSM Number) as wished, then modify any JTAG settings;
2. **File → Generate All Action/Sequence Files for DAQ** to generate all action and sequences files.

Case 2: Number of CSM is changed or from scratch.

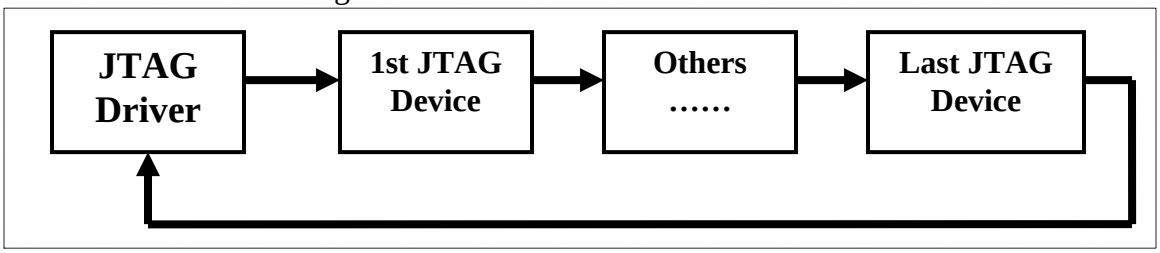
1. Edit DAQControlpara.txt to change the parameter value of "Normal JTAG Operation" to 0;
2. **File → Generate All Text Files for DAQ;**
3. Select number of CSM (button Number CSM). **PAY ATTENTION**: if the number of CSM is changed, the settings for any CSM (including GOL/TTCrx and mezzanine cards) will be cleared, therefore user must reprogram JTAG devices for each CSM (including related GOL/TTCrx and mezzanine cards);
4. Select current CSM number (button Current CSM Number);
5. **JTAG → Setup CSM** to make sure mezzanine card enable mask is right;
6. Modify any necessary JTAG settings, especially for mezzanine cards;
7. Repeat step 3 to 5 to finish all;
8. **File → Generate All Action/Sequence Files for DAQ** to generate all action and sequences files.

All generated action and sequence files are stored in sub-directory "action".

Format of Action File:

Each action file is one JTAG Instruction/Data operation. The action file contains a list of instruction bits followed by the list of data bits that are to be sent to all devices in the JTAG chain. Instructions bits are preceded by the letter "I", data bits by "D". The list starts with instruction registers of all devices followed by data registers. The instruction and data list are formed by 0 and 1 (binary format), where the least significant bit (the right most bit) comes first, and the number of 0/1 is the length of the instruction or the data. Also there is only one instruction bits line and only one data bits line for a JTAG device (special for CSM action file), therefore it is easy to find corresponding data bits for a particular JTAG device in case it is necessary (for instance, if wishing to modify the data bits). Any thing after the character "#" is comment.

If JTAG devices are arranged as



And the last JTAG device TDO goes back to JTAG Driver. The last JTAG device in the JTAG chain should be the first in the list and the first JTAG device in the JTAG chain should be the last in the list.

Example of an action file with 5 JTAG device, where the order of JTAG devices are PROM, CSM (Vertex-II chip), GOL, TTCrx and AMT (on a Mezzanine Card):

```
##############################################################################:
# action file for CSM 0:
# Generated by CSM JTAG Control on Sun May 11 2003 17:33:26
```

```
#
# Download GOL Setup
#
# -------- JTAG Instruction List ----------
#
I 01111                 # AMT Instruction 'BYPASS' for mezz. card 17
I 1111                  # TTCrx Instruction 'BYPASS'
I 01001                 # GOL Instruction 'CONFRW'
I 111111                # CSM Instruction 'BYPASS'
I 11111111              # PROM Instruction 'BYPASS'
#
# ********* JTAG Bit Stream ***********
#
# Bit stream length is 1
#
D 1
#
# Bit stream length is 1
#
D 1
#
# Bit stream length is 55
#
D 0110100001000000001000000011111001100111010100000000000
#
# Bit stream length is 1
#
D 1
#
# Bit stream length is 1
#
D 1
#
# end of action
###############################################################################:
```

Format of Sequence File

The sequence file contains a list of actions to be performed for the JTAG chain. The first command which is preceded by character “C” in this file selects the JTAG signal output port, where it is assumed that CSM N is connected with JTAG output port N. The next command which is preceded by character “A” lists the JTAG action, where the name of the action file (without file extension “.act”) is provided. Any thing after character “#” are considered as comment.

Following is an example for the sequence file:

```
###############################################################################:
```

```
# Sequence file
# Generated by CSM JTAG Control on Sun May 11 2003 17:33:35
# List of actions. Each action refers to a file with name xxxxx.act
# with command 'A xxxxx'
#
# Perform start CSM DAQ with following steps:
#   1. Turn Off Mezzanine Card JTAG Signals;
#   2. Start CSM DAQ;
#   3. Get CSM Status;
# ----------------------------------
#
C 0 0x03fc      # (no broadcast) plain to port 0 and no asp!
A turnOffMezzJTAG0000
#
C 1 0x03fc      # (no broadcast) plain to port 1 and no asp!
A turnOffMezzJTAG0001
#
# ----------------------------------
#
C 0 0x03fc      # (no broadcast) plain to port 0 and no asp!
A startCSMDAQMezzJTAGOff0000
#
C 1 0x03fc      # (no broadcast) plain to port 1 and no asp!
A startCSMDAQMezzJTAGOff0001
#
# ----------------------------------
#
C 0 0x03fc      # (no broadcast) plain to port 0 and no asp!
A getCSMStatus0000
#
C 1 0x03fc      # (no broadcast) plain to port 1 and no asp!
A getCSMStatus0001
#
#
# end of sequence list
##########################################################################:
```

4 Useful Information

4.1 *JTAG Control Parameter File*

Basic JTAG control parameters are written into file <DAQControlpara.txt> for future usage. The saved JTAG control parameters are listed below:

```
Normal JTAG Operation:      1
Default Profile Saved   :   0
Number of CSM           :   2
Current CSM Number      :   1
PROM in JTAG Chain      :   1
CSM in JTAG Chain       :   1
GOL in JTAG Chain       :   1
TTCrx in JTAG Chain     :   1
Mezz. in JTAG Chain     :   1
Mezz. Card Enables      : 0x00020002
CSM0 Base               : 0x40000000
Corelis 1149.1 Base     : 0x00000000
VMIC 2510 Base          : 0x00000000
TTCvi Base              : 0x00FF1000
```

Normally it is not necessary for user to change any JTAG control parameter, except the parameter "**Normal JTAG Operation".** No JTAG operation will be performed if one turns off "**Normal JTAG Operation**", which is useful when user only wish to generate action and sequence files for varies JTAG settings. Be sure to turn it on when one wants to use JTAG control program CSM1 and mezzanine cards.

4.2 ***DAQ** Control*

Since the event number and bunch number are counted individually by each CSM1 and mezzanine card, the DAQ initialization and start/stop DAQ should follow certain procedure, otherwise the whole DAQ system will not function correctly.

DAQ Initialization:

- Stop Trigger (TTCvi or other trigger controller);
- Initialize CSM1 including mezzanine cards;
- Initialize MROD or GOLA card;
- AMT global reset (TTCvi).

DAQ Startup:

- Start MROD or GOLA card;
- Disable JTAG signals to mezzanine card(s);
- Start CSM1.
- Event Counter Reset (TTCvi);

- Bunch Counter Reset (TTCvi).
- Start Trigger (TTCvi or other trigger controller).

Stop DAQ:

- Stop Trigger (TTCvi or other trigger controller), and wait for 100ms if user wishes to flash out all events;
- Stop CSM1;
- Stop MROD or GOLA card.

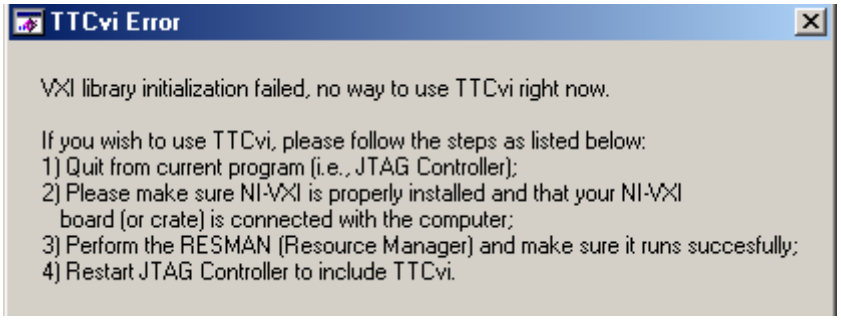
Pause/Resume DAQ:

- Disable/Enable Trigger (TTCvi or other trigger controller).

5 TTCvi Control

TTCvi (TTC-VMEbus INTERFACE, see reference [7]) is handled from the **TTCvi** pull-down menu, where only **"TTCvi → Status and Control (F12)"** is enabled at beginning as shown in the figure. To access TTCvi board, the first step is to execute **"TTCvi → Status and Control (F12)"** which will go through following steps:

- Initialize VXI library. If the VXI library initialization is failed, the TTCvi Control will be disabled totally. User will be instructed how to bring up the TTCvi Control as following:



- Search valid TTCvi BASE address in case previous used TTCvi BASE address is not accessible. The TTCvi BASE address searching will take a while since the wide BASE address range and please be patient;

- Enable all **TTCvi** pull-down menu and bring up TTCvi Status and Control window as shown in Figure 12.

The **TTCvi** pull-down menu is defined as following:

- **Status and Control (F12) :** Bring up TTCvi Status and Control panel.
- **BGO Control (F11) :** Bring up TTCvi B-GO Control panel.
- **Reset Board (F10) :** Reset TTCvi Board.

- **Reset L1A FIFO (F9) :** Reset TTCvi L1A FIFO.
- **Event Counter Reset (F8) :** Issue an event counter reset command.
- **Bunch Counter Reset (F7) :** Issue a bunch counter reset command.
- **Event and Bunch Counter Reset (F6) :** Issue an event and bunch counter reset command.
- **One Shot Software Trigger (F1) :** Generate one shot software trigger.
- **Random Software Trigger :** Select random software trigger and its rate (8 selections: 1Hz, 100Hz, 1KHz, 5KHz, 10KHz, 25KHz, 50KHz and 100KHz).
- **External Trigger :** Select external trigger and its input channel (4 possible external trigger input: channel 0, channel 1, channel 2 and channel 3).
- **Disable Trigger (F5) :** Disable TTCvi trigger.

For convenience short cut keys are defined for TTCvi control, detail list please refer to appendix C.

5.1 *TTCvi Status and Control Panel*

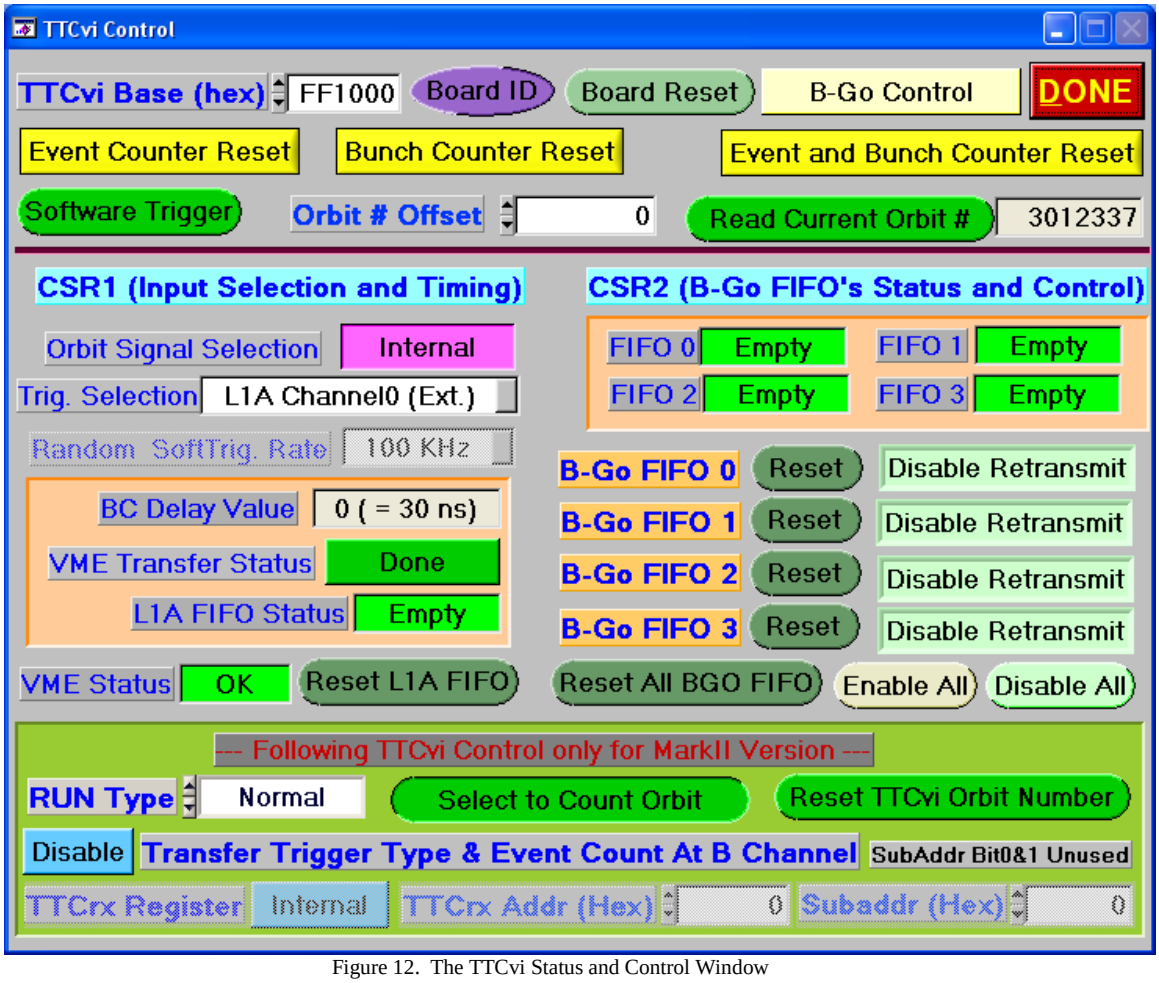


Figure 12. The TTCvi Status and Control Window

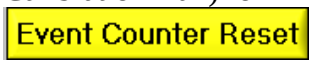
Figure 12 is the TTCvi Status and Control panel, where the TTCvi status are displayed, such as VME Status, BC Delay Value, L1A FIFO Status and B-GO FIFO Status etc.. And user will be able to control TTCvi through this panel. The most common used commands will be:

- 

allows user to change TTCvi base address which corresponding 4 rotary switch settings on TTCvi board.
- 

will reset TTCvi board.
- 

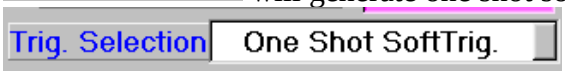
will give the manufacturer ID, Board Serial Number and Board Revised Number for TTCvi board.
- 

allows user to select run type (Normal Run or Calibration Run) for TTCvi which is only valid for MarkII version.
- 

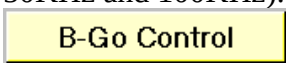
will issue an event counter reset command.
- 

will issue a bunch counter reset command.
- 

will issue an event and bunch counter reset command.
- 

will generate one shot software trigger.
- 

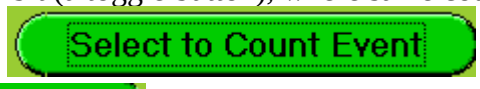
will allow user to select trigger type, there are 8 different selections.
- 

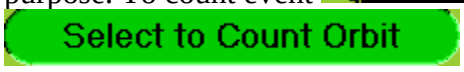
will allow user to select eight different trigger rate generated by TTCvi itself (1Hz, 100Hz, 1KHz, 5KHz, 10KHz, 25KHz, 50KHz and 100KHz).
- 

will bring up the B-GO control panel;
- 

will exit from TTCvi Status and Control panel.

Normal internal orbit signal is selected. If external orbit signal is selected, it is necessary to provide external orbit signal to TTCvi board. It is possible to reset L1A FIFO and individual B-GO FIFO, during normal data taking it is better do not reset those FIFOs.

For MarkII version TTCvi, it is possible to count orbit instead of event which is controlled by a selection bit (a toggle button), where same counter is used for different purpose. To count event 

should be selected, and 

enables orbit counting. Corresponding counter reset button is implemented also. It is also possible to send out trigger type and event counter via B channel which is turned off at default.

User should pay attention to the VME Status if it turns to RED, which means there is no VME access and TTCvi will not function at all. In that case, it is necessary to check the

hardware, such as power and TTCvi module. To see whether TTCvi is functional, select to count event, then push the button Software Trigger, the event number should be increased by 1.

5.2 *TTCvi B-GO Control*

TTCvi B-GO control panel is brought up via TTCvi pull-down menu **TTCvi → B-GO Control** or clicking at control button B-Go Control from TTCvi Status and Control Window. Figure 13 shows the TTCvi B-GO Control panel for normal run.

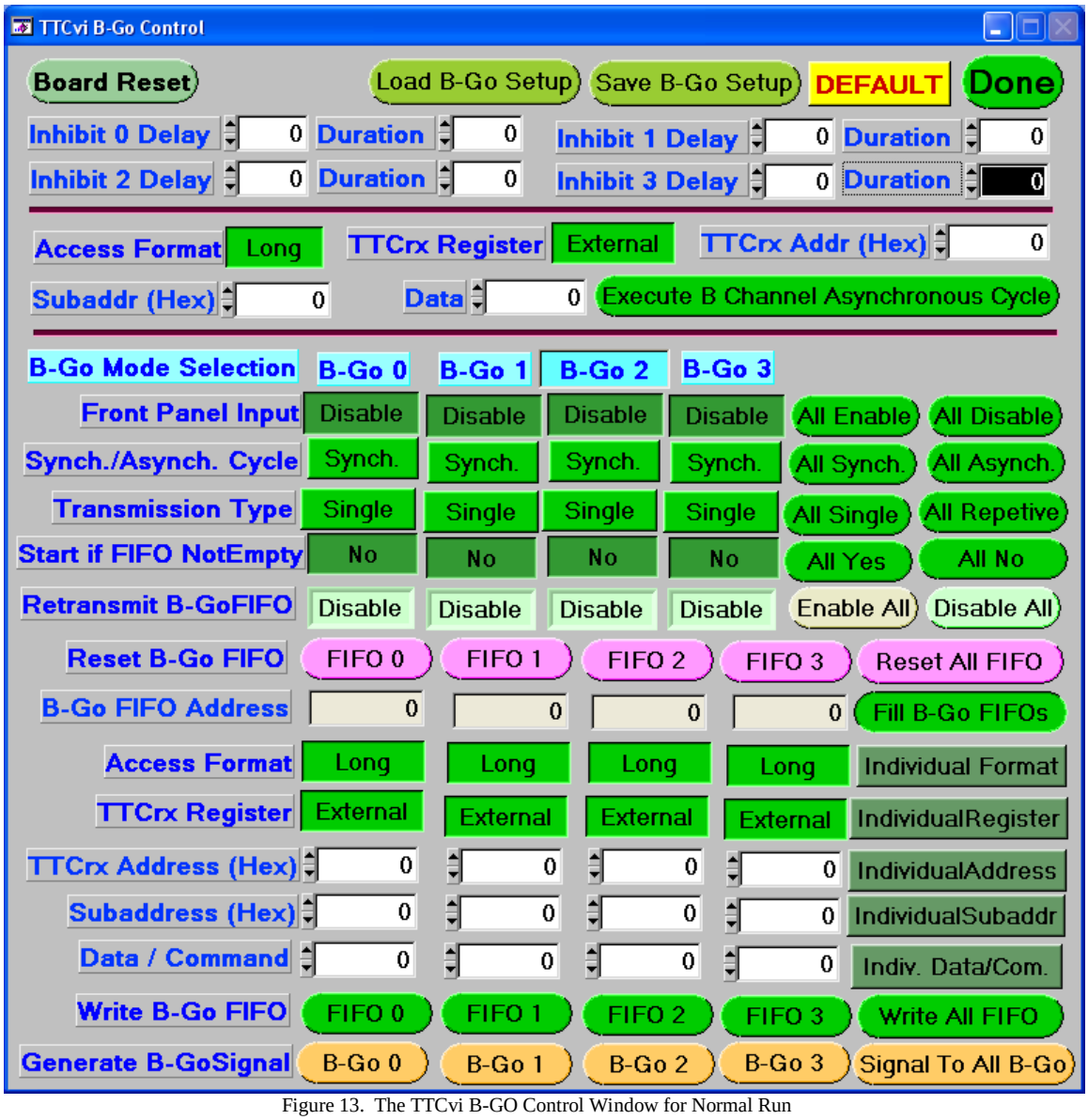


Figure 13. The TTCvi B-GO Control Window for Normal Run

If a default B-GO settings are saved into a file, it will be loaded automatically. The file name of the default B-GO settings is “default.bgo” for normal run, and is “CalibrationRunDefault.bgo” for calibration run.

There are two ways to generate B Channel command/data either by writing the specified TTCvi VME address or by using 4 B-GO FIFOs where the B Channel command/data are preloaded. An asynchronous B Channel cycle could be generated by clicking at command button Execute B Channel Asynchronous Cycle, where desired the B channel command/data should be set before clicking at the command button. The timing of these B Channel cycles is not synchronized with the LHC orbit and is generated by writing specified VME address. B-GO FIFO must be selected if external signal is used to initiate the B Channel cycle, where the front panel input must be enabled from B-GO mode selection. If a B-GO FIFO is selected to generate B Channel cycle, it is essential to set a non-zero value for corresponding inhibit duration register, otherwise no B Channel cycle will be generated.

To use a B-GO FIFO for generating B Channel cycles, first set corresponding inhibit delay and duration (a non-zero duration is required), then select the corresponding B-GO modes:

- Enable or Disable Front Panel Input;
- Select synchronous or asynchronous cycle (Synch./Asynch. Cycle);
- Select single or repetitive transmission mode (Transmission Type);
- Decide whether to start B Channel cycle if B-GO FIFO is not empty.
- Set or Unset the B-GO FIFO retransmission. For repeating usage of B-GO FIFO, the B-GO FIFO retransmission should be enabled.

Fill B-Go FIFOs should be selected to write the B-GO FIFO. After filling the B Channel control data word, the data word could be written to the B-GO FIFO by simply clicking at the corresponding command button Write B-Go FIFO. Four B-GO FIFOs could be filled individually or filled commonly depending on the setting of Individual/Same toggle button, and the depth of the B-GO FIFO is 256. The B-GO FIFO contents could be viewed by selecting View B-Go FIFOs, then change the B-GO FIFO address to examine the data word. It is easy to reset the B-GO FIFO by clicking at the B-GO FIFO reset button. The B Channel cycle could be generated by clicking at corresponding Generate B-GoSignal command button if the B-GO front panel input is disabled or by providing B-GO input signal if the B-GO front panel input is enabled.

For calibration run, the B-GO control panel is shown in Figure 14 where the default B-GO settings are in file “CalibrationRunDefault.bgo”, where the B-GO 2 is assigned for it. TTCvi front panel input signal of B-GO 2 must be supplied which initiates the calibration trigger and calibration parameter via B Channel.

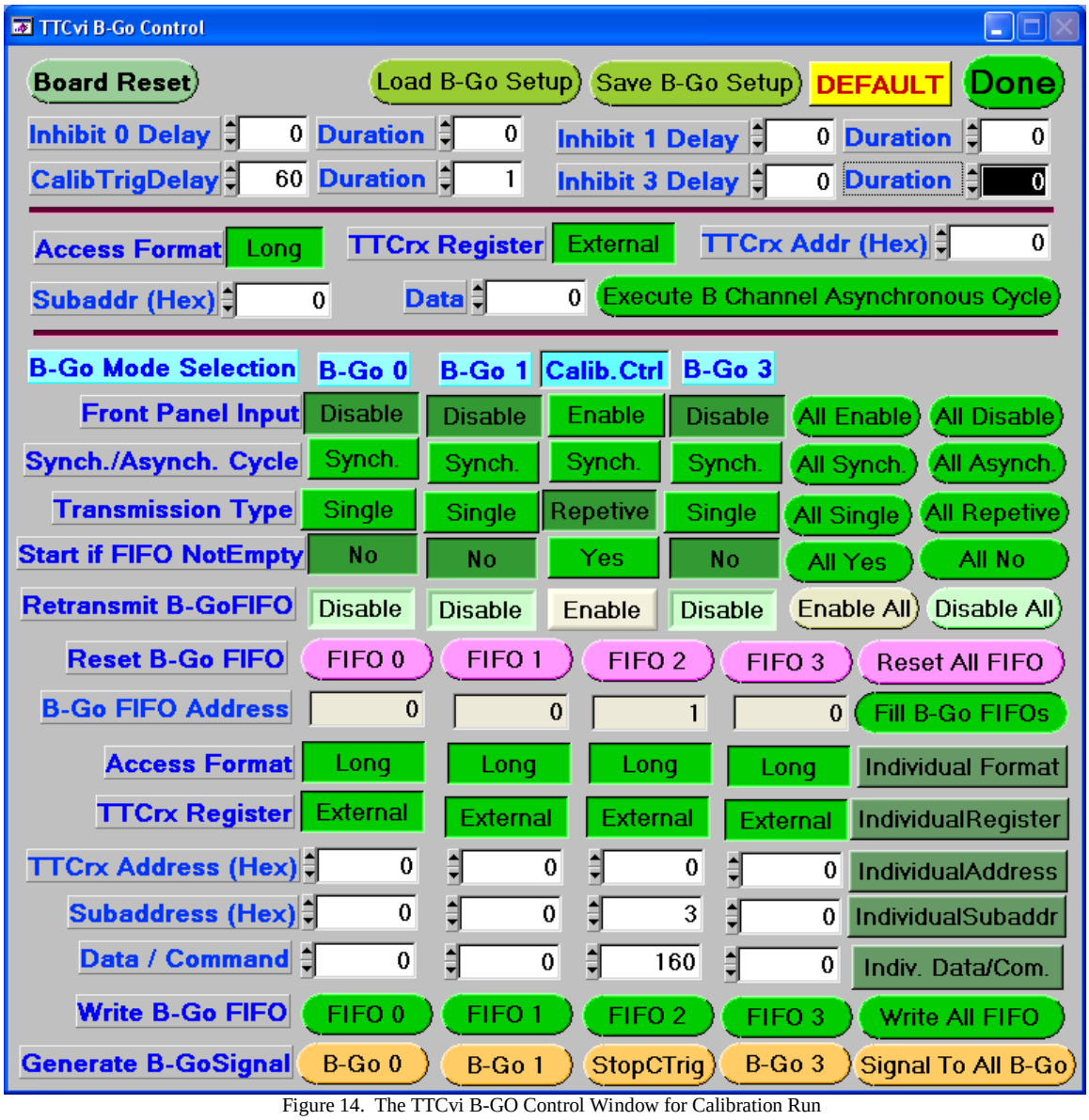


Figure 14. The TTCvi B-GO Control Window for Calibration Run

The B-GO control panel is very similar comparing with ones for normal run. Only difference is that controls for B-GO 2 becomes the controls for calibration. The calibration trigger delay is set by CalibTrigDelay 60 (Default 60), and the front panel input is enabled for B-GO 2 no matter its setting. The long calibration command is used in here, where the data value is the width of the calibration pulse and 160 represents 4us width of the calibration pulse (1 = 25ns). The calibration trigger could be stopped (StopCTrig) or started (StartCTrig) depending on trigger status. The digitized data time will be around zero by using default calibration trigger delay of 60 (1.5 us). To obtain other digitized data point, just simple reduce the calibration delay by certain amount.

Following is the list of common command buttons:

- 

will reset TTCvi board including the B-GO FIFOs.
- 

will bring up a file open dialog box and display files with file extension ".bgo". User could provide a file name or pick up an existing BGO file to overwrite it. There are two default B-GO setting files "default.bgo" for normal run and "CalibrationRunDefault.bgo" for calibration run;
- 

will bring up a file selection dialog box which displays files with file extension ".bgo", and user make the file selection;
- 

will set the B-GO control panel to its default;
- 

will close and exit from B-GO control panel.

Example of B-GO setting File:

```
// ----------------- File for TTCvi B-Go settings ----------------------
//
// Please be careful in changing the TTCvi B-Go setting file
// And do not change/modify following key words!!!
//   Inh0Delay Duration   Inh1Delay Duration   Inh2Delay Duration   Inh3Delay Duration
//   B-Go0Mode   B-Go1Mode   B-Go2Mode   B-Go3Mode
//   B-Go FIFO 0 Data List
//   B-Go FIFO 1 Data List
//   B-Go FIFO 2 Data List
//   B-Go FIFO 3 Data List
// Comments are started with `//'
//
  Inh0Delay Duration   Inh1Delay Duration   Inh2Delay Duration   Inh3Delay Duration
            0          0             0          0             0          0             0          0
//
// B-Go Mode Bit Map
//   Bit 0 : Front Panel Enable/Disable
//           0 = Front Panel Enabled
//           1 = Front Panel Disabled
//   Bit 1 : Cycle Mode (Synchronous/Asynchronous Cycle)
//           0 = Sychronous Cycle
//           1 = Asynchronous Cycle
//   Bit 2 : Transfermission Type (Single/Repetive Mode)
//           0 = Single Mode
//           1 = Repetive Mode
//   Bit 3 : Start Cycle by looking FIFO Status
//           0 = Start Cycle as soon as FIFO not Empty
//           1 = Do not look at FIFO Status
//   Bit 4 : Select Operation Mode (Should be 0 for B-Go 0, 1 & 3)
//           0 = Basic operation mode
//           1 = Calibration mode (B-Go 2 Only)
```

```
//
  B-Go0Mode   B-Go1Mode   B-Go2Mode   B-Go3Mode
               9             9             9             9
//
// B-Go FIFO Retransmission Control
//   0 = Enable B-Go FIFO Retransmission
//   1 = Disable B-Go FIFO Retransmission
//
  B-Go0ReTX   B-Go1ReTX   B-Go2ReTX   B-Go3ReTX
               1             1             1             1
//
// B-Go FIFO Data
//   Bit 31    : Data Format, Long/Short = 1/0
//   Long Format (bit 31 set)
//   Bit 30-17 : 14 bits TTCrx Address)
//   Bit 16    : TTCrx register selection, External/Internal = 1/0
//   Bit 15-08 : 8 bits subaddress)
//   Bit 07-00 : 8 bits data)
//   Short Format (bit 31 cleared)
//   Bit 30-23 : 8 bits command)
//   Bit 22-00 : Do not care)
//
  B-Go FIFO 0 Data List
        0 (Number of B-Go FIFO data words)
  B-Go FIFO 1 Data List
        0 (Number of B-Go FIFO data words)
  B-Go FIFO 2 Data List
        0 (Number of B-Go FIFO data words)
  B-Go FIFO 3 Data List
        0 (Number of B-Go FIFO data words)
```

5.3 *TTCMini Crate Cable Connection*

TTC Mini-Crate is arranged as following:

TX	TDM BM ENCODER	VXCO-PLL	-2V REG	C.GEN	MONITOR RX	PK55	PK60	POWER CONTROL

Cable and Switch Connections:

C.GEN (Switch Position : INT)

40 MHz Clock Output CH2	TTCvi Clock IN
40 MHz Clock Output CH3	VXCO-PLL REF I/P

The 40 MHz Clock Output Channel number is from top to bottom.

VXCO-PLL

160.32	TDM BM ENCODER 160.32 I/P
MON I/P	TDM BM ENCODER SYNC O/P

TDM BM ENCODER

ENC O/P	TX I/P
A Data I/P	TTCvi Channel A/ecl
B Data I/P	TTCvi Channel B/ecl

Note: Same length cable should be used for A and B data I/P to TTCvi

TX

Optical Cable	CSM1
Optical Cable	TTCvi Test Board

Appendix A. References

[1] "CSM1 User Manual", J. Chapman, … University of Michigan. April 30, 2003.

[2] "AMT-1 & 2 (ATLAS Muon TDC version 1 & 2) User's Manual", Yasuo Arai. KEK, National High Energy Accelerator Research Organization, Japan. Rev 0.91, April 30, 2001.

[3] "TTCrx Reference Manual", J. Christiansen, A. Marchioro, P. Moreira, T. Toifl. CERN-EP/MIC, Geneva Switzerland. December, 2001.

[4] "MDT-ASD: Serial data I/O and programmable parameters", http://bmc.bu.edu/bmc/asd/octal/spec/ASD00A_Prog.PDF.

[5] "MDT-ASD, CMOS front-end for ATLAS MDT", C. Posch, E. Hazen, J. Oliver. ATLAS Muon Note ATL-MUON-2002-003, http://doc.cern.ch//archive/electronic/cern/others/atlnot/Note/muon/muon-2002-003.pdf.

[6] "GOL Reference Manual", P. Moreira, T. Toifl, A. Kluge, G. Cervelli, A. Marchioro and J. Christiansen. CERN-EP/MIC, Geneva Switzerland, May 2002.

[7] "TTC-VMEBus INTERFACE TTCvi", Ph. Farthouat and P. Gallno CERN ECP.

[8] "TTCvx Technical description and users manual", Per Gallno, May 1999. http://ttc.web.cern.ch/TTC/TTCvxManual1a.pdf.

Appendix B. Programmable Parameters of AMT Mezzanine Card

The information in this appendix is from the AMT-1 & 2 user manual [2]. The default value is for typical operation and is used in University of Michigan for cosmic data taking. If the default or name is underlined, it is required for normal operation of the CSM0 with AMT mezzanine cards.

B.1 AMT Main Setup Panel

Name in AMT Main Setup Panel (AMT Name) [DEFAULT] Description

- **Automatic Reject** (enable_auto_reject) [ON] Reject hits when the channel buffers are full.
- **Buffer Overflow Detect** (enable_l1ovr_detect) [ON] Detect L1 buffer overflows.
- **Channel 0 to 23** (enable_channel) [ON] Enable individual channel input.
- **Clkout Mode** (clkout_mode) [40 MHz] One of four clock modes:
    1. Start Sync: Clock is synchronized with the START signal.
    2. 40 Mhz: output of the PLL clock /2, typical in most logics.
    3. 80 Mhz: output of the PLL clock.
    4. CCount carry: carry out of the coarse counter, used to extend the time range.
- **Coarse Offset** (coarse_time_offset) [0] BCID counter offset.
- **Count Roll Over** (count_roll_over) [4095] Roll over value for the coarse counter.
- **Direct Control** (enable_direct) [OFF] Trigger reset comes from direct input pins.
- **Disable Encode** (disable_encode) [OFF] Disable fine timer encoder and output.
- **Disable Ring Osc** (disable_ringosc) [OFF] Stop the ring oscillator and disable the PLL.
- **Enable Errst Bcrevr** (enable_errst_bcrecr) [ON] Reset error status on any reset.
- **Enable Mask Flags Read** (enable_mask) [ON] Enable mask flags for hits less than Match Window clock ticks before the search window.
- **Enable Serial** (enable_serial) [ON] Serial data readout, otherwise parallel readout.
- **Encoded Master Reset** (enable_mreset_code) [ON] Master reset from an encoded reset.
- **Error Mark Overflow** (enable_errmark_ovr) [ON] Flags events with buffer overflow.
- **Error Mark Rejection** (enable_errmark_rejected) [ON] Error mark if a hit is rejected in Match Window.
- **Event Offset** (event_count_offset) [0] Event ID (EVID) offset.
- **Force Rejection** (enable_rejected) [ON] Recover rejected hits from buffer overflow.
- **Global Reset** (global_reset) [OFF] Perform an AMT global reset if enabled.
- **Inclk Boost** (inclk_boost) [OFF] Double the internal clock frequency **(AMT3 only)**.
- **L1 Buffer Occupancy Readout** (enable_l1occup_readout) [OFF] Allow readout of L1 buffer occupancy.
- **L1 Full Reject** (enable_l1_full_reject) [ON] Reject hits if L1 buffer is nearly full.
- **Leading** (enable_leading) [ON] Enable leading edge measurements of hits.
- **Local Head** (enable_header) [ON] Enable TDC header.
- **Local Trailer** (enable_trailer) [ON] Enable TDC trailer.

- **Master Reset on Event Reset** (enable_mreset_evrst) [OFF] Enable master reset on event reset.
- **Mask Window** (mask_window) [30] Number of clock cycles before a trigger, where hit will be masked off if it is out mask window (comes too early).
- **Match Window** (match_window) [50] Number of clock cycles after a trigger during which hits will be considered to belong to that trigger.
- **Mezz.Card ID** (tdc_id) [NONE] TDC identifier, this ID is attached to the output data (for individual mezzanine card setting only, for common settings the TDC ID of each mezzanine card is assigned inside the procedure of downloading their settings).
- **Pair** (enable_pair) [OFF] Enable paired measurements and mask Leading and Trailing.
- **PLL Multiplier** (pll_multi) [1:2] ratio between the external clock and the internal ring oscillator.
- **Pulse Width Resolution** (width_select) [0.78125 ns] Resolution of the pulse width, for use in Pair measurements.
- **Readout FIFO Full Reject** (enable_rofull_reject) [ON] Reject hits if read-out FIFO full.
- **Reject Offset** (reject_count_offset) [3975] Offset for the rejection counter, when the rejection counter matches the BCID of a hit, the hit will be discarded.
- **Relative** (enable_relative) [ON] Subtract the trigger count from the coarse count of hits.
- **Reset Channel Buffer on Separator** (enable_resetcb_sepa) [OFF] Reset the channel buffer when a separator is inserted.
- **Search Window** (search_window) [75] Sets the number of clock cycles after a trigger to search for hits.
- **Separator on Bunch Reset** (enable_sepa_bcrst) [OFF] Enable generate separator on bunch count reset.
- **Separator on Event Reset** (enable_sepa_evrst) [OFF] Enable generate separator on event reset.
- **Separator Readout** (enable_sepa_readout) [OFF] Enable readout of internal separators (for debugging).
- **Serial Readout Speed** (readout_speed) [40 Mbits/s] Speed at which data is read from the AMT to the CSM0.
- **Set Counters on Bunch Reset** (enable_setcount_bcrst) [ON] sets all counters to be reset on a bunch count reset.
- **Strobe Select** (strobe_select) [Clock Off] Selects serial data transfer mode:
    1. DS strobe: Gated DS strobe;
    2. DS str cont: Continuous DS strobe;
    3. Clock Off: Clock output off;
    4. Edge Cont: continuous leading edge strobe. CSM0 requires this mode.

  Or select parallel data transfer mode (**(AMT3 only)**:
    1. Continuous: Continuous parallel output;
    2. Handshaked : Handshaked parallel output.
- **Test Mode** (test_mode) [OFF] Test mode for diagnosing AMT hardware problems.
- **Test Invert Mode** (test_invert) [OFF] Automatic inversion of test pattern if enabled.

- **Trailing** (enable_trailing) [ON] Enable trailing edge measurements.
- **Trigger Full Reject** (enable_trfull_reject) [OFF] Reject hits if trigger FIFO is nearly full.
- **Trigger Matching** (enable_match) [ON] Has the TDC match triggers to hits.
- **Trigger Offset** (bunch_count_offset) [4015] Sets the offset of the trigger time tag to account for delays between the trigger and the data.

B.2 AMT Error Control Panel

Name in AMT Error Control Panel (AMT Name) [DEFAULT] Description

- **Error Flag Test** (error_test) [OFF] Set all error flags to test error circuit. Don't set this bit in normal operation **(AMT3 only)**.
- **Error Mark** (enable_errmark) [ON] Enable error mark word if hard error exists.
- **Channel Select** (enable_error bit 1) [ON] A synchronization error has been detected in the priority logic used to select the channel being written into the L1 buffer.
- **Coarse Error** (enable_error bit 0) [ON] A parity error in the coarse count has been detected in a channel buffer.
- **Level1 Buffer Parity** (enable_error bit 2) [ON] Parity error detected in L1 buffer.
- **JTAG Instruction** (enable_error bit 8) [ON] Parity error in JTAG instruction.
- **Readout FIFO Parity** (enable_error bit 5) [ON] Parity error detected in readout FIFO.
- **Readout State Error** (enable_error bit 6) [ON] Illegal state detected in readout logic.
- **Setup Parity** (enable_error bit 7) [ON] Parity error detected in control registers.
- **Trigger FIFO Parity** (enable_error bit 3) [ON] Parity error detected in trigger FIFO.
- **Trigger Matching** (enable_error bit 4) [ON] Illegal state detected in trigger matching logic.

B.3 ASD Setup Panel

This summary is based on reference [5].

Name in ASD Setup Panel [DEFAULT] Description

- **Deadtime** [790 ns] An additional dead time window after each hit.
- **Calib.Capacitor** [50 fF] Calibration injection capacitor select.
- **Channel N0 to N7 Enable** [OFF] Calibration channel masks, for ASD1 N0 = 0 and N7 = 7, for ASD2 N0 = 8 and N7 = 15, for ASD3 N0 = 16 and N7 = 23.
- **Channel N0 to N7 Mode** [Active (0)] Channel mode controls, for ASD1 N0 = 0 and N7 = 7, for ASD2 N0 = 8 and N7 = 15, for ASD3 N0 = 16 and N7 = 23.
- **Chip Mode** [ADC] The global output mode control.
- **Hysteresis** [9.33 mV] Hysteresis voltage for the timing discriminator.
- **Main Threshold** [-44 mV] The threshold for timing discriminator.
- **Wil.ADCThreshold** [32 mV] Wilkinson ADC threshold.
- **Wil.DischargeCurrent** [4.5 uA] Wilkinson ADC discharge current.
- **Wil.Int.GateWidth** [15.5 ns] Wilkinson ADC integration gate width.

Appendix C. Short Cut Keys for TTCvi Pull-down Menu

Following short cut keys are defined for TTCvi pull-down menu:

Key	Function Description
F1	Generate one shot software trigger;
F2	Generate 1Hz random software trigger;
F3	Generate 10KHz random software trigger;
F4	Generate 100KHz random software trigger;
F5	Disable TTCvi trigger;
F6	Issue an event and bunch counter reset command;
F7	Issue a bunch counter reset command;
F8	Issue an event counter reset command;
F9	Reset TTCvi L1A FIFO;
F10	Reset TTCvi board;
F11	Bring up TTCvi B-GO Control panel;
F12	Bring up TTCvi Status and Control panel;

Appendix D. Detail Description for Calibration Run

This document is intended to provide a guide on how to work with calibration triggers. Details of the appropriate TTC command sequence are provided along with screen captures from the Mini-DAQ and Chipscope logic analyzer traces. The JTAG setup string for mezzanine boards is not treated.

Calibration Triggers in ATLAS:

Available ATLAS documentation indicates a broadcast B-channel cycle will initiate a calibration trigger, with the L1accept following at some fixed time after the B-channel broadcast. In this scenario however, there is no indication as to which of the available broadcast commands will be used. In fact, there is no discernable indication that a short broadcast will be used instead of a long cycle.

Further to this, the CSM-1 has a default duration of 4μs (160 clock tics) for the calibration strobe to the mezzanine boards, but for maximum flexibility this must be programmable. The mechanism we have chosen for this programming is via TTC Individually Addressed Command (IAC) to the CSM-1, utilizing both sub-address and data bits within the long format command frame. If TTC address zero is chosen, then the command is broadcast to all CSM-1 at once, allowing them all to be programmed at once.

The emerging calibration process then becomes maximally flexible if a calibration trigger can be initiated using either long or short B-channel commands. This is what we have implemented.

Short Broadcast Commands:

Because we were also testing the capabilities of the TTC/CSM-1 communications we chose to use a pair of bits set, one from the user space (bit 6) and one from the system space (bit 3), as the command indicating that a calibration trigger is being initiated. The decimal equivalent of this is the value 72 (01001000 binary). When a short format, B-channel broadcast is received by the CSM-1 with this value set on the broadcast bit lines, then a calibration signal of the programmed length is sent to the attached mezzanine boards in preparation for an L1accept calibration trigger. Note that with a delay of zero duration for the B-channel command, the L1accept will arrive 28 clock tics **before** the calibration strobe begins (Figure 15). As the delay then increases, so will the arrival of the L1accept move later in time with respect to the start of the calibration strobe. A maximum delay of 255 clock tics can be set. The default duration of calibration strobe to mezzanine cards is 4μs (160 clock tics), the default value could be changed by using TTCvi **Long External Broadcast (or Individual) Command** with sub-address 2, where the 8-bit data value associated with this command is stored and used as the duration in clock tics of future calibration strobe signals to the mezzanine boards.

Calibration bit 6 can be synchronized with either de-skewed clock 1 or clock 2, depending only on the programming of the TTC. If the latter is chosen, then changes to the fine delay of this second de-skewed clock can scan the calibration across the width of a single 25ns bucket. See the section below on "TTC Considerations" for warning notes.

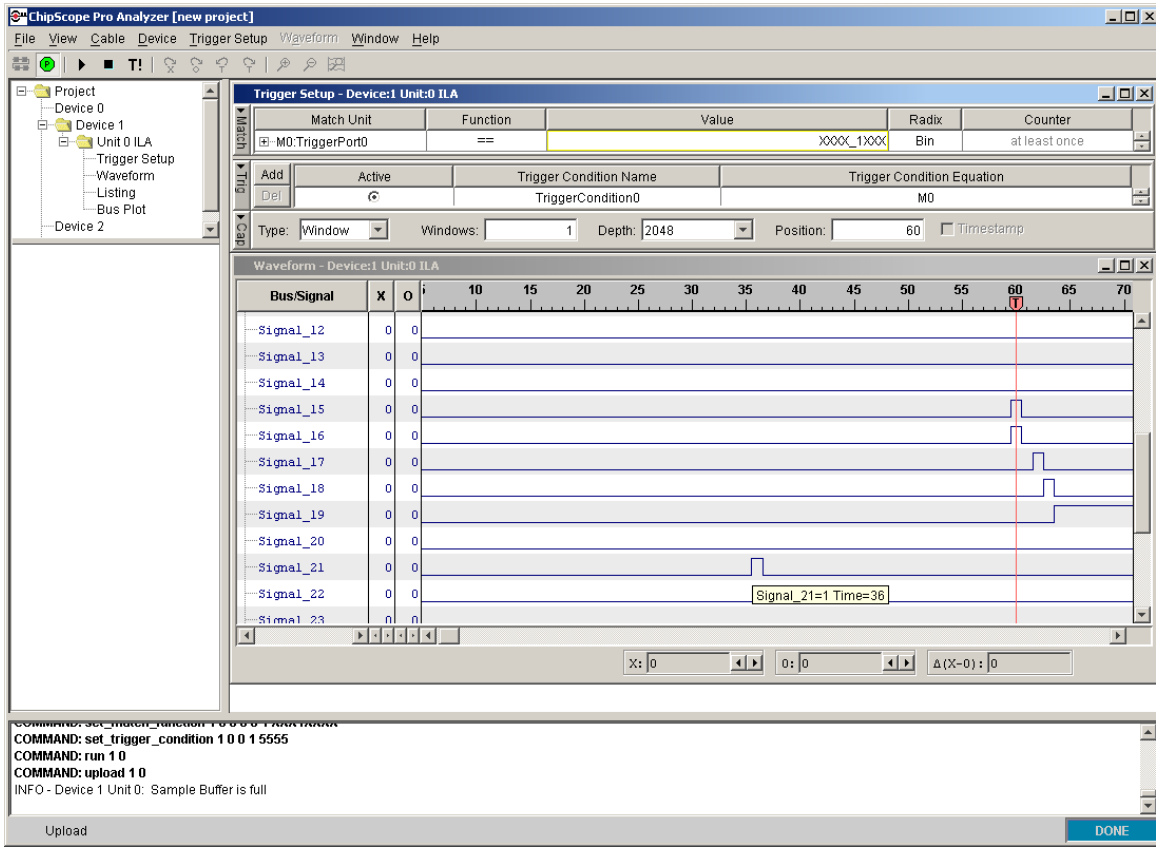


Figure 15. Chipscope trace detailing a calibration trigger initiated from a short-format, broadcast command. The L1accept is Signal_21, the TTC broadcast strobes 1 and 2 are Signals_ 15 and 16, respectively, and the calibration strobe is Signal_19.

Long Broadcast (or Individual) Commands:

The CSM-1 has been designed to respond to a variety of long-format B-channel commands. The documentation for the long-format indicates that an Internal/External bit should be set to indicate if the command is destined internally to the TTC, or externally to outside electronics. In both cases, the sub-address supplied with the command indicates exactly what command is to be executed by the addressed components. A TTC address of zero broadcasts the command to ALL TTCrx devices in the system. The **TTCrx parallel output bus enable bit must be set** in order to use this feature. The default setting of the TTCrx at power-up has this disabled.

Although the TTCrx makes the content of 10 of its 20 internal registers available on the parallel output bus in response to two internal commands (ERDUMP=4 and CRDUMP=5) the CSM-1 fpga no longer monitors for this condition. Instead an I2C master core has been implemented which reads the content of all 20 registers over the course of an 8 second cycle and makes them available within the JTAG read-back string. The content of the 20 registers is ordered within the CSM JTAG string as shown in Table 3, page 15, of the TTCrx Reference Manual version 3.7, with lower I2C-addressed registers in the least significant bit positions.

Three external sub-addresses are recognized by the CSM-1, namely, 1, 2 and 3.

- Sub-address 1: This command causes the CSM-1 to reset the TTC, reloading its programming as directed by the CSM-1 JTAG parameters.
- Sub-address 2: The 8-bit data value associated with this command is stored and used as the duration in clock tics of future calibration strobe signals to the mezzanine boards.
- Sub-address 3: This behaves the same as sub-address 2, except the calibration strobe is also pulsed in the expectation that a L1accept will follow along just as if this were a short broadcast calibration command.

All other external sub-addresses are ignored.

The timing between the calibration strobe and the L1accept is different when using long commands instead of short commands in two aspects. First, the B-channel, long-format command is always synced to de-skewed clock1, so changes in the fine delay will have no timing-related effect. Second, it takes 26 additional clock tics to send a long command than it does to send a short command, and so the calibration strobe associated with sub-address 3 will be 26 clock tics later. This means, for example, with a delay of zero duration for the B-channel command, the L1accept will arrive 54 clock tics **before** the calibration strobe begins (Figure 16). And last, but hardly least, the interpretation and use of the LHC clock by the TTC is not quite the same as that used internally by the CSM-1. The TTC documentation is quite specific about when its external signals are, and are not, valid. However, internally in the CSM-1 a four-phase core is used, which allows the LHC clock division by a factor of four. The primary clock of these four is not exactly in phase with the TTC clock (although the difference is quite precise) and so it gives rise to different delays in instances such as the long-format calibration. **It may be wise to re-visit this last issue prior to the fabrication of the final CSM.**

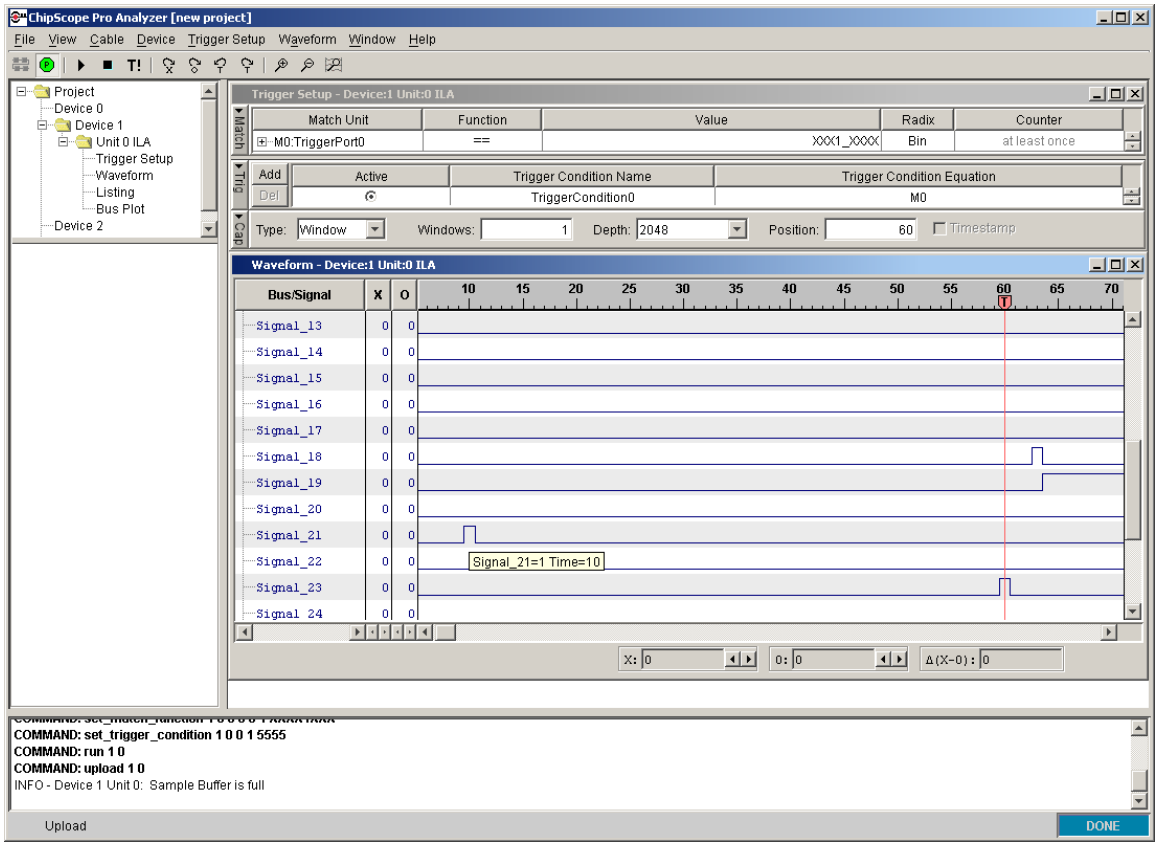


Figure 16. Chipscope trace detailing a calibration trigger initiated from a long-format, broadcast command. The L1accept is Signal_21, the calibration strobe is Signal_19, and the initiating "dout" strobe, occurring at time = 60, is Signal_23.

Mini-DAQ Operation for Calibration Triggers

Figures 17 through 20 illustrate the TTCvi command screens and hardware interconnect during a calibration trigger sequence. The initial TTCvi control screen (Figure 17) is selected from the Mini-DAQ "Execute→TTCvi Board Control" menu item. When the "RUN Type" is switched to "Calibration" from "Normal", the "Trig. Selection" will automatically switch to "L1A Calib. Trigger", completing the needed background setups. Now, the "B-Go/Calib. Control" button in the upper right corner can be clicked, bringing up the screen shown in Figure 18. B-Go number 2, which is used for calibration triggers, is now labeled as such. In this figure, it is configured for a short-format calibration. In Figure 19 it is configured for a long-format calibration, and appropriate values for the Data/Command (and TTCrx address, sub-address in the case of the long-format) have been entered in each case. Click the "FIFO 2" button at the bottom of the screen to initialize the software, and connect a pulser to the "B-Go 2" lemo input of the TTCvi (Figure 20) to begin triggering.

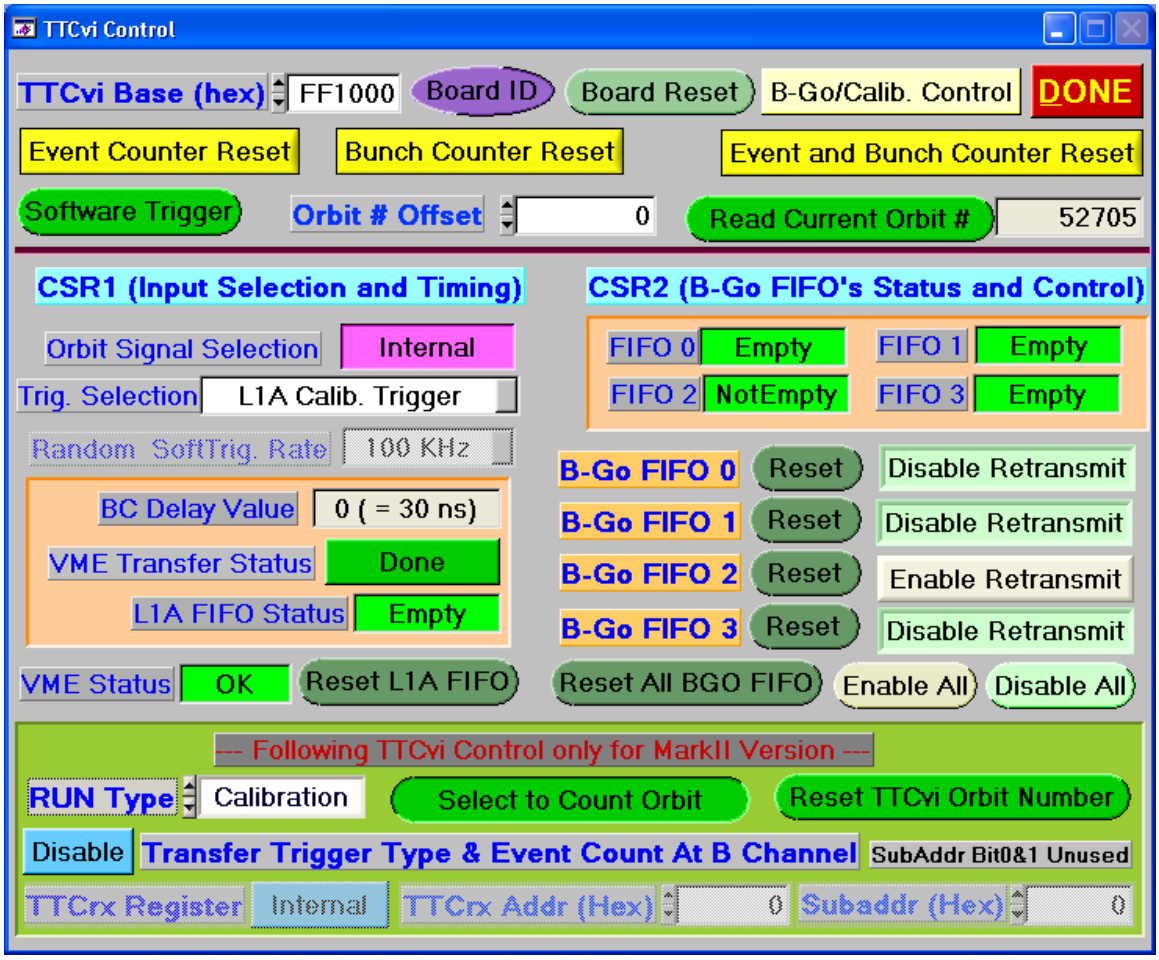


Figure 17. The TTCvi Control screen as it appears for a calibration trigger.

TTC Considerations

The delay between the calibration strobe and the L1accept could change with the final CSM. This is due to some pin-assignment problems with the current CSM-1 design, and the consequent choices made in the Verilog to overcome the poor placement.

The default TTC programming has its external parallel buses and de-skewed clock 2 disabled to save power. The current CSM-1 default programming for the TTC has the parallel buses turned on, but de-skewed clock 2 is not used. These settings will be established for the TTC each time the CSM-1 resets it if the "TTC_use_prom" bit is set in the CSM-1 JTAG programming.

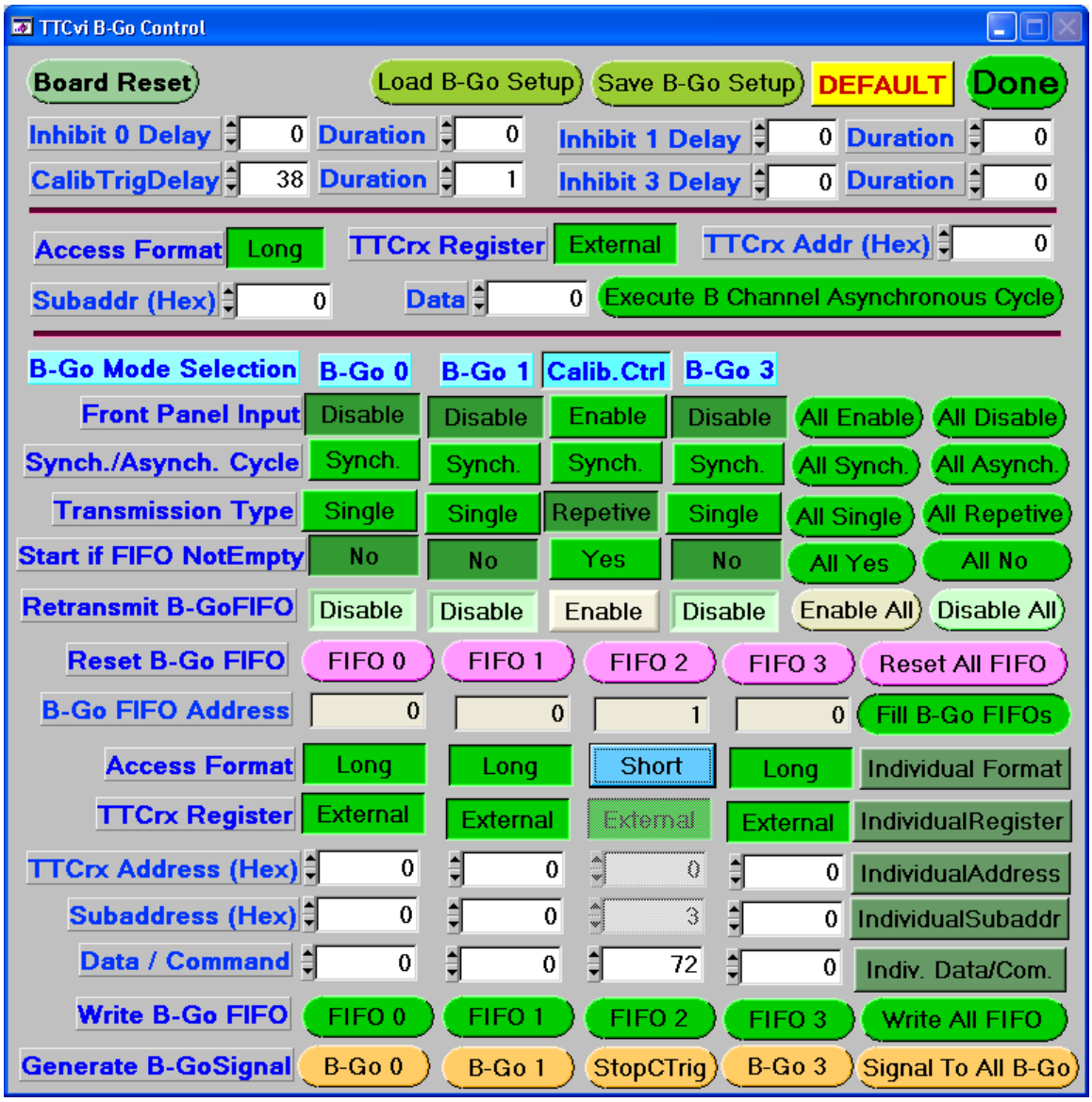


Figure 18. The B-Go control screen set up for a short-format, calibration trigger.

If the TTC control register is modified using a TTC internal IAC, the CSM-1 has no way of knowing this. You could, for example, turn on de-skewed clock 2 and select it for broadcast command synchronization, expecting to do a fine-delay calibration scan. This would not work though because the CSM-1 would be unaware of the change and would still attempt synchronization off clock 1.

Similarly, the registers could be modified to some other temporary purpose incompatible with a "standard" setup. In this case, an external IAC at sub-address 1 could be used to reset "standard" TTC operations at the completion of the special purpose task.

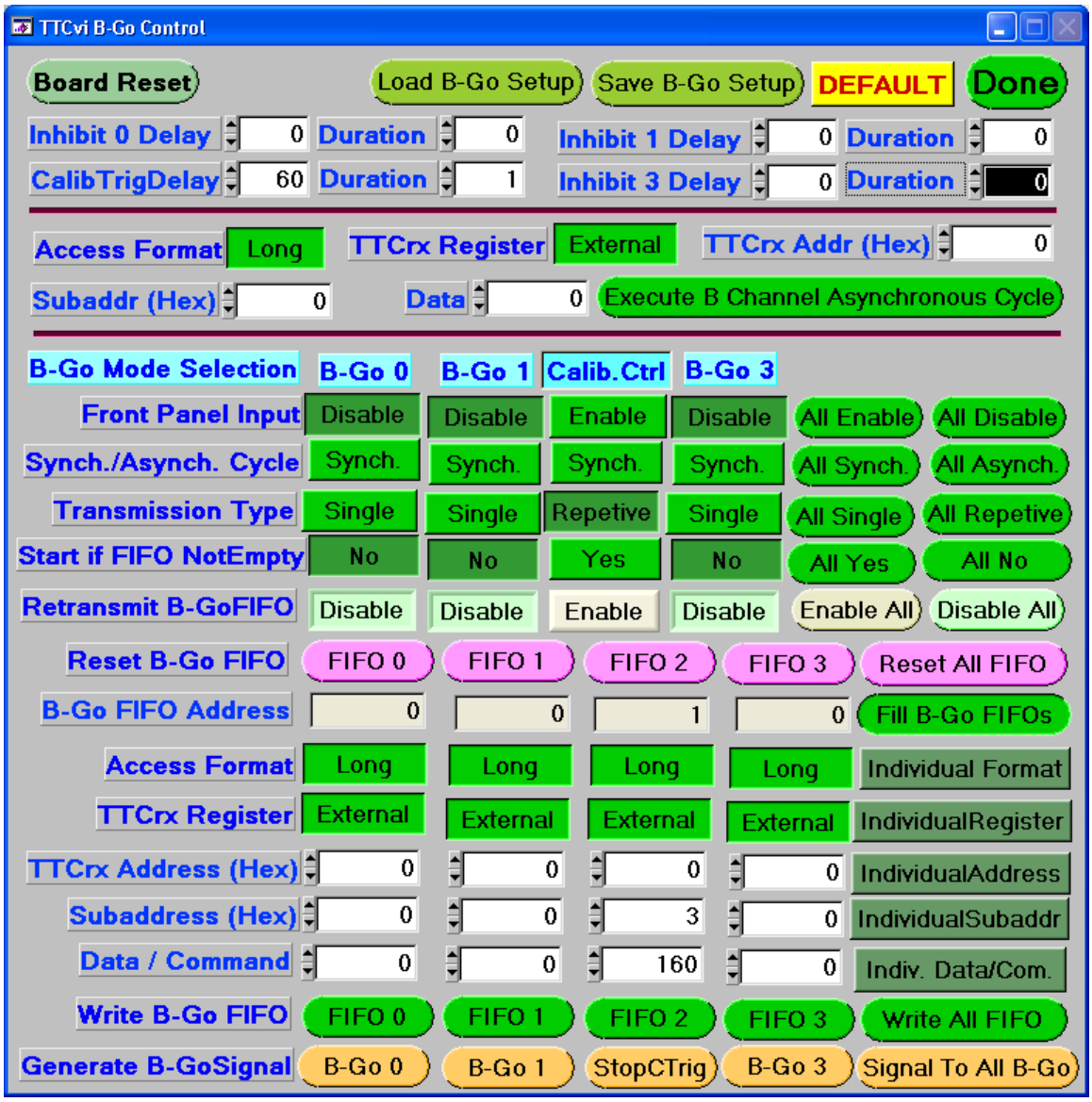


Figure 19. The B-Go control screen set up for a long-format, calibration trigger.

If the TTCrx is reset from the TTCvi without using the CSM-1 control, it will reset to its default parameters. However, the CSM-1 must present it with a valid TTC address at this time and won't know to do so. At the completion of the reset sequence it will therefore have some random and indeterminate address assigned.

A watchdog circuit reset will have this same undesirable impact.

Figure 20. Front panel of the VME, TTCvi module showing the lemo connection to the B-Go 2 trigger input (green cable stretching away to the lower left).