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1 TDC V2 Pin Assignment

1.1 Pin map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	GND	GND	CHNL_7P	CHNL_6P	CHNL_5P	CHNL_4P	CHNL_3P	CHNL_2P	CHNL_1P	CHNL_0P	TDO	TMS	A
B	CHNL_8P	CHNL_8N	CHNL_7N	CHNL_6N	CHNL_5N	CHNL_4N	CHNL_3N	CHNL_2N	CHNL_1N	CHNL_0N	Reset_in	TRST	B
C	CHNL_9P	CHNL_9N	GND	GND	GND	GND	GND	GND	GND	GND	TCK	TDI	C
D	CHNL_10P	CHNL_10N	GND	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST3	VDD_PST3	VDD_PST3	D
E	CHNL_11P	CHNL_11N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	TDC_DOUT1_N	TDC_DOUT1_P	E
F	TDC_CLK_P	TDC_CLK_N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	GND	GND	F
G	BCR_P	BCR_N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	TDC_DOUT0_N	TDC_DOUT0_P	G
H	CHNL_12P	CHNL_12N	VDD_PST0	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST2	TTC_N	TTC_P	H
J	CHNL_13P	CHNL_13N	GND	VDD_A	VDD_A	GND	GND	VDD_D	VDD_D	VDD_PST1	VDD_PST1	VDD_PST1	J
K	CHNL_14P	CHNL_14N	GND	GND	GND	GND	GND	GND	GND	GND	GND	ASD_DIN	K
L	CHNL_15P	CHNL_15N	CHNL_16N	CHNL_17N	CHNL_18N	CHNL_19N	CHNL_20N	CHNL_21N	CHNL_22N	CHNL_23N	ASD_LOAD	ASD_DOUT	L
M	GND	GND	CHNL_16P	CHNL_17P	CHNL_18P	CHNL_19P	CHNL_20P	CHNL_21P	CHNL_22P	CHNL_23P	ASD_DOWN	ASD_TCK	M
	1	2	3	4	5	6	7	8	9	10	11	12	

1.2 Pin type

GND	Chip ground, connect to same ground net on board
1.2V Analog Power	connect both VDD_A and VDD_PST0 to 1.2V analog power supply
1.2V Digital Power	connect both VDD_D and VDD_PST2 to 1.2V digital power supply
3.3V Power	connect both VDD_PST1 and VDD_PST3 to 3.3V power supply (3.0~3.6V)
SLVS_Input	CERN SLVS Rx in 130nm CMOS, 100 Ohm termination embedded

SLVS_Output	CERN SLVS Tx in 130nm CMOS
CMOS_3p3	VIL(-0.3~0.8V), VIH(2~3.6V), VOL(~0.4V), VOH(2.4V~)

1.3 Pin description

Pin Name	Type	Description
CHNL_xP(N)	IN	Differential pin pair of channel x
TDC_CLK_P(N)	IN	40MHz LHC clock
TTC_P(N)	IN	Trigger Time Control signal, could be decoded to trigger, BCR, master reset, event reset. All could be used in normal/legacy triggered mode. BCR and master reset could also be used in triggerless operation.
BCR_P(N)	IN	Bunch Count Reset, functions the same as TTC decoded BCR. Left floated or tied to ground if not used.
TDC_DOUT1_P(N)	OUT	Even bits for 160/320Mbps mode (Data[0](first serial bit out), [2], [4] , [6] ,[8]); Bits for 80Mbps legacy mode
TDC_DOUT0_P(N)	OUT	Odd bits for 160/320Mbps mode (Data[1], [3], [5] , [7] ,[9]) Inverted bits for 80Mbps legacy mode (DOUT0 = !DOUT1)
Reset_in	IN	Active low master reset. Resets the whole logic EXCEPT configuration register values in JTAG
TDI	IN	Standard JTAG TDI port
TDO	OUT	Standard JTAG TDO port
TCK	IN	Standard JTAG TCK port
TMS	IN	Standard JTAG TMS port
TRST	IN	Standard JTAG TRST port. Tied to HIGH if not used, can't be left floated
ASD_DIN	IN	Data received from ASD chain
ASD_DOUT	OUT	Data sent to ASD chain
ASD_TCK	OUT	Clock provided to ASD chain
ASD_LOAD	OUT	SLOAD signal provided to ASD chain
ASD_DOWN	OUT	SDOWN signal provided to ASD chain
VDD_A	POWER	1.2V analog power supply
VDD_PST0	POWER	1.2V analog IO power supply. Could connect to VDD_A
VDD_D	POWER	1.2V digital power supply
VDD_PST2	POWER	1.2V digital IO power supply. Could connect to VDD_D
VDD_PST1	POWER	3.3V ASD interface power supply.
VDD_PST3	POWER	3.3V JTAG interface power supply. Could connect to VDD_PST1
GND	GROUND	Chip ground, connect to same ground net on board

Notes about power pin filtering:

Power planes for VDD_A and VDD_D should connect to separate LDOs' output. VDD_PST0 could connect to the power plane of VDD_A, and VDD_PST2 could connect to power plane of VDD_D. For these six types of power pins, each type should have at least one decouple capacitor next to its pins. If the quadrant alignment BGA fanout is used, there will be space for at least six 0402 100nF decouple capacitors in the bottom plane right under the chip. Suggested two capacitors for VDD_A, two for VDD_D, one for VDD_PST0, and one for VDD_PST1. Decouple capacitors for VDD_PST1 and VDD_PST3 could be placed outside the chip, as these pins are next to the edge of the chip.

2 JTAG Chain

TDC V2 has a standard JTAG interface with control line TCK, TMS, TDI, TDO and TRST. There is no TRST pin reserved from the CSM 40-pin connector, which means TRST should be kept HIGH at all time to enable the JTAG interface. Besides IDCODE and BYPASS, there are 5 data register chains for the configuration of the TDC, 2 read-only chains for the chip status check, and 2 instructions for ASD write and read operation.

2.1 JTAG data register chain assignment

All data register chains are assigned as tables given below. For every chain, bit #0 is the last JTAG bit to enter the chain. Registers listed that have multiple bits have the following matching: In data register chain setup0, rising_is_leading [23:0] corresponds to JTAG bit [12:35], with rising_is_leading[23] corresponding to JTAG bit [12].

Instructions

	Instruction	length
IDCODE	5'h11	32
BYPASS	5'h0F	1
SETUP0	5'h12	115
SETUP1	5'h03	94
SETUP2	5'h14	36
CONTROL0	5'h05	8
CONTROL1	5'h06	47
STATUS0	5'h17	33
STATUS1	5'h18	25
ASDWRITE	5'h09	-
ASDREAD	5'h0A	-

2.1.1 SETUP0

Bit #	reg	length	default value	**note**
[0]	enable_new_ttc	1	0	0: Use legacy TTC protocol 1: Use new TTC protocol
[1]	enable_master_reset_code	1	0	Set to 1 to enable master reset from TTC
[2]	enable_direct_bunch_reset	1	0	Enable BCR from: 1: BCR pins 0: TTC pins
[3]	Disable event reset	1	0	Set to 1 to disable event reset
[4]	Disable trigger from TTC	1	0	Set to 1 to disable trigger from TTC
[5]	auto_roll_over	1	1	0: Use external BCR signals 1: Use internal periodic BCR set by roll_over values

[6]	bypass_bcr_distribution	1	0	Bunch count reset takes effect when: 0: a configurable delay defined by coarse_count_offset after BCR arrives 1: BCR arrives
[7]	enable_trigger	1	0	TDC working in: 0: triggerless mode 1: trigger mode
[8]	channel_data_debug	1	0	Set to 1 to enable debug mode
[9]	enable_leading	1	0	01: Pair mode (default) 00: Both edge in one data word (not available for 80Mbps) 1X : Single edge
[10]	enable_pair	1	1	
[11]	enable_fake_hit	1	0	Periodically reject out of date hit(only effective in trigger mode)
[12:35]	rising_is_leading	[23:0]	24'hFF_FFFF	0: Falling edge is leading edge 1: Rising edge is leading edge
[36:59]	channel_enable_r	[23:0]	24'hFF_FFFF	enable rising edge measurement
[60:83]	channel_enable_f	[23:0]	24'hFF_FFFF	enable falling edge measurement
[84:102]	TDC_ID	[18:0]	19'h7aaaa	Configurable TDC ID, TDC_ID[3:0] are used in AMT data format as TDC_ID
[103]	enable_trigger_timeout	1	0	If set to 1, a trigger trail will be sent out if not all the channel data has been sent out in 25.6us.
[104]	enable_high_speed	1	1	Serial interface working in: 1: 320Mbps/line 0: 160Mbps/line
[105]	enable_legacy	1	0	Set to 1 to enable 80Mbps AMT data format
[106]	full_width_res	1	0	The width information in pair mode will contain: 0: 8 bits 1: 16 bits.
[107:109]	width_select	[2:0]	3'b000	Width resolution in pair mode = (2^width_select)*finetime_LSB.
[110]	enable_8b10b	1	1	enable 8b/10b encoding for 320Mbps/160Mbps serial interface
[111]	enable_insert	1	0	Set to 1 to add IDLE packet
[112]	enable_error_packet	1	0	Set to 1 to add error packet in triggerless mode when channel overflow
[113]	enable_TDC_ID	1	0	If set to 1, output will be 5’b11111+19’b TDC_ID (not available in 80Mbps serial interface)

[114]	enable_error_notify	1	0	Not used

2.1.2 SETUP1

#	reg	length	default value	note
[0:9]	combine_time_out_config	[9:0]	40	The maximum pair width in case we lost the trailing edge (LSB=6.25ns)
[10:21]	fake_hit_time_interval	[11:0]	256	the period of the fake hit (LSB=25ns)
[22:33]	syn_packet_number	[11:0]	12'hFFF	the maximum no IDLE packet
[34:45]	roll_over	[11:0]	12'hFFF	The period of the internal bcr singal (LSB=25ns)
[46:57]	coarse_count_offset,	[11:0]	12'h000	The delay of the BCR taking effect after it arrives in TDC (LSB=25ns)
[58:69]	bunch_offset,	[11:0]	12'hF9C	Trigger matching offset (LSB=25ns)
[70:81]	event_offset,	[11:0]	12'h000	Trigger event offset
[82:93]	match_window	[11:0]	12'h01F	Trigger matching window (LSB=25ns)

2.1.3 SETUP2

#	reg	length	default value	note
[0:3]	fine_sel	[3:0]	4'b0011	raw TDC fine time digilization decoder
[4:5]	lut0	[1:0]	2'b00	
[6:7]	lut1	[1:0]	2'b01	
[8:9]	lut2	[1:0]	2'b10	
[10:11]	lut3	[1:0]	2'b01	
[12:13]	lut4	[1:0]	2'b11	
[14:15]	lut5	[1:0]	2'b00	
[16:17]	lut6	[1:0]	2'b10	
[18:19]	lut7	[1:0]	2'b10	
[20:21]	lut8	[1:0]	2'b00	
[22:23]	lut9	[1:0]	2'b00	
[24:25]	luta	[1:0]	2'b00	
[26:27]	lutb	[1:0]	2'b01	
[28:29]	lutc	[1:0]	2'b11	
[30:31]	lutd	[1:0]	2'b00	
[32:33]	lute	[1:0]	2'b11	
[34:35]	lutf	[1:0]	2'b00	

2.1.4 CONTROL0

#	reg	length	default value	note
[0]	rst_ePLL	1	0	reset ePLL
[1]	reset_jtag_in	1	0	reset TDC logic
[2]	event_reset_jtag_in	1	0	reset event ID from JTAG
[3]	chnl_fifo_overflow_clear	1	0	reset channel FIFO overflow indicator
[4:7]	debug_port_select	[3:0]	4'b0000	for debug purpose

2.1.5 CONTROL1

#	reg	length	default value	note
[0:4]	phase_clk160	[4:0]	5'b00000	ePll parameter
[5:8]	phase_clk320_0	[3:0]	4'b0100	
[9:12]	phase_clk320_1	[3:0]	4'b0000	
[13:16]	phase_clk320_2	[3:0]	4'b0010	
[17:20]	ePllResA	[3:0]	4'b0010	
[21:24]	ePllIcpA	[3:0]	4'b0100	
[25:26]	ePllCapA	[1:0]	2'b10	
[27:30]	ePllResB	[3:0]	4'b0010	
[31:34]	ePllIcpB	[3:0]	4'b0100	
[35:36]	ePllCapB	[1:0]	2'b10	
[37:40]	ePllResC	[3:0]	4'b0010	
[41:44]	ePllIcpC	[3:0]	4'b0100	
[45:46]	ePllCapC	[1:0]	2'b10	

2.1.6 STATUS0 (read only)

#	reg	length	note
0	instruction_error	1	pairty of the current instruction code
[1:32]	CRC	[31:0]	CRC of whole registers

2.1.7 STATUS1 (read only)

#	reg	length	note
[0]	ePll_lock	1	the lock statu of ePLL
[1:24]	chnl_fifo_overflow	[23:0]	the channel fifo overflow indicator

3 Working Mode and Data Format

3.1 Working Mode

The TDC could be configured to work in triggerless mode by setting the enable_trigger bit, SETUP0[7] to 0, or triggered mode by setting to 1.

With two output data lines running at 320Mbps or 160Mbps, both the triggered mode and the triggerless mode have 4 working modes: single-edge, double-edge, pair, pair with full width. The debug mode in triggerless mode gives extra information such as dropped coarse counter, fine-time register raw data, and a 2-bit hit number counter. The TDC could also send the programmable 19-bit TDC_ID out continuously if the enable_TDC_ID bit (SETUP0[113]) is set to 1. All modes with the corresponding values of the JTAG bits are shown below.

Reg Name	enable_trigger	channel_data_debug	enable_leading	enable_pair	full_width_res	enable_TDC_ID
Reg #	SETUP0[7]	SETUP0[8]	SETUP0[9]	SETUP0[10]	SETUP0[106]	SETUP0[113]
single-edge	X	0	1	X	X	0
double-edge	X	0	0	0	X	0
pair	X	0	0	1	0	0
pair full width	X	0	0	1	1	0
TDC ID	X	X	X	X	X	1
debug	0	1	X	X	X	0

When configured as one data line running at 80Mbps (enable_legacy bit, SETUP0[105] set to 1), the TDC could run in single edge mode and pair mode, both for triggerless and trigger modes.

3.2 Data Format

3.2.1 Triggerless mode (320/160 Mbps * 2 lines)

Width	5b	2b	17b	8b	8b	Total
Single-edge mode: Leading or trailing	Chnl ID	Edge mode “00”/”01”	Leading edge Time Measurement	nan	nan	24b
Double-edge mode:	Chnl ID	Edge mode “10”	Leading edge Time Measurement	Trailing edge Time Measurement 16LSB		40b
Pair mode: Leading + 8'b width	Chnl ID	Edge mode “11”	Leading edge Time Measurement	Pulse width	nan	32b
Pair mode full width: Leading + 16'b width	Chnl ID	Edge mode “11”	Leading edge Time Measurement	Pulse width		40b

Width	2b	5b	17b	2b	1b	2b	15b	4b	Total
debug	00	Chnl ID	Leading edge Time Measurement	11	edge type	hit #	dropped coarse counter	fine Q	48b

3.2.2 Triggered mode (320/160 Mbps * 2 lines)

Width	12b	12b			Total
Event Header	Event ID	Bunch ID			24b

Width	5b	2b	17b	8b	8b	Total
Edge-only mode: Leading or trailing	Chnl ID	Edge mode “00”/”01”	Leading edge Time Measurement	nan	nan	24b
Double-edge mode:	Chnl ID	Edge mode “10”	Leading edge Time Measurement	Trailing edge Time Measurement 16LSB		40b
Pair mode: Leading + 8'b width	Chnl ID	Edge mode “11”	Leading edge Time Measurement	Pulse width	nan	32b
Pair mode full width: Leading + 16'b width	Chnl ID	Edge mode “11”	Leading edge Time Measurement	Pulse width		40b

Width	14b	10b			Total
Event Trailer	Error Flag	Hit number			24b

3.2.3 Legacy mode (80 Mbps * 1 line)

Width	2b	4b	4b	12b	12b	1b	1b	Total
Header	01	1010	TDC ID	EVID	BCID	Parity	0	36b
Trailer	01	1100	TDC ID	EVID	BCID	Parity	0	36b

Width	2b	4b	4b	5b	1b	1b	17b	1b	1b	Total
Edge	01	0011	TDC ID	Channel	edge type	over-flow	leading edge time measurement	Parity	0	36b

Width	2b	4b	4b	5b	8b	11b	1b	1b	Total
Pair	01	0100	TDC ID	Channel	width	leading edge time measurement	Parity	0	36b

4 Serial Data Interface

4.1 8b/10b encoding format

For a triggerless pair mode 32bit TDC word, 8b/10b encoding starts at the MSB byte [31:24]. The MSB in every byte corresponds to bit H, and the LSB corresponds to bit A according to 8b/10b encoding definition. The odd and even bits of the encoded 10b data will be sent via two data lines. The dline1 (data line according to CSM motherboard interface) will transmit the serial data in the order of a, c, e, f, h, and dline2 (strobe line according to CSM motherboard interface) will transmit the serial data in the order of b, d, i, g, j, as shown in figure below. The dline1[4] and dline0[4] are sent out at the same 320MHz clock rising edge, and so are the following bits dline1[3:0] and dline0[3:0]. The entire TDC word will be sent out consecutively via the 2 data lines. After that, the serial interface will send out the next available TDC word stored in the interface FIFO, or comma code if the interface FIFO is empty at this moment.