UMHE-05-1

UMHE-http://atlas.physics.lsa.umich.edu/docushare

CSM-4 & Final CSM Design Manual

Design of the Chamber Service Module & Prototype 4(Rev E-)

University of Michigan
February 22, 2007

J. Chapman, P. Binchi, R. Ball, T. Dai, & J. Gregory

Final CSM Design & Development at UoM

OVERVIEW OF PROGRAM

The CSM-0 (a prototype CSM) is documented in specifications[1] on the University of Michigan ATLAS web server Docushare. It was developed as a first step toward the design of a production muon front-end readout multiplexer, initialization controller, timing distributor, and calibration controller. Documents on the DocuShare server are linked via ATLAS Electronics > MDT Electronics and are called “CSM-0 Development and Users Manual” and “CSM-0 Design Internals Document”. The general characteristic of the design has not changed and is specified in numerous ATLAS muon publications as the near chamber part of the NIMROD[2]. The work to design the CSM began with simulations of the dataflow and were reported in the LEB99 meeting in Snowmass[3] and are available on the Docushare server. The simulations were performed in VerilogHDL. A similar VerilogHDL description of the AMT-3[4] will when a similar description of the ROD[5] is complete, provide a tool for continuously evaluating the design as it matures. The prototype CSM-0 synthesized from the original VerilogHDL code will serve as an active test fixture for the design. This prototype was built as a 6U VME module containing the CSM unit, a JTAG interface, an LHC clock emulation, and a VME readable output FIFO. Since the timing and control functions of the LHC, the TTCrx[6] chip and its associated driver components, were not available in the test envi-

1. http://atlas.physics.lsa.umich.edu/docushare/default.htm
2. http://umaxp1.physics.lsa.umich.edu/~chapman/atlas/nimrod.ps
3. Proceedings of the LEB99 conference at Snowmass (1999)
4. http://atlas.kek.jp/%7earaiy/amt1/index.html
5. http://www.nikhef.nl/pub/departments/et/atlas)mdt/index.html
6. http://www.cern.ch/Atlas/GROUPS/FRONTEND/Ttc1.htm

ronments, these functions are designed into a separate Xilinx called the TTCem circuit. This additional Xilinx is required to accept the external trigger, to provide the EVID and BCID, and to synchronize the trigger with the free running clock that generates the simulated LHC crossing intervals.

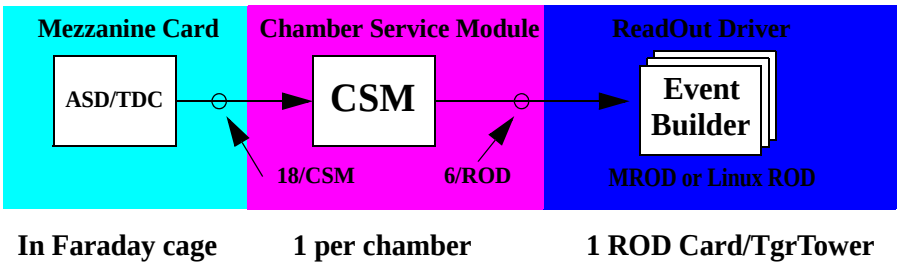
The differences between the CSM-0 and the final CSM unit mounted on chambers are significant but the two units have a one to one correspondence. The final on-chamber version is simpler in that it does not need to perform event building. Since the ROD must form events from 6+ CSM output streams, there is no need to do this job twice. The on-chamber CSM is therefore expected to do simple time-division multiplexing of data from the 18 TDCs. With this scheme the TDC from which any particular unit of data originates is determined from the word position in the time sequence. If no data is available from a specific TDC, an idle position-holder is sent. The full event building version of the CSM-0 can be thought of as a CSM/ROD pair that handles only one chamber in contrast to the input ROD module (called an MROD) where the event building takes place. Thus, the on-chamber CSM does not have a trigger ID FIFO, a deep input FIFO, or a word count FIFO. It has an optical output encoder and driver to send 32-bit words to the MROD module which accepts its output and the output from other CSM modules.

For compatibility with the CSM-0, the CSM-4 can be configured to do event building in exactly the same format as done by the CSM-0. In this mode the CSM-4 prepares an output record exactly in the format of the CSM-0 but transmits this data to the optical output link. When no data is being sent, optical idle codes are sent. This version can be used with a simple receiver/recorder package developed as a Linux data recorder only. The hardware of the Linux package was developed at CERN and can be either based on the S32PCI64 PCI card with a GOLA receiver board for a single chamber readout or with a 4 channel Filar card for readout of up to 4 chambers. This software is documented separately and available on the Docushare server at Michigan. As an alternate to the GOLA/Filar option a Linux based event builder in software is available. This option uses the time division version of the CSM for compatibility with the MROD and performs the MROD tasks in software. Output in this version is compatible with the MROD but data rates possible are far short of that demanded of the MROD.

The overall flow of data from the chamber wires up through the readout drive is represented in Figure 1 on page 2. In the final MDT system the Readout Driver will be the MROD. In test systems tit can be a single Linux processor with Filar cards. The simulation performed for the CSM/ROD contained the 18 TDC inputs each with their own serial data and clock. It described the output flow of data along the channel destined for the ROD. Event data units were collected from the TDCs by the CSM and transmitted in turn to the ROD modules. Data is transmitted from the CSM as 32-bit units serialized and sent on a single fiber. The 32-bit data units are either TDC headers, trailers, time digitizations, or various control words. The primary task of the CSM, called the CSM-4, is time-division multiplexing. Data from each TDC is sent as requested by the level 1 trigger when the front-end link from the individual TDC becomes free, *i.e.*, when data from all previous triggers are sent. Individual events are separated by header and trailer words. These header and trailer words are selectively enabled for transmission in the TDC. At least trailer words are required to indicate the end of event. The simulation assumes that both headers and trailers are sent for redundancy. In time division multiplexing mode all the 32-bit data words sent along the optical fiber to the ROD are sent

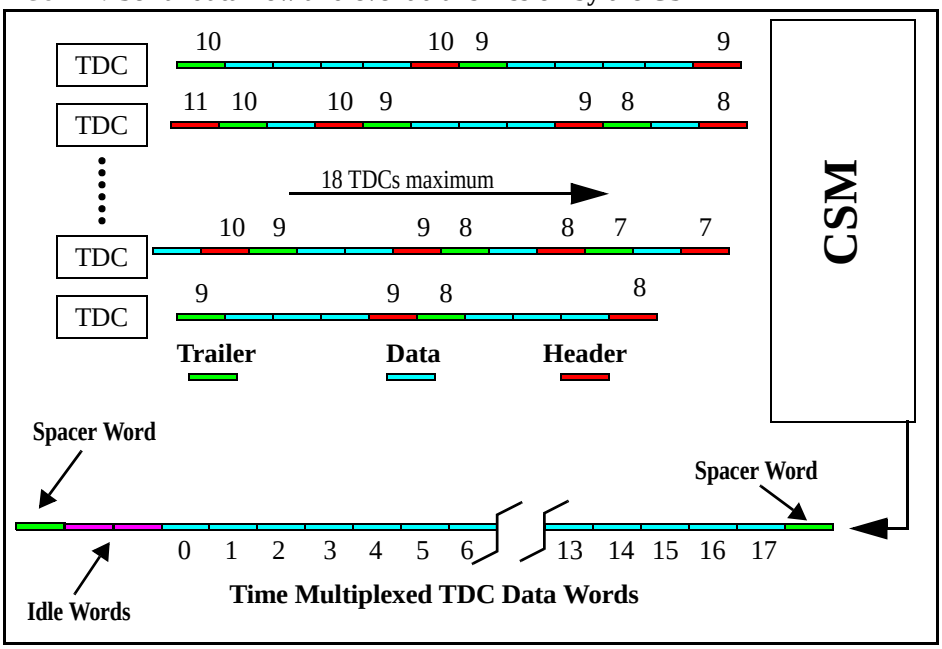
with "odd" parity. This parity is placed in the TDC source field (bits 27-24) of each word. The specific bit assignments are given below. For words received from the TDCs, one of these bits represents bad parity seen for the word during the TDC to CSM-4 transmission.

FIGURE 1. The Position of the CMS in the muon data flow.



The time-division CSM collects data from each of 18 individual TDCs into individual FIFOs, polls for data available in these 18 FIFOs, and if present simply forwards the TDC data to the ROD module in the time slot specified for that TDC. The time position in the output stream defines the source of the data. As a means to guarantee that the time positions are synchronized between the sending CSM and the receiving ROD module, a spacer word is sent as the 19th data unit each cycle. To insure synchronization of the sending and receiving clock, 2 optical link idle words (not to be confused with the idle word used to flag "no data" from an individual TDC) are sent following the spacer word. The basic flow of information is illustrated in Figure 2 on page 2.

FIGURE 2. Serial data flow and event transmission by the CSM



DESIGN SPECIFICATIONS

Module Subsections

The CSM will have six subsections. Figure 3 on page 5 illustrates these blocks, the JTAG initialization, the trigger timing and control, the optical transmitter, the serial to parallel receivers, the multiplexer, and the environment monitor. The list below further defines the content of these blocks.

1. The JTAG initialization block communicates to an external controller. This controller can be any unit which adheres to the JTAG standard that does not use the pause state during instruction or data shifting. The CERN designs for the TTCrx and GOL chips do not function correctly with JTAG tap controllers that use continuous clocks and enter pause states. Opto-isolation circuits provide for local ground separation from the external JTAG controller. Thus the external controller must supply its own power and ground to the CSM unit.

2. A second subsection contains the TTCrx chip and its optical receiver. It contains the reset functions, the EVID and BCID registers, the phase adjustments for the 40MHz clock, the decoding of the LVL1 trigger, and the calibration functions. The CSM makes standard use of the TTC system and requires no special interconnections. Since the CSM is configured as a simple time division multiplexer, it does not use the BCID and EVID registers when configured as a time division multiplexer.

3. The optical transmitter is based on the CERN-designed radiation-hard GOL chip and along with an Advanced Laser Systems VCSEL diode. The GOL unit accepts 32-bit words at up to 40Mhz for transmission along an optical fiber. The original design of the CSM assumed that 32-bit words at 25MHz was the maximum rate at which data needed to be sent. When data words are received at 40MHz from all TDCs (along with the spacer/idle words), the CSM can operate with an output transmitter at 25Mhz. An alternate option permits the CSM to transmit 32-bit data at 40MHz. This can be accommodated by the GOL and VCSEL if needed. At the MROD the 32-bit words are collected, the spacer word checked, the TDC empty words removed, and the actual TDC data stored. The optical transmission idle words do not appear at the receiver output. They serve only as synchronization characters.

4. Input from the TDCs arrives as a serial bit stream that is assembled into 32-bit words under the control of a sequence that seeks a start bit, assembles 32 data bits, tests a parity bit, and outputs the 32-bit data word with an accompanying data available bit. Since the entering data from the TDC arrives with arbitrary phase with respect to the local copy of the serial AMT output clock, a phase sampling circuit must be activated during the initialization to select the appropriate phase for sampling the incoming data. After this sample period the bit clock from the TDCs can be disabled to reduce EM noise and the mezzanine card power associated with generation of this clock. The AMT output clock rate can be selected to be 40MHz or 80MHz. The original design planned for use of the 40MHz rate. However, when the pair mode of the ASD-AMT chain was found to have difficulties when narrow noise pulses, the 80MHz option has been adopted and verified to function successfully.

5. An input multiplexer subsection polls for data from the Serial to Parallel circuit at the AMT output clock rate, transmits found data to 18 individual FIFOs, one for each TDC. Once the data is stored the data available bit is reset. This section include

input buffer overflow control which is necessary when 80MHz input operation is enabled. To avoid critical data loss the CSM selectively ignores incoming data when the input buffers are in danger of overflow. Since input words from the AMT are of varying importance, a hierarchy of word types is defined. Header and trailers are designated as critical, leading edges and errors as next, and trailing edges and mask words as the lowest priority. Two buffer capacity thresholds are defined. When data words in the buffer exceed the lower threshold, no additional trailing edges or mask words are accepted. When the higher threshold is exceeded no leading edges or error words are accepted. If the thresholds are set properly, headers and trailers will never overflow the buffers at the trigger rates permitted. To inform the MROD of any deletions, two flags are sent with the event trailer. Bits 25 and 24 of the words sent to the MROD accept these two flags. In normal words these bits are set to zero. In the trailer word from an AMT, bit 24 flags the rejection of one or more leading edges or error words and bit 25 flags the rejection of one or more trailing edges or mask words. These two bits originally contained the TDC number which is both redundant (the time division position specifies the TDC) and limited to 4 bits with 18 AMTs permitted.

6. A second polling multiplexer scans the individual TDC FIFOs for data and if found sends the 32-bit data unit to the optical transmitter. If no data is present in the FIFO for the polled TDC, an empty TDC flag word is transmitted for the TDC. This section was designed for 25MHz operation but with the change to accept data from the AMT at 80MHz, operation of this polling multiplexer at 40MHz is anticipated but must still be checked.

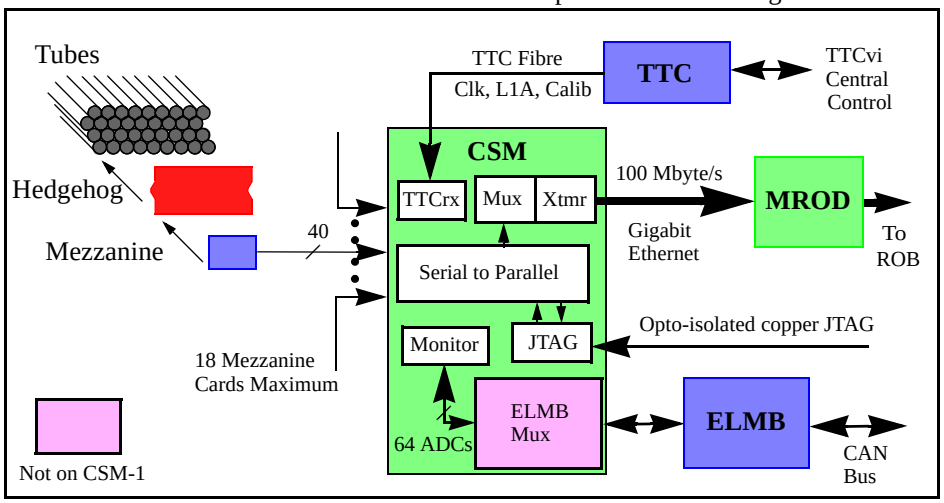
7. At the conclusion of the 18 step TDC poll, a spacer word is inserted to insure time step synchronization between the CSM and the MROD. This word contains a special code, Dnnnnnnn, in hex. Two optical link idle code words follow the spacer word. These insure link synchronization and do not appear as words to the MROD.

8. The TDC data words and their parity bits are modified so as to include parity information both for the received parity from the TDC and to define independently the outgoing parity. Since the TDC identifier field (4-bits) of the TDC word is redundant, given that the data source is defined by the location of the word in the time sequence, part of this field is overwritten with two parity related bits. The lower two bits are used for flags as discussed in a later section. Bit 27 is set to contain a parity error flag if the incoming word from the TDC fails the parity test done within the CSM. Bit 26 of the outgoing TDC word is set so that the parity of the outgoing word is odd (including the Bit 27 error flag).

9. The final subsection provides for voltage and temperature monitoring. The cable from each mezzanine card provides a connection to its analog voltage regulator output, its digital voltage regulator output, and to an on-board temperature sensor. These 18 x 3 lines plus similar lines from the CSM regulators and temperature sensor, are routed to a 64 channel analog multiplexer and ADC. The 64-channel ADC is a direct copy of the ELMB version fabricated on the back side of the CSM. The

The Block Diagram

FIGURE 3. The Block Diagram. The Opto-isolated JTAG connection is provided by the ELMB in addition to the analog multiplexer for voltage and temperature sensing. Several different sources of the JTAG have been implemented for testing as well.



Serial to Parallel

The TDC resets to an idle state from which it sends no data. The reset can be derived from the TTCrx and also received by the CSM via JTAG. This reset erases any previous activity on the input lines from the TDC. After a reset, the phase of the incoming data from the TDCs must be sensed. This is done using the 4 phases of the serial clock provided by the Xilinx Digital Clock Manager, DCM. This unit includes a DLL for clock locking and also provides 0, 90 180, and 270 degree versions of the clock. To perform the needed sampling of the phase of each TDCs arriving data bits, an automatic selection of the best choice between the 4 phases is made. The clock phase is chosen so that the data changes between 180 and 270 degree versions of the chosen clock phase. When the sampling circuit stores its choice (after sampling over 2-3 cycles), normal data sensing can begin. At this point the individual clocks from each of the TDCs can be disabled saving power and potential clock noise pickup at the mezzanine card.

In normal operation, the start bit is sensed, 32 data bits are assembled into a shift register, parity is tested, and a stop bit is demanded for each TDC data word. Parity is tested and an error bit is saved for reporting to the MROD. At this time the data ready flag is set indicating that the 32-bit output register plus a parity flag contains data. This register cannot change more than once every 36 bit times since the data stream contains a start bit, 32 data bits, parity bit, and 2 stop bits.

Input Accumulation

The 32-bit data words arrive from each TDC based on the data present in that particular TDC and the availability of its output sequencer. Therefore, although all TDCs send data for a given EVID before processing the next, data from a given TDC does not have a well defined timing relationship to data for the same EVID from other TDCs. The CSM is designed to be a simple time division multiplexer and is not responsible for event building. Thus, it can simply transmit the assembled 32-bit words to the MROD in the next available time slot for the particular TDC. At the 40MHz serial clock rate data

arrives at a maximum rate of 1.143 MBits/s from each TDC. One word from each channel is transmitted each 21 word cycle. Any rate of serial transmission on the fiber greater than 97 MBytes/s will not require any buffering within the CSM. This data rate can easily be handled by the GOL sending 32-bit words at 25MHz or greater. For operation with a serial input clock at 80MHz, the situation is such that twice this rate would be required to assure that no data is lost. Since the GOL and VCSEL are certified to run only up to 40MHz, a possibility of data loss exist even at the highest rate possible.

To prevent the loss of critical sequencing information, a buffer control scheme is included that will selectively delete trailing edges and mask words at one threshold and leading edges and error words at a higher threshold always leaving room for heders and trailers. When deletions occur the MROD is informed on an event by event basis by providing two flags in the event trailer word when words are deleted in these two classes. The AMT word count is not changed when these deletions occur providing the MROD with a second indication that deletions occurred. Note, it is possible that only the higher threshold flag is set since deletion flags are only set when a word of their respective class is deleted. If no low threshold word type appears in the data stream no deletion can occur even if the buffer is filled above its threshold.

Multiplexer

It is expected that both header and trailer words will be enabled in the TDC. These header and trailer words each contain the EVID. Since the CSM does no test beyond parity checking, these words are processed the same as any other data words from the TDC. Data words can be sent to the MROD whenever the link is up and the currently polled TDC has data available. The link will be unavailable from a reset until resynchronization is established. The CSM will send data only when the link is active and must therefore, be resynchronized whenever the link goes down. The amount of data lost will generally be significant since resynchronization requires many clock cycles. The loss of synchronization is sensed at the MROD, were a reset will be initiated. This reset will probably need to set the CSM and TDC to idle over JTAG, disable triggers being sent from the CSM to the TDCs, resynchronize the link, and reestablish triggers. Lost data for the interval required to do this resynchronization needs to be flagged at the MROD where the BCID and EVID for triggers is available. Information defining the last event fully transmitted to the MROD is available in the EVID/BCID values within the data. A reset and resynchronization for any reason will require EVID/BCID resynchronization between units that have not lost data and have advanced their EVID. BCID resynchronization will take place every turn of the LHC machine. If triggers are initiated only after a complete turn, synchronization of BCID is assured.

Fibre Protocol

The output from the CSM is in 32-bit data units, either TDC data words, empty TDC codes for TDCs that have no data, spacer words, or link idle codes. These words are to be sent to a fiber encoder/driver. The low power CERN GOL chip can accept 32-bit words at rates up to 40MHz. This is well above the 25MHz required to remain ahead of the data arriving from the TDCs at 40MHz serial input rate. The choice of the 25MHz transmission clock, was based on the expectation of 40MHz serial rate. With an 80MHz serial input rate we expect to operate the output link at its highest speed, 40MHz. The code in the CSM-4 is currently arranged to send no data to the GOL until the first trigger

is seen and to not send data for time division cycles (19 word groups) when no data is available from any TDC.

Data Word Formats

The data words from the TDC are described in the AMT-3 document[7] and summarized in Table 1 on page 7. Note that the header and trailer words from the TDC provide the EVID and the BCID words. The location of these bits permits a check of the data arrival consistency as described above. The TDC data words also contain an error bit that indicates when data has been missed. The data miss bit is to be interpreted as a flag that data was lost between the time of the last data unit without a flag set for a given TDC and the data units with flags for that TDC. The CSM defines two additional IDs, one for the TDC empty word and one for the spacer word. The IDs for these words are tentatively

TABLE 1. TDC Data Word IDs and contents

ID	Word Contents Depends on ID Type																													
31-28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1010	TDC				EVID												BCID													
1100	TDC				EVID												Word Count													
0010	TDC				Mask Flags																									
0011	TDC				Channel					T	E	Coarse Time													Fine Time					
0100	TDC				Channel					Width									Coarse Time						Fine Time					
0110	TDC				Unused																							Errors		
0111	TDC				0000												BCID													
0111	TDC				0001															R	L1 Occupancy									

defined in Table 2 on page 7. In the time division multiplexing scheme each TDC word is sent in a time slot defined in terms of the spacer word position. Following the spacer word, TDC unit 0 data is sent or if no data is available, an TDC empty word is sent. The next time slot contains TDC unit 1 data if any is available. This process is described in a note by Thei Wijnen[8] on the NIKHEF web page. The TDC field in Table 1 on page 7 is

TABLE 2. CSM IDs for TDC empty (0000) and Spacer word (1101)

ID	Word Contents Depends on ID Type																													
31-28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0000	0	1	0	0	0																									
1101	0	0	0	0	0																									

replaced by the 4-bit field [Bit 27 - 24] composed of [a TDC parity error flag (bit 27), a force odd parity bit (bit 26), and a 2-bit buffer control flag (bits 25 and 24)], where TDC

7. http://atlas.kek.jp/%7earaiy/amt1/index.html
8. http://...lookup Thei Wijnen note on the data stream for TDM

parity error flag = 1 if the parity of the received TDC word was not correct and where the force odd parity bit is set to make the overall 32-bit word odd parity. The 2-bit buffer control flag is only sent with an AMT trailer (in other words the bits are 00) with bit 25 indicating deletion of one or more trailing edges or mask words and bit 24 indicating the deletion of one or more leading edges or error words.

A special set of formats exist for the CSM-4 when operating in event building mode. In this mode the CSM-4 generates output comparable to that of the CSM-0. These special outputs are defined in Table 3 on page 8. There are CSM headers and trailers defined, wire encoding for TDC 16 and 17, and a set of error conditions that flag incomplete events, events with one or more parity errors in transmission from one or more TDC, and the conditions that caused the error. The wire encoding used in the CSM-0 is also used here. See the CSM-0 Users manual[9] for details of this encoding.

TABLE 3. Special CSM-4 Output Word Formats in Event Builder Mode

ID	Word Contents Depends on ID Type																													
31-28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
CSM-4 event builder output formats defined to date																														
0101	1001	EVID																	BCID											
0101	1011	EVID																	Word Count											
0101	1101[a]	EVID																	Word Count											
0101	0000	Error Code								Abnormal TDC																				
0101	0010[b]	EVID																	Word Count											
1010	TDC	EVID																	BCID											
1100	TDC	EVID																	Word Count											
0011	Wire Number										T	E	Coarse Time												Fine Time					
0100	Wire Number										Width										Coarse Time						Fine Time			

a. This subID flags an abnormal event termination which is preceded by the error word with subID zero.

b. This CSM sub-type is a pad word, and appears only when event buffers are padded to a multiple of 64(256) words. These follow the CSM trailer (sub-type 1101 or 1011), and the Word Count does not include them in the total.

For the CSM-4 event builder, the error words beginning with ID and subID 0x0101 and 0x0 the meanings of the remaining bits are given in Table 4 on page 8 below.

TABLE 4. Flag Bits for CSM-4 Event Builder Errors

Error or Flag	Bit Posn
Abort was due to missing header/trailer (hdr_trl_abort)	23
Abort was due to missing header (miss_hdr_abort)	22
Abort was due to dpram over threshold	21
Abort was due to a timeout waiting for data	20

9. http://atlas.physics.lsa.umich.edu/docushare/dscgi/ds.py/View/Collection-207

TABLE 4. Flag Bits for CSM-4 Event Builder Errors

Error or Flag	Bit Posn
Flag -- BCID matching is disabled	19
Flag -- EVID matching is disable	18
Flags for AMTs with both good and complete data	17-0

THE CSM MODULE SPECIFICATIONS

Component Details

The TTCrx

The TTCrx has the following functions:

- The TTCrx receives fibre data from the central timing and control logic, regenerates the 40MHz LHC clock, receives the commands, and presents these commands including the LVL1 trigger to external logic. It maintains counters for EVID and BCID that are presented to external pins along with the LVL1 accept and other commands.
- It provides for independent phase adjustments of two copies of the 40MHz clock.
- It provides for calibration pulses coordinated with LVL1 triggers appropriately delayed from the calibration timing.

The timing and calibration role of the TTC system is illustrated in Figure 4 on page 10. In this figure, the role of the TTCrx for timing and calibration pulsing is shown. In addition, the role of the JTAG in establishing the parameters for the test calibration within the CSM and mezzanine cards is illustrated. The TTCrx provides two clock outputs each with its own phase adjustment down to the 104ps least count. One of these phases will be adjusted for gating of commands from the TTCrx including the LVL1 accepts and resets. The second phase will be used to initiate the calibration pulse, permitting adjustable timing to the TDCs in 104ps steps.

The CSM-4 acts in response to a subset of both long and short format TTC commands. The only short format command to which it responds, besides the EVID and BCID resets, is that which initiates a calibration trigger sequence for the attached mezzanine boards. This command has user bits 3 and 6 set on, and all other bits set off or ignored (010010xx). The two least significant bits are ignored as they correspond to the EVID and BCID clear strobes. A document specifically concerned with calibration[10] is available.

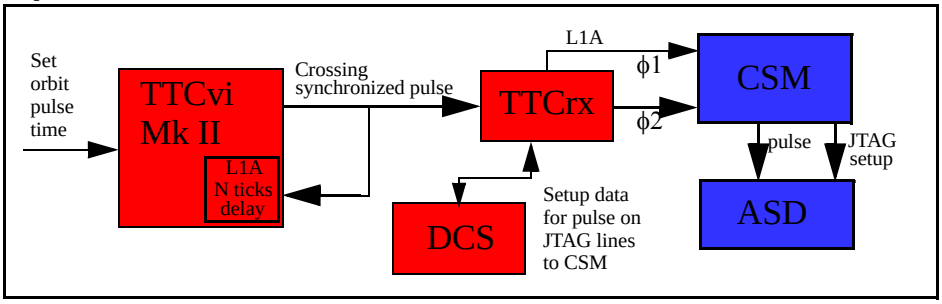
Three Individually Addressed Commands (IAC), or long format commands, initiate CSM-4 activity. These are detailed in Table 5 on page 9 below, and are discussed at length in Reference on page 10.

TABLE 5. Individually Addressed Commands recognized by the CSM-4

SubAddress	Data Bits	Action
1	xxx	Initiate TTC reset
2	Strobe Duration	Set the duration of the calibration strobe to the given number of 25ns clock tics
3	Strobe Duration	Set the duration of the calibration strobe, as above, and initiate the strobe itself.

The three commands detailed in Table 5 on page 10 are “external” TTC commands, i.e., they are relayed to the circuitry attached to the external busses and lines of the TTCrx. Each TTCrx also responds to several “internal” commands, sometimes with detectable external actions. In particular, the CSM-4 monitors for the response to the internal ERDUMP and CRDUMP commands, which result in the external presentation by the TTCrx of the contents of 10 of its 20 8-bit registers. This content is latched by the CSM-4 and included in the JTAG bit-stream shifted out of the chip. See the section on JTAG programming in this manual for more details.

FIGURE 4. The Role of the TTCrx and JTAG Systems for Calibration. Calibration parameters are established via JTAG from the DCS system followed by TTCvi commands as needed to generate the signal injection and to trigger a level 1 accept for acquisition of the data.



The Serial to Parallel Units

In the CSM-0 the serial to parallel conversion of data from the TDCs was done in three small Xilinx FPGAs, each processing 6 channels of TDC data. This same arrangement could be implemented in the final CSM. However, the availability of more logic and higher pin counts in newer FPGAs makes it possible to place all channels in a large chip along with logic for the multiplexer. The presence of DLL clock circuits with multiple, phase outputs further aids this process by enabling incoming data sensing at the phase appropriate channel by channel. The serial to parallel circuits implement the logic to:

10. CSM-4 Calibration Triggers, http://atlas.physics.lsa.umich.edu/docushare/dscgi/ds.py/View/Collection-214

- Autosense the individual TDC data streams and select the appropriate 1of 4 possible clock phase to sample the arriving data. Disable the TDC clock after sampling through the JTAG programming of the AMT-3.
- Reset to a quiescent state expecting a logic true start bit as the first data element from each TDC.
- After a start bit is received, begin assembly of the next 32-bits into a register.
- Compute and test the parity of the 32-bit string, setting an error flag if a fault is seen.
- Transfer the 32-bits to a holding register upon receipt of the stop bit, set a “data ready” flag indicating data present, and return to the quiescent state.
- Reset the “data ready” flag upon receipt of an “acknowledge” signal from the polling multiplexer.

The JTAG Interface

The JTAG signals connect to the CSM at a programmable PROM, and then to the FPGA, passing next to the GOL chip, and finally to the TTCrx. From there it returns to the FPGA on user handled pins. The JTAG chain is distributed to the mezzanine cards as defined by the enable bits for individual TDCs. Connection of the JTAG bus to the mezzanine cards is totally controlled in the FPGA code and can be modified as required. The Virtex-II series of Xilinx chips used for the CSM implementation support numerous I/O levels and standards which include LVDS and differential PECL. The chips power-up and initialize to an active TAP (JTAG) control for downloading configuration data. To provide external control of this bootstrap procedure, external circuitry must be able to force this “first state” for configuration to occur. The external JTAG can be provided by any commercial controller or by the DCS system. One means of forcing the “first state” will be to cycle the power. The TTCrx system could also generate a global reset. Careful evaluation of the startup operation must be done to insure that no frozen states exists other than through a true hardware device failure. This JTAG link will support the following functions:

- Initialization of the FPGA code within the Xilinx chips.
- Initialization of the parameters of the CSM and ASD/TDC cards
- Initialization of the parameters of the TTCrx.
- Controlling the run/reset/resynchronization of the CSM, TDC, and ASD

The Polling Multiplexer

The polling multiplexer is actually two polling multiplexers, one that scans for data ready flags from the 18 serial to parallel units and enters data found into 18 distinct FIFOs and a second that scans for FIFO data and if found places it into the time division sequence of the output optical transmitter. The polling rate of the first multiplexer is based on the 40MHz LHC clock and the rate of the second is 25MHz as set to guarantee to empty the FIFO faster than it can fill. The first multiplexer sequences through the steps:

- Reset to polling address to TDC 0 and to idle mode (not active).
- If in active mode, examine the “data ready” flag for the currently addressed TDC.

- If data is available, send it to the FIFO for the addressed channel and reset the flag.
- Increment the TDC addressed and loop.

The second multiplexer has 21 steps. Eighteen of these steps are associated with the 18 FIFOs that hold data from the individual TDC. One, 18, defines the state when the spacer word is to be transmitted. The remaining two correspond to optical fiber idle words. The sequence through the steps:

- Reset the polling to address 18 and to idle mode (not active).
- If the polling multiplexer address is 18 output a TDM spacer word to the GOL chip.
- If the multiplexer address is 19 or 20 send a Gigabit Ethernet idle code.
- If the address is 0-17, test the FIFO for data in the addressed channel.
- If no data is present in the FIFO, send a TDC empty word.
- If data is available for FIFO (TDC) addressed, send an “acknowledge” to the FIFO to declare that the word has been taken and send the word to the GOL chip.
- Increment the polling address modulo 21 to advance to the next step.

The Fibre Sequencer

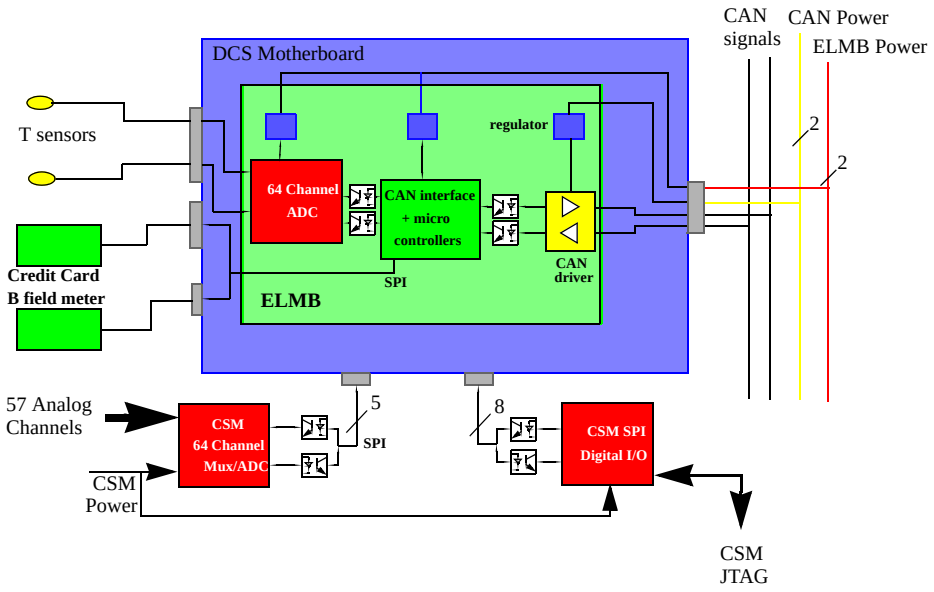
The GOL chip accepts 32-bit data words from the polling multiplexer and a 2-bit write control that:

- Sends a Gigabit Ethernet idle, if the 2-bit control is 00. The 32-bit data is ignored.
- Sends the 32-bit data presented to the GOL, if the control is 01.
- Sends an Extend code, if the control is 10.
- Sends a transmit error code, if the control is 11.

The DCS Analog Monitor

The 64-channel analog monitor is a direct copy of the 64-channel ELMB multiplexer designed by the DCS group and is assembled on the CSM to monitor the voltages and temperatures of the mezzanine cards and of the CSM itself. It is powered by the CSM 3.3 volts via a switched capacitor regulator that outputs 5 volts for the unit. Connections to the ELMB processor are optical isolated using the same components as used for the ELMB multiplexer that monitors chamber conditions. The location of the monitor on the CSM is chosen to minimize the interchange of signals between the CSM and the DCS circuitry. Only 5 opto-isolated signals are needed to provide JTAG to the CSM. In addition, a second set of 8 I/O lines from the ELMB processor will be extended to the CSM and opto-isolated. The extension provides for monitoring 64 differential signals or 128 connections. Of these 57 differential signals are anticipated, 3 from each mezzanine card and 3 from the CSM. Figure 5 on page 13 illustrates the relationship of the DCS to the CSM mounted portions of the DCS.

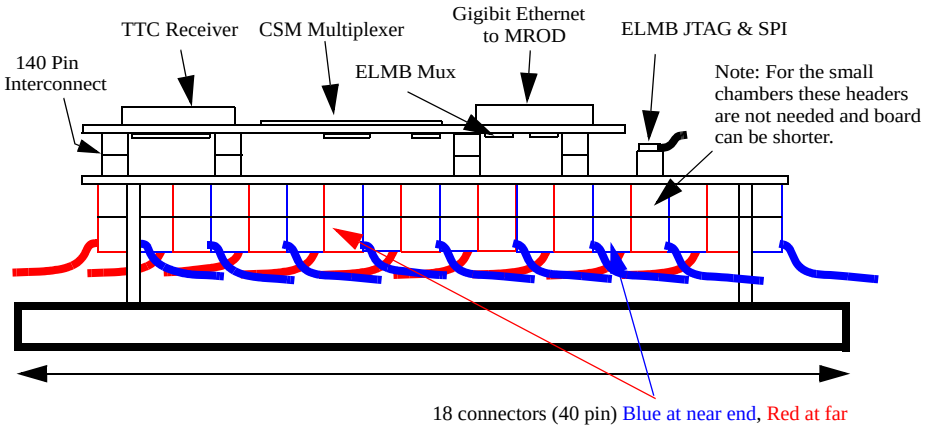
FIGURE 5. Relationship of the DCS elements on the CSM to the DCS System



CSM Interconnects

Figure 6 on page 13 shows the layout of the CSM. An arrangement with all passive components on a motherboard whose role is to provide attachment to the 18 mezzanine cards via their 40-pin connectors.

FIGURE 6. The Layout and Interconnection of the CSM



Note: ELMB Mux is copy of 64 channel DCS mux

These signals must be routed to various subsections according to the list below.

- Mezzanine to CSM Motherboard x 18 max
  8 JTAG (LVDS), 8 Data/CLK (LVDS) = 16 lines
  8 Analog PWR, 8 Digital PWR, 6 Sense, 2 Calibration = $24 \rightarrow 40$ lines total

- CSM to CSM Motherboard - 3 x 140 pins = 420 pins
  8 JTAG (LVDS), 10 Data/CLK (LVDS) x 18 mezzanine cards = 324 lines
  6 Sense, 8 Digital PWR, 8 ELMB PWR = 22 lines
- ELMB Mux to CSM Motherboard
  6 Sense x 18 Mezzanine cards, 6 Sense x 1 CSM = 114 lines
  5 JTAG I/O, 5 ELMB SPI, & 3 Spares = 13 lines

The Layout, as seen from above, is shown in Figure 7 on page 14. Note that for chambers not requiring more than 12 TDCs, that the motherboard can be reduced in size to the area required by the active components. This will entail the design of 2 different motherboards but affords the option of a short unit for small chambers.

Need new picture of real CSM-4

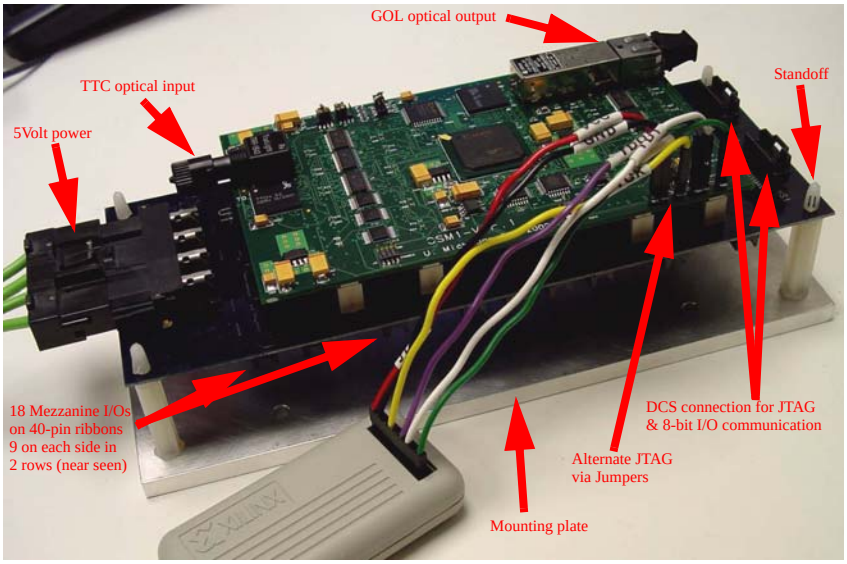


FIGURE 7. The CSM-4 and Motherboard.

Pseudo-pair Mode

Pseudo pair mode is designed to take leading and trailing edges into pairs in the same format that was defined for the AMT-3. The implementation of this pair mode is straight forward in the pipelined operation of the CSM-4 with some exceptions that must be handled. Since the 32 deep input FIFOs of the CSM can fill if dataflow from the AMT-3 arrives at 80MHz, sensing of overflow conditions is required. The number of words present in these FIFOs is known so actions can be taken dependent on the remaining space in the 32 words. We propose two thresholds, the first set when AMT mask and trailing edge words are to be discarded and the second when AMT leading edge and error words are discarded. In addition, we propose to define two flags in TDC to indicate that words in the event have been discarded. Bit (24) flags the removal of trailing edge trailer (ID=0011 and T=0) and mask words (ID=0010) and Bit (25) flags the removal of leading edge (ID=0011 and T=1) and error words (ID=0110 or 0111). Four slots in the 32 word FIFOs will always be reserved for headers and trailers.

When operating in pseudo pair mode, the first of two consecutive leading edges will be deleted. This deletion will not be flagged as a data loss (no bit 25 flag will be set). Correspondingly, if the first edge to arrive is a trailing edge, it will not be sent and no data loss flag will be set. Also, if a leading edges is stored awaiting a trailing edge that does not arrive before the event trailer, the leading edge will be lost and no data deleted flag will be set in the event trailer.

The above referenced thresholds for deletion will be in effect at all times. These thresholds are programmable via JTAG? In addition, a non-pair mode will be implemented where AMT data is not pair associated but output as it arrives. In this case all AMT data will be sent unmodified except for the overflow prevention based on the two thresholds just described.

To convert the two words of ID=0011 (the first with a T=1 leading edge and the second with T=0 trailing edge) into a single word of ID=0100, the leading edge must be stored awaiting the arrival of the trailing edge. Some special cases deserve attention:

1. When there are 2 leading edges in sequence
2. When a trailing edge is first seen within the match window of the AMT
3. Where a leading edge has been received but no trailing edge falls within the match window

The special case of two leading edges in sequence is thought to come from the narrow pulses that confuse the AMT-3 pair matching circuits. For the purposes of CSM-4 "pseudo pair" mode this case can be handled by simply ignoring the first leading edge.

The data representing leading edges are stored and a flag set to indicate that the edge is present. If a second leading edge arrives without an intervening trailing edge, the second leading edge simply overwrites the first. This is the result desired since the first leading edge is thought to be due to a narrow pulse whose trailing edge is lost.

A trailing edge arriving first implies that its leading edge was outside the match window and thus lost to digitization. Since the match window is designed to cover the full drift time expected for real hits from the detector, this trailing edge has no meaning for the current trigger and can be discarded. The "pseudo pair" mode logic of the CSM-4 will reset the leading edge flags for all channels when a TDC header (ID=1010) is seen. A trailing edge seen on a given channel before any leading edge from that channel is received and flagged will be discarded.

A stored leading edge for which no trailing edge is seen before a TDC trailer (ID=1100) is seen, will also be discarded. This happens automatically in that the leading edge would be processed at the arrival of its corresponding trailing edge. Since all flags representing stored leading edges are cleared at the arrival of a TDC header no use of the leftover leading edge will be made.

All word IDs will be passed without modification if the buffer space is available for the data type according to the thresholds set. Headers and trailers will be stored (pass into the buffer) if any buffer space is available. All word types will be stored (passed into the buffer) if the buffer word count is below its programmed discard threshold.

Pair mode as implemented in the CSM-4 should mimic that coded into the AMT.

The AMT-3 provides 3 bits of width resolution, this same programming should be incorporated into the "Pseudo Pair" mode of the CSM-4. The 3 bits of width resolution determine which 8 bits of width data (calculated as 17 bits of trailing edge time minus leading edge time) are to be loaded into the output. The default precision (0) sends the lower 8 bits of the width (7-0) to the output. A width precision of 7 sends bits 14-7 of the width calculation to the output.

To provide diagnostics on the CSM-4 preparation of "pseudo pair" mode data, two debug parameter fields of the CSM-4 are defined. One single bit (debug) selects a mode where the CSM-4 sends data for diagnostic checks of the "pseudo pair" mode itself. In this mode, the leading edge data is passed unchanged along with a modified form of pair data. The pair data in this case will include the calculated width but with the trailing edge time in place of the leading edge time as in normal pair mode. With this data, software can calculate the width for comparison to that provided by the CSM since the leading edge time has been sent along with modified pair word that contains the trailing edge time.

Another debug option is provided where edges are sent rather than calculated pseudo pairs for events (or hits) satisfying a prescale count. The prescale is selected with 2 bits in the CSM-4 status register (ps). The scaling will be 816 (ps=0), 4016 (ps=1), 20016 (ps=2), and 1000 16(ps=3).

The two diagnostic modes are not simultaneously useful. Prescale can be used with pair mode or non-pair mode. However, when use with non-pair mode all events are sent as edges so the prescaled event selection will not be unique in any way. Diagnostic "pseudo pair" mode where leading edges are sent and the pair word has trailing edge times should only be used with pair mode.

In summary, selection between all edges (pair mode off) and pair mode (pair mode on) is controlled by one bit of the CSM-4 JTAG register. If operating in pair mode, a diagnostic mode (established by one bit in the JTAG setup) provides for leading edges to be sent followed by a modified pair mode output (width and trailing time). A 2-bit JTAG register field controls a prescale fraction of the EVID range for which event data is sent as edges rather than in pair mode. If the JTAG bit for pair mode selection is off, this prescale has no effect since all events will be sent as edges. Two additional JTAG register fields of 4-bits define the low and high thresholds for deletion of AMT error words and AMT data words. These 4 bit thresholds are prepended to a zero bit to match the buffer depth of 32. Hence a threshold programmed to 1100 (12) is interpreted as 11000 (24) when applied to the 32 words of the input FIFO.

Implementation details

The sequence of steps in non-pair mode are:

- Upon receipt of an AMT-3 TDC event header

  If the buffer has any free location, pass the header to the output stream and reset the data deleted flags.
- Upon receipt of a leading edge

1. If the buffer word count is below high threshold, pass the leading edge to the output stream.
2. If the buffer word count is above the high threshold, discard the data and set high threshold data deleted flag.

- Upon receipt of a trailing edge
  1. If the buffer word count is below the low threshold, pass the trailing edge to the output stream.
  2. If the buffer count is above low threshold, discard the word and set the low threshold data deleted flag.
- Upon receipt of AMT-3 TDC trailer

  Pass the AMT trailer and the state of the high and low data deleted flags.

The sequence of steps in pair mode for non-debug operation are:

- Upon receipt of an AMT-3 event header,
  1. Reset the leading edge found flags (24).
  2. Reset the word count to 1 for this AMT.
  3. Pass the TDC header and reset the data deleted flags.
- Upon receipt of a leading edge,
  1. Store the leading edge in RAM indexed by10-bits (AMT+channel).
  2. Set leading edge found flag (1-bit) for the particular10-bit (AMT+channel).
- Upon receipt of a trailing edge,
  1. If no leading edge is stored, discard the trailing edge.
  2. If a leading edge is stored and the buffer word count is above high threshold, set the high threshold data deleted flag, discard the trailing edge, andreset the leading edge stored flag.
  3. If a leading edge is stored and the buffer word count is below the high threshold, calculate the pair mode data,increment the word count for this TDC-channel, reset the leading edge stored flag, and pass the pair data to the output.
- Upon receipt of AMT-3 event trailer
  1. Clear leading edge flag
  2. Count event trailer for this AMT
  3. Forward event trailer to RAM with stored count
- Upon receipt of other words,
  1. If the buffer word count for this word type is above threshold, discard the word.
  2. If the buffer word count for this word type is below threshold, pass the word to the output, and increment the word count for this TDC-channel.

The sequence of steps in pair mode with prescale set

- If event number masked with modulo prescale = 0
  1. Run as non-pair mode above

Run as pair mode above

The sequence of steps in pair mode with debug bit set

Upon receipt of an AMT-3 event header

Reset the leading edge found flags (24)

2. Reset the word count to 1 for this AMT
3. Pass the event header, data deleted, and error flags to RAM for polling multiplexer, reset the error and data deleted flag, and count the word

- Upon receipt of a leading edge
  1. Store in RAM indexed (10-bits) by AMT-channel
  2. Set leading edge flag (1-bit) for the 10-bit AMT-channel
  3. If the buffer word count is below high threshold, pass the leading edge, data, and error deleted flags to RAM for polling multiplexer, reset the data and error deleted flags, and increment the count of word sent
  4. If the buffer word count is above high threshold, discard the data and set data deleted flag
- Upon receipt of a trailing edge

If no leading edge is stored

"Discard trailing edge (i.e. do not forward)

If a leading edge is stored

If buffer word count is above high threshold

1. set data deleted flag

- If buffer word count is below high threshold
  2. Calculate the pair mode data using trailing edge time
  3. Count word forwarded for this AMT
  4. Clear leading edge flag
  5. Forward data and delete flags to RAM for polling multiplexer and reset delete flags
- Upon receipt of AMT-3 event trailer
  1. Clear leading edge flags
  2. Count event trailer for this AMT
  3. Forward event trailer , data deleted, and error flags to RAM with prepared word count

THE CSM-4 PROTOTYPE DEVELOPMENT

Design Elements

The CSM-4 has as it goal the rapid design of a module more closely aligned with the final CSM than is the CSM-0. It presumes an early version of the MROD and the use of fiber connections to the trigger, timing, and control and to the data acquisition flow. The fiber interconnect more realistically represents the clock noise, data noise, and grounding environment of the final configuration. The only justification for the intermediate design of a second prototype is expediency. The goal is to have a fiber connected design that can reside on chamber using the same interconnect motherboard, TTC system, and the opto-isolated JTAG connection anticipated in the final CSM. The items to be included in the CSM but not present in the CSM-4, are the analog multiplexer for voltage and temperature sensing, and the final TTC system with calibration programming. The connections to do calibration will be in place in the CSM resident FPGA, but perhaps not from the TTCvi programming. The TTC system is described on the CERN web pages at CERN[11] where the TTCvi Mark I is described. The specifics of the CSM-4 are:

- The main multiplexing task of the CSM-4 has been compressed from 4 FPGAs into one using a scheme of clock phase sampling to remove the need for many independent clock networks, using a large fine pitch ball grid array chip, and using a LVDS compatible FPGA from Xilinx, the XC2V1000FPBG456. Prototype testing of the optical fiber output to the MROD will be done using the CERN GOL chip and the Infineon V23818-K305-L57. The final design will likely use a simple laser diode in place of the transceiver since the input channel is unused in the CSM to MROD link.
- The CSM-4 requires clocking and event triggering. For the CSM-4 design the Trigger, Timing, and Control will be based on the CERN developed TTC system. Our transition from the internal simulation of the trigger and timing to the externally generated functions implies and integration of the CERN chip into the module and the software integration of the TTCvi module into our environment. We plan to use the Mark I version of the TTCvi initially and switch to the Mark II version in 2003.
- The initialization of the ASD/TDC mezzanine cards is done via JTAG protocol which in the case of the CSM-0 is built into the VME functions of the CSM-0 module. In the CSM-4 no VME connections is available. The CSM-0 will use an opto-isolated JTAG function as will the final CSM. However, the final CSM will have a DCS connection and a CAN bus interface to provide the programming for the JTAG. To make progress toward this final goal, the opto-isolated JTAG will be driven from a commercial module.
- The CSM will interconnect to the ASD/TDC modules via shielded ribbon cables that leave the Faraday cages and converge at the spacer plate of the MDT. At this location they will attach to a passive interconnect on which the active CSM will reside. To make use of the current CSM-0 with the new interconnect board, a MiniAdapter board has been constructed with the same circuit design as the adapter currently in use with the CSM-0, but designed to attach to the passive interconnect. Following use with the CSM-0, a simple replacement of this new adapter with the CSM-4 will convert a chamber from CSM-0 readout to the MROD readout via the CSM-4.

11. TTC system web pages, http://ttc.web.cern.ch/TTC/intro.html

- The CSM-4 will not contain the analog multiplexer nor will it interact with the DCS system initially.
- The CSM-4 will not contain any Single Bit Upset detection or correction code. Since this code is firmware, it is anticipated that work on this code will follow the certification of the design in the first half of 2003.

JTAG PROGRAMMING

CSM-4 JTAG

The CSM-4 has a JTAG string which is a composite of several bit strings for the TTCrx register initial values, the CSM module RW parameters, the AMT RO parity error flags, the TTC RO status, and the CSM module RO status. These strings are defined in the CSM VerilogHDL code and can be modified rather easily. The current sizes of the JTAG elements are represented in Table 6 on page 20 along with the overall order of these strings in the JTAG sequence.

TABLE 6. JTAG String Lengths & Position

String Name	# bits	Bit posn
TTCrx_init_len	80	278
CSM_parm_len	72	206
TTC_readback_len	160	46
AMT_parity_err_len	18	28
CSM_status_len	28	0

The entire JTAG string can be read or written. Individual sections can also be read and written. The subsections that can be separately accessed are defined in Table 7 on page 20. The individual subsections are accessed with different values of the 6-bit instruction register. In this table the designation RW implies the register is loaded with the outgoing string and the RO designation implies that the register is read back but that the outgoing JTAG string is ignored. Of course, for the read only bits in the full register, the outgoing JTAG string is always ignored.

TABLE 7. CSM JTAG Instructions

Register Subsection	Length	Read-Write	Instruction
FULL JTAG String	358	RW	000011
FULL JTAG String	358	RO	110001
TTC Readback	160	RO	110010
AMT Parity Errors	18	RO	110011
CSM Status Flags	28	RO	110100
AMT Phase Sampling Errors	18	RO	110101

TABLE 7. CSM JTAG Instructions

Register Subsection	Length	Read-Write	Instruction
All Configuration Bits	152	RO	110110
All Configuration Bits	152	RW	110111
CSM Parameters	72	RO	111000
CSM Parameters	72	RW	111001
CSM Version Date	32	RO	111010
Read only Bits	206	RO	111011

The subsections of the JTAG string are shown in Figure 8 on page 21.

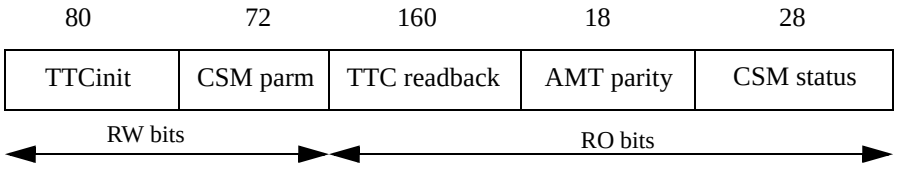


FIGURE 8. Position of Control and Status Strings in JTAG

If the full JTAG string is sent, the order must be obeyed with the CSM status bits exiting the CSM first and new values sent low order bit first. The individual bit positions for the subsections are shown in Table 6 on page 20 where the length of the read-write section is the sum of the first two, 152, and the length of the read-only section is the sum of the last three, 206.

The TTCrx string is defined in the TTCrx manual[12]. In the CSM, this string is loaded via JTAG and presented to the TTCrx chip following a reset signal. This reset initiates the timing sequence for loading the TTCrx from PROM with the FPGA taking the role of the PROM. The CSM parameter string of 72 bits provides RW control for the CSM, the GOL, and TTCrx as shown in Table 8 on page 21. The CSM status bits are RO and represent the version number of the CSM code, the state of various DLL lock lines, and a few error flags.

TABLE 8. CSM JTAG Control Bit Definitions

Field	Bit posn	Length
TDC enable low bit	0	18
Include mezzanine cards in JTAG flags low	18	1
CSM enable trigger bit	19	1
Mezzanine command delay pipe length low	20	7
80mhz operation bit	27	1
Pair width resolution low	28	3

12. Timing receiver ASIC (TTCrx) Reference Manual, http://ttc.web.cern.ch/TTC/intro.html

TABLE 8. CSM JTAG Control Bit Definitions

Field	Bit posn	Length
CSM make pairs bit	31	1
Pair debug bit	32	1
Spare bit 0	33	1
Suppress idle cycle bit (TDM only)	34	1
Include sync status bit (TDM only)	35	1
GOLdiff bit	36	1
GOL ld0 bit	37	1
GOL ld1 bit	38	1
GOL pll bit	39	1
GOL laser bit	40	1
GOL negative edge selection bit	41	1
GOL mode selection bit	42	1
Enable GOL tdi bit	43	1
MaxAMTconnect low	44	5
Spare bit 1	49	1
Enable TTC tdi bit	50	1
TTC use prom bit	51	1
CSM next state low	52	4
CSM command bit	56	1
CSM BCID no match bit (event builder only)	57	1
CSM EVID no match bit (event builder only)	58	1
CSM send all AMT types bit (event builder only)	59	1
CSM no header or trailers bit (event builder only)	60	1
Pair prescale mode low	61	3
Ram trailing edge threshold low	64	4
Ram leading edge threshold low	68	4

The TTCrx readback bits hold the contents of the 20 I^2C addressed 8-bit registers of the TTCrx. Two fpga build versions are possible. In the default version, one I^2C register is read every 400ms, covering all 20 registers. In the second version, only the first ten reg-

TABLE 9. TTCrx Readback Register

Field	bit posn
TTCrx registers 9 to 0	0
TTCrx registers 19 to 10 (I^2C access only)	80

isters are available. These 10 registers are accessed passively via the ERDump and CRDump commands of the TTCrx. (See Table 9 on page 22) The CSM status register

bits reflect this difference, with the first column describing the ERDump/CRDump situation, and the second describing the I^2C situation. (See Table 10 on page 17) The ERDump/CRDump version will eventually be phased out.

The AMT parity error bits are cleared when data acquisition is enabled and accumulated from the parity error calculation for each data word separately for each of the AMT chips (each mezzanine card). A stop and restart of the data acquisition begins another set of 18 accumulated OR bits.

TABLE 10. AMT Parity Error Flags

Field	bit posn
TDC 0 Flag	0
TDC 1 Flag	1
TDC 2 Flag	2
TDC 3 Flag	3
TDC 4 Flag	4
TDC 5 Flag	5
TDC 6 Flag	6
TDC 7 Flag	7
TDC 8 Flag	8
TDC 9 Flag	9
TDC 10 Flag	10
TDC 11 Flag	11
TDC 12 Flag	12
TDC 13 Flag	13
TDC 14 Flag	14
TDC 15 Flag	15
TDC 16 Flag	16
TDC 17 Flag	17

The CSM status register bit definitions are indicated in Table 11 on page 23 using the same convention as provided in the parameters file. In this case the bits are RO with the data sent via the JTAG output stream being ignored.

TABLE 11. CSM Status Register Bit Definitions

Field	Position	Length
CSM version number low	0	12
GOL ready bit	12	1
TTC ready bit	13	1
LHC clock locked bit	14	1
XMT internal clock lock bit (FPGA)	15	1
XMT external clock lock bit (GOL)	16	1

TABLE 11. CSM Status Register Bit Definitions

Field	Position	Length
Unused OR (for fooling synthesizer)	17	1
TTC prom load error flag	18	1
CSM state low	19	4
Sample phase error bit	23	1
I^2C Operation Failure	24	1
TTC I^2C compare error	25	1
TTC dump compare error bit	26	1
CSM error bit	27	1

If the Suppress Idle Cycle bit is turned on in the CSM JTAG Control Bit sequence, then any 21 word GOL transmission cycle which contains only TDC empty words (Table 2 on page 6) will be suppressed in favor of optical idle transmissions for the duration of the cycle. If this bit is not set, then all cycles will be transmitted over the fiber once acquisition is enabled and the data from the first trigger is sent. This bit can be changed at any time and will take effect at the start of the next transmission cycle.

If the Include Sync Status bit is turned on in the CSM JTAG Control Bit sequence, then 26 bits of additional information will be output in each transmitted TDC Spacer Word. The nominal value of this word as shown in Table 2 on page 6 is 0xdnnnnnnn. When the control bit is turned on the content of this word is modified from 0xd0000000 to that shown in Table 11 on page 18. With the bit set, when a trigger is received by the CSM-4 the number of clock tics (32 bits) since the previous trigger is latched. This value is transmitted in the next two Spacer Words as shown in the table. The spacer word then reverts to transmitting a fill content type zero word until the next trigger arrives.

TABLE 12. Modified TDC Spacer Word content

Bit Range	Value	Meaning
31-28	0xd	ID Code (fixed)
27	0x0	None (fixed)
26	0,1	Fiber transmission parity (odd)
25	Status bit 7	Always zero
24	Status bit 6	LHC clock locked
23	Status bit 5	XMT internal clock lock
22	Status bit 4	XMT external clock lock
21	Status bit 3	Sample phase error
20	Status bit 2	I^2C Operation Failure
19	Status bit 1	TTC I^2C compare error
18	Status bit 0	CSM error bit
17-16	0x0,1,2	Fill content type
15-0	Fill content	Type definitions, see next

Care should be taken in setting this bit, as it is likely that the MROD does not understand any value for the Spacer Word other than the default, 0xd0000000, and will not work if that value is not transmitted. A similar caution exists for older versions (such as that used at H8) for the Michigan CSMtest code. Fill word content definitions appear in Table 13 on page 25.

TABLE 13. Fill content Type Definitions

Type	Meaning
00	Zero
01	Low 16 bit count of clk25 since last trigger (32 bit value)
10	High 16 bit count of clk25 since last trigger (32 bit value)

CSM-4 States

The CSM-4 operates in states defined currently according to Table 14 on page 25. Most of the states have to do with initialization. Once running the CSM-4 requires no intervention as long as synchronization is maintained and errors are rare. Since the CSM-4 continues to be under development, one should expect the number of states, parameters, and status bits to be fluid. Check regularly for updates of this manual by examining the Docushare pages for new versions.

TABLE 14. CSM-4 States

State	Code
IDLE_STATE	0
FPGA_RESET_STATE	1
RESET_TTC	2
RESET_GOL	3
WAIT_LOCK	4
DCM_RESET_CLK25	5
SAMPLE_AMT_PHASE	6
JTAG_RESET	7
TTC_LOAD	8
WAIT_PROM	9
AMT_RESET	10
TRY_RESET_ERROR	11
CHECK_AMT_PHASE	12
TOGGLE_GOL_CLOCK	13

The CSM-4 Operational State Machine

The states detailed in Table 14 on page 25 can be individually entered, but a few are really only useful when automatically entered as a result of selecting some other operation.

This section documents the actions taken as a result of selecting the various states. Following each state name is the decimal value of the enumerated type to which it corresponds, a'la Table 14 on page 25.

IDLE_STATE (0): This is the normal state in which the FPGA operates. All other states eventually flow back to this one following the completion of any actions taken in those other states. Issued JTAG Operational State changes will only be made if this is the current state when the JTAG command is received.

FPGA_RESET_STATE (1): Entry to this state re-initializes the CSM-4 FPGA to its power up state. Exit from this state is through the RESET_TTC and RESET_GOL states as detailed below for the Power-Up Sequence of events.

RESET_TTC (2): Entry to this state toggles the Reset_b pin of the TTCrx chip for approximately 400ns. Exit from this state at the end of the reset period depends upon the setting TTC_use_prom_bit of the CSM parameters JTAG register. If the TTC should use the FPGA as its load prom, then that is the next action taken (state WAIT_PROM). Otherwise, reset of the DCM core controlling the re-generation of the 25ns LHC clock within the FPGA is undertaken (state DCM_RESET_CLK25).

RESET_GOL (3): Entry to this state toggles the reset_b pin of the GOL chip for approximately 400ns. Exit from this state is to the WAIT_LOCK state.

WAIT_LOCK (4): Wait while the GOL chip re-synchronizes and re-locks itself. This wait is approximately 800ms long. Exit from this state is to the IDLE_STATE.

DCM_RESET_CLK25 (5): If the TTCrx is reset, then the DCM core within the CSM-4 FPGA must be reset to restart the local clocks. Exit from this state is normally to the IDLE_STATE (see the Power Up Sequence detail below).

SAMPLE_AMT_PHASE (6): Entry to this state initiates a sampling of the phase of the data and strobe signals returning from each mezzanine board. At the end of the sample period, the CSM-4 clock phase most appropriate for acquiring the serial bit stream from each active mezzanine board will be known and selected for use. Exit from this state is to the IDLE_STATE.

--> IMPORTANT NOTE: The FPGA “assumes” the serial clock is already JTAG enabled from each active mezzanine board. If it is not, the CSM error bit of Table Table 11 on page 23 will be set due to the failed phase sampling.

JTAG_RESET (7): Toggle the JTAGTRST_b signal line to the TTCrx and GOL chips for approximately 350ns. Exit from this state is to the IDLE_STATE. NOTE: The JTAG instruction register of both the GOL and the TTCrx is loaded with the IDCODE instruction as a side-effect of this operation.

TTC_LOAD (8): Force a TTC PROM load from the FPGA independent of the setting of the “TTC use prom flag” JTAG bit. Other operations are identical to those of the RESET_TTC state operating in a non-power-up sequence.

WAIT_PROM (9): Wait while the TTCrx chip uses the CSM-4 FPGA as its load prom. Exit from this state is to the DCM_RESET_CLK25 state.

AMT_RESET (10): Toggle the mezzanine board AMT reset line for approximately 800ns. Exit from this state is to the IDLE_STATE.

TRY_RESET_ERROR (11): During the course of operations within the CSM-4 state machine, an error could occur. This results in setting the “CSM-4 Error” bit. Entry to the TRY_RESET_ERROR state results in an attempt to determine and correct the cause of the error. If the attempt succeeds the bit will be cleared. Exit from this state is to the state appropriate to correcting the error. If more than one error exists, it could take two or three entries to this state before they are all handled.

CHECK_AMT_PHASE (12): Examine the phase sampling of the mezzanine card clocks to insure that all have selected valid phases.

TOGGLE_GOL_CLOCK (13): Switch between 25MHz GOL clock and 50MHz GOL clock. This state must be followed by a RESET_GOL command state.

All other values for the CSM-4 State are ignored, and treated as if they were the IDLE_STATE.

Note that a JTAG request to enter a state will be ignored if the state machine is not in an IDLE_STATE when the JTAG register is updated. No error will be reported in this situation.

Power Up Sequence

Following a board power up, we recommend the following sequence of states and operations before the FPGA is used for data acquisition. The first two operations are automatically performed as a result of the FPGA initialization sequence.

1. RESET_TTC. Note that all TTCrx initialized during power up will have the same address, which is hard-coded in the CSM-4 initial programming strings. If individual TTCrx addresses are desirable, then the correct addresses should be set in the JTAG strings of each CSM-4, in conjunction with a RESET_TTC command.

2. RESET_GOL

3. Enable the connected set of mezzanine boards, and enable the CSM-4 to JTAG program them. The IDLE_STATE should be selected while doing this, or it can be done at the same time as the RESET_GOL state is selected.

4. JTAG program the mezzanine boards, selecting the IDLE_STATE in the process. A continuous return clock should be selected.

5. SAMPLE_AMT_PHASE

6. Disable the mezzanine boards AMT clock return to the CSM-4 (IDLE_STATE).

7. Disable mezzanine board JTAG operations, and enable CSM-4 acquire data JTAG bit (IDLE_STATE).

CSM JTAG Signals

A short definition is provide for each of the bits or bit groups in the JTAG sequence. Since the number of bits is large, only a brief definition is provided. Elaboration of these bit definitions can be provided by the authors. The power up default value is given after the name. This is not the running value, however.

TDC enable low [0] - The 0 channel flag to enable data from the first TDC. This bit is followed by 17 other enable bits for the 18 mezzanine boards permitted.

Include mezzanine cards in JTAG flags low [0] - This single bit places the mezzanine cards in the JTAG chain

CSM enable trigger bit [0] - A single trigger enable bit. This instructs the CSM to accept

Mezzanine command delay pipe length low [0] - The 7 bit number that specifies how many 40MHz clock ticks are to be passed before a trigger is sent to the mezzanine cards.

80mhz operation bit [0] - Set the serial clock inside the CSM to expect data at 80MHz. This includs enabling 80MHz phase sampling. The AMT must also be programmed to send data at 80MHz.

Pair width resolution low - [0] Set the resolution of pair mode time digitizations. See the table in the pair mode section of this manual.

CSM make pairs bit - [0] Enable the CSM to compress leading and trailing edges into pairs.

Pair debug bit - [0] This enables a debug mode of the CSM pair mode.

Spare bit 0 [0] - Unused

Suppress idle cycle bit (TDM only) [0] - Empty 21 word data cycles output from the CSM are replaced with optical link idles which provide synchronization but do not appear in the data stream at the receiving end.

Include sync status bit (TDM only) [0] -

GOLdiff bit [1] - Set the GOL to differential input (for CSM-1=1) (for CSM-2/4 = 0)

GOL ld0 bit [1] - Sets the Laser driver current

GOL ld1 bit [0] - Sets the Laser driver current

GOL pll bit [0] - Sets the charge pump current when the configuration regiser is zero.

GOL laser bit [1] - Sets Laser mode when 1 (CSM-2/4) or differential when 0 (CSM-1)

GOL mode selection bit [0] - Set Gigabit Ethernet mode when 0.

Enable GOL tdi bit [1] - Place the GOL in the JTAG chain

MaxAMTconnect low [00000] - Maximum number of TDCs connected to this CSM

Spare bit 1 [0] - Unused

Enable TTC tdi bit [1] - Place the TTC in the JTAG chain

TTC use prom bit [1] - Instruct the TTC to load from PROM

CSM next state low [0000] - Lowest bit of the to be requested new state for the CSM

CSM command bit [0] - Execute the request for transition to a new CSM state.

CSM BCID no match bit (event builder only [0] - Do not require a match to the BCID. This is a common option that avoids the need to synchronize the offsets mezzanine to mezzanine.

CSM EVID no match bit (event builder only) [0] - Do not require a match to the EVID between the trigger and the data from the AMT. This is a diagnostic mode.

CSM send all AMT types bit (event builder only) [0] - Send all ID from the AMT even if they are not defined for the AMT. This is a diagnostic option.

CSM no header or trailers bit (event builder only) [0] - Do not output the headers or trailers. The wire encoding defines the wires from which the data originates.

Pair prescale mode low [000] - Prescale mode control. See the section on pair mode implementation

Ram trailing edge threshold low{1000] - Buffer control delection of trailing edges and mask words begins at twice this number of words in the buffer.

Ram leading edge threshold low [1100] - Buffer control delete leading edges and error words threshold. Since there are 32 buffer slots, this number is multiplied by 2 so the default 12 is actually 24, making the deletion of leading edges start when there are 24 words in the 32 word buffer

DIGITAL I/O LINES TO/FROM ELMB

The JTAG and Output Digital I/O lines

The four JTAG lines TCLK, TMS, TDI, and TDO are provided by the ELMB through the JTAG connector as shown in Figure 9 on page 30. This figure also show the 4 Digital I/O lines that provide for control of the FPGA reprogram and reset. In addition the selection of HW_TDO selects a JTAG composed of the PROM and FPGA alone. In this configuration the PROM and FPGA can be initialized when no programming or faulty programming exists in the FPGA. The selection of SW_TDO establishes the full operational mode of the CSM including the TTCrx, GOL, CSM, and Mezzanine cards.

function	pin	pin	function	comment
GND	**20**	**19**	**GND**	
GND	**18**	**17**	Dig I/O 4 (PA7)	*Reprogram_FPGA**
GND	**16**	**15**	Dig I/O 3 (PA6)	*Reset_FPGA*
+3.3V	**14**	**13**	Dig I/O 2 (PA5)	*Sel_SW_TDO**
+3.3V	**12**	**11**	Dig I/O 1 (PA4)	*Sel_HW_TDO**
+3.3V	**10**	**9**	TDI (PA3, in)	JTAG interface
+3.3V	**8**	**7**	TMS (PA2, out)	JTAG interface
GND	**6**	**5**	TCK (PA1, out)	JTAG interface
GND	**4**	**3**	TDO (PA0, out)	JTAG interface
GND	**2**	**1**	**GND**	

FIGURE 9. Layout of the *JTAG* connector pins: 8 general-purpose digital in and outputs. In brackets the ELMB microcontroller pin name is shown,in italics theCSM's name for the signal function.

The Input Digital I/O

There are three Digital I/O lines read by the ELMB that form an encloded CSM status and 5 that provide for access to the 64 channel multiplexer on the CSM. In the table the three status lines are marked not-connected but the table will be reloaded with the definitions in place. The lines that control the 64 channel multiplexer are labeled Aux I/O.

The signals connected to the 64 channels of the multiplexer are shown in . Calibration of the multiplexer is provided by channel 15 which is tied to an precision 2.5 volt reference. All channels are scaled by the value needed to set channel 15 at precisely 2.5 volts. A second copy of the reference is connected to channel 11 as a means to verify the accuracy of the calibration. The channels connected to voltages greater than 4 volts are scaled with precision resistors to insure that they fall below the reference. There are two

such voltages, the incoming Vcc and the +5 volts associated TTCrx optical receiver and the -5 volt negative rail to the ADC.

function	pin	pin	function	comment
GND	**20**	**19**	**GND**	
GND	**18**	**17**	Dig I/O 7 (PF4)	*Status2*
GND	**16**	**15**	Dig I/O 6 (PF3)	*Status1*
+3.3V	**14**	**13**	Dig I/O 5 (PF2)	*Status0*
+3.3V	**12**	**11**	MUX (PE7, out)	for ADC
+3.3V	**10**	**9**	CS (PC3, out)	for ADC
+3.3V	**8**	**7**	SDO (PE6, in)	for ADC
GND	**6**	**5**	SDI (PE5, out)	for ADC
GND	**4**	**3**	SCLK (PE4, out)	for ADC
GND	**2**	**1**	**GND**	

FIGURE 10. Layout of the *CSM-ADC* connector pins: SPI serial interface (SCLK,SDI and SDO) with Chip-Select (CS) and ADC-multiplexer latch signal (MUX) go to the ADC on the CSM (which has a copy of ELMB on-board ADC circuitry). In addition there are 3 general-purpose Digital I/Os. In addition there are 3 general-purpose Digital I/Os. In brackets the ELMB/microcontroller pin name is shown, in italics the CSM's name for the signal function.

ADC ch	Source	ADC ch	Source	ADC ch	Source	ADC ch	Source
0	Mezz 16 Temp	16	Mezz 6 Temp	32	Mezz 10 Temp	48	Mezz 0 Temp
1	Mezz 16 Analog	17	Mezz 6 Analog	33	Mezz 10 Analog	49	Mezz 0 Analog
2	Mezz 16 Digital	18	Mezz 6 Digital	34	Mezz 10 Digital	50	Mezz 0 Digital
3	CSM 2.5V	19	CSM 3.3V	35	CSM 3.3V_B	51	CSM V_{CC}
4	Mezz 15 Temp	20	Mezz 5 Temp	36	Mezz 12 Temp	52	Mezz 2 Temp
5	Mezz 15 Analog	21	Mezz 5 Analog	37	Mezz 12 Analog	53	Mezz 2 Analog
6	Mezz 15 Digital	22	Mezz 5 Digital	38	Mezz 12 Digital	54	Mezz 2 Digital
7	CSM 1.5V	23	Mezz 7 Temp	39	Mezz 11 Temp	55	Mezz 1 Temp
8	Mezz 17 Temp	24	Mezz 8 Temp	40	Mezz 14 Temp	56	Mezz 4 Temp
9	Mezz 17 Analog	25	Mezz 8 Analog	41	Mezz 14 Analog	57	Mezz 4 Analog
10	Mezz 17 Digital	26	Mezz 8 Digital	42	Mezz 14 Digital	58	Mezz 4 Digital
11	CSM 2.5V Ref	27	Mezz 7 Analog	43	Mezz 11 Analog	59	Mezz 1 Analog
12	Half CSM +5V_{CC}	28	Mezz 9 Temp	44	Mezz 13 Temp	60	Mezz 3 Temp
13	CSM Temp	29	Mezz 9 Analog	45	Mezz 13 Analog	61	Mezz 3 Analog
14	Half CSM -5V_{EE}	30	Mezz 9 Digital	46	Mezz 13 Digital	62	Mezz 3 Digital
15	CSM 2.5V Ref	31	Mezz 7 Digital	47	Mezz 11 Digital	63	Mezz 1 Digital

FIGURE 11. Mapping of CSM FE-electronics voltages/temperatures to CSM-ADC channels.