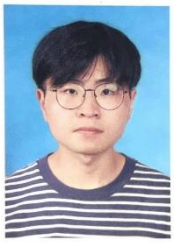

Weihua Xiao

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Email: 019370910014@sjtu.edu.cn
Location: Shanghai, China
Research interests: Logic synthesis, approximate computing, standard cell synthesis, Ising model

Education

PhD, University of Michigan–Shanghai Jiao Tong University Joint Institute, CN Sep. 2019 – Present

Major: electronic science and technology, **Advisor**: Weikang Qian (Associate Professor)

Visiting PhD Student, University of Alberta, CA Jan. 2023 – Jan. 2024

Advisor: Jie Han (Professor)

Bachelor, Xidian University, CN Oct. 2015 - June 2019

Major: communication engineering, **Overall GPA**: 3.71/4.0

Publications

During my PhD study, I published **five** papers in **Top Conferences** as the **first author or co-first author**:

1. **Weihua Xiao***, Tingting Zhang*, Xingyue Qian, Jie Han and Weikang Qian, "Efficient Approximate Decomposition Solver using Ising Model," in Proceedings of the 2024 ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, USA. **Acceptance Rate: 23%**. (*These authors **contributed equally**.)
2. **Weihua Xiao**, Shanshan Han, Yue Yang, Shaoze Yang, Cheng Zheng, Jingsong Chen, Tingyuan Liang, Lei Li, and Weikang Qian, "MiniTNtk: An Exact Synthesis-based Method for Minimizing Transistor Network," in Proceedings of the 2023 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, USA. **Acceptance rate: 23%**.
3. **Weihua Xiao**, and Weikang Qian, "ASPPLN: Accelerated Symbolic Probability Propagation in Logic Network," in Proceedings of the 2022 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Francisco, CA, USA. **Acceptance rate: 22.5%**.
4. **Weihua Xiao**, Cheng Zhuo, and Weikang Qian, "OPACT: Optimization of Approximate Compressor Tree for Approximate Multiplier, " in Proceedings of the 2022 Design, Automation & Test in Europe Conference & Exhibition (DATE), virtual event. **Acceptance rate: 25%**.
5. **Weihua Xiao**, Weikang Qian, and Weiqiang Liu, "GOMIL: Global Optimization of Multiplier by Integer Linear Programming, " in Proceedings of the 2021 Design, Automation, and Test in Europe Conference & Exhibition (DATE), virtual event. **Acceptance rate: 23.9%**.

I also published three other papers:

1. Yi Wu, Chuangtao Chen, **Weihua Xiao**, Xuan Wang, Chenyi Wen, Jie Han, Xunzhao Yin, Weikang Qian, and Chuo Zhuo, "A Survey on Approximate Multiplier Designs for Energy Efficiency: From Algorithms to Circuits," in ACM Transactions on Design Automation of Electronic Systems (TODAES), 2023.
2. Chenfei Lou, **Weihua Xiao**, and Weikang Qian, "Quantified Satisfiability-based Simultaneous Selection of Multiple Local Approximate Changes under Maximum Error Bound," in Proceedings of the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, Texas, USA.
3. Chen Wang, **Weihua Xiao**, John P. Hayes, and Weikang Qian, "Exploring Target Function Approximation for Stochastic Circuit Minimization," in Proceedings of the 2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), virtual event. **Acceptance rate: 27.0%**.

Summary of Research

1. **Transistor-level Logic Synthesis**
   - **Definition**: generate a transistor network with the minimized hardware cost for implementing the desired Boolean function;
   - **Application**: an essential step of advanced standard cell design techniques;
   - **Proposed Work**:
     - **For the first time** models the synthesis of the transistor network for a Boolean function as a **Boolean satisfiability** (SAT) problem and can return a transistor network with the fewest transistors;
     - Reduces #transistors by up to **9.39%** over all 4-input P-class representative Boolean functions compared to state-of-the-art related works;
     - Publishes at the **top conference ICCAD23** (Github link: https://github.com/FCHXWH/MiniTNtk-An-Exact-Synthesis-based-Method-for-Minimizing-Transistor-Network).

2. **Gate-level Logic Synthesis:**
   - **Definition**: generate a logic network with the minimized hardware cost for implementing the desired Boolean function;
   - **Application**: gate-level logic synthesis, including exact case and approximate case, is significant to some emerging applications, such as machine learning, image processing;
   - **Proposed Work**:
     - For the exact gate-level synthesis of digital multipliers, proposes an advanced synthesis method for multipliers, **a global optimization** method for multiplier by integer linear programming (ILP); Reduces the **power-delay product (PDP) by up to 71%**, compared to the multipliers developed in industry; Publishes at the **top conference DATE21** (Github link: https://github.com/SJTU-ECTL/GOMIL);
     - For the approximate gate-level synthesis of multipliers, proposes an advanced synthesis method for approximate multipliers based on ILP, targeting at co-optimizing the introduced error and area; Achieves an average reduction of **24.4%** and **8.4%** in **PDP** and **mean error distance (MED)**, respectively, compared to the best existing designs; Publishes at the **top conference DATE22** (Github link: https://github.com/FCHXWH/ApproximateMult);
     - For the approximate gate-level synthesis of generic circuits, proposes a high-performance method based on Ising model for advancing the approximate disjoint decomposition of generic circuits; Compared to state-of-the-art methods, the proposed Ising model-based approach achieves a **11% reduction in MED and an average speedup of 1.16×**; Publishes at the **top conference DAC24** (Github link: to be updated).

3. **Gate-level Probability Analysis in Logic Networks:**
   - **Definition**: derive the signal probability of each logic gate in a logic network by a propagation through it, given the signal probabilities at the primary inputs (PIs) of the network;
   - **Application**: dynamic power estimation; approximate computing;
   - **Proposed Work:**
     - Proposes an accelerated symbolic probability analysis algorithm, which **has a linear complexity** with #nodes in a logic network;
     - Improves the **estimation accuracy** of switching activity by up to **24.70%**, while it also has **a speedup of up to 29×**, compared to the existing methods;
     - Publishes at the **top conference ICCAD22** (Github link: to be updated).

Project

1. **ASIC Standard Cell Customization under 45nm and 7nm Technology** Oct. 2022-June 2023
   - **Overview**: Extend the standard cell library in very large scale integrated circuit (VLSI) designs for better VLSI circuit performance and lower power consumption under 45nm

and 7nm technology.

- **Flow**:
  - **Extract new standard cells** from digital circuits based on the Frequent Subgraph Mining (FSM) algorithm.
  - Synthesize the minimal transistor network for the extracted new standard cells by our proposed automatic synthesis tool, **MiniTNtk** (**published at ICCAD'23**), which can achieve the minimum transistor networks over benchmarks.
  - Automatically **generate the VLSI layout** for the extended standard cells and extract parasitic parameters.
  - Use the extended standard cell library to do logic synthesis over EPFL benchmarks, **reducing area by at most 12.6%**.

Selected Honors & Achievements

Academic Scholarships, SJTU, CN	2019,2020
National Mathematics Competition of College Students, CN (**First Prize**)	2017
Excellent Student Award, XDU, CN	2016,2017,2018

Other Experiences

1. **Review experiences**: DAC, ICCAD, DATE, TCAD, JCST
2. **Programming skills**: C++, C, Python (pytorch, tensorflow), Verilog
3. **EDA tools:**
   - **Commercial**: Synopysy Design Compiler, Synopsys Power Compiler, Intel Quartus
   - **Academic**: Berkeley ABC, Berkeley SIS, EPFL Mockturtle
   - Read codes of ABC (C) and Mockturtle (C++), and develop our own algorithms based on their data structures, especially about technology independent logic synthesis and FPGA technology mapping.
4. **Mathematical tools**: Gurobi, CPLEX, MiniSAT
5. **Interested to optimization algorithms**:
   - **Continuous case**: Convex Optimization
   - **Discrete case**: Integer Programming, SAT Algorithm, Reinforcement Learning, Ising Model