LLM4ChipDesign Course Prerequisite Survey

## Student Background Assessment Form

**Dear Student,**Welcome to the LLM4ChipDesign course! This course explores the intersection of Large Language Models (LLMs) and chip design, covering topics such as automated Verilog generation, testbench creation, SystemVerilog assertions, and hardware-software co-design using AI.  
  
To ensure you have the necessary background knowledge and to tailor the course content to your experience level, please complete this prerequisite assessment survey. Your responses will help us understand your current knowledge and provide appropriate support during the course.  
  
Please answer all questions honestly. This survey is for assessment purposes only and will not affect your grade.

# Student Information

|  |  |
| --- | --- |
| **Name:** |  |
| **Student ID:** |  |
| **Email:** |  |
| **Academic Year/Level:** |  |
| **Major/Program:** |  |
| **Date:** |  |

# Prerequisite Course Assessment

Please indicate your experience level with the following subject areas that are fundamental to this course. Rate your experience using the scale:  
• No Experience (0): Never studied or worked with this area  
• Basic (1): Introductory course or minimal exposure  
• Intermediate (2): One or more courses with practical experience  
• Advanced (3): Extensive coursework and/or professional experience  
• Expert (4): Teaching/research level knowledge

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Course Area** | **No Exp (0)** | **Basic (1)** | **Inter (2)** | **Adv (3)** | **Expert (4)** |
| Digital Logic Design & Boolean Algebra | ☐ | ☐ | ☐ | ☐ | ☐ |
| Computer Architecture & Organization | ☐ | ☐ | ☐ | ☐ | ☐ |
| Hardware Description Languages (Verilog/SystemVerilog) | ☐ | ☐ | ☐ | ☐ | ☐ |
| Programming Languages (Python, C/C++) | ☐ | ☐ | ☐ | ☐ | ☐ |
| Data Structures & Algorithms | ☐ | ☐ | ☐ | ☐ | ☐ |
| Machine Learning & Artificial Intelligence | ☐ | ☐ | ☐ | ☐ | ☐ |
| Natural Language Processing (NLP) | ☐ | ☐ | ☐ | ☐ | ☐ |
| Formal Verification & Model Checking | ☐ | ☐ | ☐ | ☐ | ☐ |
| Electronic Design Automation (EDA) Tools | ☐ | ☐ | ☐ | ☐ | ☐ |
| FPGA/ASIC Design Flow | ☐ | ☐ | ☐ | ☐ | ☐ |
| High-Level Synthesis (HLS) | ☐ | ☐ | ☐ | ☐ | ☐ |
| Hardware-Software Co-design | ☐ | ☐ | ☐ | ☐ | ☐ |
| Computer Systems & Operating Systems | ☐ | ☐ | ☐ | ☐ | ☐ |
| Software Engineering & Version Control | ☐ | ☐ | ☐ | ☐ | ☐ |
| Mathematics (Linear Algebra, Statistics) | ☐ | ☐ | ☐ | ☐ | ☐ |

# Specific Course Experience

Please list any specific courses you have completed in the following areas (include course names/codes if possible):

|  |  |
| --- | --- |
| **Digital Circuit Design / Logic Design:** |  |
| **Computer Architecture:** |  |
| **Verilog/VHDL/SystemVerilog:** |  |
| **Machine Learning / AI:** |  |
| **Programming (Python/C/C++):** |  |
| **Formal Methods / Verification:** |  |
| **Embedded Systems:** |  |
| **Other Relevant Courses:** |  |

# Tools and Software Experience

Please indicate your familiarity with the following tools and software (check all that apply):

|  |  |  |
| --- | --- | --- |
| EDA Tools ☐ Vivado (Xilinx) ☐ Quartus (Intel) ☐ ModelSim/QuestaSim ☐ Synopsys Tools ☐ Cadence Tools ☐ Verilator ☐ GTKWave | Programming Tools ☐ Python ☐ C/C++ ☐ MATLAB ☐ Git/GitHub ☐ Jupyter Notebooks ☐ Linux/Unix ☐ Command Line | AI/ML Frameworks ☐ TensorFlow ☐ PyTorch ☐ OpenAI API ☐ Hugging Face ☐ scikit-learn ☐ NLTK/spaCy ☐ Google Colab |

# Project Experience

1. Have you worked on any hardware design projects? If yes, please describe briefly:

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. Have you used any AI/ML tools or APIs in your projects? If yes, please describe:

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. Have you written Verilog or VHDL code before? What was the complexity level?

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. Have you used any LLMs (ChatGPT, Claude, etc.) for coding assistance? Please describe your experience:

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# Learning Goals and Expectations

1. What specific aspects of LLM-based chip design are you most interested in learning?

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. Do you have any specific career goals related to hardware design or AI?

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. What challenges do you expect to face in this course?

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. How do you prefer to learn new technical concepts? (hands-on, theory-first, examples, etc.)

Answer: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# Additional Information

Please provide any additional information about your background, interests, or concerns that might be relevant to this course:

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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Thank you for completing this survey! *This information will help us provide the best possible learning experience tailored to your background and goals.*

Course: LLM4ChipDesign - Generative AI for Chip Design  
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