Sorting Networks

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Sorting

- Sorting is a critical operation in computer systems.
  - In numerous application domains,
    sorting is an indispensable part of applications
    with or without the knowledge of users.
- Sorting algorithms have been extensively investigated during the entire era of computer science.
- The exponential increase in data volumes
  drives the search for
  efficient, faster, and parallelized sorting algorithms.
- Algorithms that previously were impractical or inadequate have re-emerged with the development of new technologies.

Comparison-based sorting algorithms

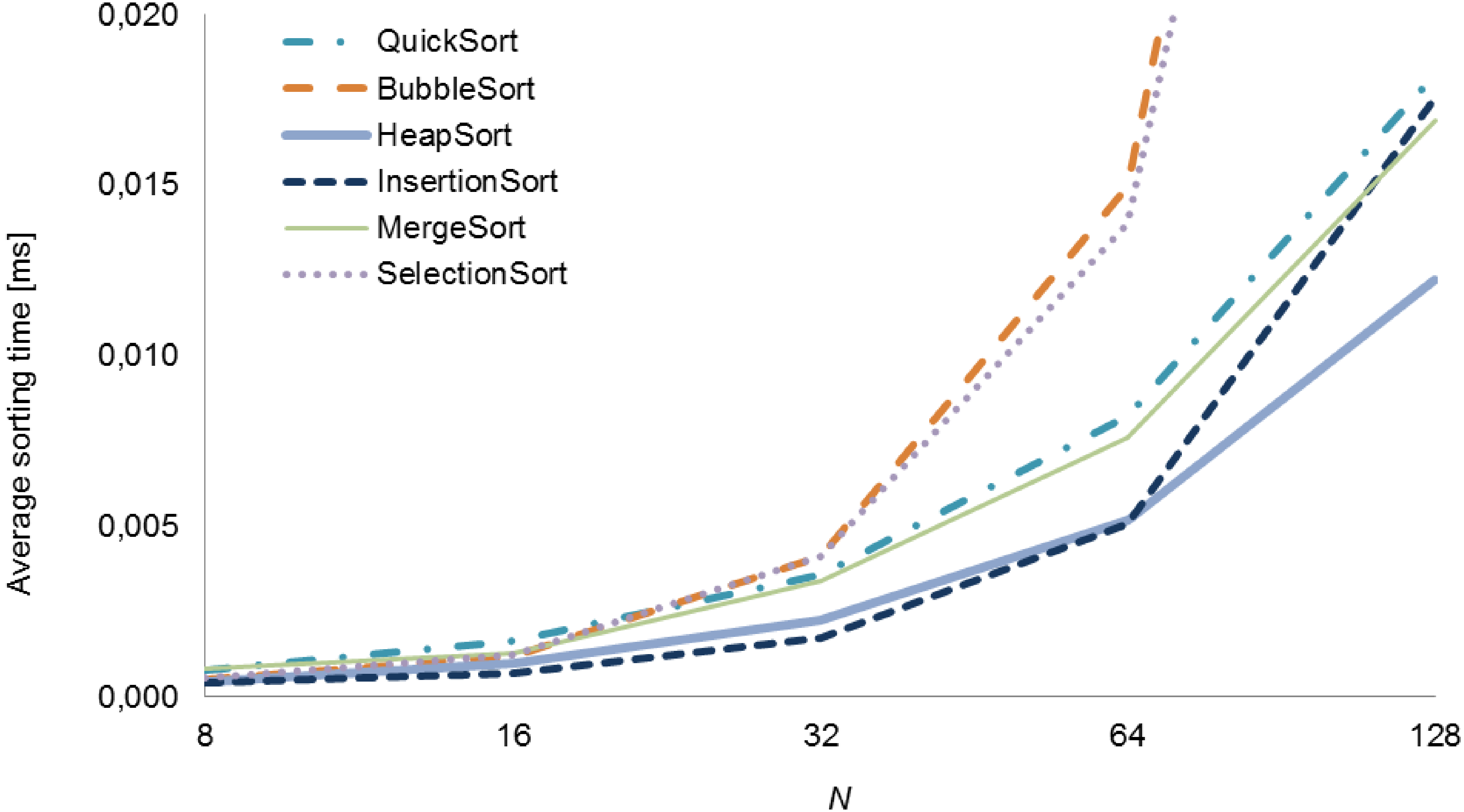
- Comparison-based sorting algorithms are classified into three groups based on the time order of the execution of comparison operations
  - **sequential** sorting algorithms
    consecutively execute the comparison operations;
  - **parallel** sorting algorithms
    simultaneously execute several comparison operations
  - **network** sorting algorithms are parallel algorithms;
    they exhibit the property in which the sequence of comparison operations is identical for all possible input data.

- A particular sorting algorithm can have
  - one or more versions
  - belonging to one or more of the above groups.

Most popular sorting algorithms

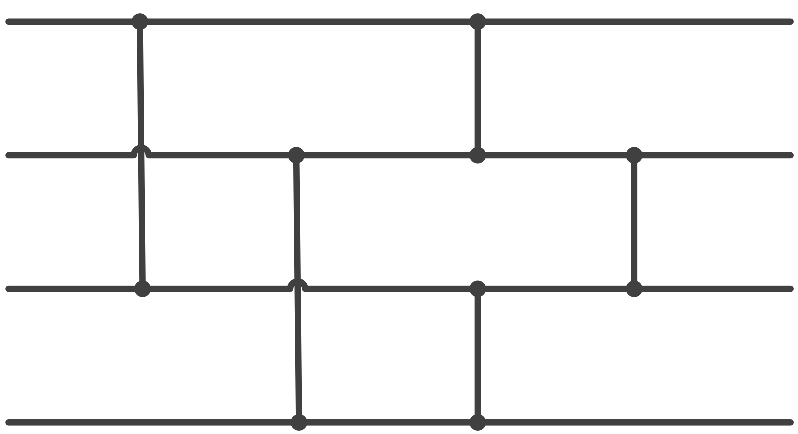
Algorithm	Sorting time – O(x) notation		
	Average	Best	Worst
Insertion sort	N^2	N	N^2
Selection sort	N^2	N^2	N^2
Bubble sort	N^2	N	N^2
Shell sort	$N \cdot (\log_2 N)^2$	N	$N \cdot (\log_2 N)^2$
Quicksort	$N \cdot \log_2 N$	$N \cdot \log_2 N$	N^2
Merge sort	$N \cdot \log_2 N$	$N \cdot \log_2 N$	$N \cdot \log_2 N$
Heap sort	$N \cdot \log_2 N$	$N \cdot \log_2 N$	$N \cdot \log_2 N$
Binary tree sort	$N \cdot \log_2 N$	N	$N \cdot \log_2 N$

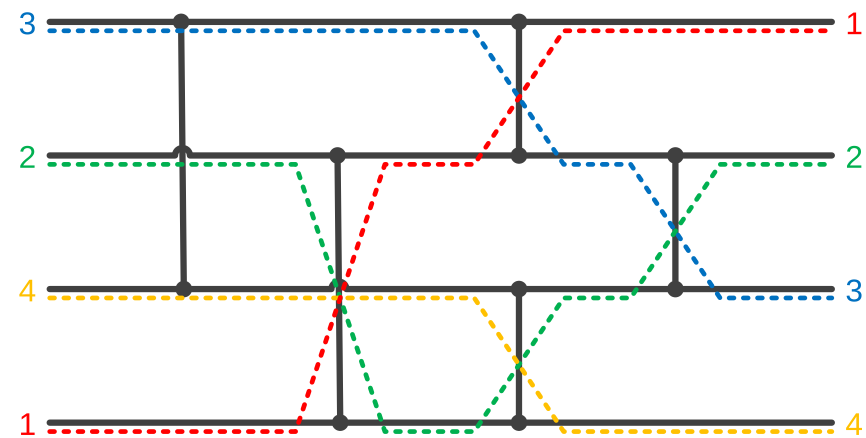
Average sorting times



Sorting Networks

- Sorting networks are:
  - a subset of comparison networks
  - abstract machines that are solely constructed of wires and comparators
- The wires that interconnect comparators must form a directed acyclic graph!





Sorting Network Properties

- A sorting network can be characterized by
  - its size, denoted as *C*
  - its depth, denoted as *D*.

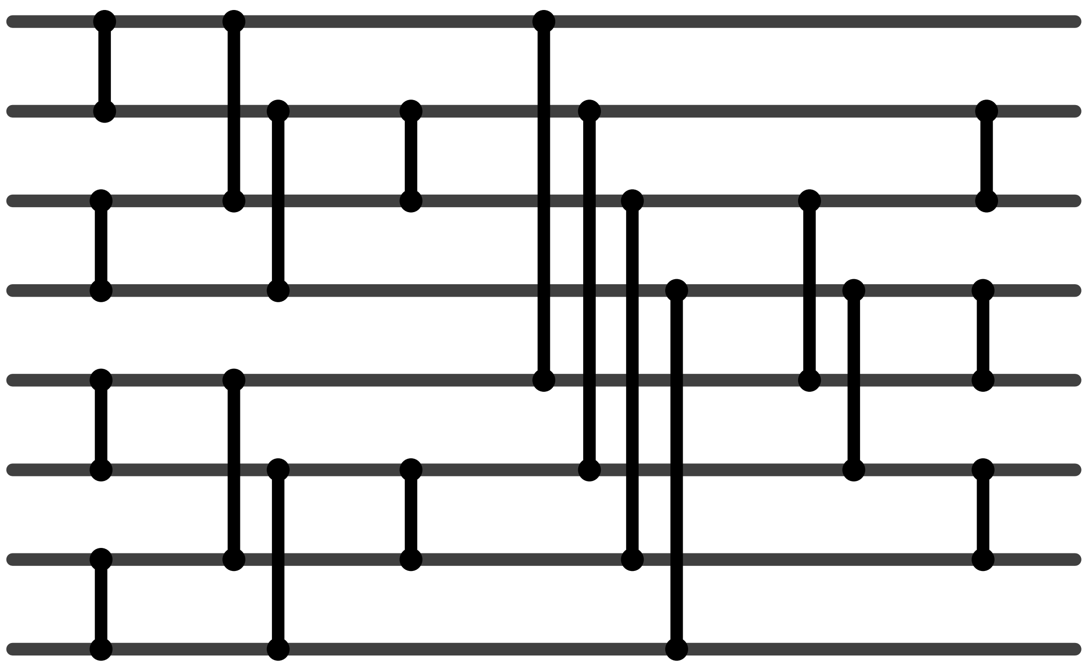
- The ***size*** of a sorting network is defined by the total number of comparators in the network.
- The ***depth*** of the sorting network is defined as the maximum number of comparators along any valid path from any input to any output.

- For example, the sorting network in the previous slide has a size of 5 and a depth of 3.

Example - Odd-Even Merge Sorting

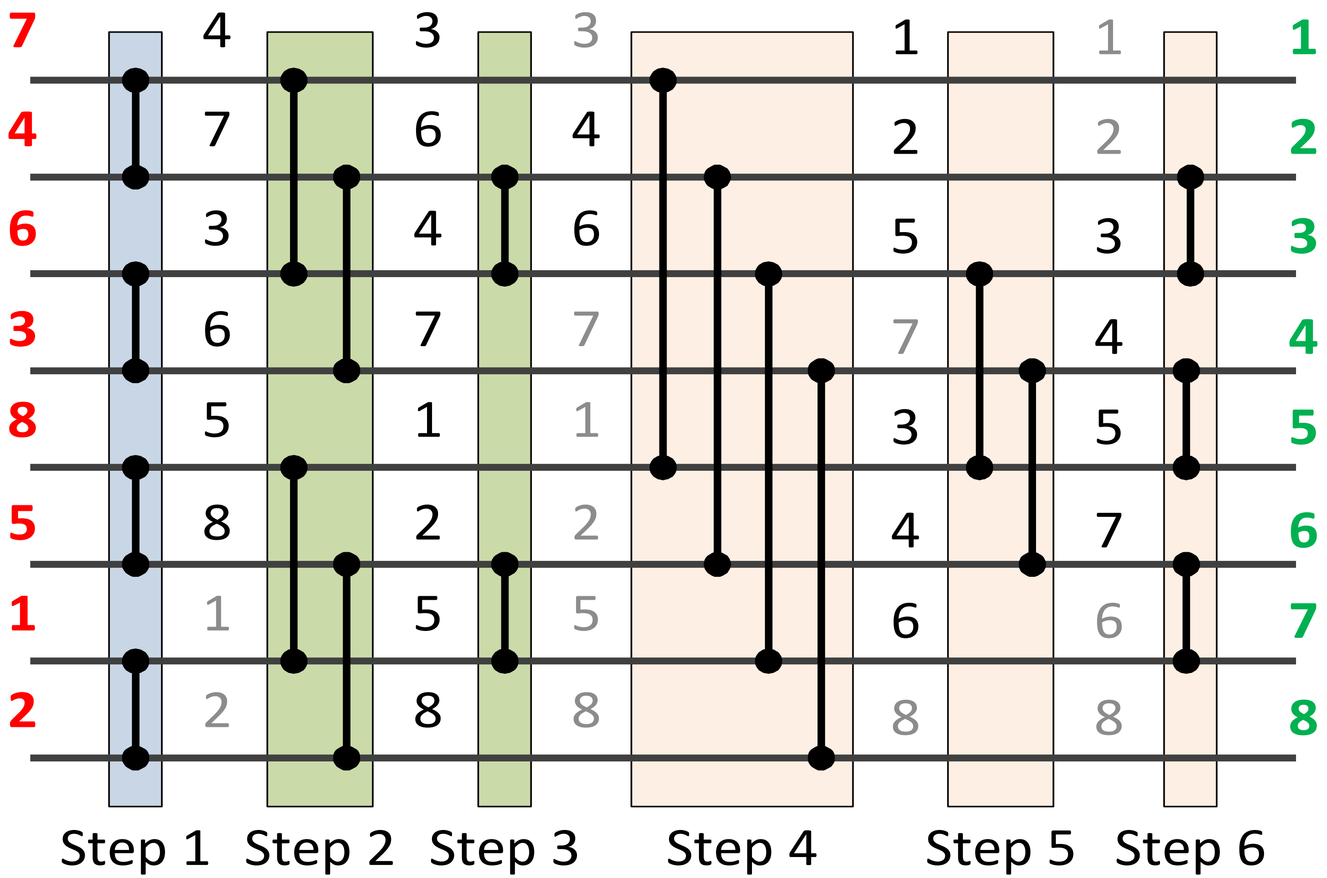
$$C_{merge}(N) = \frac{N \cdot \log_2 N \cdot (\log_2 N - 1)}{4} + N - 1$$

$$D_{merge}(N) = \frac{\log_2 N \cdot (\log_2 N + 1)}{2}$$



Operation Example

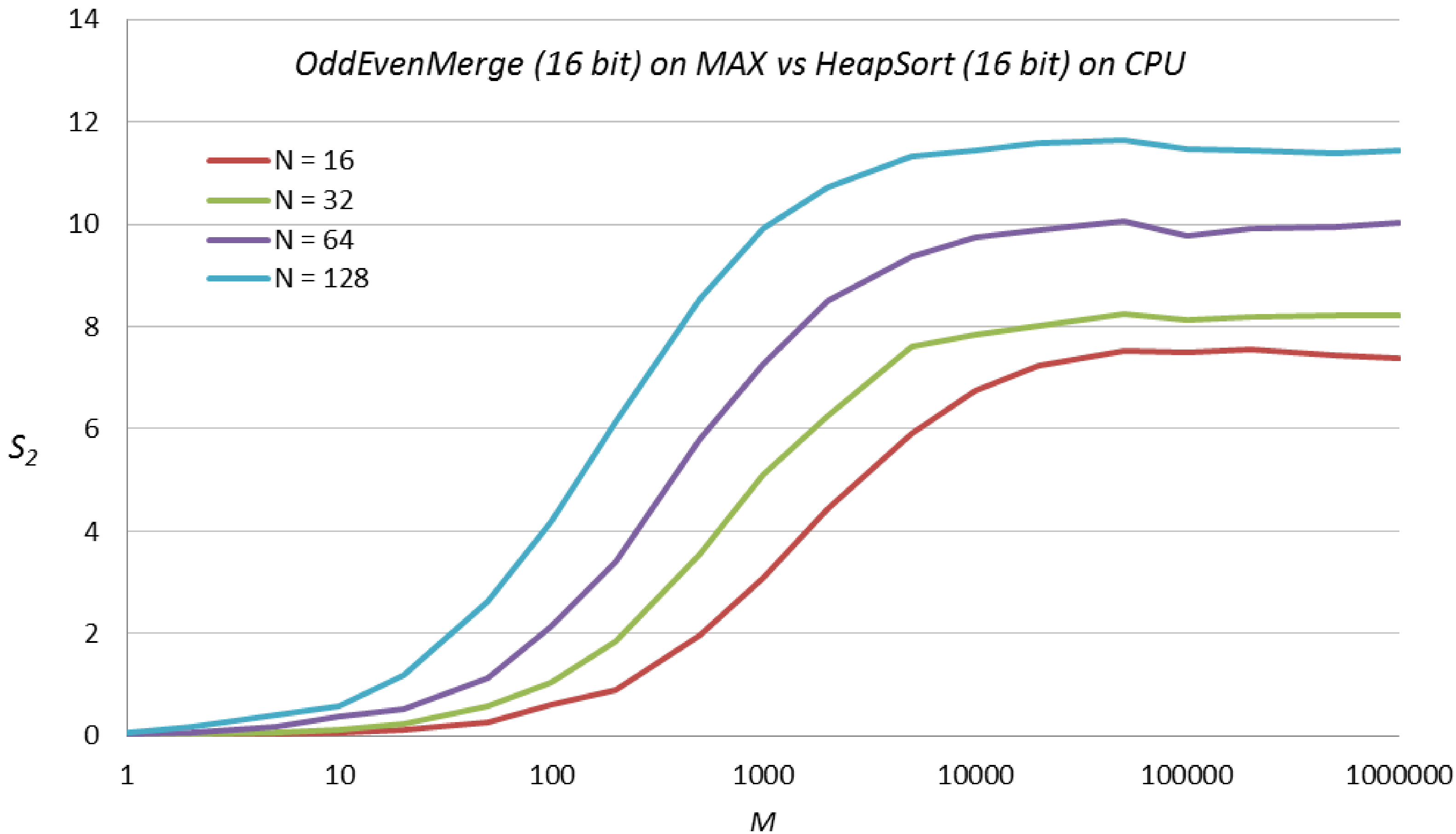
Odd-even merge sorting network



Comparison of Network Sorting Alg.

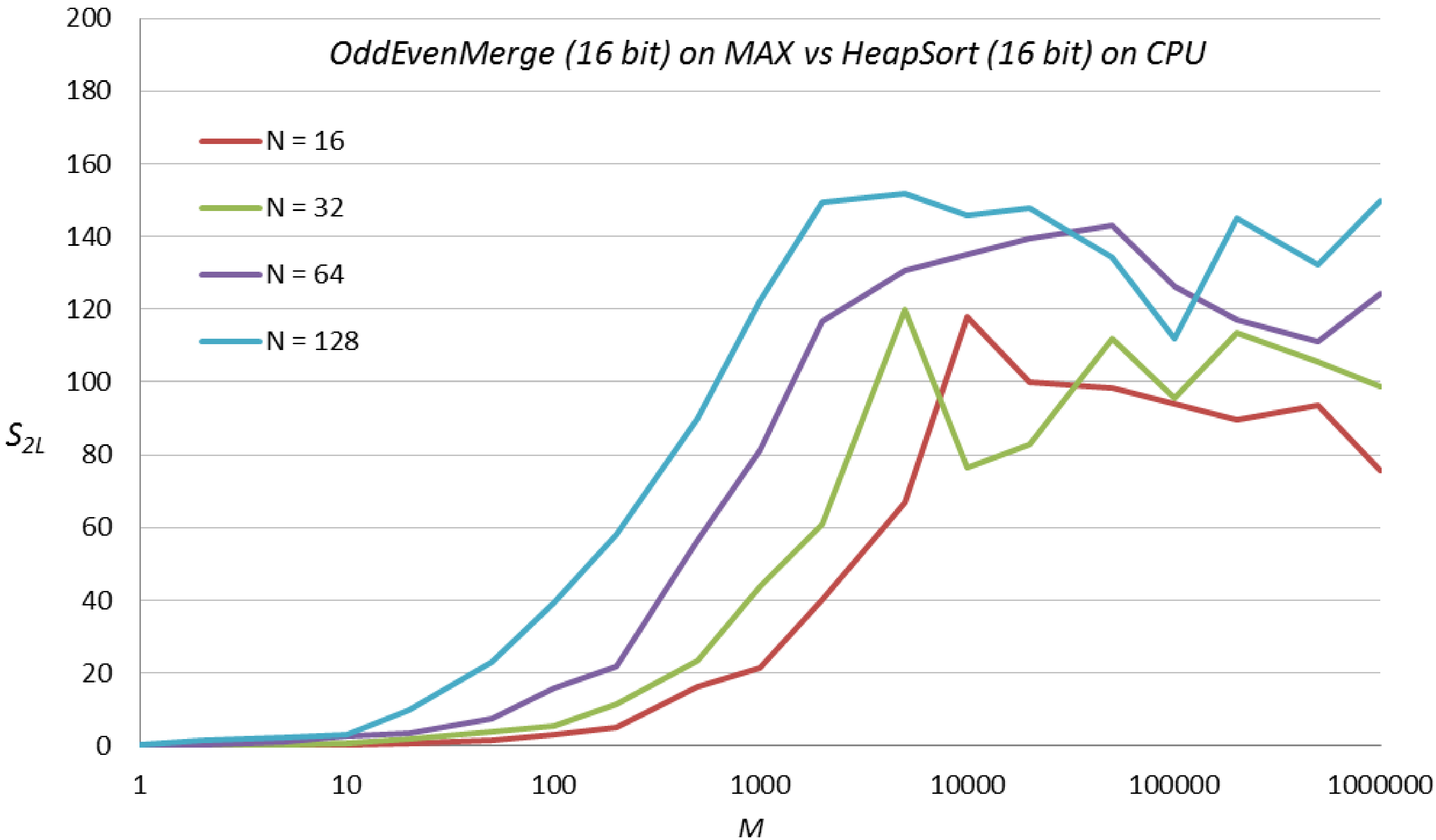
Sorting network	Depth	Size
Bubble	$2N-3$	$\frac{N(N-1)}{2}$
Odd-even	N	$\frac{N(N-1)}{2}$
Bitonic	$\frac{\log_2 N \cdot (\log_2 N + 1)}{2}$	$\frac{N \cdot \log_2 N \cdot (\log_2 N + 1)}{4}$
Odd-even merge	$\frac{\log_2 N \cdot (\log_2 N + 1)}{2}$	$\frac{N \cdot \log_2 N \cdot (\log_2 N - 1)}{4} + N - 1$
Pairwise	$\frac{\log_2 N \cdot (\log_2 N + 1)}{2}$	$\frac{N \cdot \log_2 N \cdot (\log_2 N - 1)}{4} + N - 1$

Experimental Results



Speedup for different array size N. We use a 16-bit fixed point number format. The curves show the ratio between the sorting time of sequential heap sorting on the host CPU and odd-even merge network sorting on the MAX2 card.

Experimental Results



Speedup (deducting the loopback transmission times) for different array size N using a 16-bit fixed point number format. The curves show the ratio between the sorting time of sequential heap sorting on the host CPU and odd-even merge network sorting on the FPGA.

Sorting Speedup

- Between **7** and **12**
  - depending on numer format (numer of bits
  - comparing network sorting to the fastest sequential sorting algorithm
  - sorting times includ communication delays between the PC and Mexeler
- Between **100** and **160**
  - depending on numer format (numer of bits
  - comparing network sorting to the fastest sequential sorting algorithm
  - considering only the sorting time inside the FPGA

Conclusion

- Nearly forgotten algorithms, which were previously impossible or impractical to implement,
  can re-emerge with advances in technology that enable their use (DataFlow computers).

- Sorting networks and their implementation on DataFlow computers are a natural match.

- We achieved the speedups of:
  - > 10 (considering the communication times) and
  - > 100 (considering only the sorting time inside the FPGA)