

SP CARD

	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title		
Verified by : NARESH N			Size A4	Document Number SP CARD	Rev 1.0
Aproved by : NARESH N			Date: Tuesday, June 20, 2023 Sheet 1 of 50		

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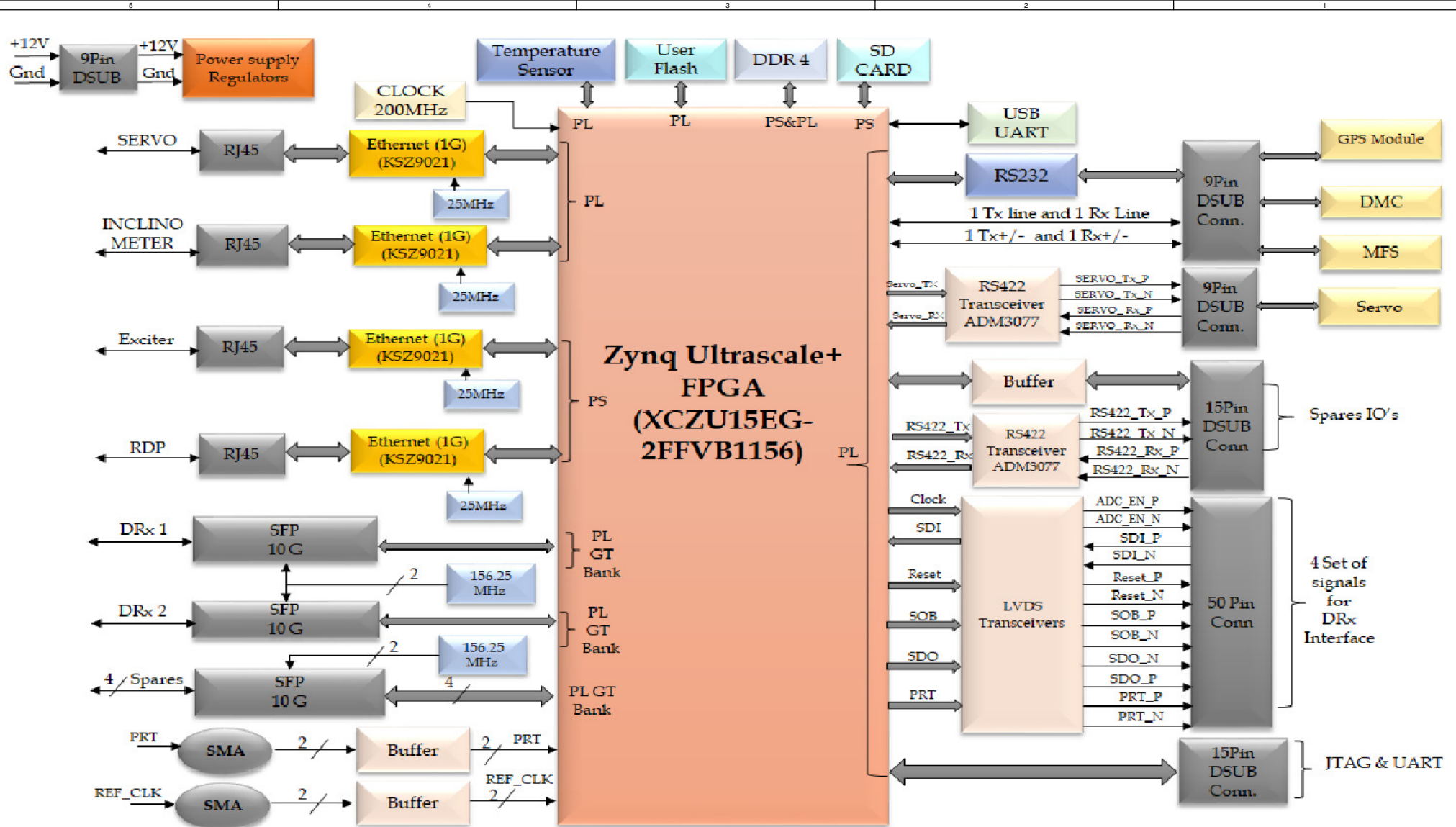
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REV Change Record

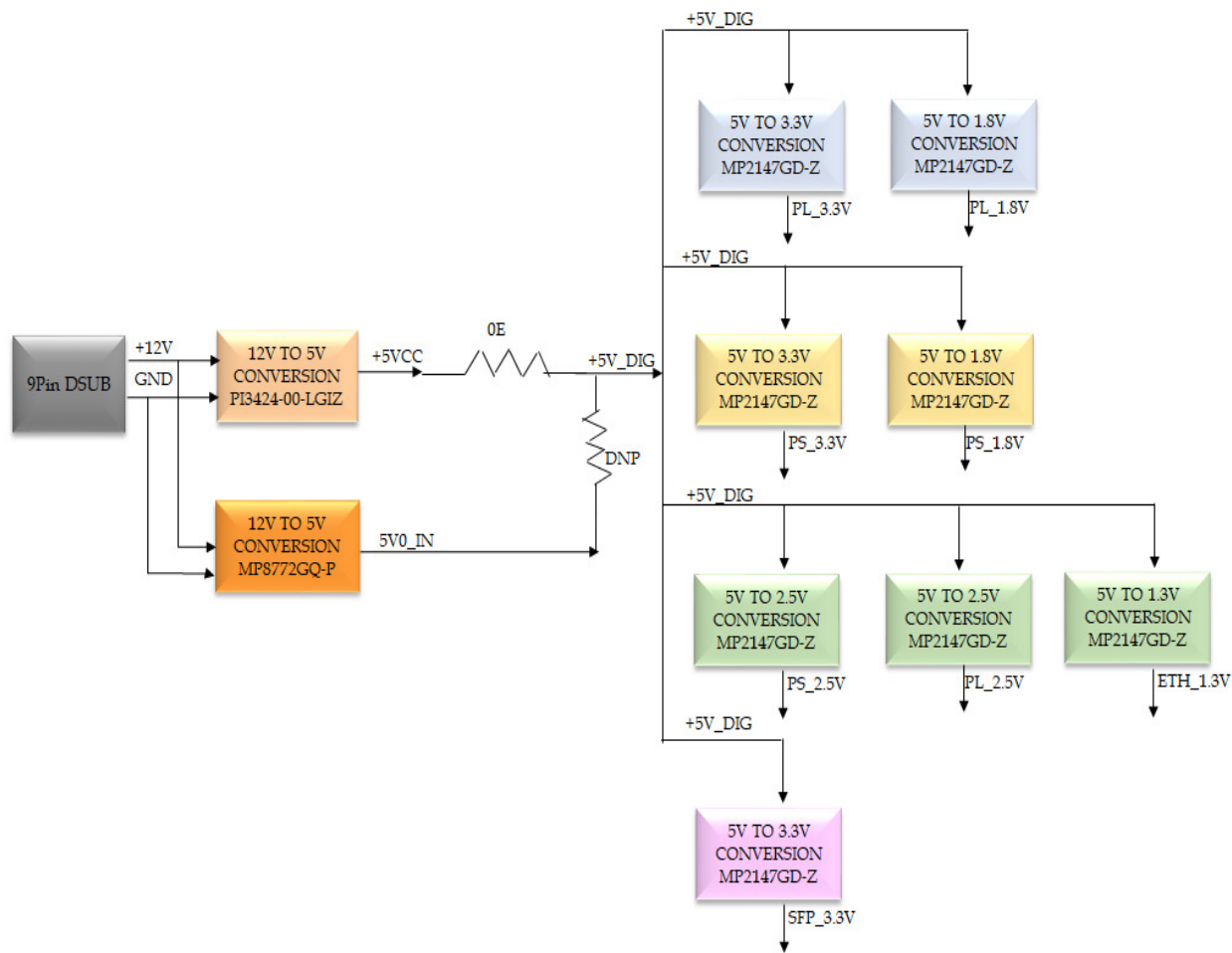
S.NO	DATE	REVISION.	BRIEF CHANGE

	Date	Signatue	FALCONX ELECTRO TECHNOLOGIES PVT LTD	
Designed by : LAVANYA.B			Title Revision History	
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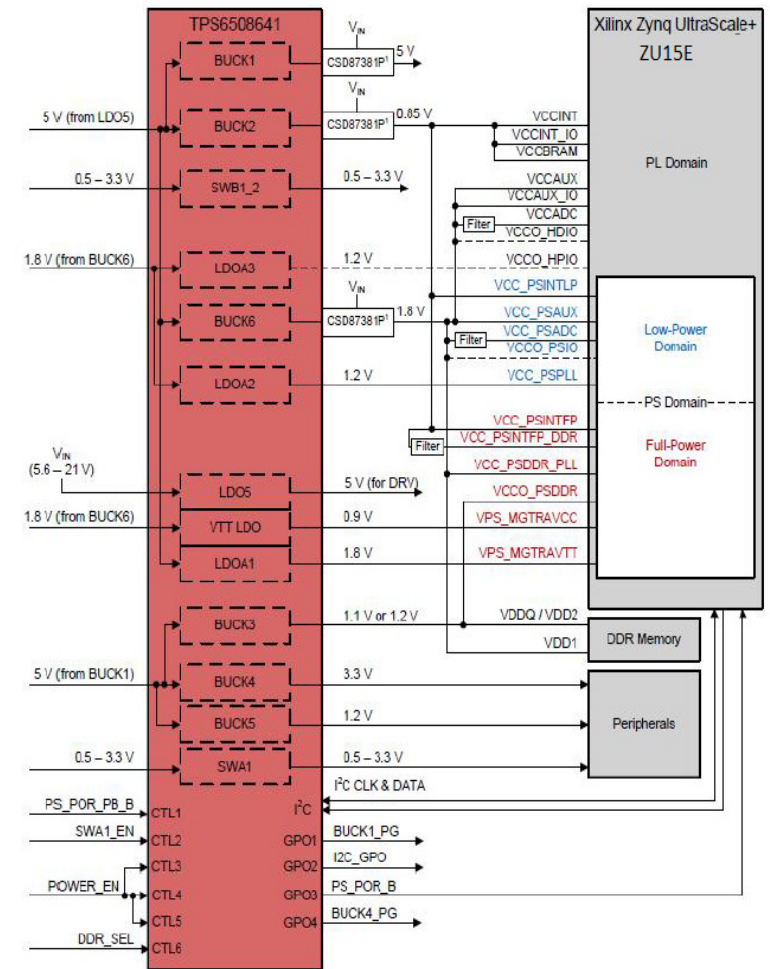


	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD	
Designed by : LAVANYA.B			Title Block Diagram	
Verified by : NARESH N			Size B	Document Number SP CARD
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PERIPHERALS SUPPLY FLOW

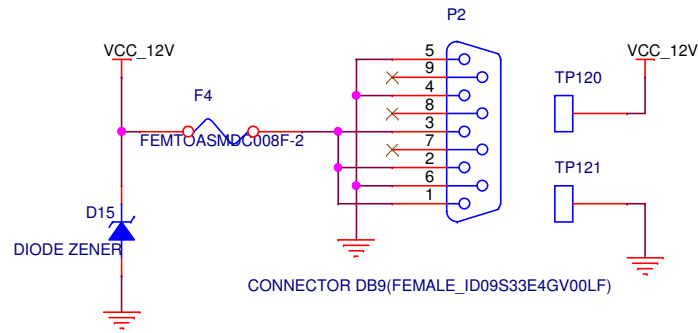


FPGA SUPPLY FLOW

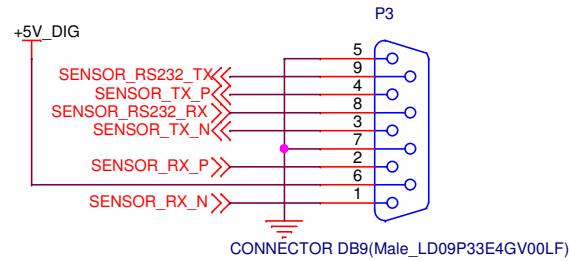


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Designed by : LAVANYA.B			Title Power Supply Flow Diagram	
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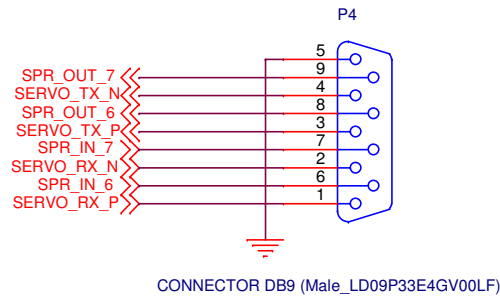
Power Supply Conn



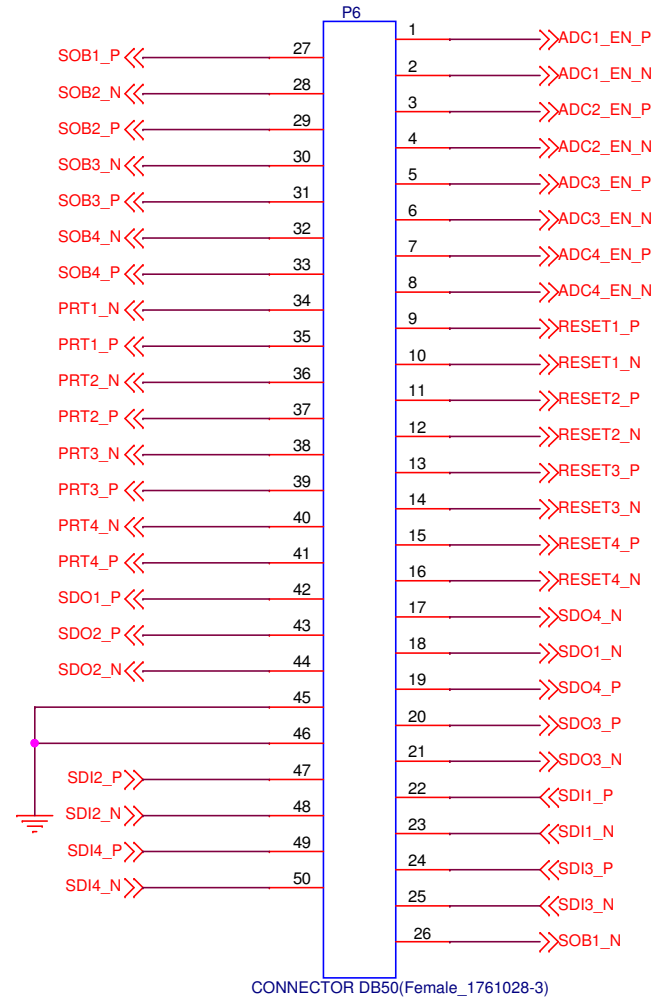
GPS,DMC,MFS Conn



SERVO Conn

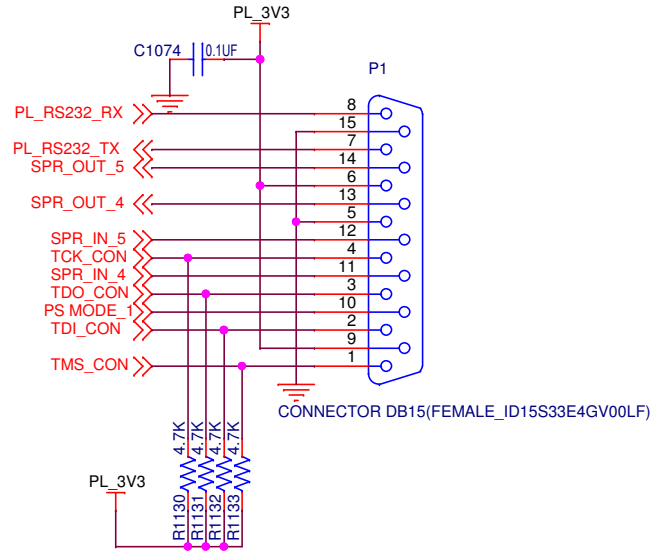


LVDS IO'S Conn

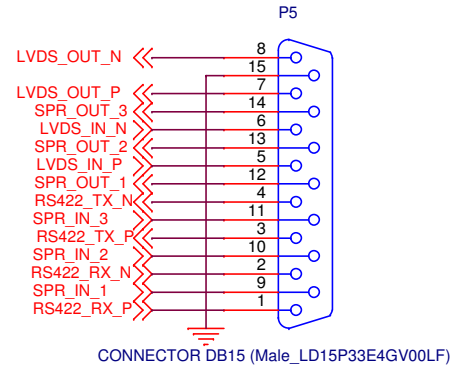


	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title Connectors - PS, Sensors, LVDS		
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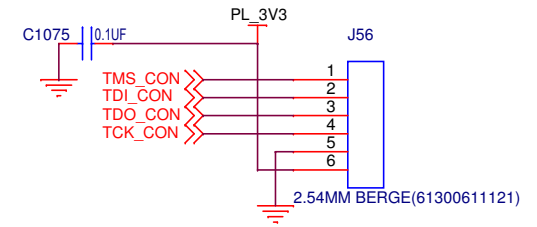
JTAG & UART Conn



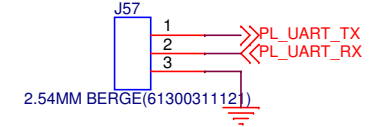
Spare IO'S Conn



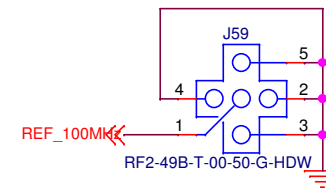
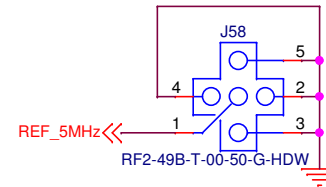
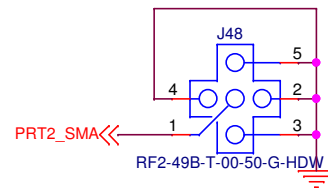
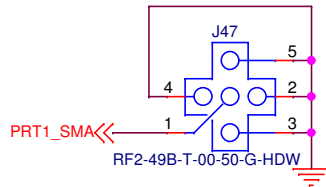
ON BOARD JTAG CONNECTOR



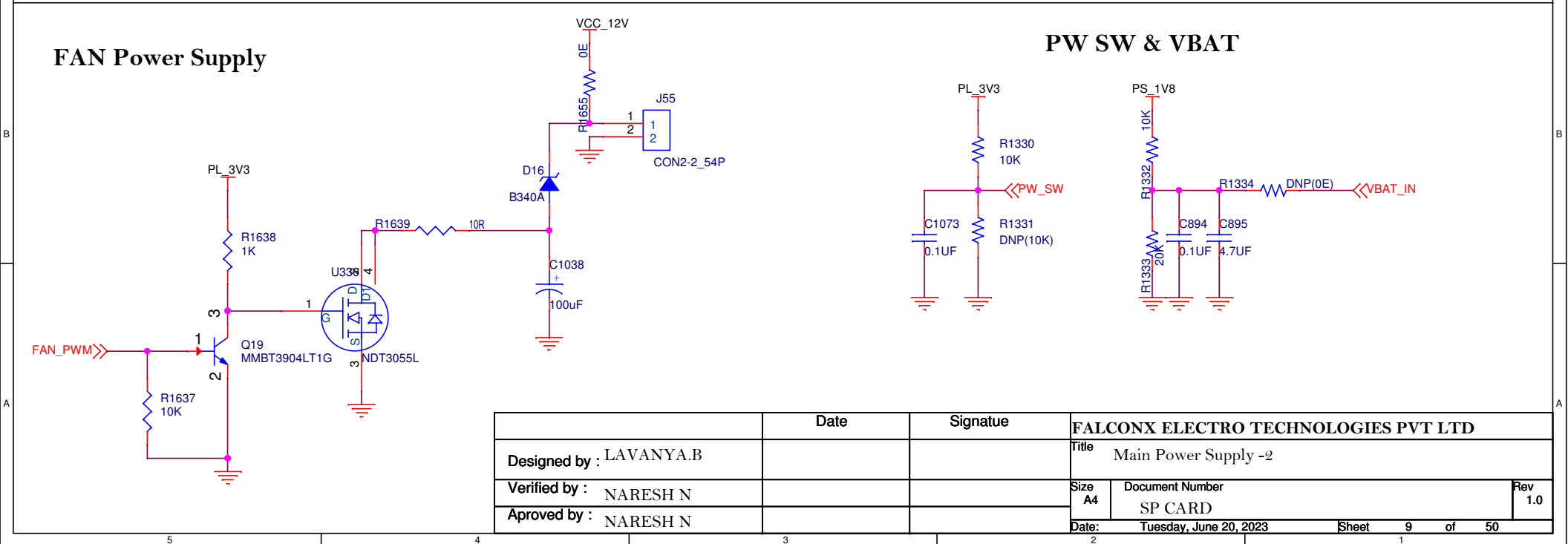
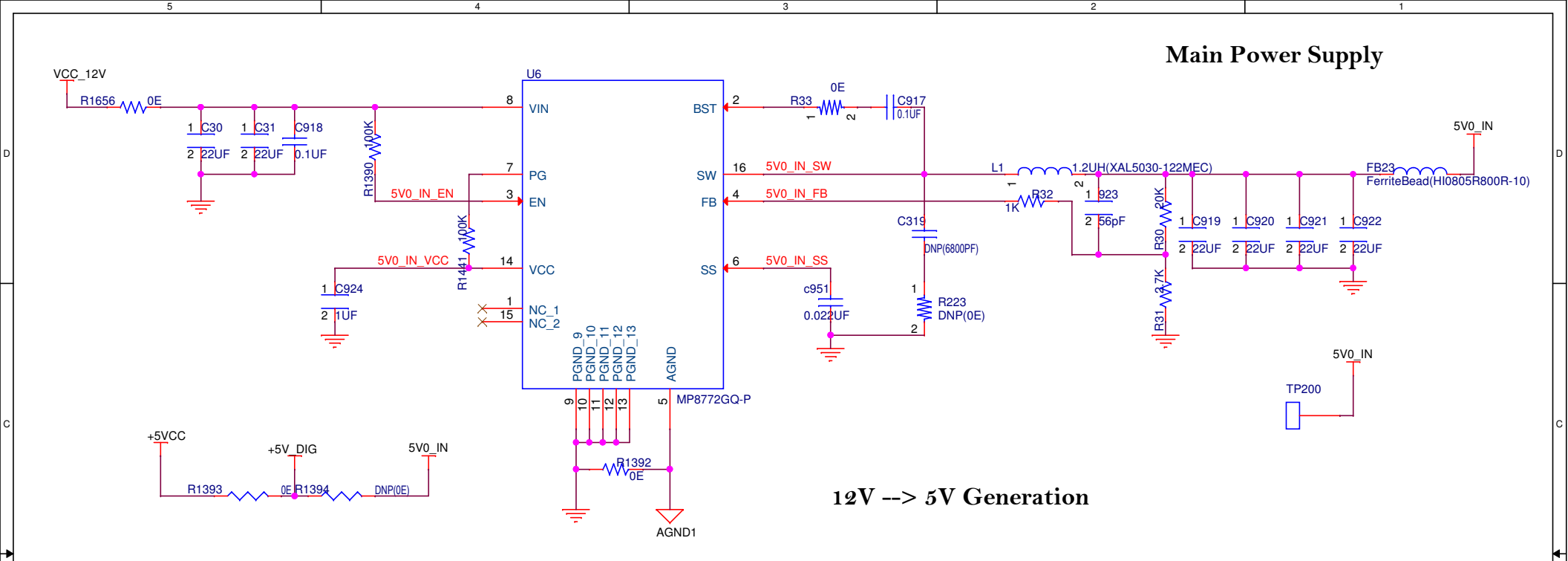
PL UART



SMA CONNECTORS

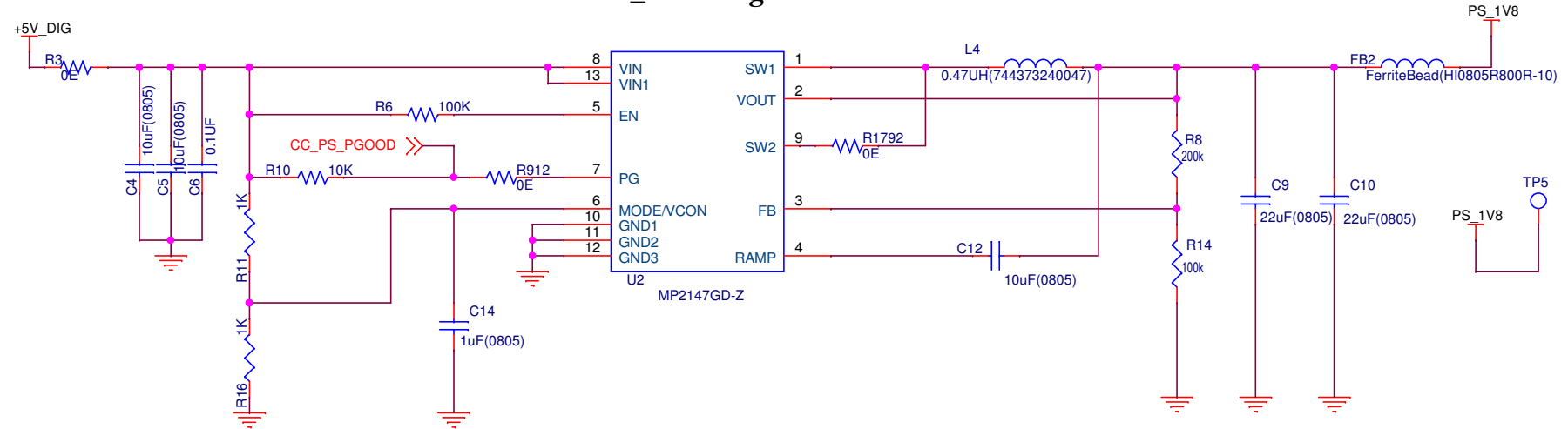


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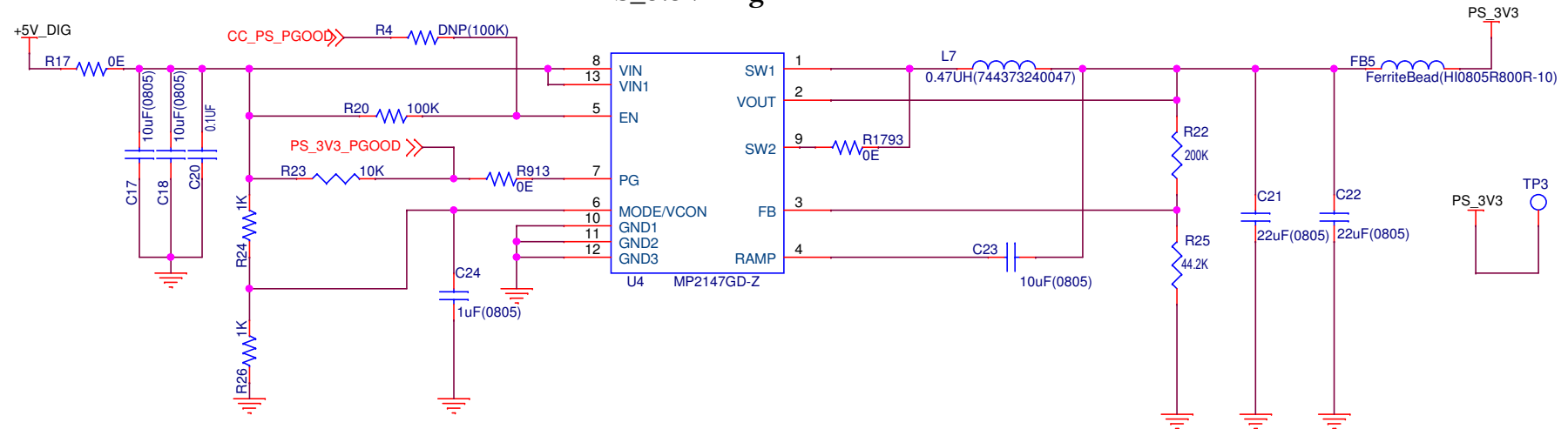
5V --> 1.8V Generation

PS_1.8V Regulator



5V --> 3.3V Generation

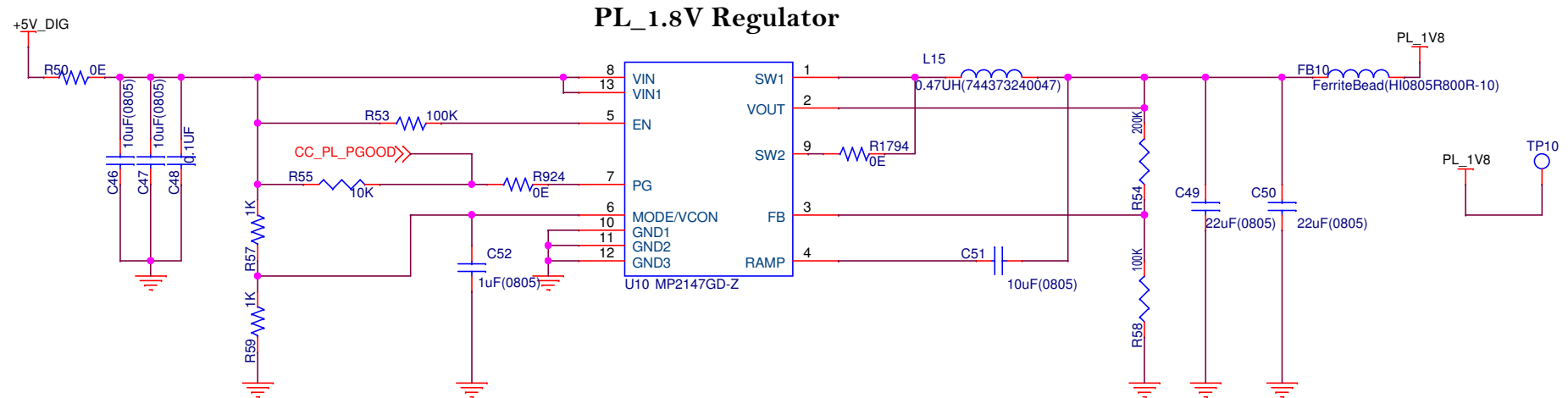
PS_3.3V Regulator



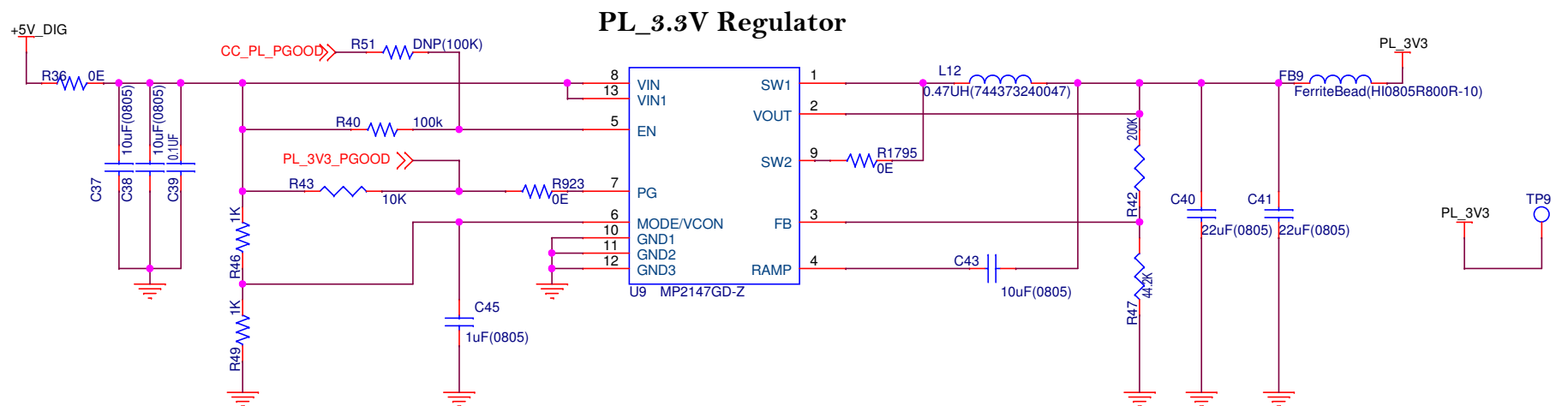
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Designed by : LAVANYA.B			Title PS Power Supply	
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5V --> 1.8V Generation



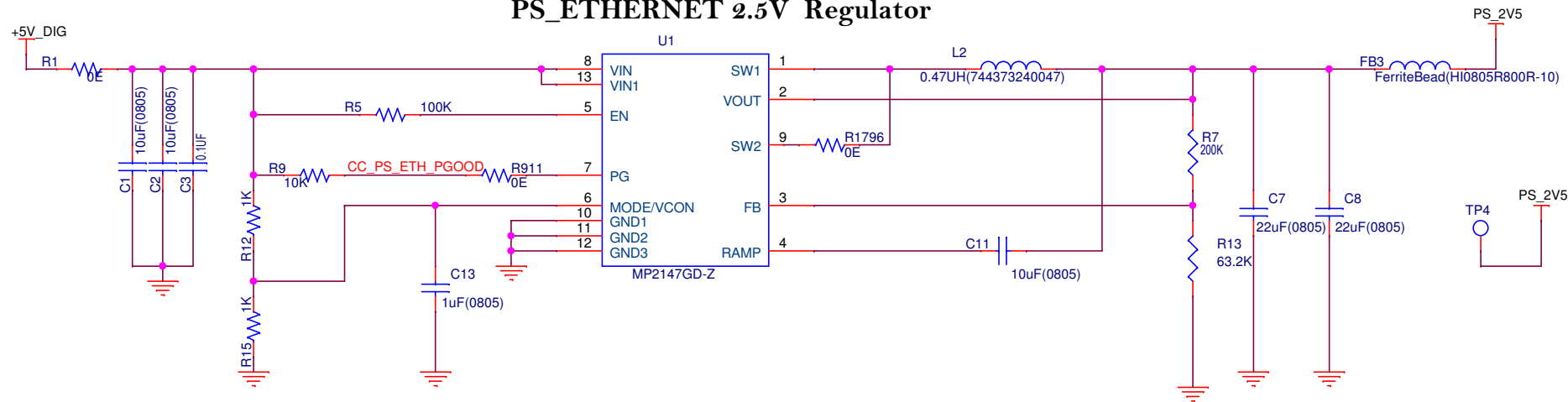
5V --> 3.3V Generation



	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title PL Power Supply		
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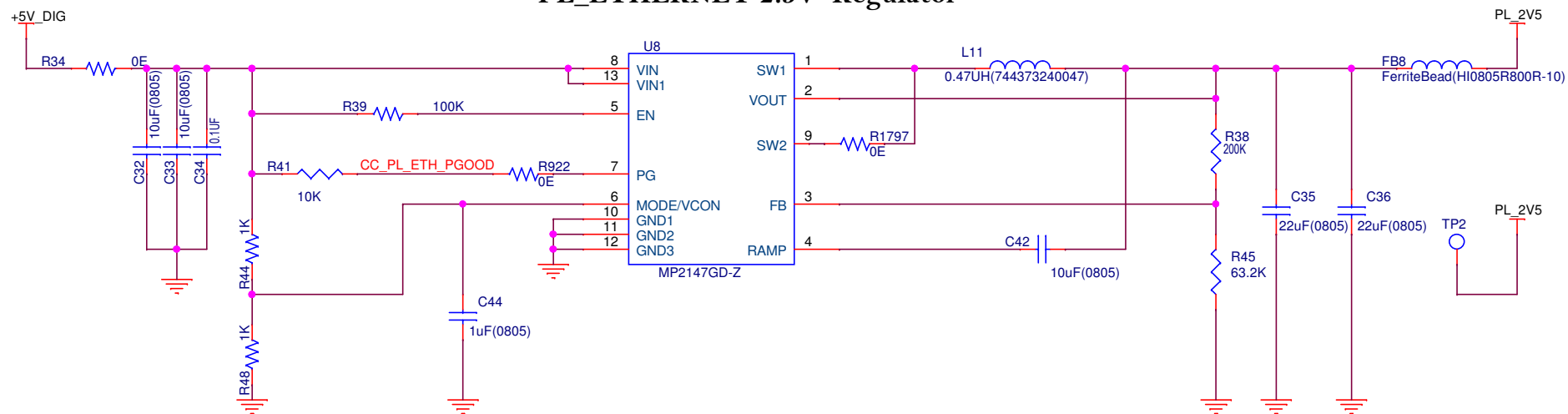
5V --> 2.5V Generation

PS_ETHERNET 2.5V Regulator



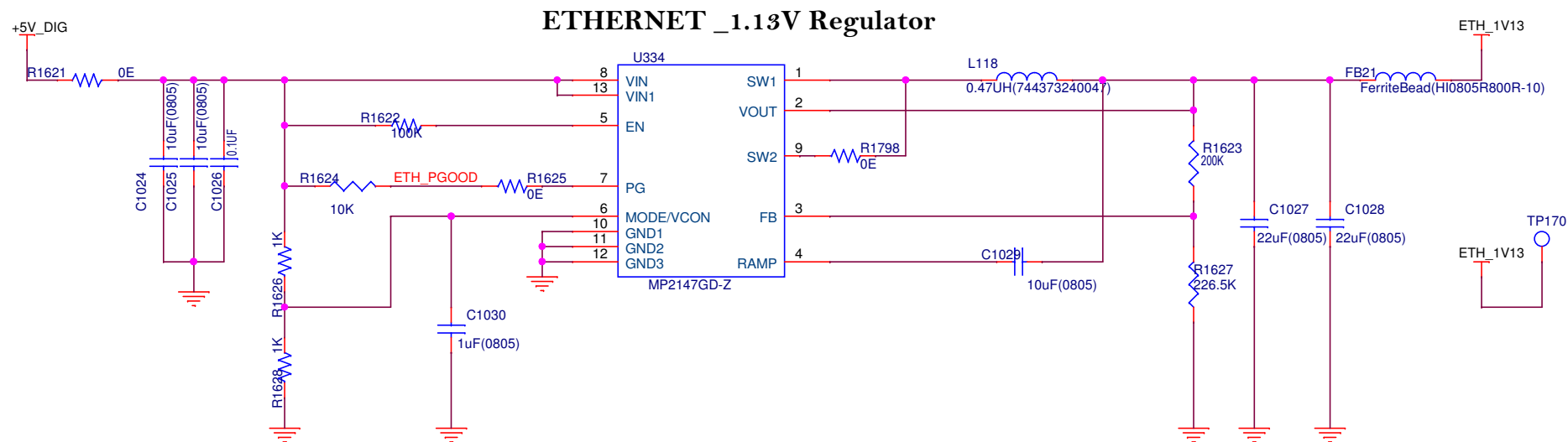
5V --> 2.5V Generation

PL_ETHERNET 2.5V Regulator

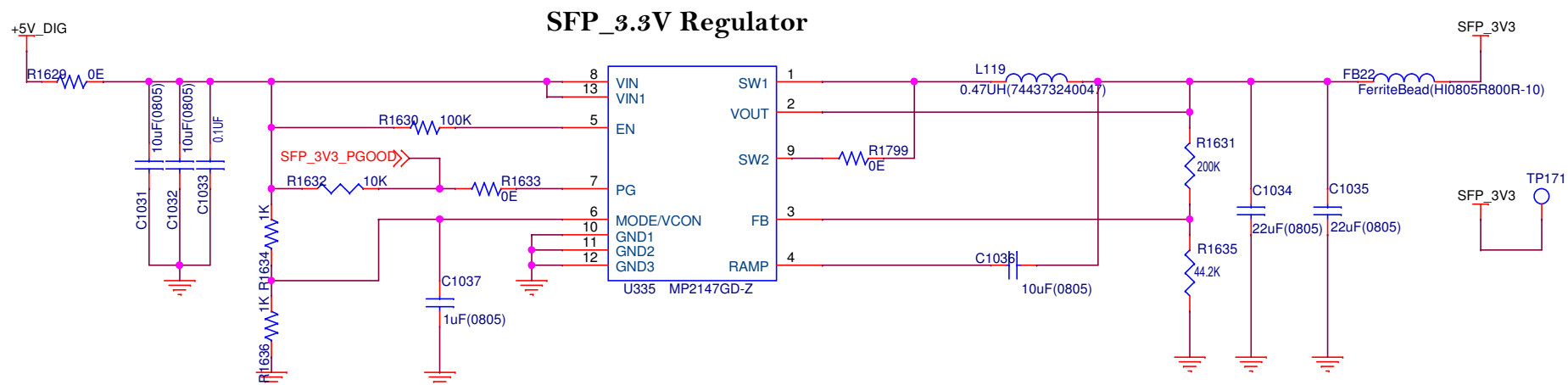


	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD	
Designed by : LAVANYA.B			Title Ethernet Power Supply	
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5V --> 1.13V Generation



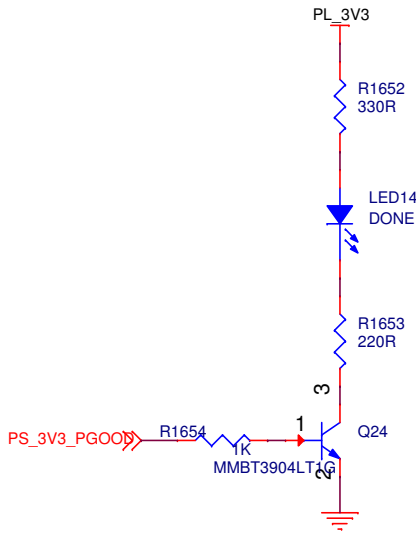
5V --> 3.3V Generation



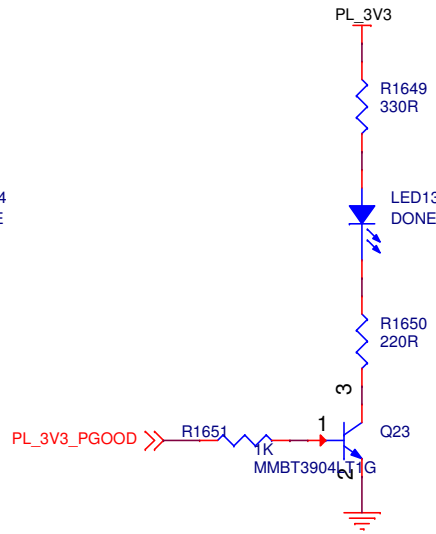
	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title Ethernet & SFP Power Supply		
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Supply LED Indications

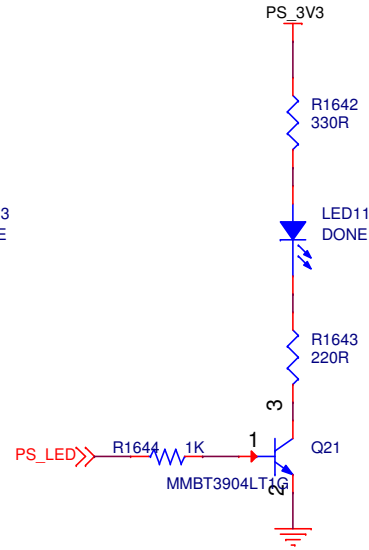
PL Supply



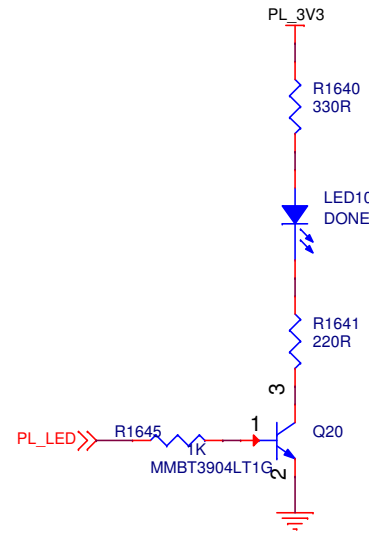
PL Supply



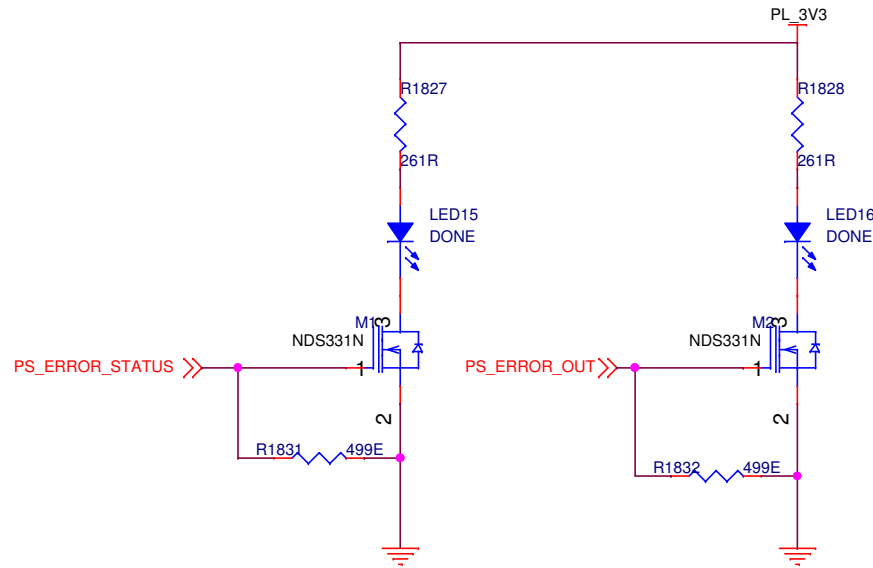
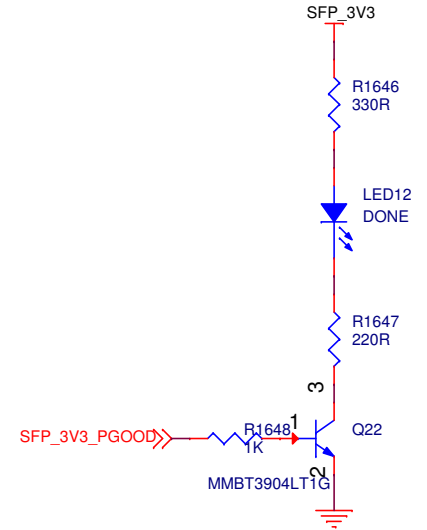
FPGA PS Bank



FPGA PL Bank

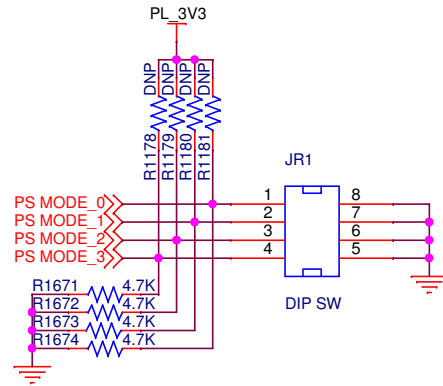


SFP SUPPLY



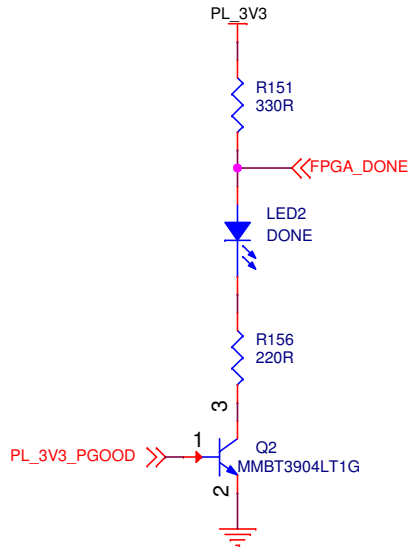
	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title Supply LED Indications		
Verified by : NARESH N			Size A4	Document Number	Rev 1.0
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Mode Selection

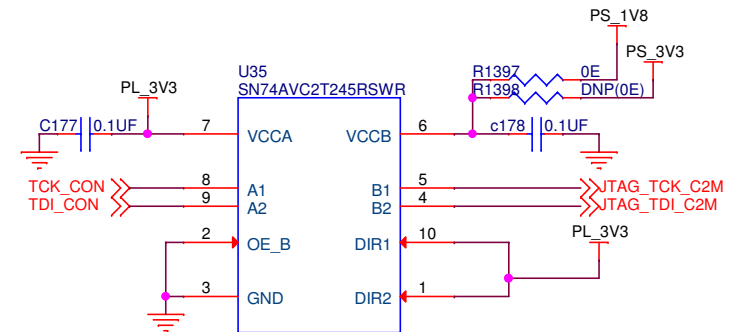
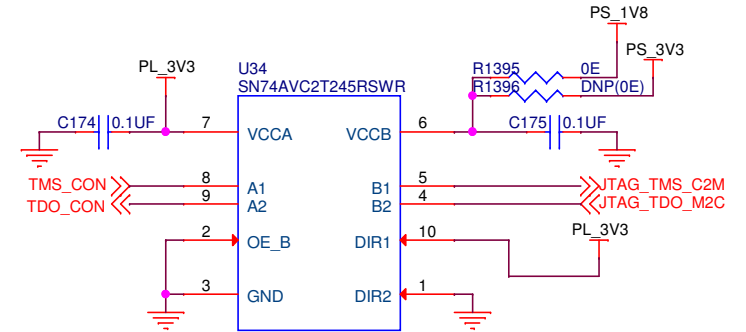


MODE[3:0]	BOOT MODE
0000	PS JTAG
0001	Quad_SPI(24b)
0010	Quad_SPI(32b)
0011	SD0(2.0)
0100	NAND
0101	SD1(2.0)
0110	eMMC(1.8V)
0111	SD1 LS(3.0)
1000	PJTAG(MIO #0)
1001	PJTAG(MIO #1)
1110	USB0(2.0)

FPGA Done LED



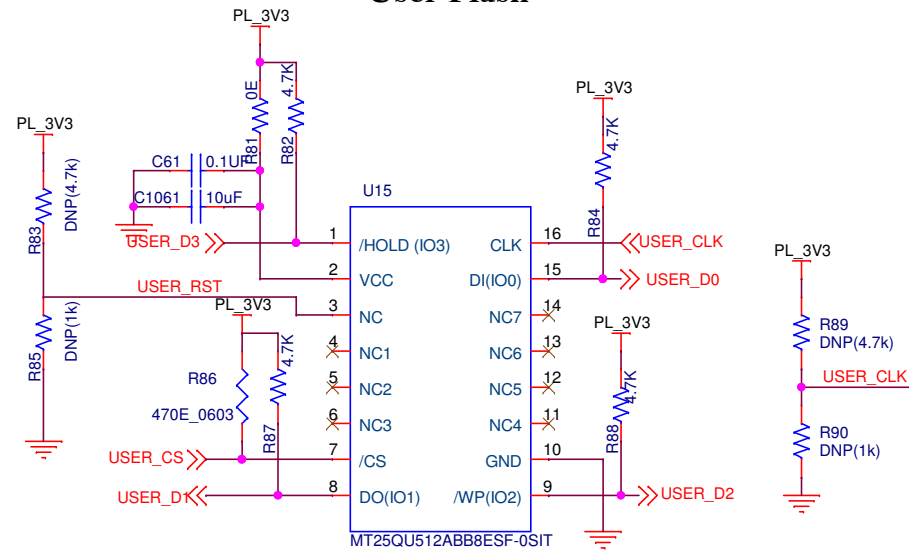
JTAG Buffers



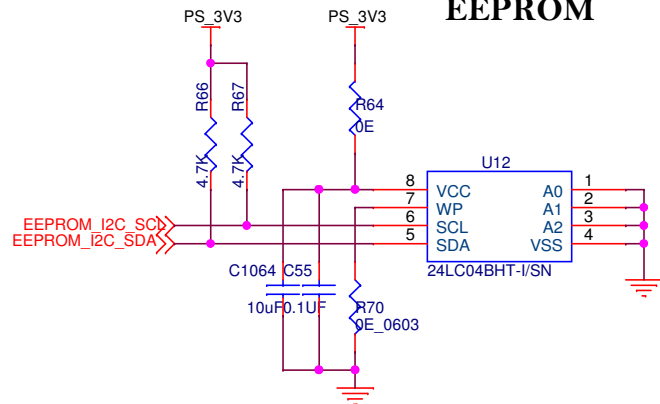
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Designed by : LAVANYA.B			Title CONFIGURATION	
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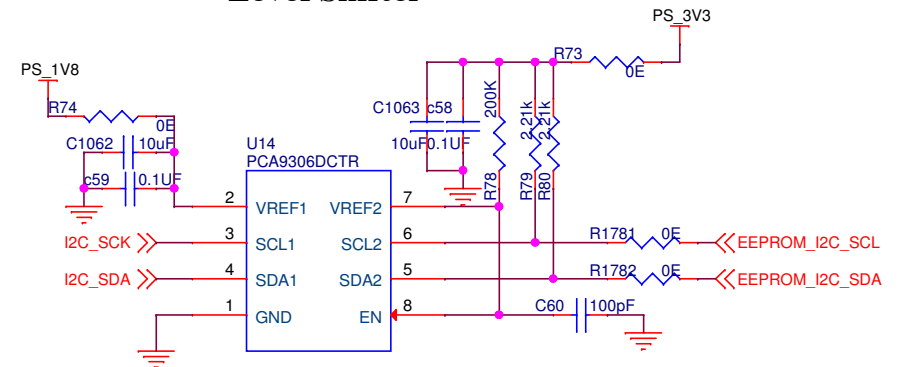
User Flash



EEPROM

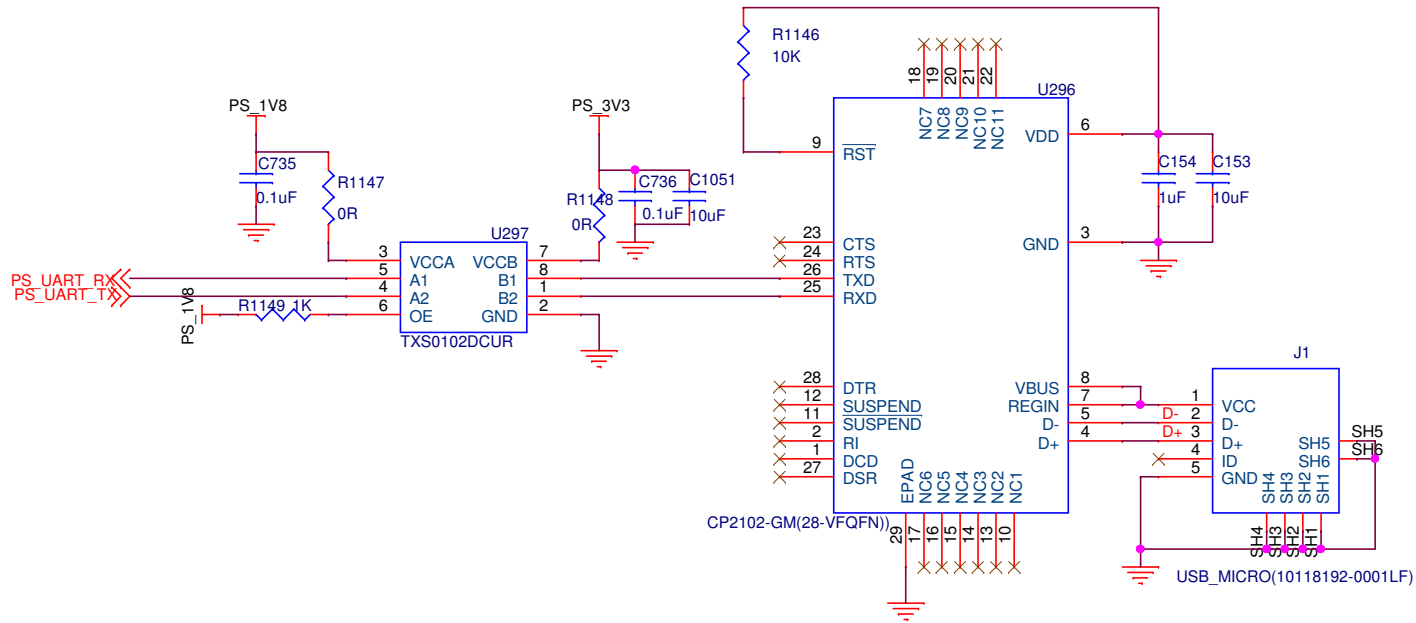


Level Shifter



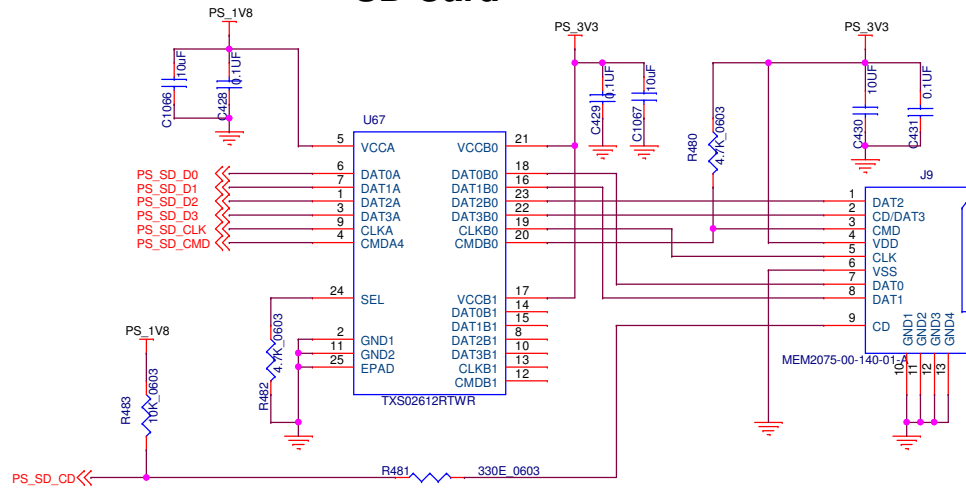
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Designed by : LAVANYA.B			Title User Flash & EEPROM	
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PS USB UART

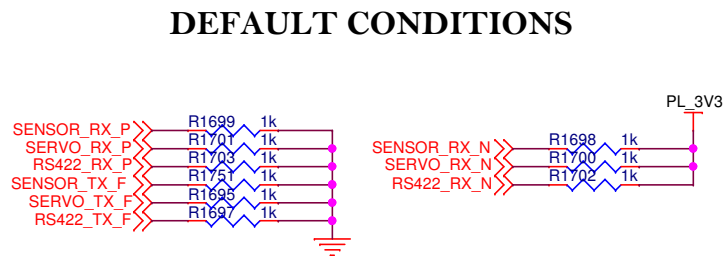
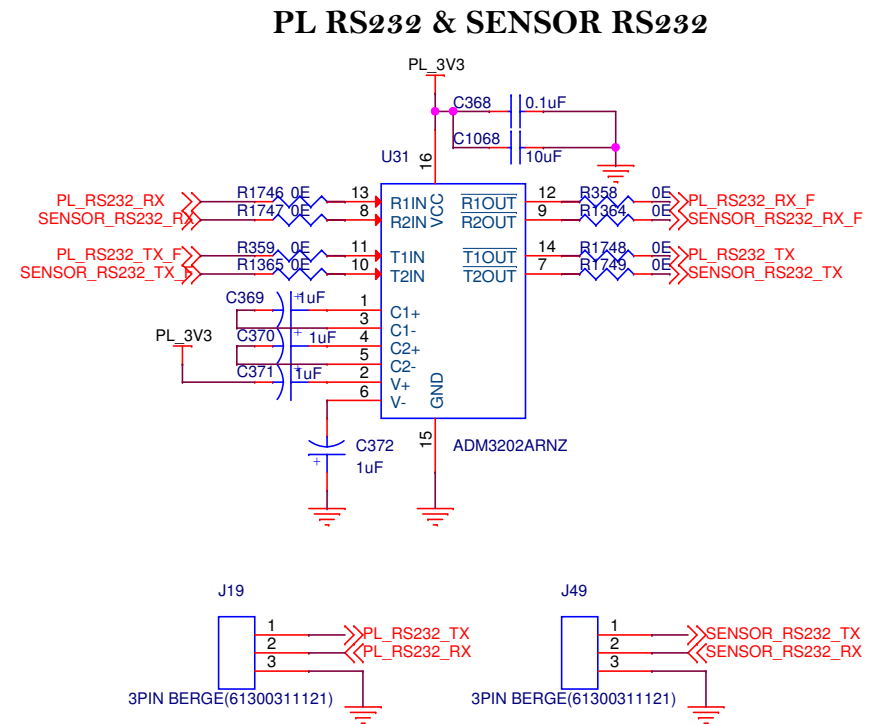
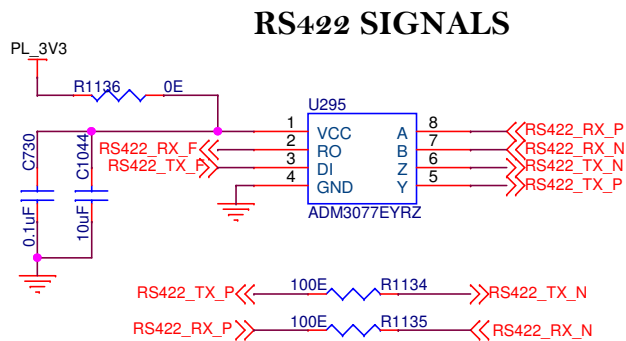
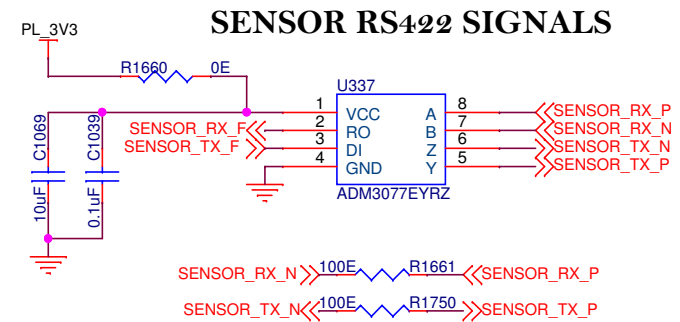
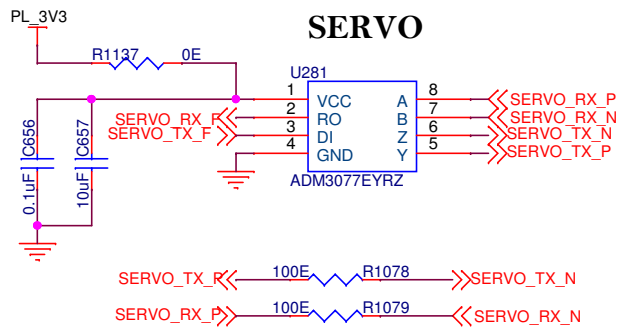


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SD Card

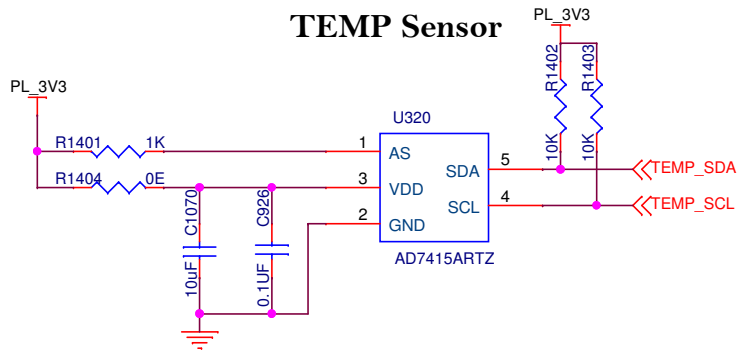


Date		Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD	
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Verified by :	NARESH N		SD CARD	
Aproved by :	NARESH N		Size B	Document Number
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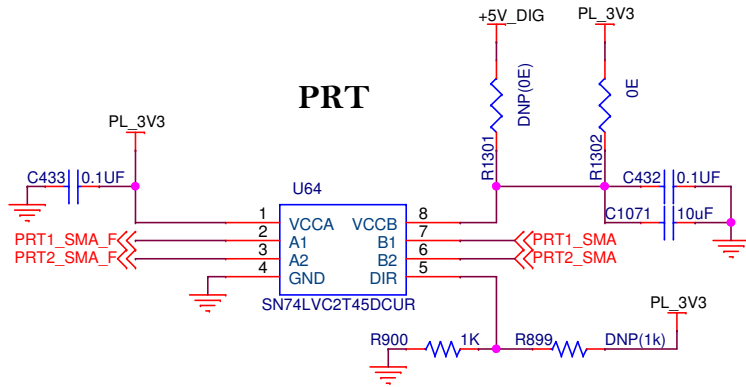


	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title	Sensor & RS422 & RS232 Ckts	
Verified by : NARESH N			Size A4	Document Number	Rev 1.0
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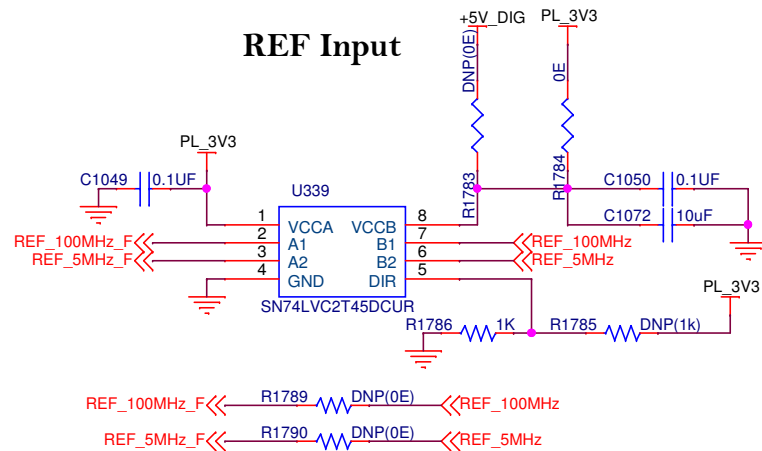
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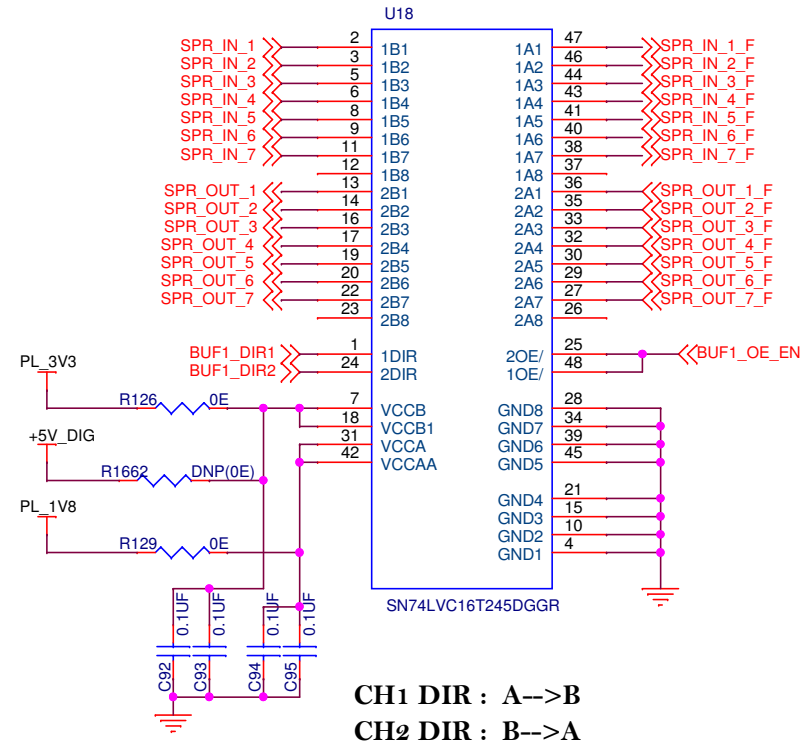
PRT



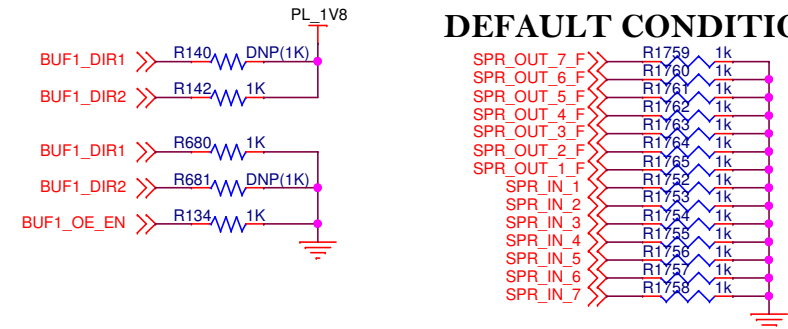
REF Input



Spare IO Signals

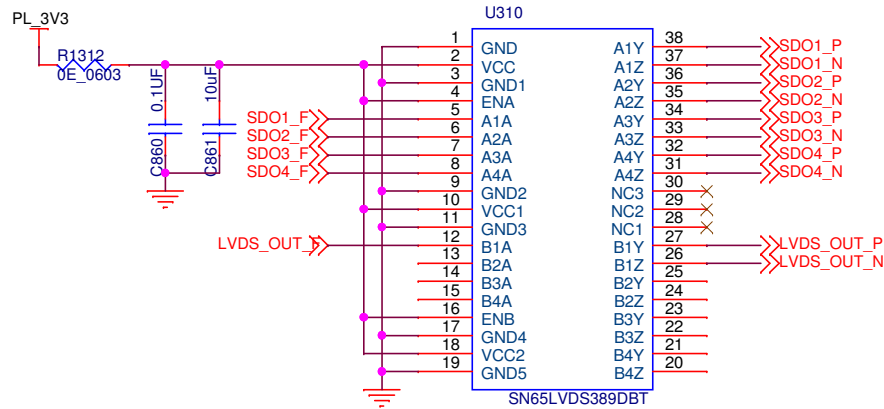
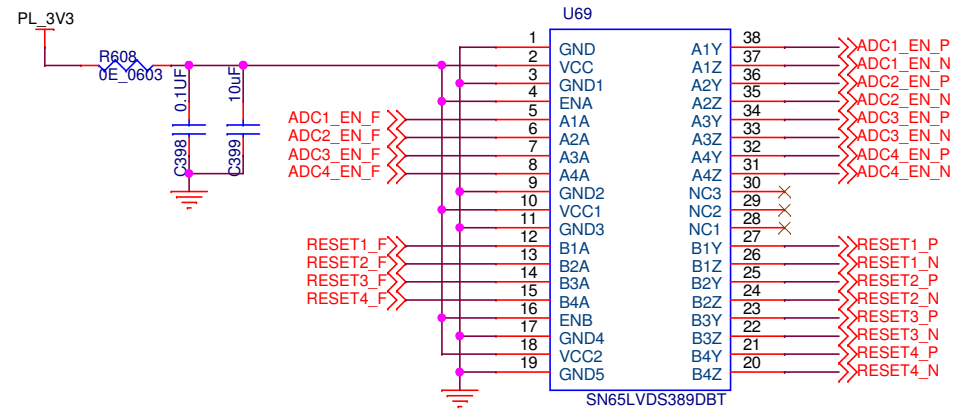
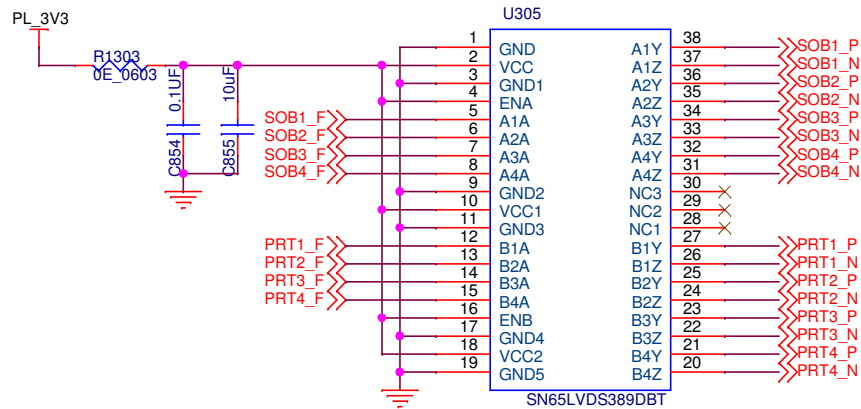


DEFAULT CONDITIONS

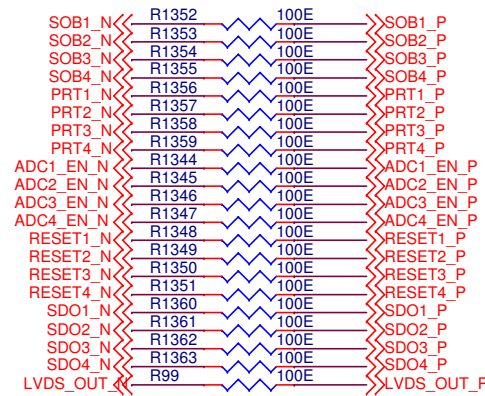


	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD	
Designed by : LAVANYA.B			Title CONTROL SIGNALS	
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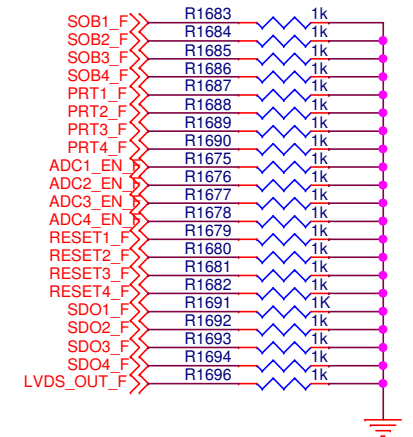
LVDS Output Signals



Termination Resistors

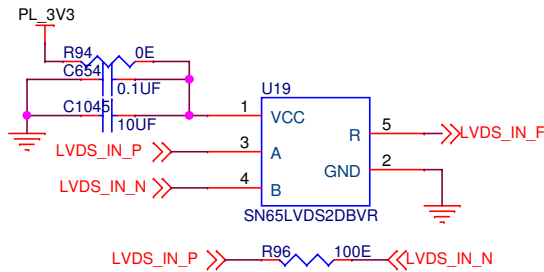
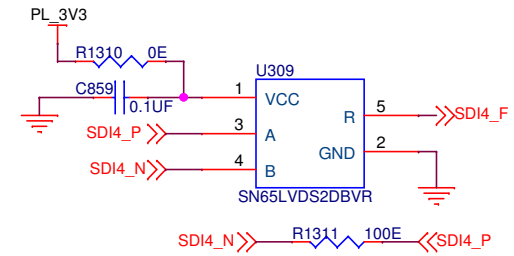
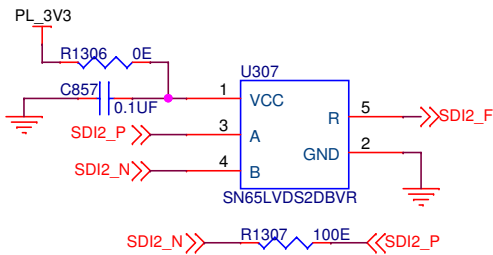
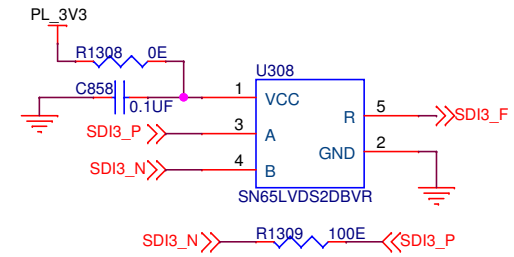
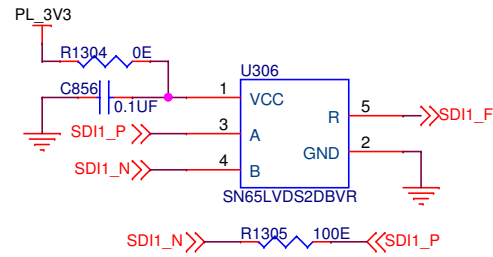


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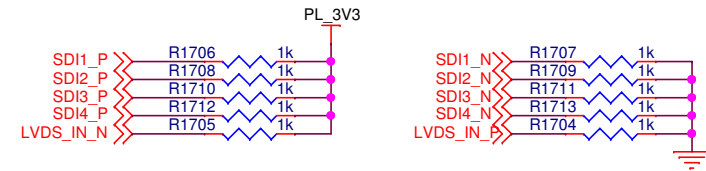


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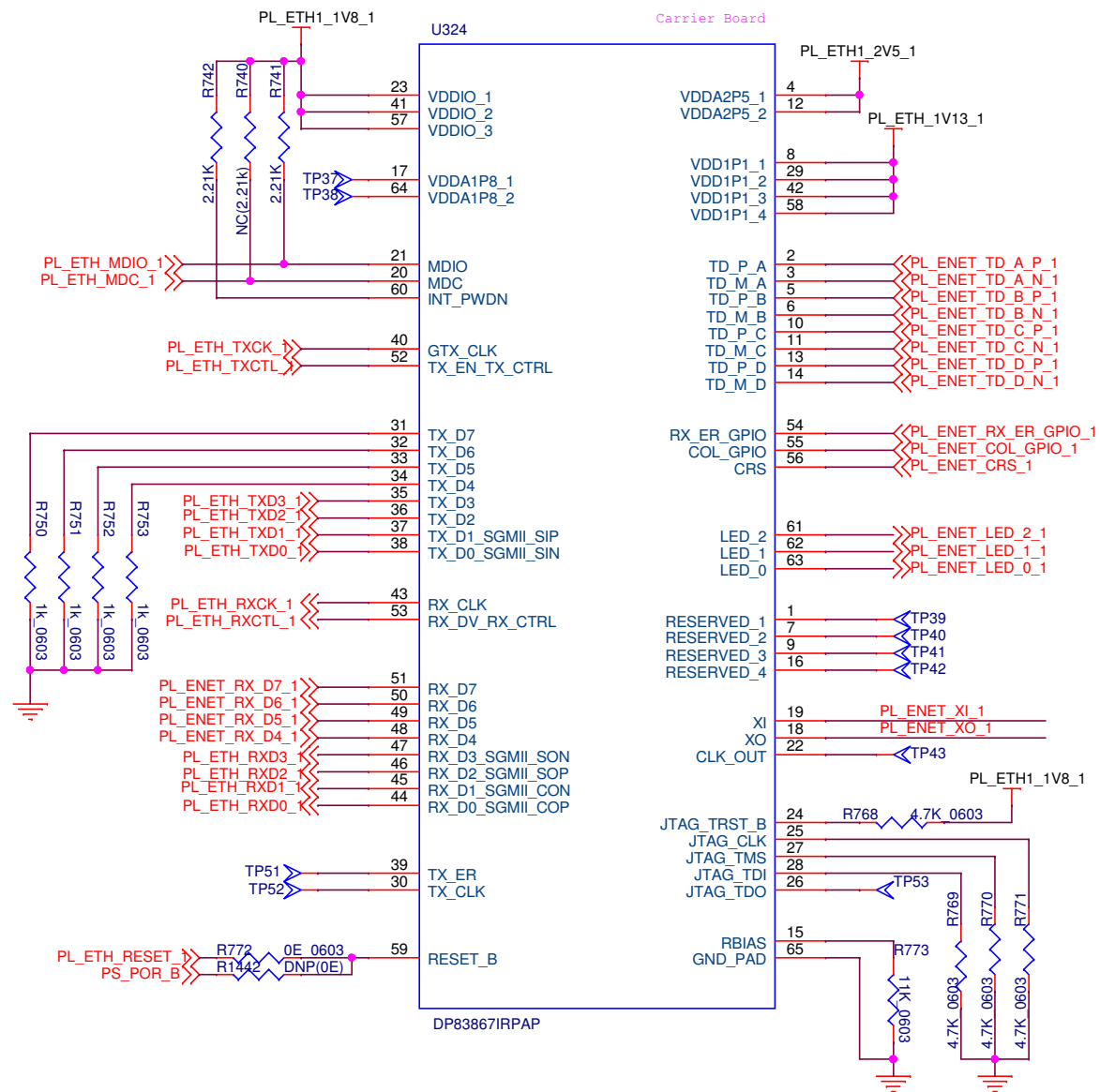
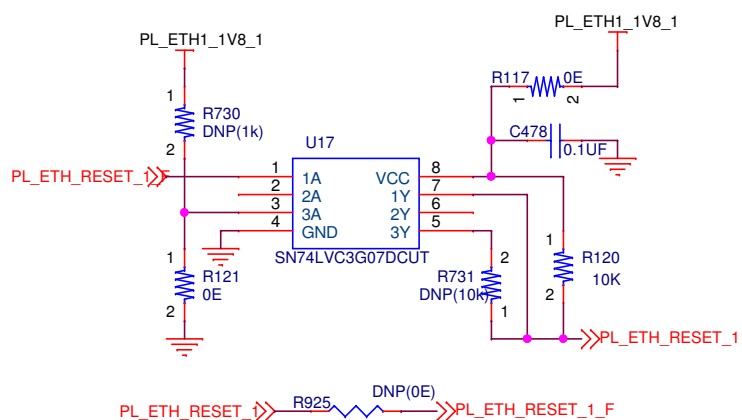
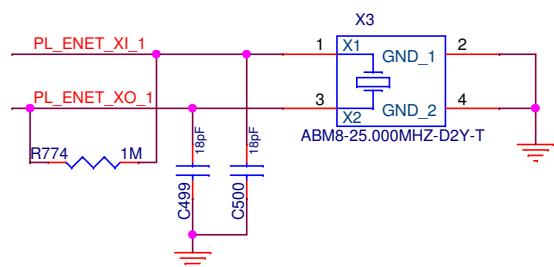
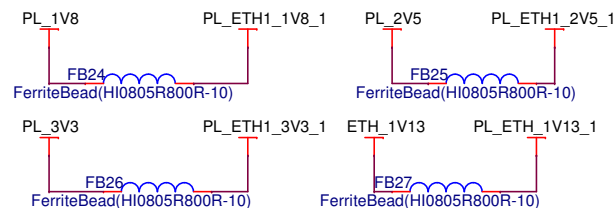
LVDS Input Signals



Default Conditions

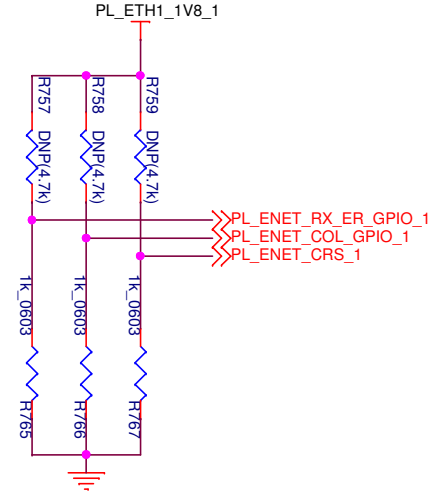
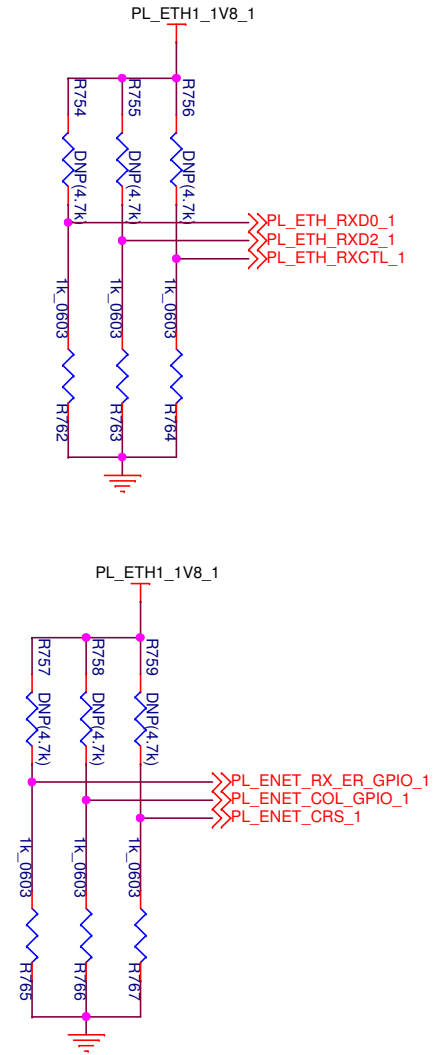
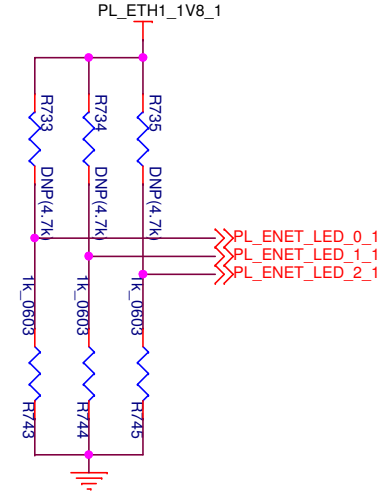
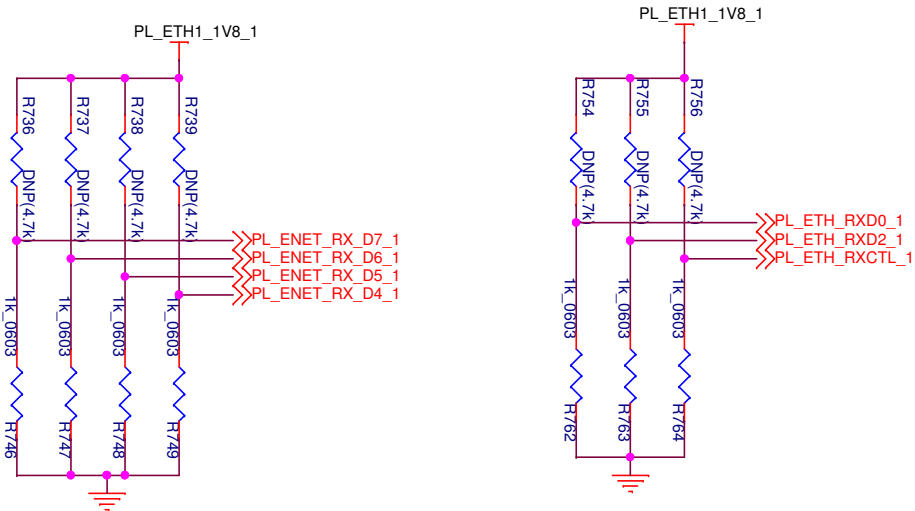
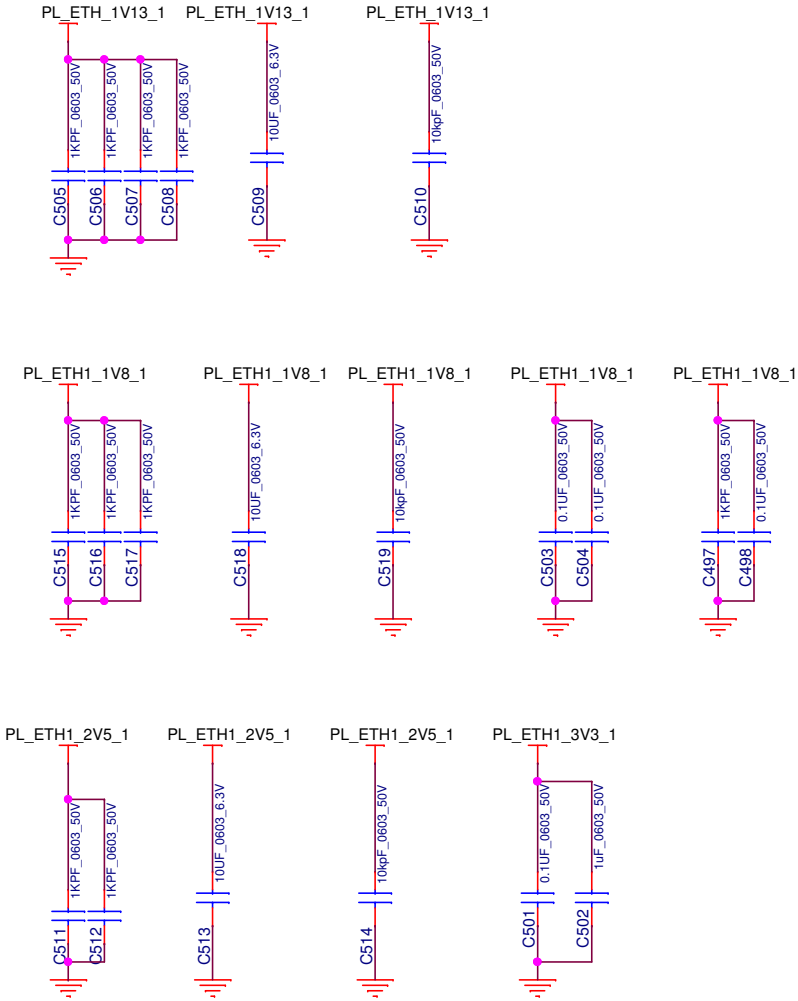


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Designed by : LAVANYA.B			Title LVDS Input Signals	
Verified by : NARESH N			Size A4	Document Number
Approved by : NARESH N			SP CARD	
		Date: Tuesday, June 20, 2023	Sheet 22	of 50
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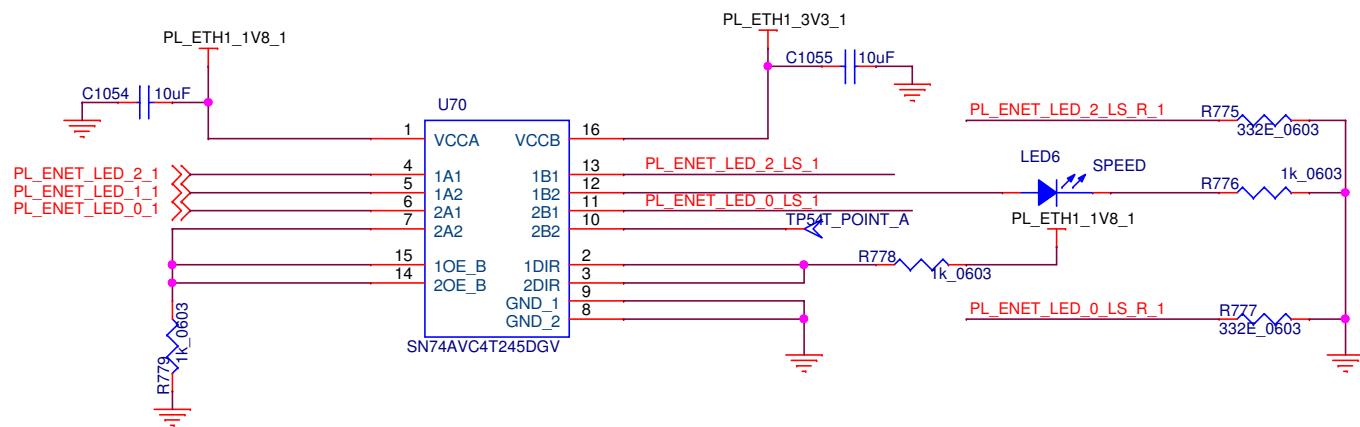
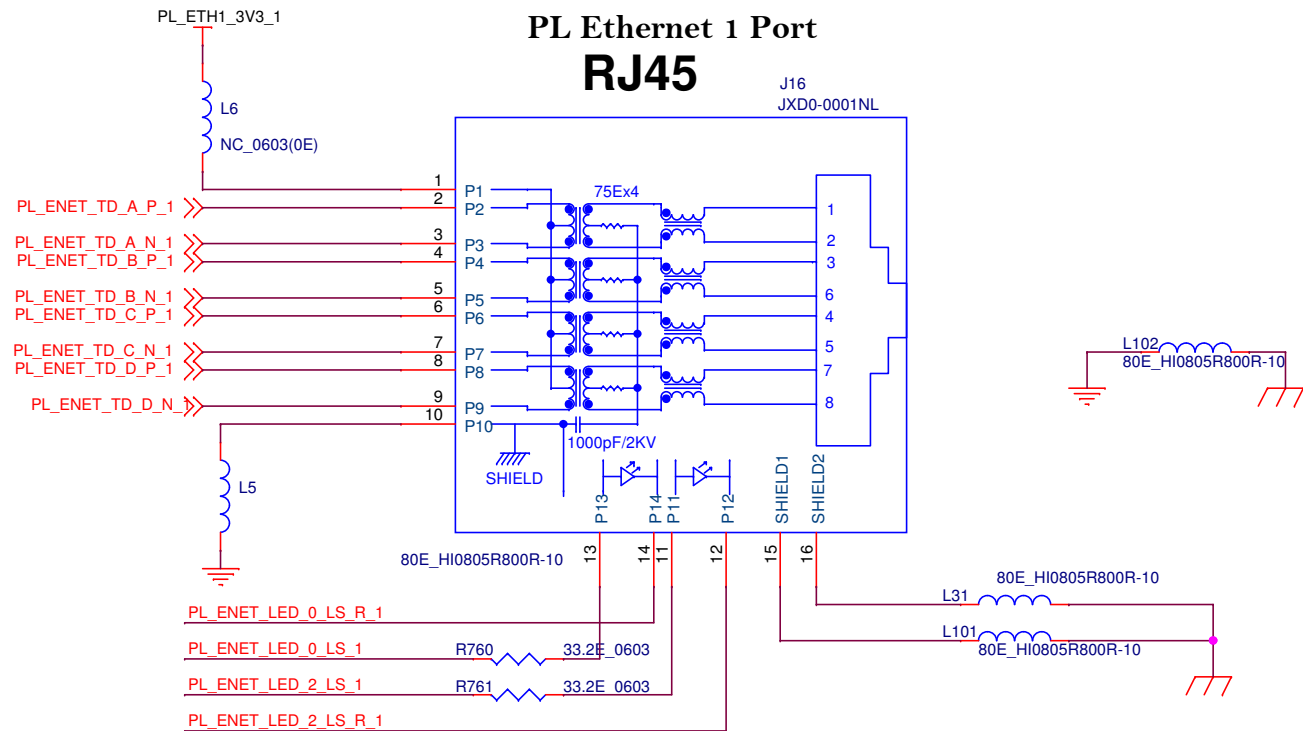


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Designed by : LAVANYA.B				Title	PL Gigabit PHY1 CKT	
Verified by : NARESH N				Size A4	Document Number	Rev 1.0
Approved by : NARESH N				SP CARD		
				Date:	Tuesday, June 20, 2023	Sheet 23 of 50

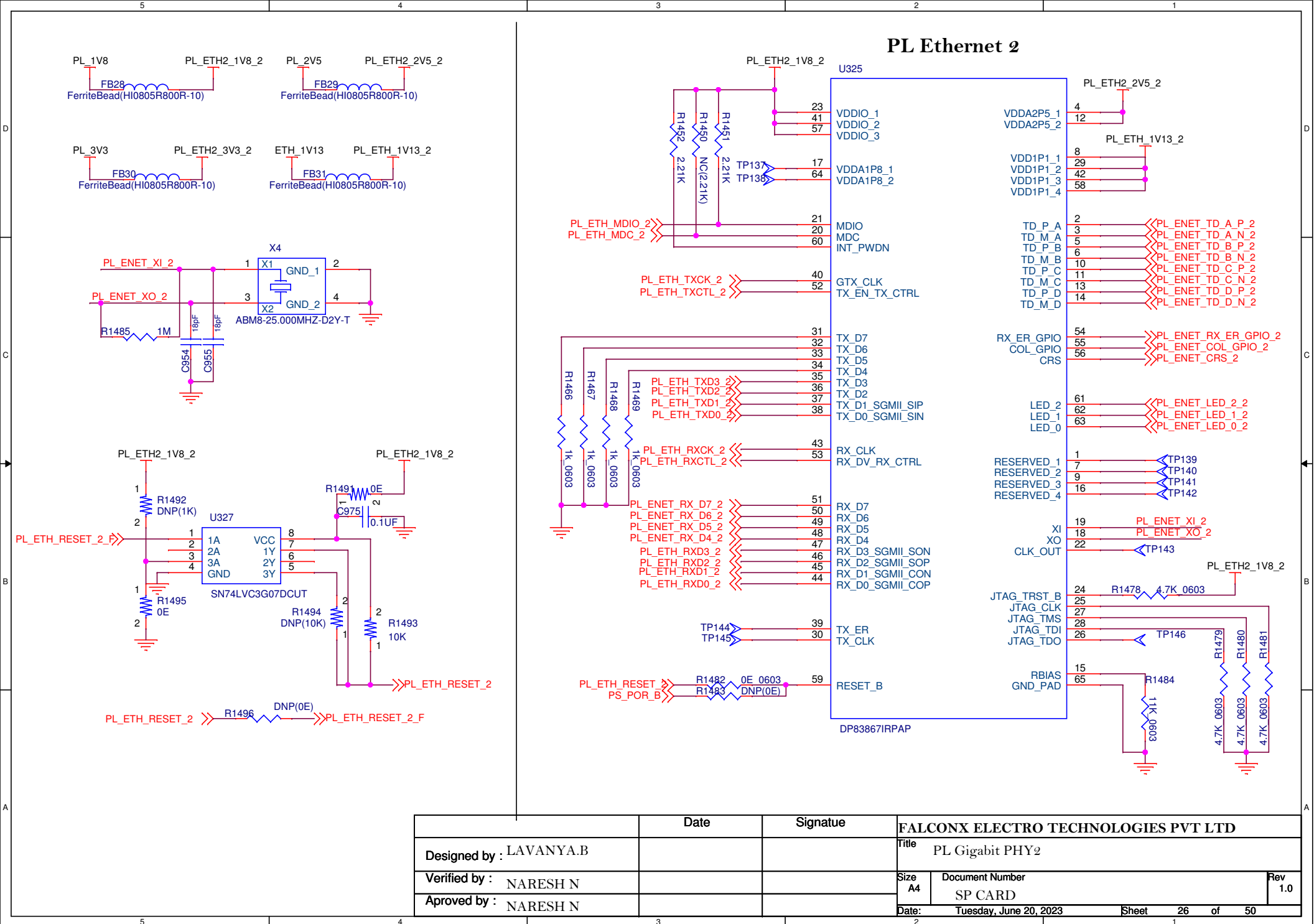
PL Ethernet1 Decaps



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Designed by : LAVANYA.B			Title PL Gigabit PHY1 Decaps	
Verified by : NARESH N			Size A4	Document Number
Approved by : NARESH N			SP CARD	
		Date: Tuesday, June 20, 2023	Sheet 24	of 50



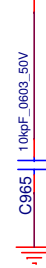
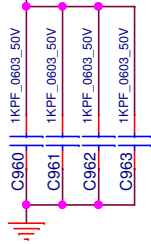
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Designed by : LAVANYA.B			Title PL Gigabit PHY1 RJ45 Jack		
Verified by : NARESH N			Size A4	Document Number	Rev 1.0
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			Date: Tuesday, June 20, 2023	Sheet 25 of 50	



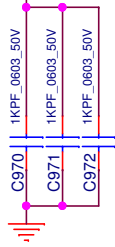
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			Date: Tuesday, June 20, 2023	Sheet 26 of 50

PL Ethernet2 Decaps

PL_ETH_1V13_2 PL_ETH_1V13_2 PL_ETH_1V13_2



PL_ETH2_1V8_2



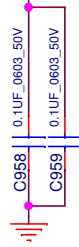
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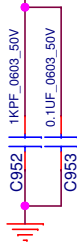
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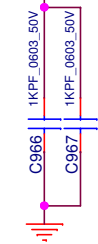
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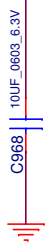
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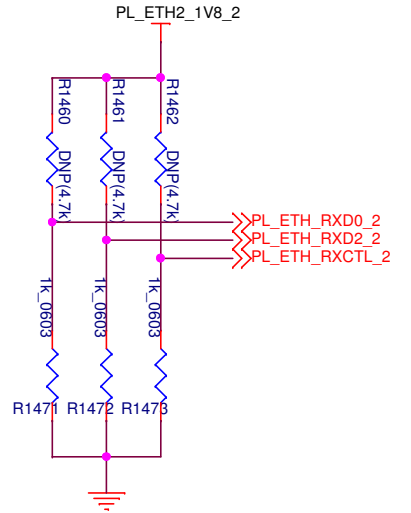
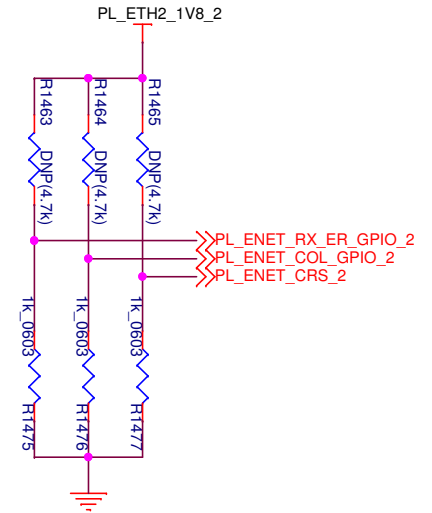
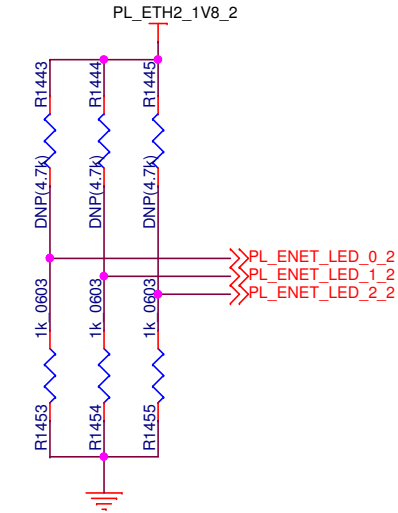
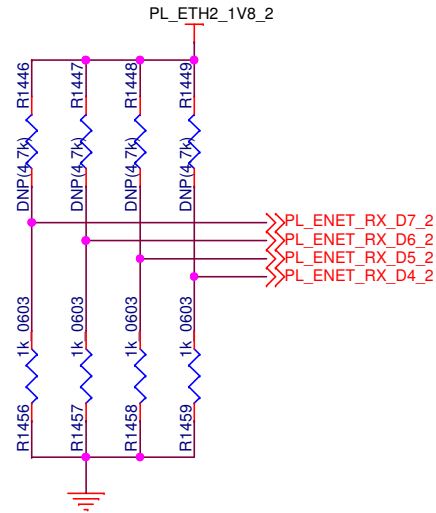
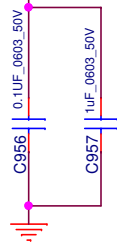
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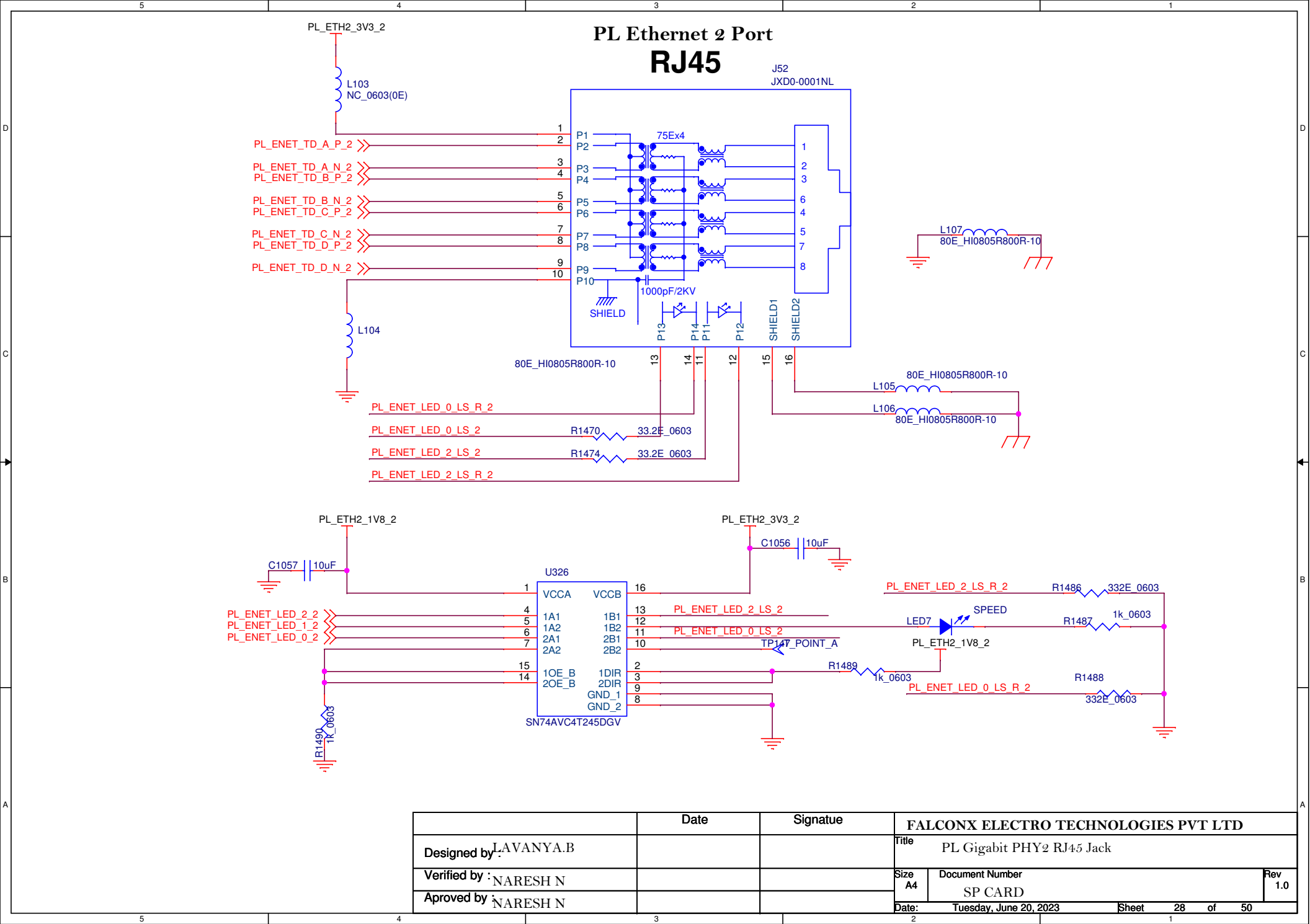
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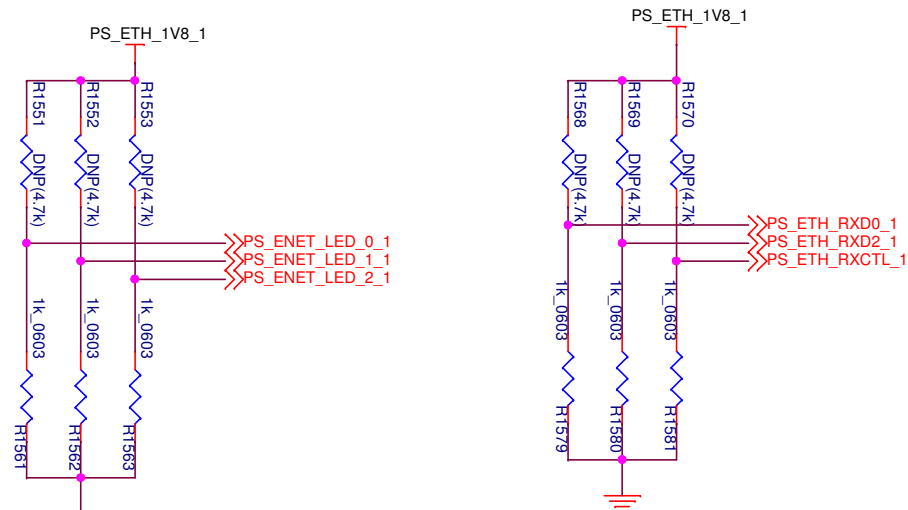
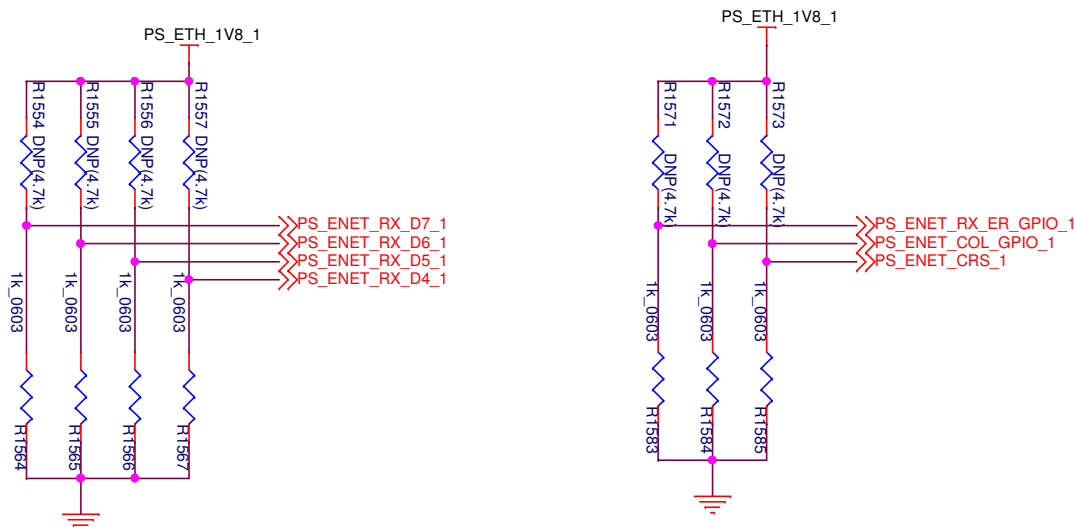
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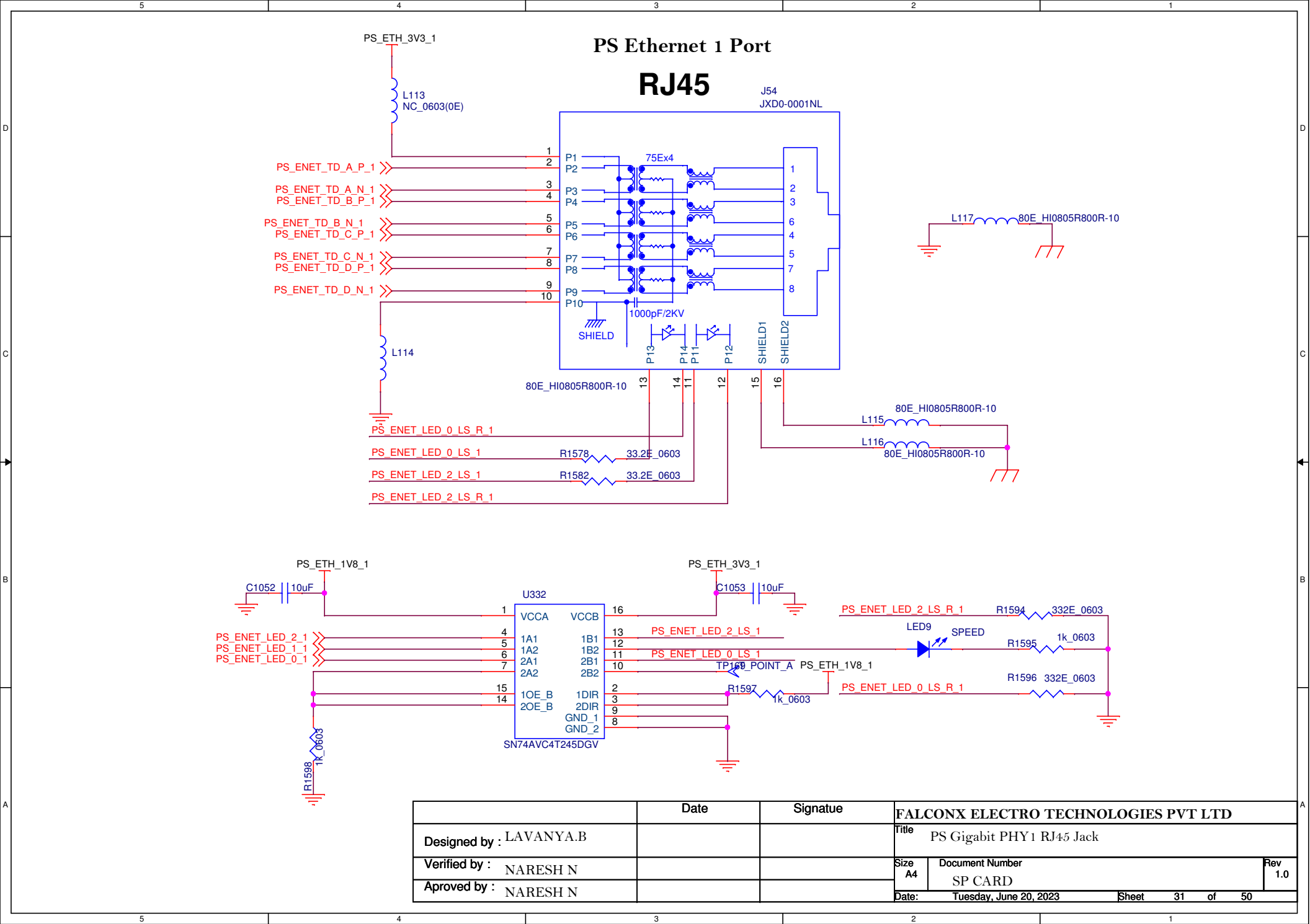
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Designed by : LAVANYA.B			Title PL Gigabit PHY2 Decaps	
Verified by : NARESH N			Size A4	Document Number
Aproved by : NARESH N			SP CARD	
			Date: Tuesday, June 20, 2023	Sheet 27 of 50
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Aproved by : NARESH N			Date: Tuesday, June 20, 2023 Sheet 28 of 50		

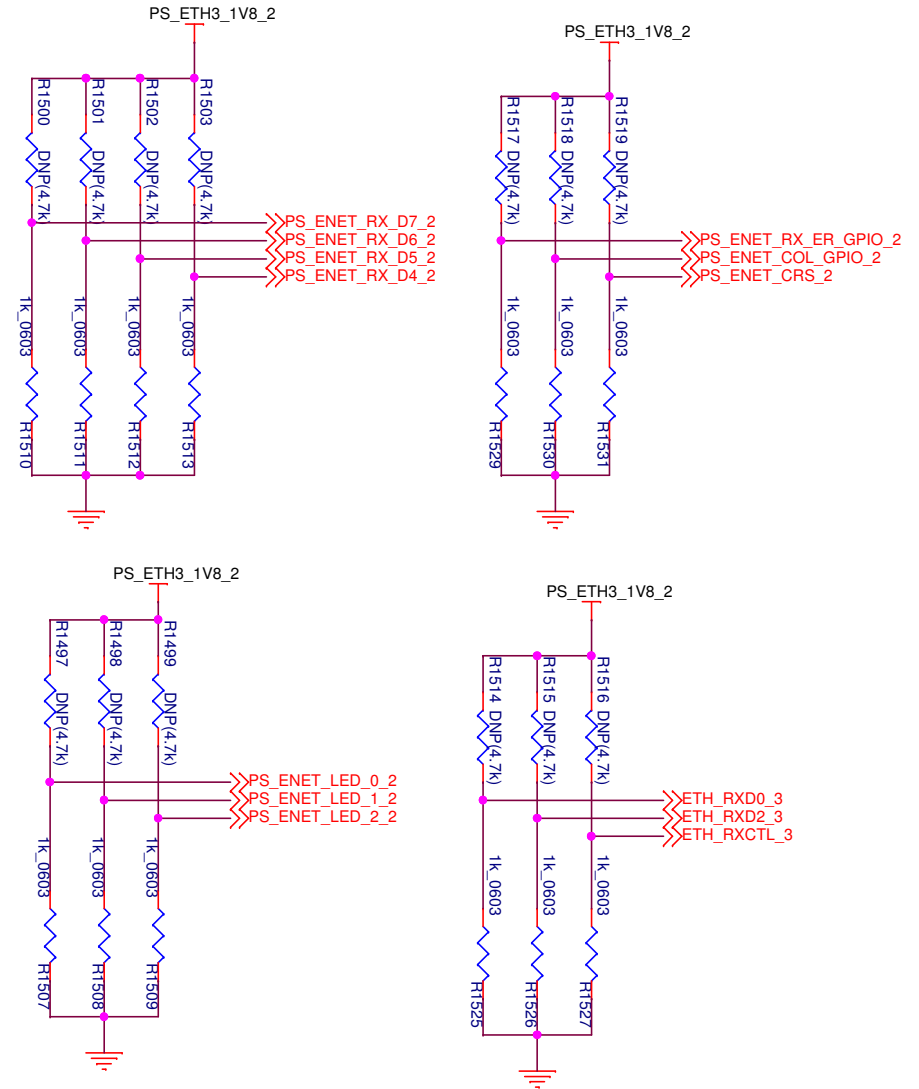
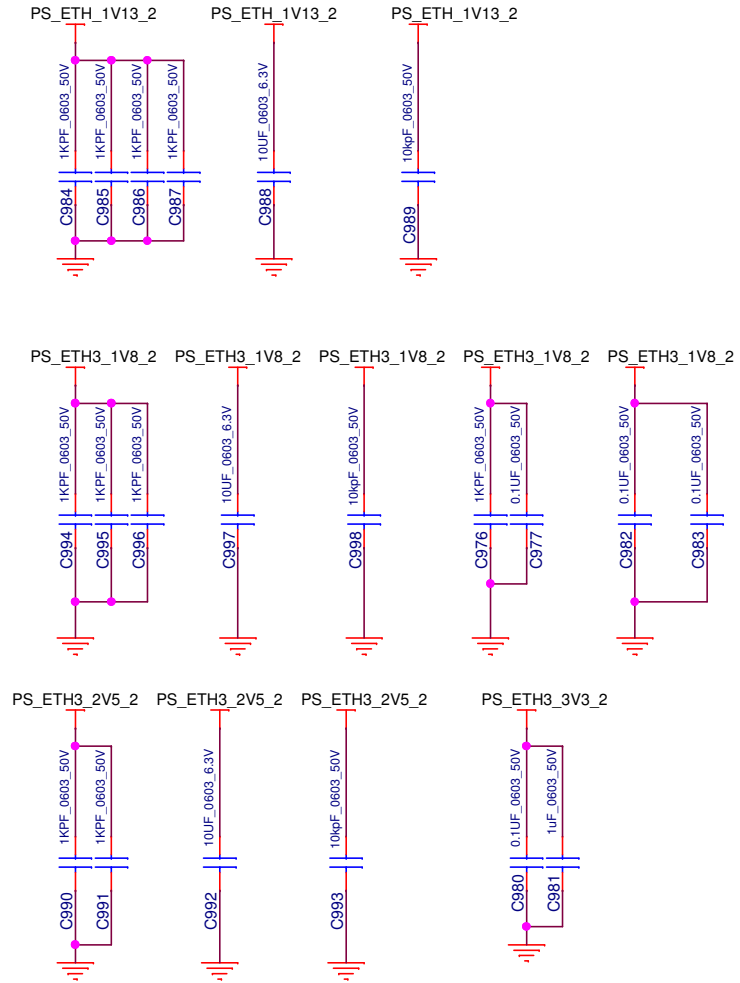


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Verified by : NARESH N			Size A4	Document Number SP CARD	Rev 1.0
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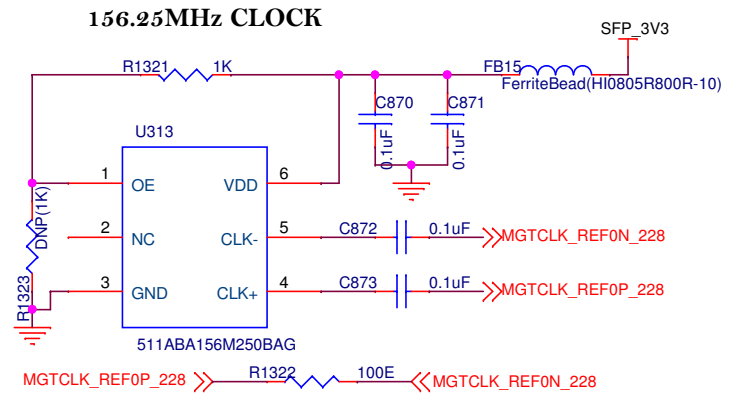
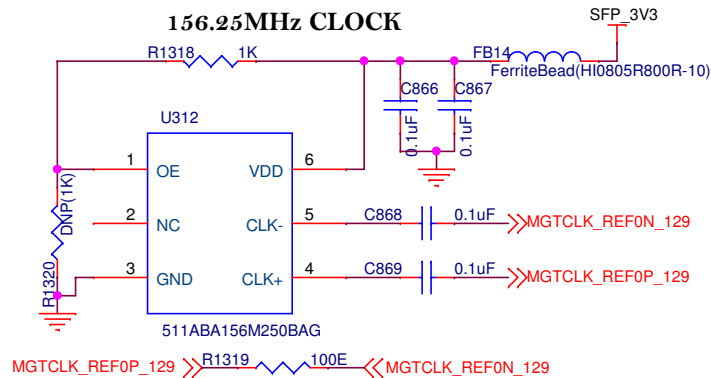
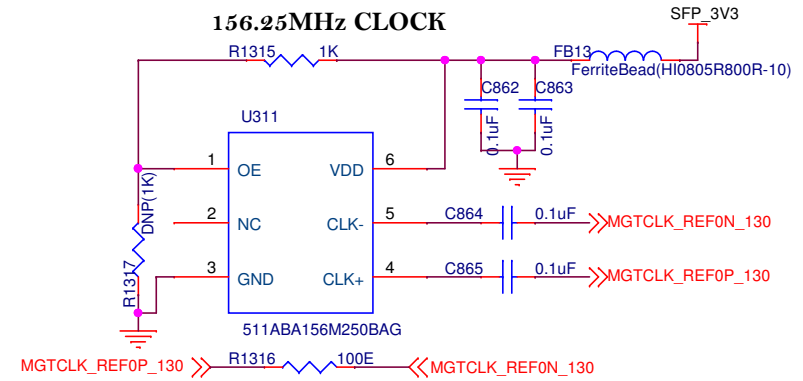
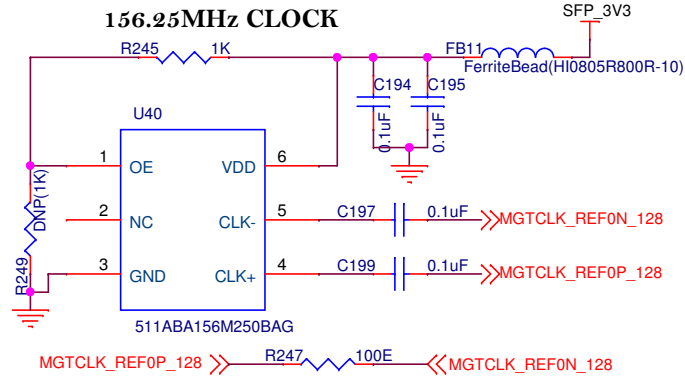
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Designed by : LAVANYA.B			Title PS Gigabit PHY1 RJ45 Jack		
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PS Ethernet 2 Decaps



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			Date: Tuesday, June 20, 2023	Sheet 33	of 50		

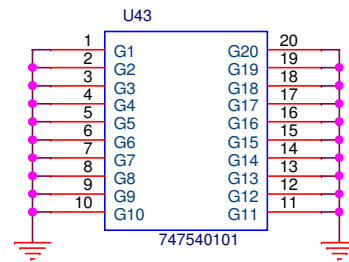
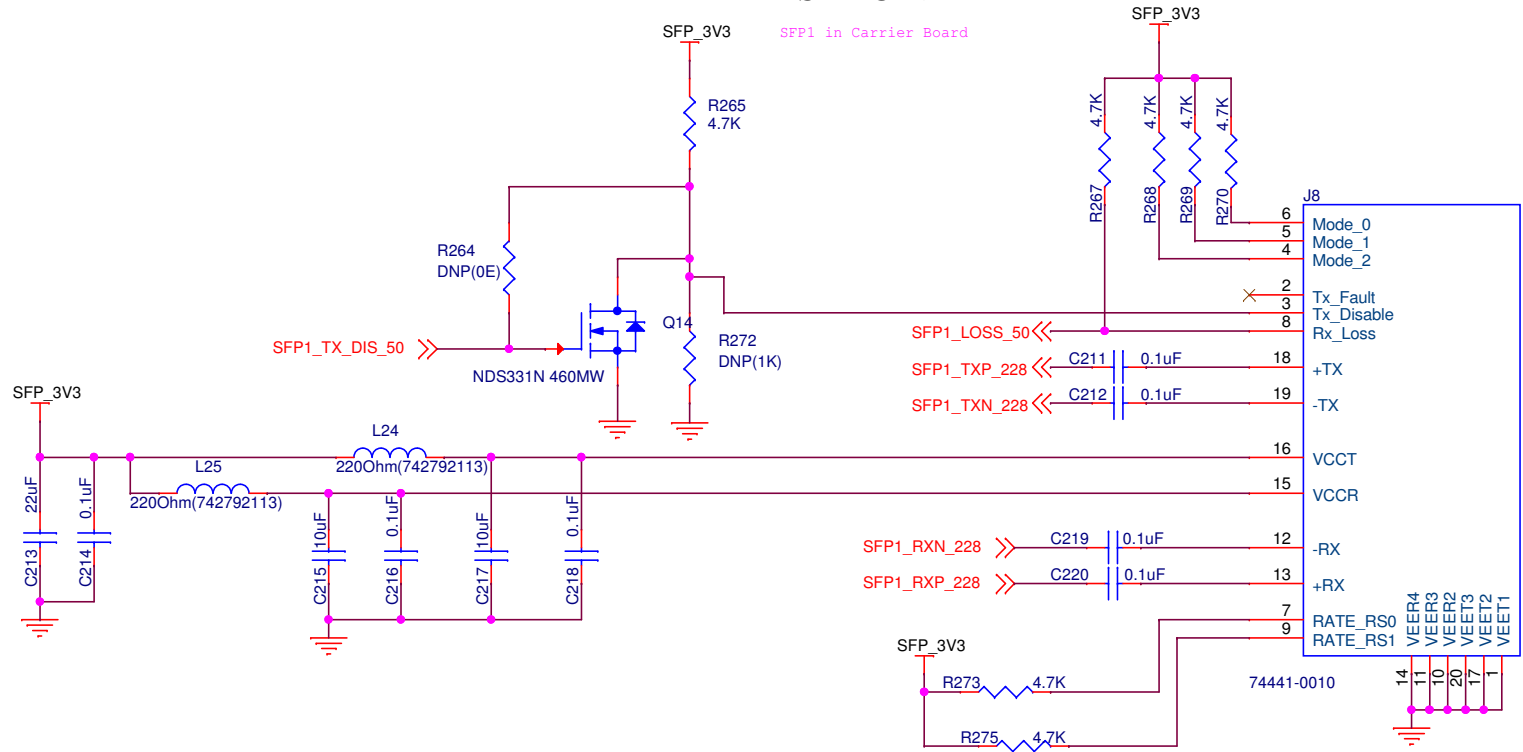
SFP CLOCK CKT



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Designed by : LAVANYA.B			Title SFP CLOCK		
Verified by : NARESH N			Size A4	Document Number SP CARD	Rev 1.0
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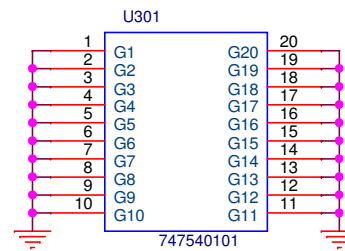
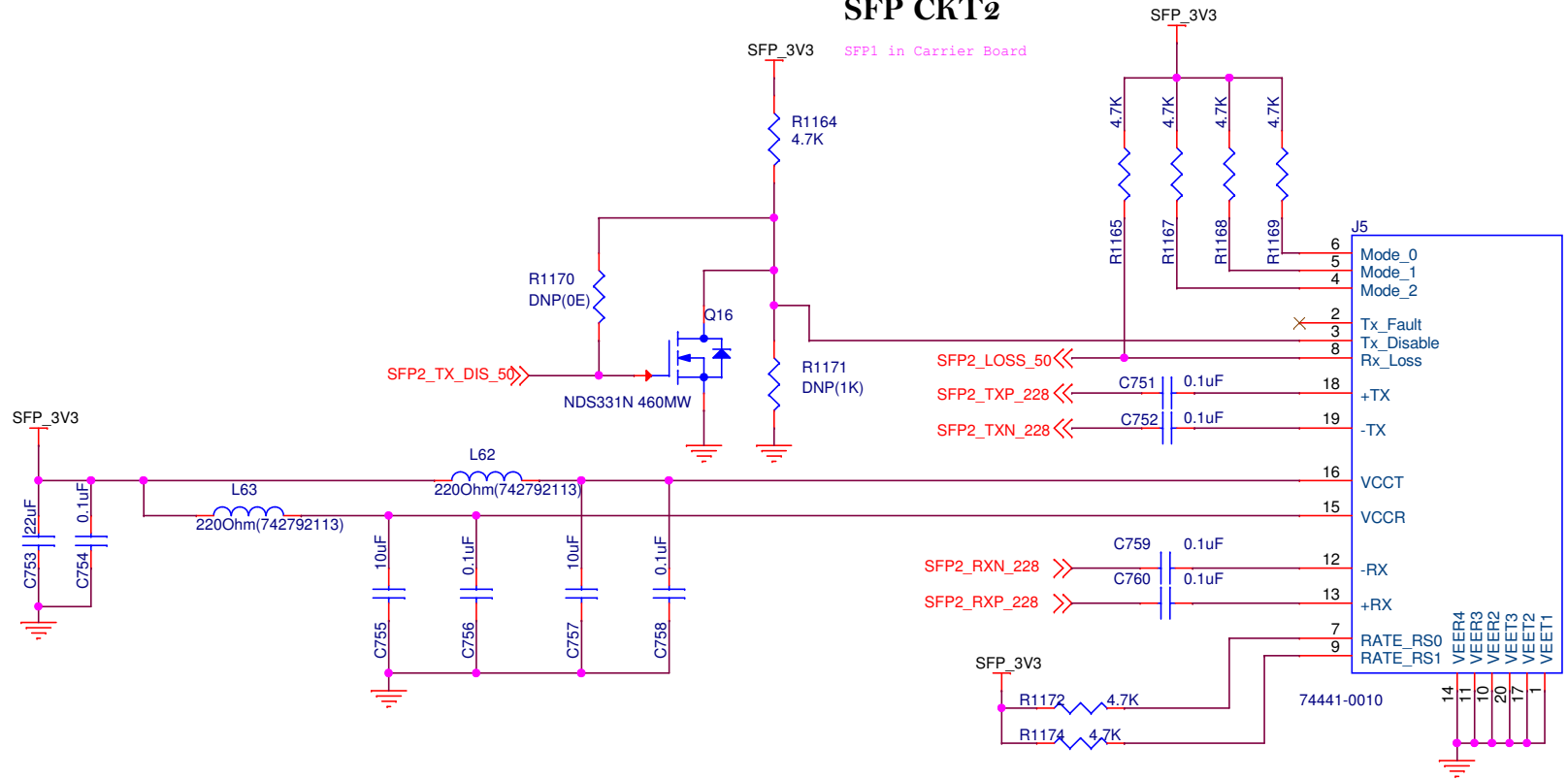
SFP CKT1

SFP1 in Carrier Board



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Designed by : LAVANYA.B			Title SFP CKT	
Verified by : NARESH N			Size A4	Document Number
Approved by : NARESH N			SP CARD	
		Date: Tuesday, June 20, 2023	Sheet 36	of 50
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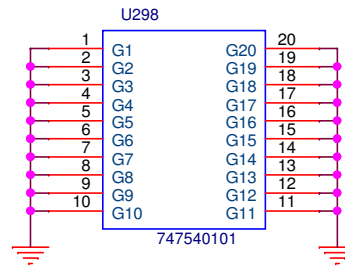
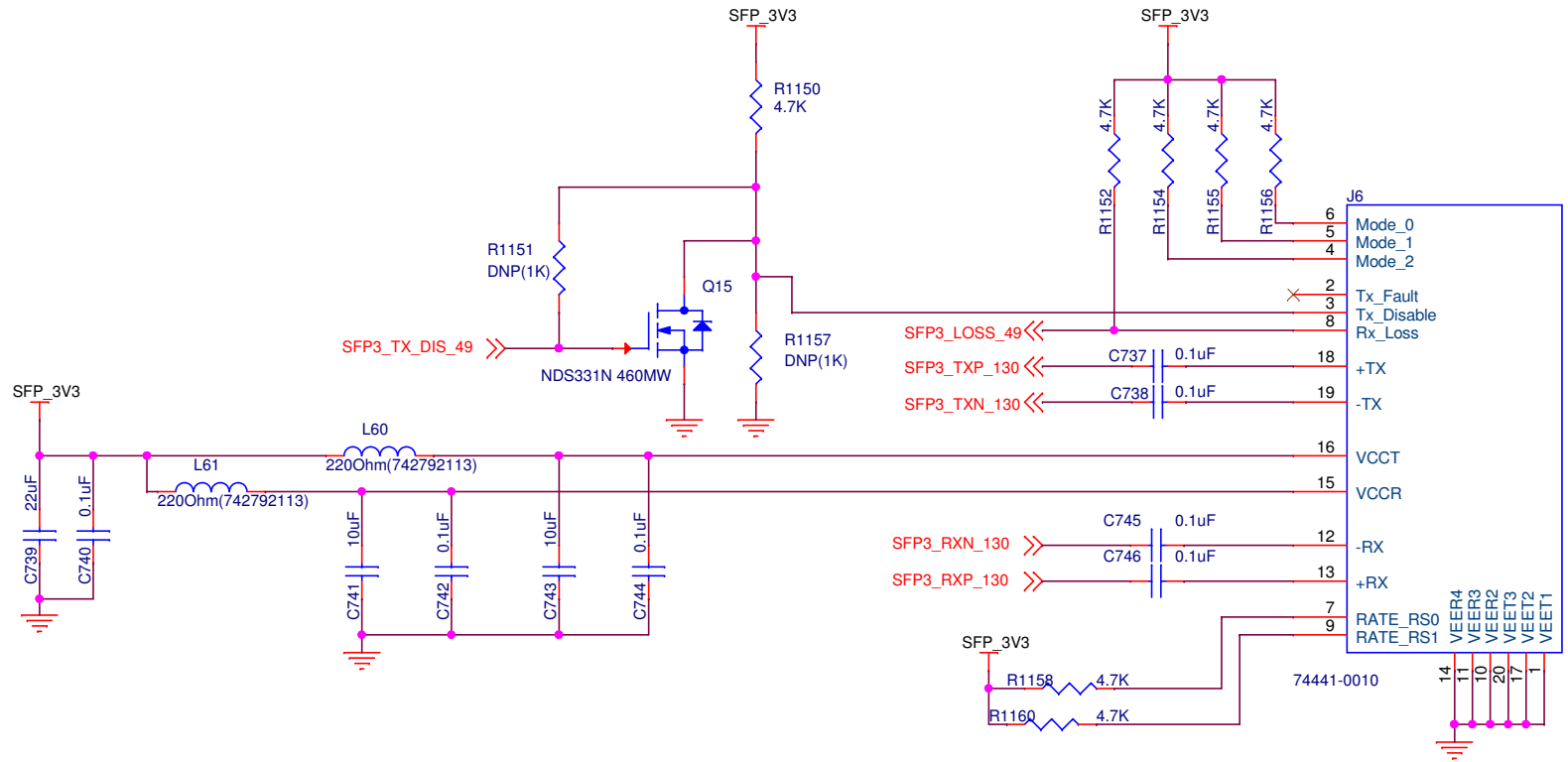
SFP CKT2



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		Date: Tuesday, June 20, 2023	Sheet 37	of 50

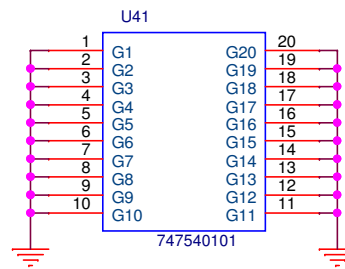
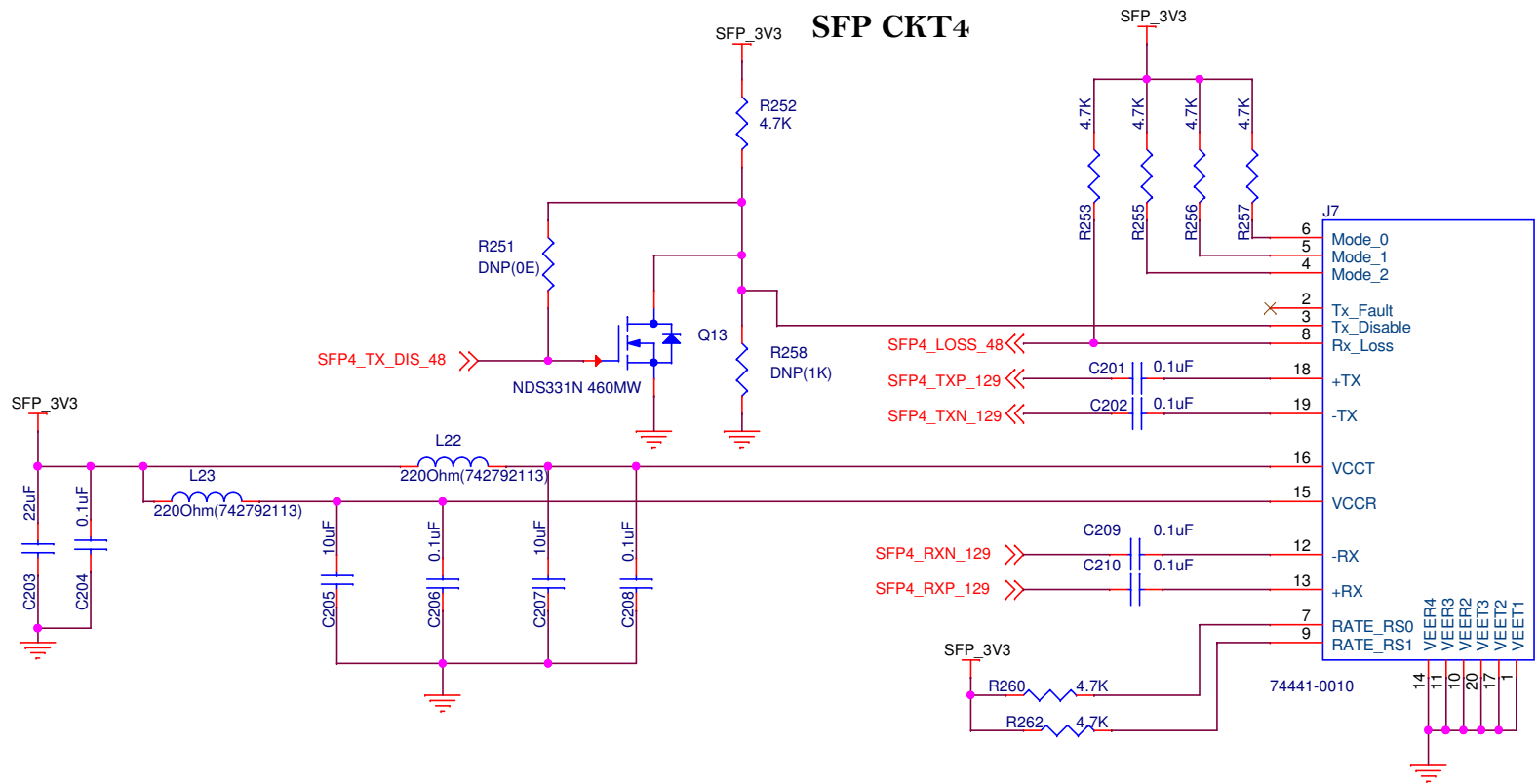
Rev 1.0

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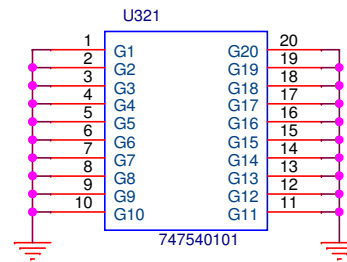
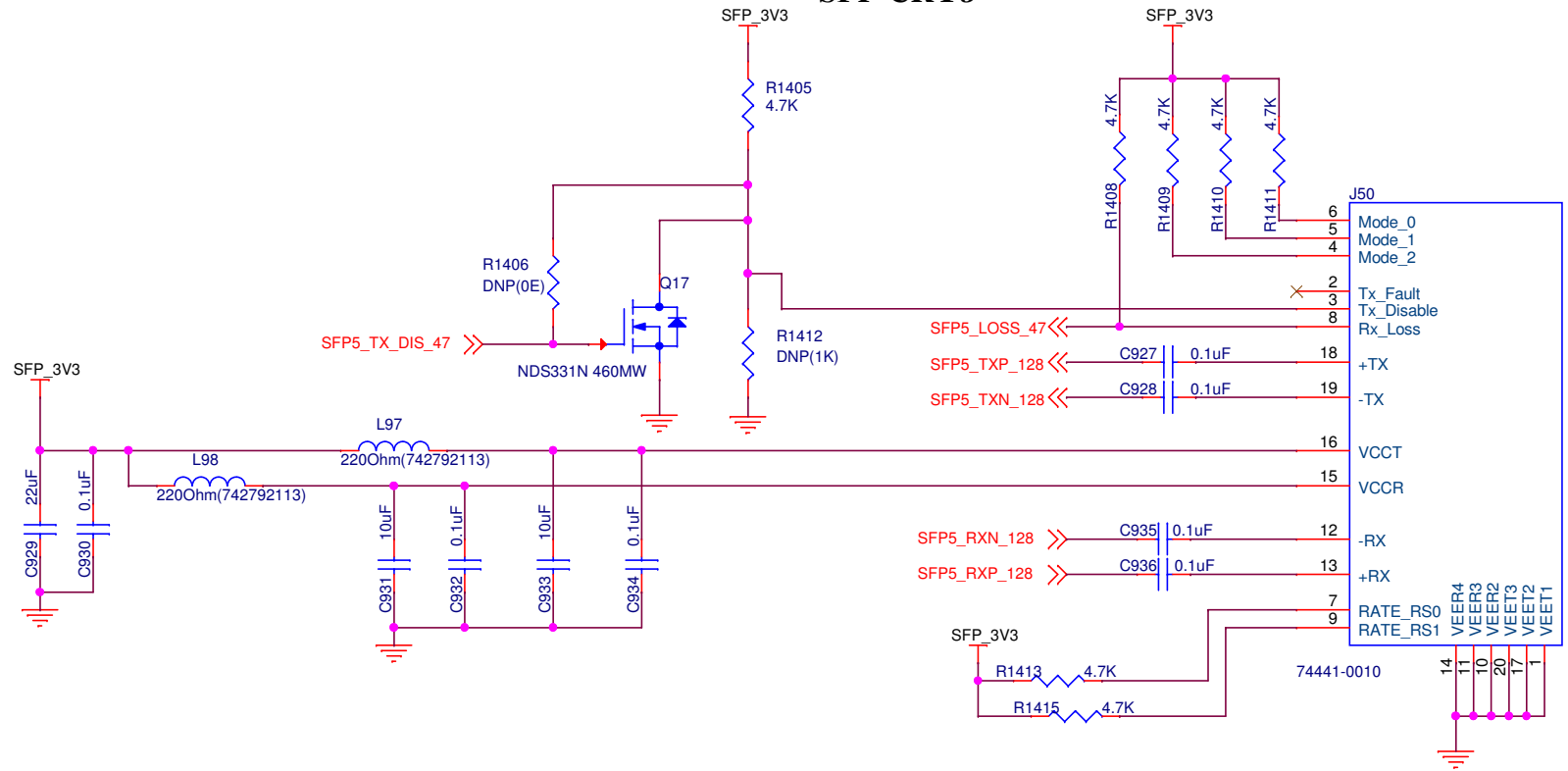
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Designed by : LAVANYA.B			Title SFP CKT	
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Approved by : NARESH N			Date: Tuesday, June 20, 2023	Sheet 38 of 50

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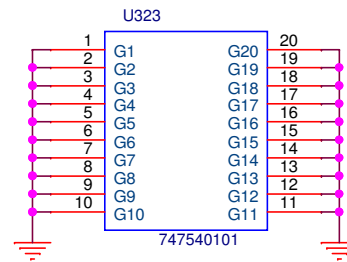
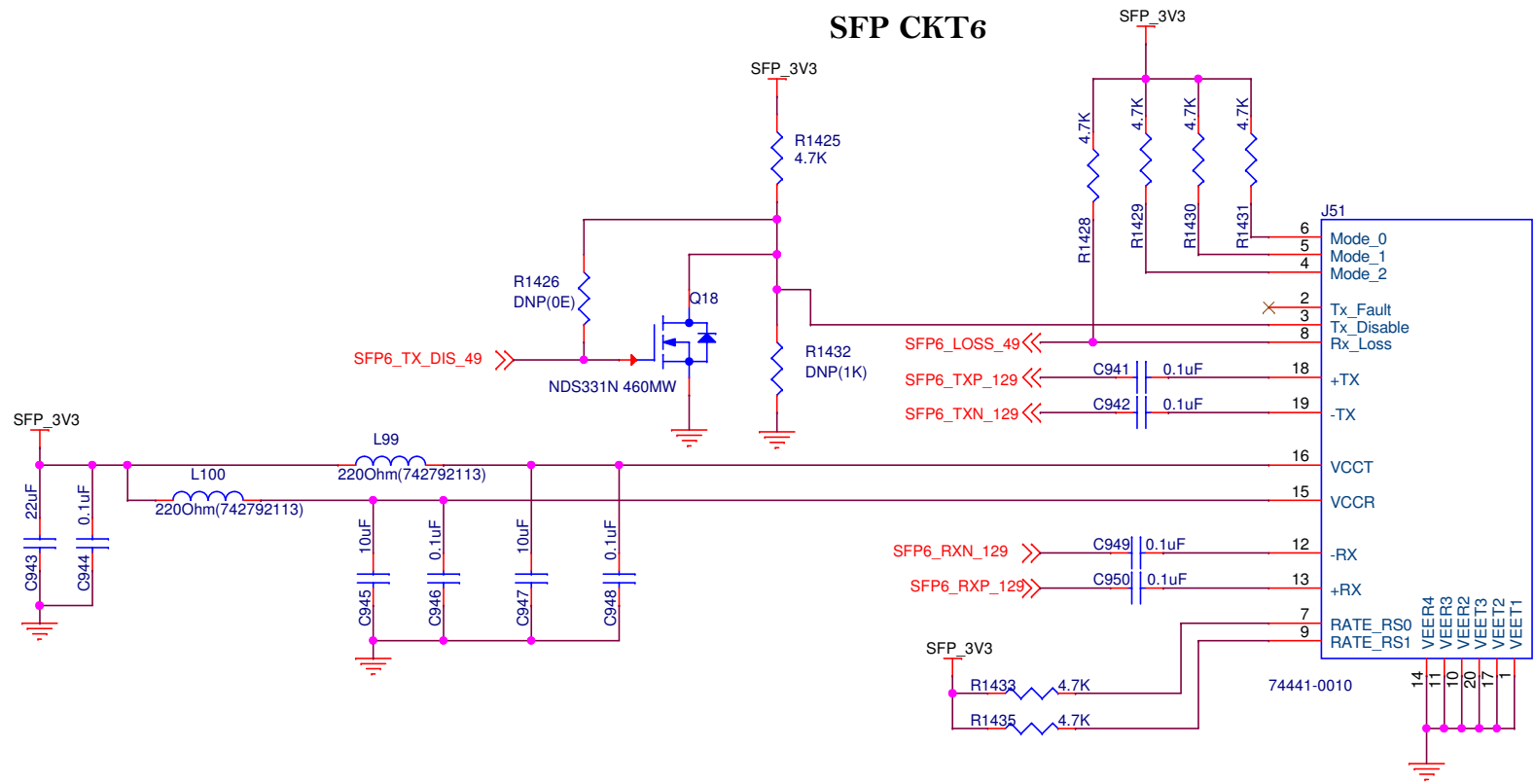
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Designed by : LAVANYA.B			Title SFP CKT	
Verified by : NARESH N			Size A4	Document Number SP CARD
Approved by : NARESH N			Date: Tuesday, June 20, 2023	Rev 1.0

SFP CKT5



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Designed by : LAVANYA.B			Title SFP CKT	
Verified by : NARESH N			Size A4	Document Number
Approved by : NARESH N			SP CARD	
Date: Tuesday, June 20, 2023		Sheet	40	of 50
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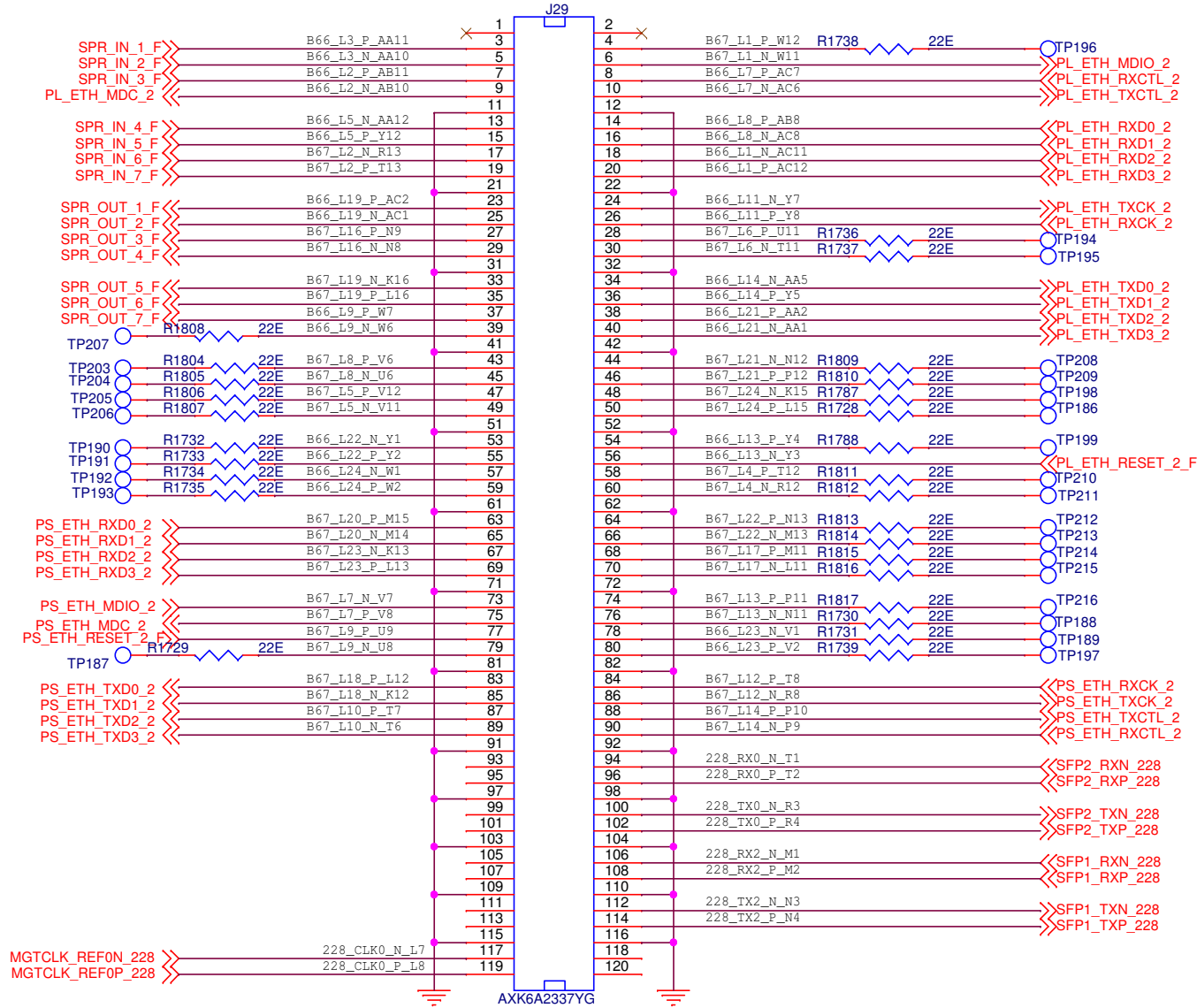
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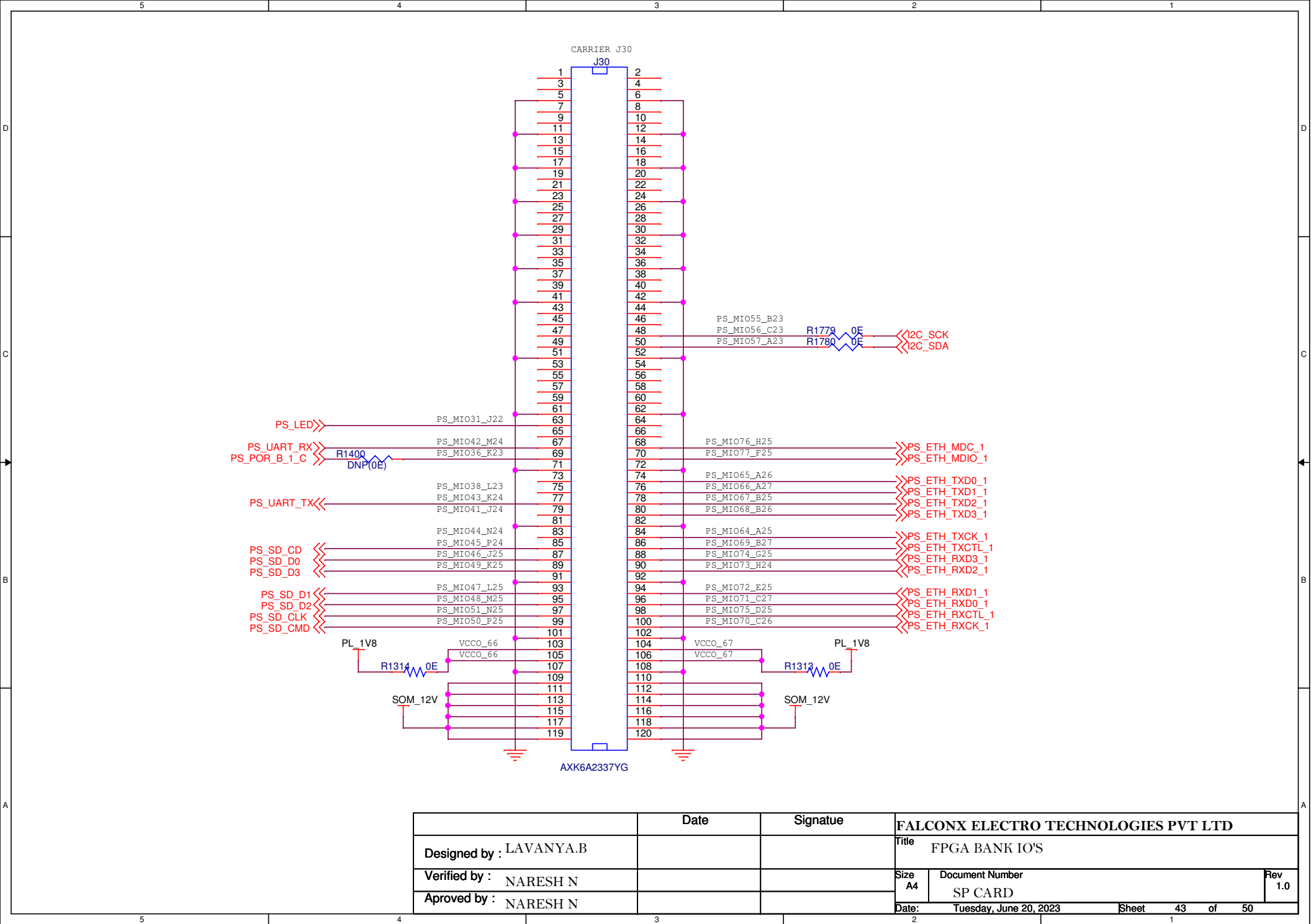
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Verified by : NARESH N			Size A4	Document Number
Approved by : NARESH N			SP CARD	
Date: Tuesday, June 20, 2023		Sheet	41	of 50
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B44,B50 is 3.3V IOs
B67,B66 is 1.8V(Default) IOs

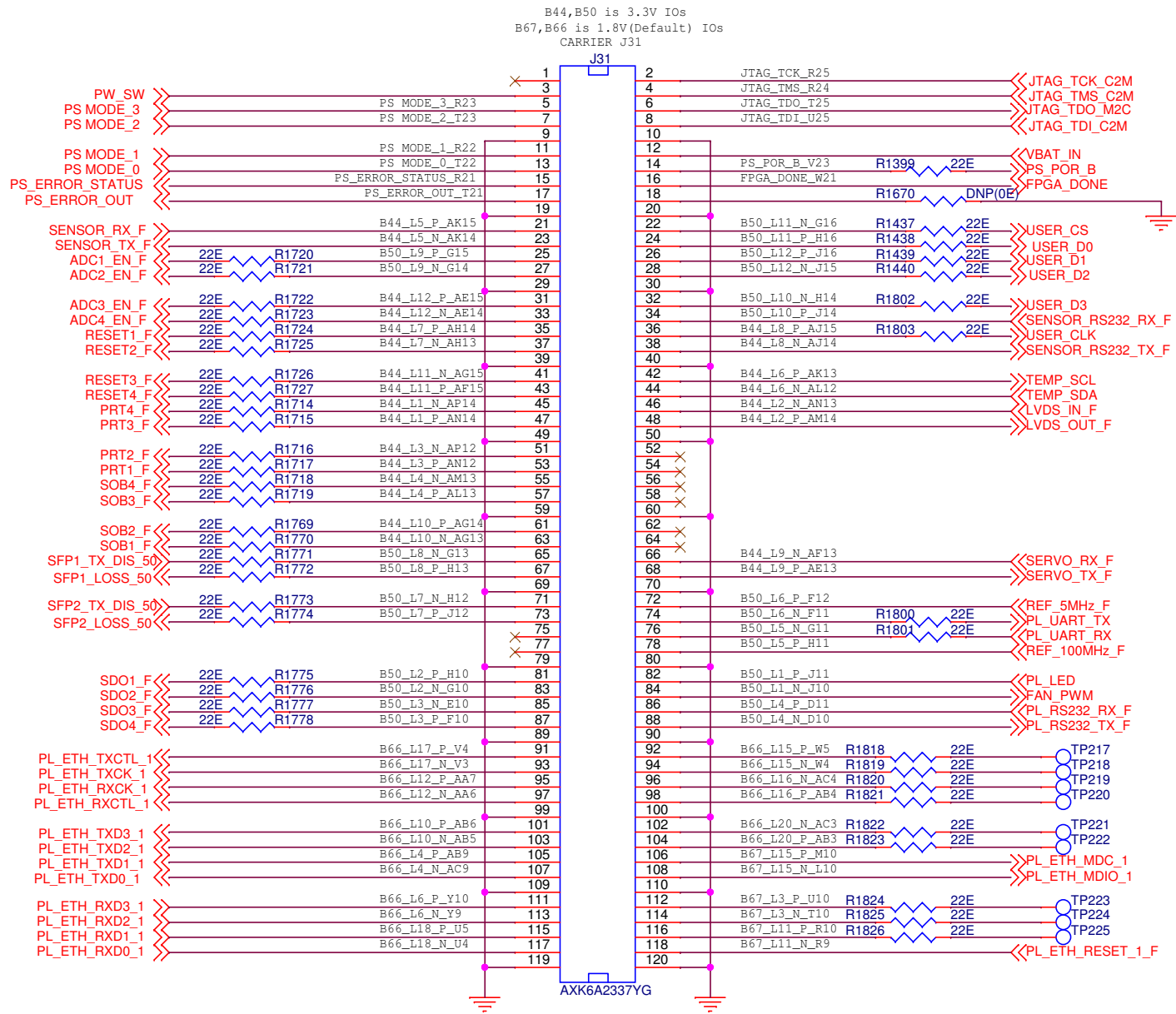
CARRIER J29



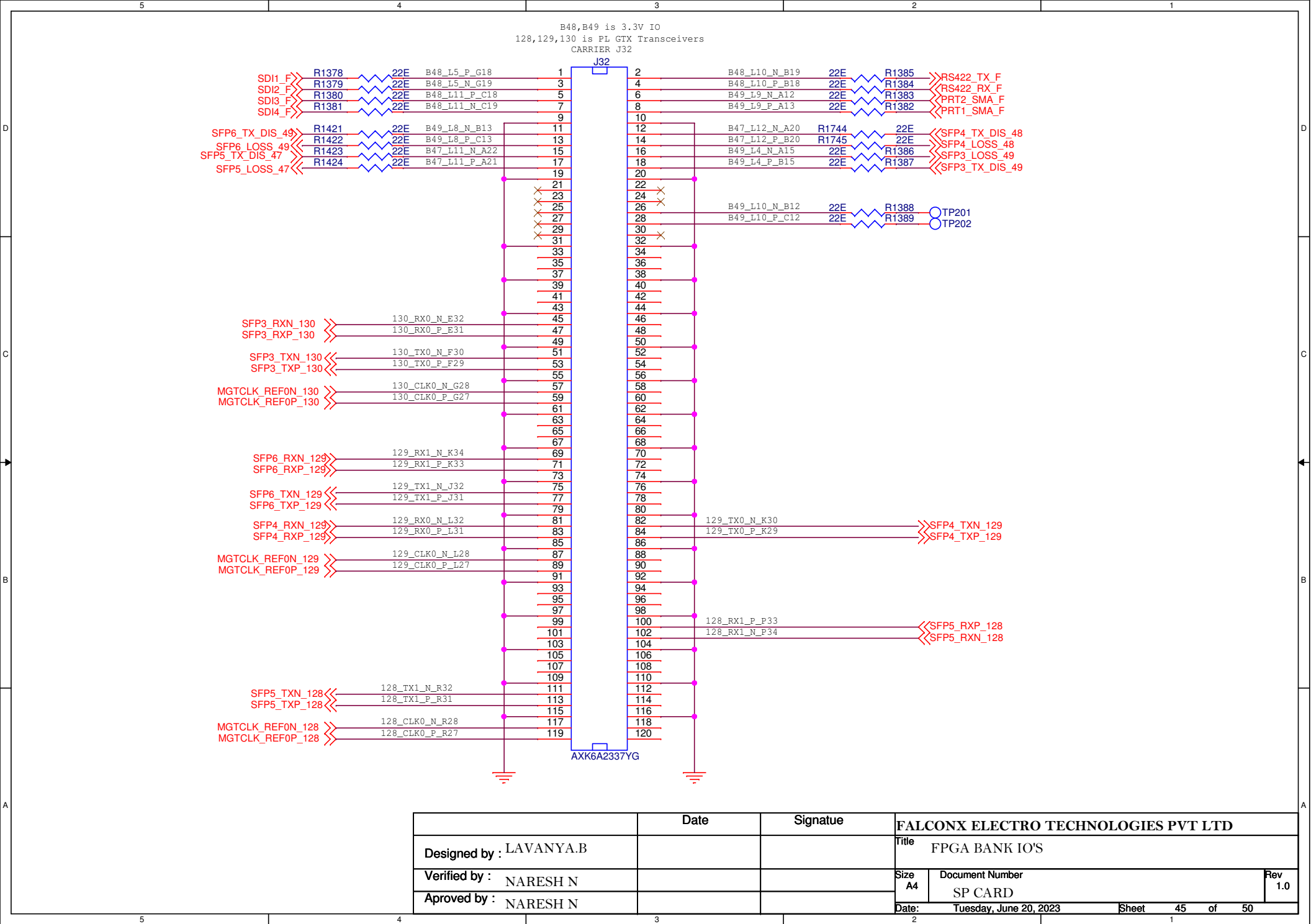
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Designed by : LAVANYA.B			Title FPGA BANK IO'S		
Verified by : NARESH N			Size A4	Document Number	Rev 1.0
Aproved by : NARESH N			SP CARD		
			Date: Tuesday, June 20, 2023	Sheet 42 of 50	



	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title FPGA BANK IO'S		
Verified by : NARESH N			Size A4	Document Number	Rev 1.0
Aproved by : NARESH N			SP CARD		
			Date: Tuesday, June 20, 2023	Sheet 43 of 50	



	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title FPGA BANK IO'S		
Verified by : NARESH N			Size A4	Document Number	Rev 1.0
Approved by : NARESH N			SP CARD		
			Date: Tuesday, June 20, 2023	Sheet 44 of 50	



	Date	Signature	FALCONX ELECTRO TECHNOLOGIES PVT LTD		
Designed by : LAVANYA.B			Title FPGA BANK IO'S		
Verified by : NARESH N			Size A4	Document Number SP CARD	Rev 1.0
Aproved by : NARESH N			Date: Tuesday, June 20, 2023	Sheet 45	of 50