Project Report on Last Level Cache Simulator

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Introduction:

A cache is a hardware or software component that stores data so that future requests for that data can be served faster. Data stored in a cache may be the outcome of an earlier computation or a copy of data saved elsewhere. When the requested data can be located in a cache, it is called a cache hit; when it cannot, it is called a cache miss. The more requests that can be satisfied from the cache, the faster the system operates since cache hits are satisfied by reading data from the cache, which is faster than recalculating a result or reading from a slower data storage.

Design Specifications:

Following specifications are used to implement the Last Level Cache:

- Cache byte Line: 64 - byte
- Total capacity: 16MB
- Associativity : 8 - way
- Coherence Protocol: MESI
- Page Replacement Policy: Pseudo- LRU
- Write decision policy: Write back
- Write Miss Decision policy: Write allocate

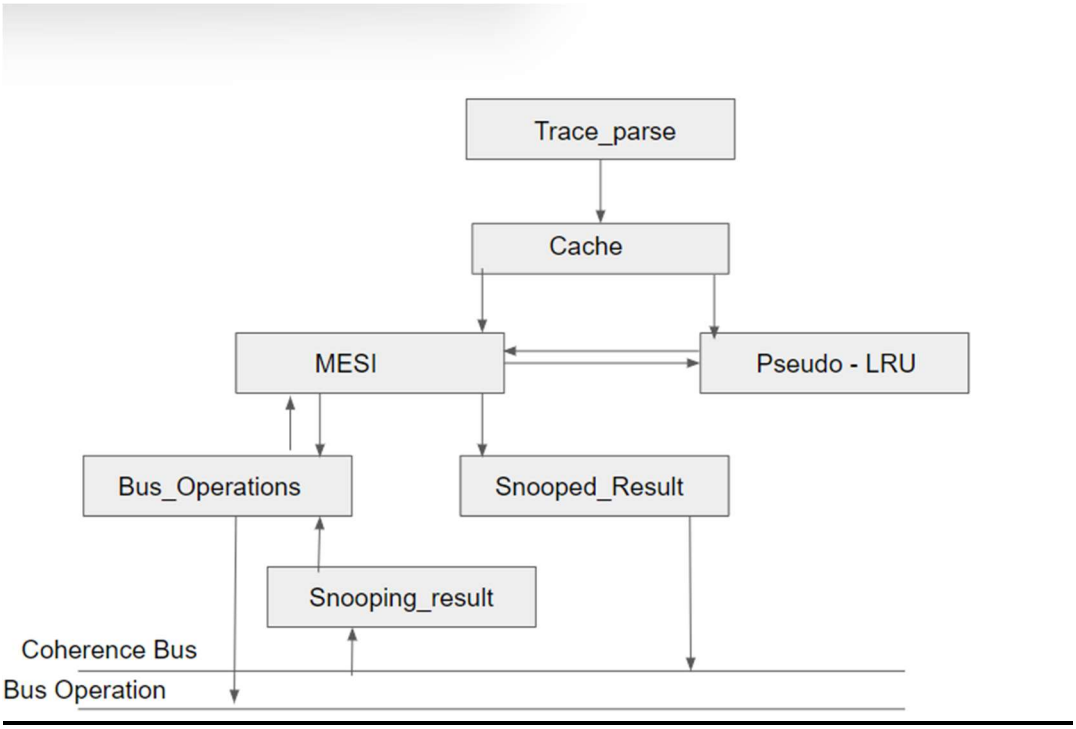
Following specifications are considered for the implementation of Higher level cache:

- Cache Byte Line: 64 - byte
- Write decision policy: Write through(once),
  Write back
- Associativity: 4 - way

Assumptions:

- Single Byte addressable mode is used for write and read references.
- The CPU address is 32 bit wide.

Design Architecture:



Source code modules:

Following files are used in our project:
cache_define.sv: The package file where all the variables are parameterised and have global scope.
trace_parse.sv: This file Reads parse the trace file and gives command and address input to cache
cache_LRU_MESI.sv: The main design file which performs all the operations read from the trace file.

Applications:

Cache is used in the following ways:
In hierarchical manner in Graphic Processing Unit (GPU) and Digital Signal Processors (DSP).
For translations from virtual memory to physical memory as memory cache called the translation lookaside buffer (TLB).
For usage in subsequent sessions, browsers each feature a cache that stores data from past browsing sessions.

Test Plan:

Test Cases for CPU Read and Write -

```
1 03885D40
1 13885D40
1 23885D40
1 33885D40
1 43885D40
1 53885D40
1 63885D40
1 73885D40
9

0 03885D40
0 13885D40
0 23885D40
0 33885D40
0 43885D40
0 53885D40
0 63885D40
0 73885D40
9
```

Output :

```
# Mode: SILENT_MODE
# File Opened
# Number of commands =                    9
# Total CPU requests =                    8
# Total Cache hits   =                    0
# Total Cache Miss   =                    8
# Cache Hit Ratio    =                    0.000000
# Cache Hit percentage: =                 0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     M|000000|   924|  8565|     0|
# |------|------|------|------|------|
# |     M|000000|   412|  8565|     1|
# |------|------|------|------|------|
# |     M|000000|   668|  8565|     2|
```

```
# |------|------|------|------|------|
# |     M|000000|   156|  8565|     3|
# |------|------|------|------|------|
# |     M|000000|   796|  8565|     4|
# |------|------|------|------|------|
# |     M|000000|   284|  8565|     5|
# |------|------|------|------|------|
# |     M|000000|   540|  8565|     6|
# |------|------|------|------|------|
# |     M|000000|    28|  8565|     7|
# |------|------|------|------|------|
# Number of commands =                  18
# Total CPU requests =                  16
# Total Cache hits   =                   8
# Total Cache Miss   =                   8
# Cache Hit Ratio    =                0.500000
# Cache Hit percentage: =             50.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     M|000000|   924|  8565|     0|
# |------|------|------|------|------|
# |     M|000000|   412|  8565|     1|
# |------|------|------|------|------|
# |     M|000000|   668|  8565|     2|
# |------|------|------|------|------|
# |     M|000000|   156|  8565|     3|
# |------|------|------|------|------|
# |     M|000000|   796|  8565|     4|
# |------|------|------|------|------|
# |     M|000000|   284|  8565|     5|
# |------|------|------|------|------|
# |     M|000000|   540|  8565|     6|
# |------|------|------|------|------|
# |     M|000000|    28|  8565|     7|
# |------|------|------|------|------|
```

Test cases for Pseudo-LRU-

Cases where it works as expected -

```
0 18885D40
0 F4885D40
0 94885D40
```

```
0 93885D40
0 91885D40
0 C4885D40
0 8F885D40
0 7C885D40
0 F4885D40
0 22885D40
0 F4885D40
0 94885D40
0 93885D40
0 91885D40
0 C4885D40
0 8F885D40
0 7C885D40
9
```

Output:

```
# Mode: SILENT_MODE
# File Opened
# Number of commands =                  18
# Total CPU requests =                  17
# Total Cache hits   =                  8
# Total Cache Miss   =                  9
# Cache Hit Ratio    =                  0.470588
# Cache Hit percentage: =               47.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     S|000000|   996|  8565|     0|
# |------|------|------|------|------|
# |     S|000000|  1180|  8565|     1|
# |------|------|------|------|------|
# |     S|000000|  1572|  8565|     2|
# |------|------|------|------|------|
# |     S|000000|  1956|  8565|     3|
# |------|------|------|------|------|
# |     S|000000|  1148|  8565|     4|
# |------|------|------|------|------|
# |     S|000000|  1188|  8565|     5|
# |------|------|------|------|------|
# |     S|000000|  1164|  8565|     6|
# |------|------|------|------|------|
```

```
# |     S|000000|   276|  8565|     7|
# |------|------|------|------|------|
```

Cases where output is unexpected-

```
0 18885D40
0 F4885D40
0 94885D40
0 93885D40
0 91885D40
0 C4885D40
0 8F885D40
0 7C885D40
0 91885D40
0 22885D40
0 F4885D40
0 94885D40
0 93885D40
0 91885D40
0 C4885D40
0 8F885D40
0 7C885D40
9
```

Output:

```
# Mode: SILENT_MODE
# File Opened
# Number of commands =                    18
# Total CPU requests =                    17
# Total Cache hits   =                    5
# Total Cache Miss   =                    12
# Cache Hit Ratio    =                    0.294118
# Cache Hit percentage: =                 29.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     S|000000|   996|  8565|     0|
# |------|------|------|------|------|
# |     S|000000|  1188|  8565|     1|
# |------|------|------|------|------|
# |     S|000000|  1572|  8565|     2|
# |------|------|------|------|------|
# |     S|000000|   276|  8565|     3|
```

```
# |------|------|------|------|------|
# |     S|000000|  1148|  8565|     4|
# |------|------|------|------|------|
# |     S|000000|  1956|  8565|     5|
# |------|------|------|------|------|
# |     S|000000|  1164|  8565|     6|
# |------|------|------|------|------|
# |     S|000000|  1180|  8565|     7|
# |------|------|------|------|------|
```

Test cases for MESI protocol -

<u>Processor - Initiated transitions:</u>

The following test cases are for the transition from Invalid to Modified state, snoop result is HIT.

```
0 44885D41
0 44885D41
1 44885D41
0 44885D41
1 44885D41
1 44885D41
0 44885D41
0 44885D41
1 44885D41
0 44885D41
1 44885D41
9
```

Output:

```
# Mode: NORMAL_MODE
# File Opened
#
# ------READ COMMAND------
# Hit / Miss: Cache Miss
```

```
# Evict addess = 0xzzZ85d41
# MESI:
# Bus Operation : READ TOTAL_Address: 44885d41, Get Snoop Result: HITM
#
# State: S
# L2 Message: SENDLINE
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# Bus Operation : INVALIDATE TOTAL_Address: 44885d41, Get Snoop Result: HITM
#
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------READ COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------READ COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
```

```
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------READ COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d41 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                 9
# Total CPU requests =                 8
# Total Cache hits   =                 7
# Total Cache Miss   =                 1
# Cache Hit Ratio    =                 0.875000
# Cache Hit percentage: =              87.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     M|1000101|   548|  8565|     7|
# |------|------|------|------|------|
```

The following test case is for the transition from Invalid to Modified state, snoop result is NOHIT.

```
0 44885D43
0 44885D43
1 44885D43
0 44885D43
1 44885D43
9
```

Output:

```
# Mode: NORMAL_MODE
# File Opened
#
# ------READ COMMAND------
# Hit / Miss: Cache Miss
# Evict addess = 0xzzZ85d43
# MESI:
# Bus Operation : READ TOTAL_Address: 44885d43, Get Snoop Result: NOHIT
#
# State: E
# L2 Message: SENDLINE
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d43 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------READ COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d43 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
# Tag = 44885d43 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    5
# Total CPU requests =                    4
# Total Cache hits   =                    3
# Total Cache Miss   =                    1
# Cache Hit Ratio    =                 0.750000
# Cache Hit percentage: =              75.000000
#
```

```
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     M|1000101|   548|  8565|     7|
# |------|------|------|------|------|
```

Bus - Initiated transitions:

The following test cases are for Invalid state transitions.

```
0 30985D42
6 30985D42
4 30985D42
6 30985D42
3 30985D42
9
```

Output:

```
# Mode: NORMAL_MODE
# File Opened
#
# ------READ COMMAND------
# Hit / Miss: Cache Miss
# Evict addess = 0xzzZ85d42
# MESI:
# Bus Operation : READ TOTAL_Address: 30985d42, Get Snoop Result: NOHIT
#
# State: E
# L2 Message: SENDLINE
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
```

```
# ------snoop rwim COMMAND------
# MESI:
# Put Snoop - Address: 30985d42, Put Snoop Result: HIT
# State: I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------snoop read COMMAND------
# MESI:
# Put Snoop - Address: 30985d42, Put Snoop Result: NOHIT
# State: I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------snoop rwim COMMAND------
# MESI:
# Put Snoop - Address: 30985d42, Put Snoop Result: NOHIT
# State: I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------SNOOP INVALIDATE COMMAND------
# MESI:
# Put Snoop - Address: 30985d42, Put Snoop Result: NOHIT
# State = I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    6
# Total CPU requests =                    1
# Total Cache hits   =                    0
# Total Cache Miss   =                    1
# Cache Hit Ratio    =                    0.000000
# Cache Hit percentage: =                 0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
```

The following test cases are for transition from Invalid state to Shared state, where Snoop result is HIT.

```
1 30985D40
4 30985D40
4 30985D40
9
```

Output:

```
          # Mode: NORMAL_MODE
# File Opened
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Miss
# Evict addess = 0xzzZ85d40
# MESI:
# Bus Operation : RWIM TOTAL_Address: 30985d40, Get Snoop Result: HIT
#
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    2
# Total CPU requests =                     1
# Total Cache hits   =                     0
# Total Cache Miss   =                     1
# Cache Hit Ratio    =                 0.000000
# Cache Hit percentage: =                  0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     M|1000101|   388| 24949|     7|
# |------|------|------|------|------|
#
# ------snoop read COMMAND------
# MESI:
# Put Snoop - Address: 30985d40, Put Snoop Result: HITM
# State: S
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                     4
# Total CPU requests =                     1
# Total Cache hits   =                     0
# Total Cache Miss   =                     1
# Cache Hit Ratio    =                    0.000000
# Cache Hit percentage: =                 0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     S|1000101|   388| 24949|     7|
# |------|------|------|------|------|
#
# ------snoop read COMMAND------
# MESI:
# Put Snoop - Address: 30985d40, Put Snoop Result: HIT
```

```
# State: S
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    6
# Total CPU requests =                    1
# Total Cache hits   =                    0
# Total Cache Miss   =                    1
# Cache Hit Ratio    =                    0.000000
# Cache Hit percentage: =                 0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     S|1000101|   388| 24949|     7|
# |------|------|------|------|------|
```

The following test cases are for transition from Invalid to Shared state, where Snoop result is NOHIT.

```
0 30985D43
4 30985D43
4 30985D43
9
```

Output:

```
    # Mode: NORMAL_MODE
# File Opened
#
# ------READ COMMAND------
# Hit / Miss: Cache Miss
# Evict addess = 0xzzZ85d43
# MESI:
# Bus Operation : READ TOTAL_Address: 30985d43, Get Snoop Result: NOHIT
#
# State: E
# L2 Message: SENDLINE
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------snoop read COMMAND------
# MESI:
# Put Snoop - Address: 30985d43, Put Snoop Result: HIT
# State: S
```

```
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    3
# Total CPU requests =                    1
# Total Cache hits   =                    0
# Total Cache Miss   =                    1
# Cache Hit Ratio    =                    0.000000
# Cache Hit percentage: =                 0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
# |     S|1000101|   388| 24949|     7|
# |------|------|------|------|------|
```

Transition from Shared state to Invalid State. Initial state is Shared.

```
3 30985D42
9
```

Output:

```
# Mode: NORMAL_MODE
# File Opened
#
# ------READ COMMAND------
# Hit / Miss: Cache Miss
# Evict addess = 0xzzZ85d43
# MESI:
# Bus Operation : READ TOTAL_Address: 30985d43, Get Snoop Result: NOHIT
#
# State: E
# L2 Message: SENDLINE
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------snoop read COMMAND------
# MESI:
# Put Snoop - Address: 30985d43, Put Snoop Result: HIT
# State: S
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------SNOOP INVALIDATE COMMAND------
```

```
# MESI:
# Put Snoop - Address: 30985d42, Put Snoop Result: HIT
# State: I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    4
# Total CPU requests =                    1
# Total Cache hits   =                    0
# Total Cache Miss   =                    1
# Cache Hit Ratio    =                    0.000000
# Cache Hit percentage: =                 0.000000
#
# ////Valid lines in L3cache/////
# | MESI State|  LRU|  Tag| Index|  Way|
```

The following traces are used for a combination of Processor initiated and Bus initiated processes-

```
0 3E776D42
0 3E776D42
0 3E776D42
1 3E776D42
1 3E776D42
0 3E776D42
4 3E776D42
4 3E776D42
6 3E776D42
3 3E776D42
9
```

Output:

```
    # Mode: NORMAL_MODE
# File Opened
#
# ------READ COMMAND------
# Hit / Miss: Cache Miss
# Evict addess = 0xzzZ76d42
# MESI:
# Bus Operation : READ TOTAL_Address: 3e776d42, Get Snoop Result: NOHIT
#
```

```
# State: E
# L2 Message: SENDLINE
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------WRITE COMMAND------
# Hit / Miss: Cache Hit
# Tag = 3e776d42 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------READ COMMAND------
# Hit / Miss: Cache Hit
# Tag = 3e776d42 LRU 1000101
# MESI:
# L2 Message: SENDLINE
# State: M
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------snoop read COMMAND------
# MESI:
# Put Snoop - Address: 3e776d42, Put Snoop Result: HITM
# State: S
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------snoop rwim COMMAND------
# MESI:
# Put Snoop - Address: 3e776d42, Put Snoop Result: HIT
# State: I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
#
# ------SNOOP INVALIDATE COMMAND------
# MESI:
# Put Snoop - Address: 3e776d42, Put Snoop Result: NOHIT
# State = I
# ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
# Number of commands =                    7
# Total CPU requests =                    3
# Total Cache hits   =                    2
# Total Cache Miss   =                    1
# Cache Hit Ratio    =                    0.666667
# Cache Hit percentage: =                 66.000000
#
```

////Valid lines in L3cache/////
| MESI State| LRU| Tag| Index| Way|