EE419/519 Experiment #1 (v2)

Buck Converter

Preliminary (Due Oct 4, 2024)

Consider the Buck converter shown below. Note that this is a negative Buck converter that converts a negative voltage $-V_d$ to a smaller negative voltage $-V_o$.

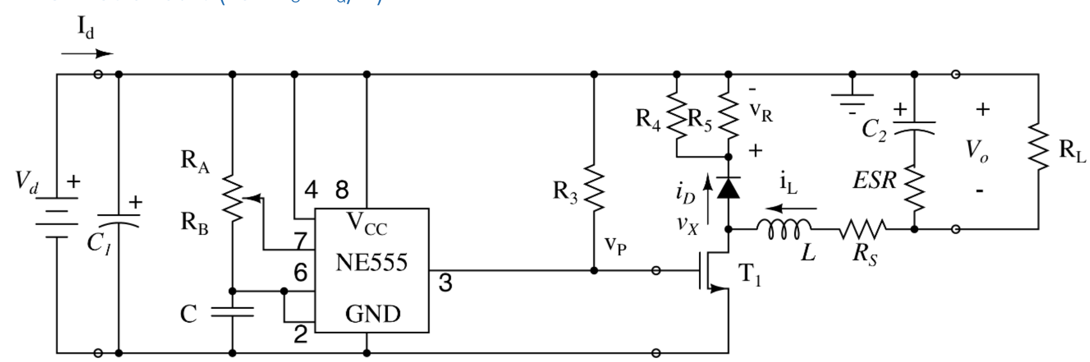
V_d=9+mod(BilkentID,7)

V_o=2.5+mod(BilkentID,7)+mod(BilkentID,4)

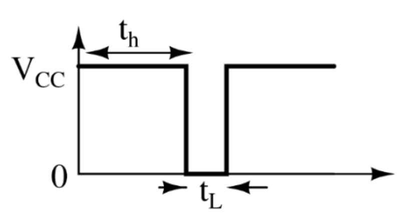
where mod(x,y) is the remainder of the x divided by y.

The Buck converter uses a pulse generator (NE555) generating a pulse of adjustable duty cycle between 0 and V_{CC}. NE555 can generate pulses with a duty cycle greater than 50%. So, the first circuit shown below is suitable for $V_o>V_d/2$. If your assignment requires $V_o<V_d/2$, use the second circuit, which includes an inverter built by a PNP transistor, BC308, to generate pulses with a duty cycle smaller than 50%. Use UF4007 fast diode as the Buck converter diode. IRFZ44 is the switching transistor. Use a 100µF (at least 25V) capacitor for C_1, which acts like a power supply bypass capacitor.

The first circuit (for $V_o>V_d/2$):



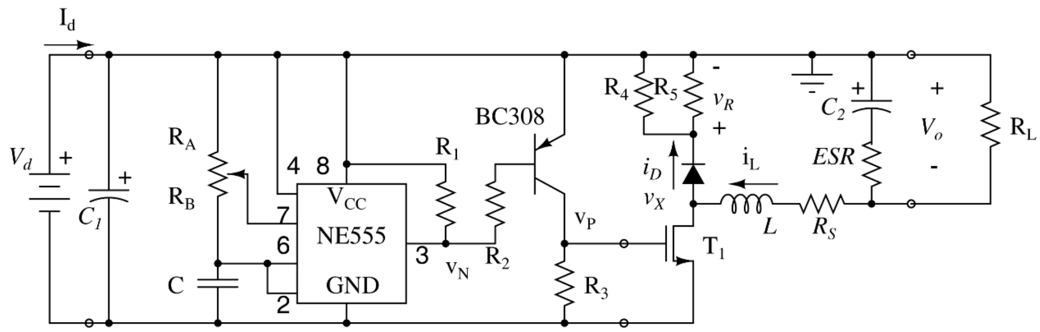
R_3 is a pull-up resistor connected between the output pin (3) and V_{CC} (pin 8) of NE555 since NE555 output contains an open-collector output transistor. Choose the current through R_3 as about 20mA when output is low ($R_3=V_d/0.02$). R_L represents the load resistance. R_S is the series resistance of the inductor. ESR is the equivalent series resistance of the filter capacitor. R_A, R_B, and C set the pulse repetition frequency and pulse duration applied to the transistor gate. R_4 and R_5 are small resistors (1Ω each) used to measure the diode's current.



The figure above shows the output voltage (pin 3) of NE555. The output of NE555 (V_P) high-level duration (when T_1 is ON) is $t_h=0.693C(R_A+R_B)$ while the repetition period is given by $T_s=0.693C(R_A+2R_B)=0.693C(R_A+R_B)(1+R_B/(R_A+R_B))$. Choose standard resistor and capacitor values.

For R_A+R_B, use a trimpot of $R_A+R_B=10K\Omega$ to adjust the switching timing and, hence, the output voltage accurately. Use a repetition period, T_S, between 15µs to 40µs.

The second circuit (for $V_o<V_d/2$):



R_1 is a pull-up resistor connected between the output pin (3) and V_{CC} (pin 8) of NE555 (an open-collector output). Choose the current through R_1 as about 5mA ($R_1=V_d/0.005$). R_2 provides the base current for the pnp transistor. Choose R_2 to provide a base current of 1mA ($R_2=V_d/0.001$). R_3 is the collector resistance of the pnp transistor. Choose R_3 to pass a current of 20mA ($R_3=V_d/0.02$). R_4 and R_5 are small resistors (1Ω each) used to measure the diode's current.

The output of NE555 (v_N) low-level duration (when v_P is high and T_1 is ON) is $t_L=0.693CR_B$ while the repetition period is given by $T_s=0.693C(R_A+2R_B)$. Choose standard resistor and capacitor values.

To change R_B, use a trimpot of $R_A+R_B=10K\Omega$ to adjust the switching timing and, hence, the output voltage accurately. Use a repetition period, T_S, between 15µs to 40µs.

Inductor

The parameters of the inductors are given in the following list. The series resistance, R_S, of the inductor, is also given in the list. You will be assigned to one of the inductors.

Questions

a) Find the *maximum* value of load resistance, R_{max}, such that the inductor current is never $i_L=0$ (continuous case). Find the *minimum* value of the load resistance, R_{min}, to keep the inductor peak current below 1.5A.

b) Choose a load resistance, $R_L=R_{L1}$, with a sufficient power rating (8.2, 10, 15, 33, 47, 68, 100, and 150Ω power resistors are available in the lab) between those limits ($R_{min}<R_{L1}<R_{max}$), find the corresponding duty cycle, D, to generate the required output voltage. Ignore the voltage drop on the diode and the resistors, R_S, R_4, and R_5, for this calculation.

c) Estimate and plot the diode current, $i_D(t)$, waveform for the chosen R_{L1}, and the diode voltage, $v_X(t)$ in PSS. Note that the diode current and the inductor current are equal when the switch is off. Hence, the peak diode current is the same as the peak inductor current.

d) Estimate and plot the output ripple voltage. Assume that the ESR is the dominant mechanism for the ripple and ESR=0.25Ω.

e) Keeping all parameters the same, estimate the output voltage, V_o, if the load resistance, R_L, is increased to above the maximum limit, $R_L=R_{L2}>R_{max}$. For R_{L2}, choose one of the standard values. In this case, the inductor current is sometimes zero (discontinuous case). Estimate and plot $i_D(t)$ and $v_X(t)$ in this case.

f) What should be the duty cycle, D, to keep the output voltage the same at the desired output voltage with $R_L=R_{L2}$?

g) Perform an LTSpice simulation of the circuit using $R_L=R_{L1}$ as in (b). Use .include uf4007.txt spice directive to simulate UF4007 fast diode. Use .include irfz44.txt spice directive to simulate IRFZ44 nMOS transistor. Use C_2=100µF with ESR=0.25Ω as the filter capacitor. Do not ignore the resistors, R_S, R_1, and R_2 for this case. By trial and error, find the duty cycle D to get the required output voltage. Note that the duty cycle, D, value will be greater than that found in (b) because of the voltage drop on the diode and the resistances.

h) From LTSpice simulation, plot the diode current, $i_D(t)$, and the diode voltage, $v_X(t)$ in PSS (all for $R_L=R_{L1}$).

i) From LTSpice simulation, plot the output voltage in PSS and determine the value of the peak-to-peak ripple (V_{ripple}).

j) From LTSpice simulation, determine the converter's efficiency (η) in PSS. For this purpose, record the supply current, I_d, and use the equations: $P_{in}=V_dI_d$, $P_{out}=V_o^2/R_L$, $\eta=P_{out}/P_{in}$.

k) Perform an LTSpice simulation using the load resistor $R=R_{L2}$ as in (d) while the duty cycle is kept at the same value as (f). Determine the output voltage.

Inductors:

Inductor #	L (µH)	R_s (Ω) (@ 50 KHz)
1	502	0.96
2	446	1.06
3	131	0.50
4	119	0.41
5	347	0.91
7	652	1.11
8	173	0.61
9	169	0.56
11	326	0.52
12	337	0.55
13	169	1.14
14	119	0.43
17	201	0.53
18	315	0.43
24	408	0.55
25	108	1.39
26	326	1.90
27	155	0.80
28	147	1.09
29	174	0.92
30	137	0.49
31	482	1.91
33	160	0.60
34	319	0.55
35	278	0.55
36	258	0.42
37	459	1.22
40	245	1.23
41	245	1.06
45	356	0.61
47	435	1.25

Experimental work (Due Oct 12, 2024)

Bring with you an oscilloscope probe and a breadboard.

a) First, set up only your NE555 circuit on the breadboard, including the pull-up resistor at the output pin. If you use the second circuit, add the BC308 (pnp) transistor and its resistors (R_2 and R_3). Do not add the switch transistor, the diode, or the inductor, yet. As C_1, use a 100µF (25V or higher) capacitor. Watch out for the polarities of electrolytic capacitors. Incorrectly placed electrolytic capacitors may explode and cause serious injury. Apply the supply voltage, V_d. Using the oscilloscope probe measure the voltage v_P to GND. Note that GND is the positive end of the power supply V_d. You should have a periodic negative pulse of magnitude varying between $-V_d$ and zero at the intended repetition period. This voltage will be applied to the gate of the MOSFET transistor. To turn on the MOSFET transistor fully, the gate pulse should vary between 0 to $-V_d$. The duty cycle is determined by the ratio of zero voltage duration to the repetition period. If the waveform is incorrect, check the timing resistors and the capacitor connections.

b) If the repetition period and the duty cycle are correct, add the transistor IRFZ44 as the switch and UF4007 as the diode. You may find the datasheets of these components in Moodle. Add the inductor and the capacitor C_2. Make sure that the diode direction and capacitor polarity are correct. Add a load resistor of R_L=560Ω. Apply the supply voltage V_d, and using the oscilloscope probe, measure the voltage between v_X and GND. The voltage should vary between +0.6 to $-V_d$. There will also be an oscillatory portion in the waveform toward the end of the cycle. V_o, the DC voltage across R_L, measured by the multimeter, should be nearly equal to V_d. If not, check your connections. Some breadboard pins may be loose and not make good contact.

c) If $v_X(t)$ voltage looks like the expected waveform, change the load resistor to R_{L1}. Apply the supply voltage, V_d. Record the output ripple voltage. Use AC coupling in the oscilloscope channel to zoom in on the waveform. Use external triggering using the NE555 output pulse. Compare with the results of the preliminary work (g), (i), and (j).

	V_d	I_d	$R_L=R_{L1}$	D	V_o	η (%)	V_{ripple}
Preliminary							
Experiment							

d) Record $v_X(t)$ and $i_D(t)$. Use $v_R(t)$ to measure the diode current: $i_D(t)=2 \times v_R(t)$ (since $R_1 \parallel R_2=0.5\Omega$). If $v_R(t)$ is noisy, use the averaging option of the oscilloscope to get a cleaner waveform. Compare the waveforms with those found in (h) of the preliminary work.

e) Replace the load resistance to $R=R_{L2}$. Find the output voltage while D is kept unchanged. Compare the results with the preliminary work (k).

	V_d	$R_L=R_{L2}$	D	V_o
Preliminary				
Experiment				