EE419/519 Project (v4)

Build a high-efficiency isolated DC-DC flyback converter using MC34063A (datasheet in Moodle). An application note for this chip is also available. Each student is assigned input/output voltage, which can be found in Moodle. Consult the datasheet and application note of MC34063 for details.

DC output voltage accuracy should be better than ±5%.

The peak-to-peak ripple at the output voltage should be less than 300mV.

The output power should be as large as possible.

The project to be completed in four parts:

Part 1: Converter design, inductor design, transformer fabrication, transformer measurement.

Part 2: PCB design

Part 3: Converter fabrication, measurement

Part 4: 3-minute youtube video presentation of your project.

Available components (data sheets available in Moodle)

MC34063A (switcher and controller)

UF2003 (1A average current, 200V reverse voltage, Fast recovery PN diode) (attach DO-41m pattern)

1N4148 (0.1A 50V PN diode) (attach DO-41m pattern)

4N25 (Optocoupler) (model available in LTSpice)

TL431 (shunt regulator) (model and symbol files available in Moodle)

22µF 160V aluminum electrolytic capacitor, 10mm diameter (ESR=1.3Ω (40KHz)) (attach CAPPRD500W60D1000H1750m pattern)

150µF 35V aluminum electrolytic capacitor, 8mm diameter (ESR=0.33Ω (40KHz)) (attach CAPPRD500W60D800H1750m pattern)

100µF 50V aluminum electrolytic capacitor, 8mm diameter (ESR=0.15Ω (40KHz)) (attach CAPPRD500W60D800H1750m pattern)

10µF 25V chip capacitor (7µF and ESR=130 mΩ at 66KHz) (attach CAP_2815m pattern)

150µF 16V chip capacitor (18µF and ESR=85 mΩ at 66KHz) (attach CAP_2815m pattern)

E-core E19 (total air gap=0.25mm) $A_L \approx 160 nH/T^2$. The maximum ampere-turns 70A-turns (determines the maximum current that is allowed in an inductor. For example, if an L=56µH inductor is wound with 19 turns, 3.6A can flow without causing saturation). (Use E19 symbol with E19 pattern)

Use CONN2M connector for input connection. Use Pin 1 for positive input, pin 2 for negative input.

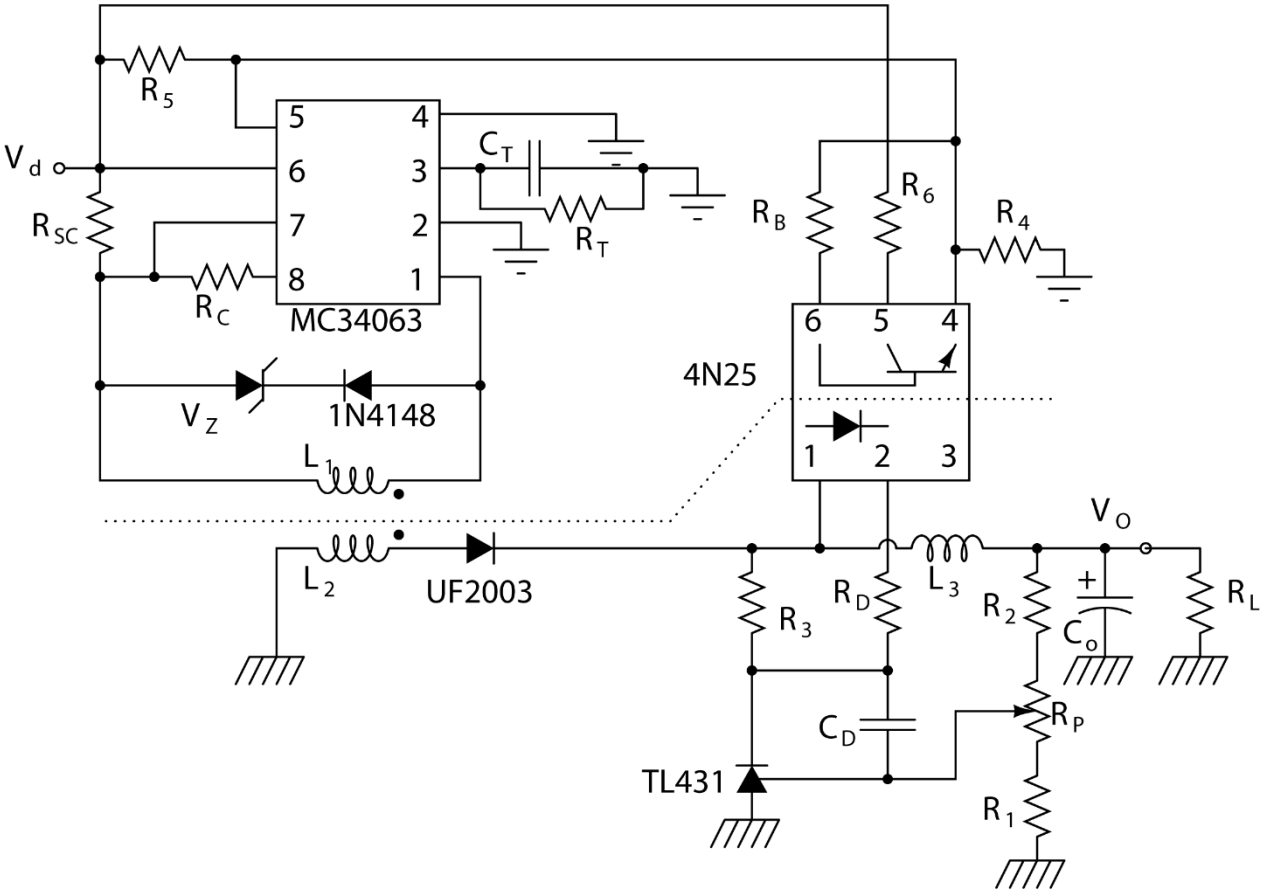
Use CONN3M connector for output connection. Use Pin 1 for positive output, pin 3 for negative output. Leave pin 2 unconnected.

The PCB board size: 53mm x 53mm.

Part 1

(LTSpice asc file and PDF report due November 13, 2024. All work should be done independently.)

A possible flyback converter circuit is shown below:



Suggested design procedure:

- Choose T_S in the range 8µs to 12µs.
- Choose i_{peak}=1.1A. Hence R_{SC}=0.33/i_{peak} (in Ω).
- Choose R_C such that it supplies sufficient base current (i_{peak}/β_{min}) to the switching transistor. $R_C=\beta_{min}\,(V_d-1.6)/i_{peak}$.
- Choose the Zener voltage such that V_d+V_Z=35V since the max allowed switch voltage is 40V.
- Choose V_{OR} such that $V_Z \gg V_{OR}$. If you choose a smaller V_{OR}, efficiency will be higher, but L_2 needs to be larger with more turns. If you choose a larger V_{OR}, T_S could be chosen smaller, meaning more output power. For the purpose of increasing the output power, you may choose V_{OR} in the range 7V to 11V.
- Let the coupling coefficient of the transformer be k=0.9. The actual value may be found by measurement of the transformer.
- Let $[D+\Delta_2]$=0.8 to 0.9 to assure discontinuous mode operation.
- Find D from $D=[D+\Delta_2]/(1+V_d/V_{OR})$
- Find Δ_1 from V_d, k, and the determined values of D, V_Z, V_{OR}.

- Find the inductance of the primary from $L_1=DT_SV_d/i_{peak}$.
- Find the turns-ratio $N_1/N_2=V_{OR}/V_O$.
- Find the inductance of the secondary from $L_2=L_1/(N_1/N_2)^2$.
- Find the number of turns of the primary: $N_1=[L_1/A_L]^{1/2}$ with $A_L=160nH/T^2$ (the value for the core with an air gap determined by the standard paper thickness).
- Find the number of turns of the secondary: $N_2=[L_2/A_L]^{1/2}$ with $A_L=160nH/T^2$.
- Find the OFF-time of the switch: $T_{OFF}=(1-D)T_S$.
- Determine the capacitor C_T from the graph in the datasheet of MC34063 using T_{OFF} curve.
- Use $R_T=1M\Omega$ to reduce the startup transient of LTSpice simulation. Do not use this resistor in the implementation.
- Choose standard values for R_1 and R_2 such that $V_OR_1/(R_1+R_2)$ is nearly 2.5V (the reference voltage of TL431, the shunt regulator). Choose R_1+R_2 in the range 50K to 150K. You may place a trimpot, R_P, of value 10KΩ between them for fine adjustment to get 2.5V (and hence the fine adjustment of the output voltage V_O.)
- Choose the output capacitor $C_o=1\mu F$ for faster steady-state response in LTSpice simulation. You may use a much larger capacitor in the implementation to reduce the output ripple.
- Choose $R_D=680\Omega$ to limit the current through the photodiode.
- Choose $R_3=10K$ to bypass the off-current of TL431.
- Choose $C_D=10nF$ to AC couple the cathode and feedback pins of TL431 for proper operation.
- Choose $L_3=1\mu H$ to $20\mu H$ range to speed up the LTSpice simulation. You may find an optimal value for minimization of the simulation time. You can short-circuit this inductor in the implementation.
- Choose $R_B=220K$ to speed up the turn-off transient of the phototransistor.
- Choose R_4 and R_5 such that $1.1V < V_d\ R_4/(R_4+R_5) < 1.20V$, i.e., slightly below the threshold voltage (1.25V) of MC34063. Choose R_4+R_5 in the range 10K to 50K.
- Choose R_6 in the range 1K to 5K to limit the current of the phototransistor.
- Determine the maximum theoretical output power and efficiency under this condition. Ignore the losses in the transformer, diode, and switch, but include the loss of the snubber network. (You can find the maximum output power from V_OI_O product when there are no missing cycles.)

Complete the design of your converter, including the full specifications of the transformer. Perform an LTSpice simulation to show that your circuit works. Determine the efficiency of the converter with the minimum allowable load resistor.

The PDF report:

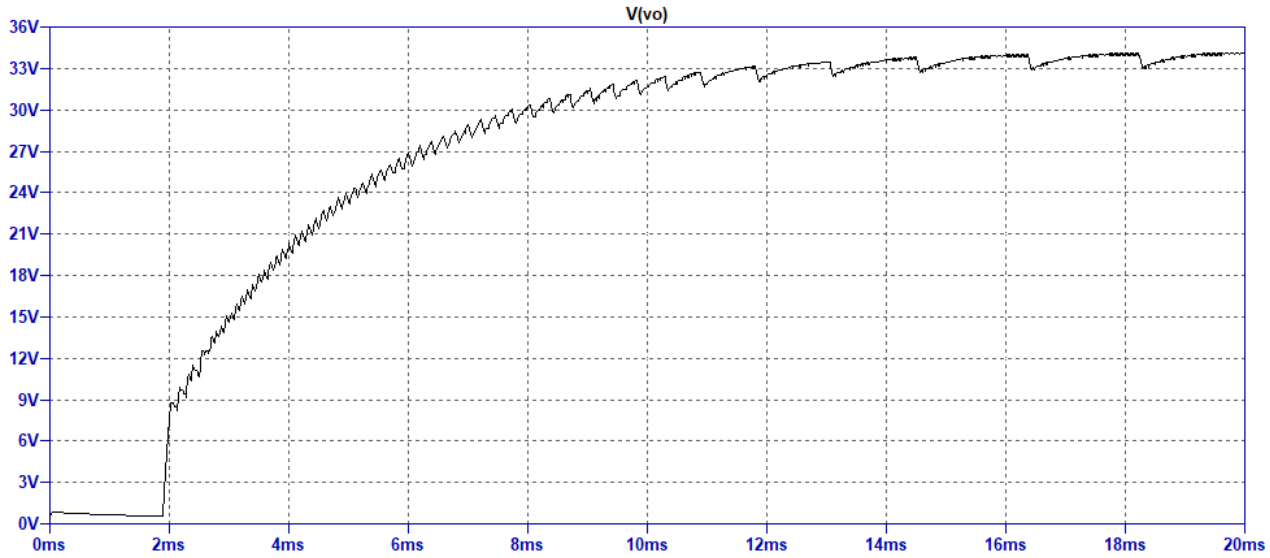
1. Show all your design steps (given above).
2. Provide LTSpice schematic.
3. Provide the three LTSpice graphs examples of which are shown below.
4. Specify the maximum output power and the efficiency at that load from LTSpice results.
5. Wound your inductor and measure the inductance and series resistance of the inductor at the switching frequency. Find the coupling coefficient between the primary and secondary. Note that the air gaps can be realized using standard-thickness paper between two E pieces.

Upload your PDF report and LTSpice source file to Moodle.

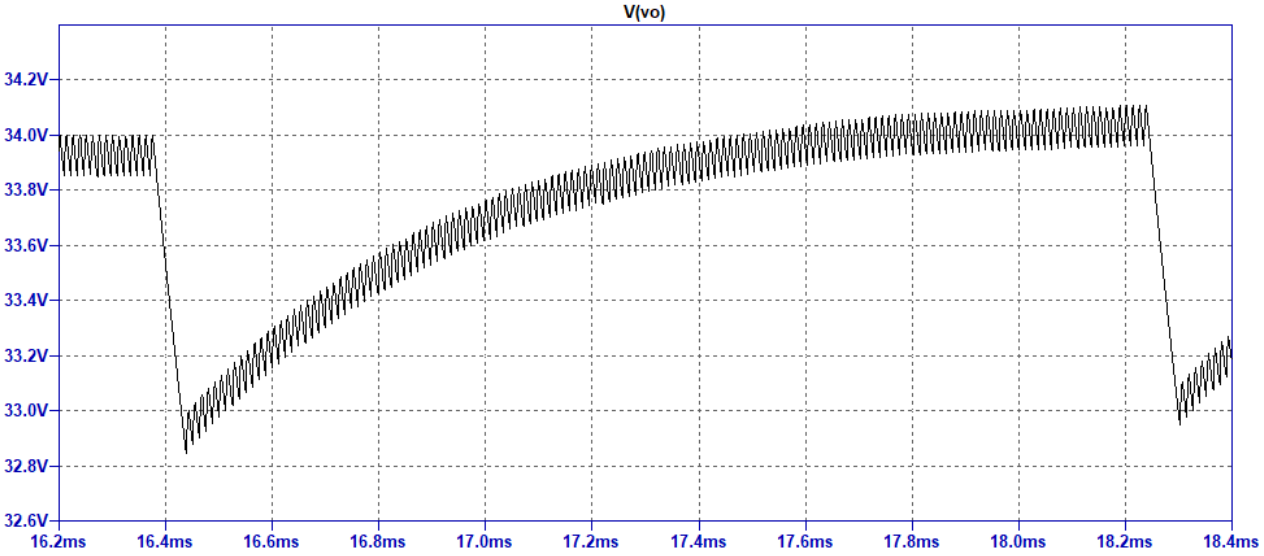
LTSpice simulation hints:

- Insert the mc34063.lib in the work directory. Use the MC34063.asy as the symbol. Set the Value parameter of the symbol to MC34063p (by CTRL-Click).
- Insert the TL431.lib in the work directory. Use the TL431.asy as the symbol.
- 4N25 is available in LTSpice library under Optos.
- For Vz you can choose a Zener diode from LTSpice diode library with the proper voltage.
- 1N4148 is available in LTSpice library under diodes.
- Insert UF2003.lib in the work directory. Use a diode symbol. Set its Value to UF2003 (by CTRL-Click).
- Use ".tran 40m startup" for transient simulation. "startup" command is necessary for a proper simulation. You may reduce the stop time to 40m if the circuit reaches the steady state earlier. Once you determine the stop time, you may limit the output display by specifying the "time to start saving data" parameter: ".tran 40m 39m startup".
- The value of the oscillator frequency may be different than what is expected from the graph in the datasheet. Change the value of C_T by trial and error to get the value you need.
- Since your output capacitor is kept small for the purpose of shorter simulation time, the output ripple will be more than the specifications
- Initially, use a large load resistor, R_L. You may reduce its value until the output voltage level can no longer be sustained. Note that at every missing cycle, the output voltage drops (it is easily visible when you choose a small output capacitor). If there is no ripple, there are no missing cycles, indicating that the output resistor is too small.

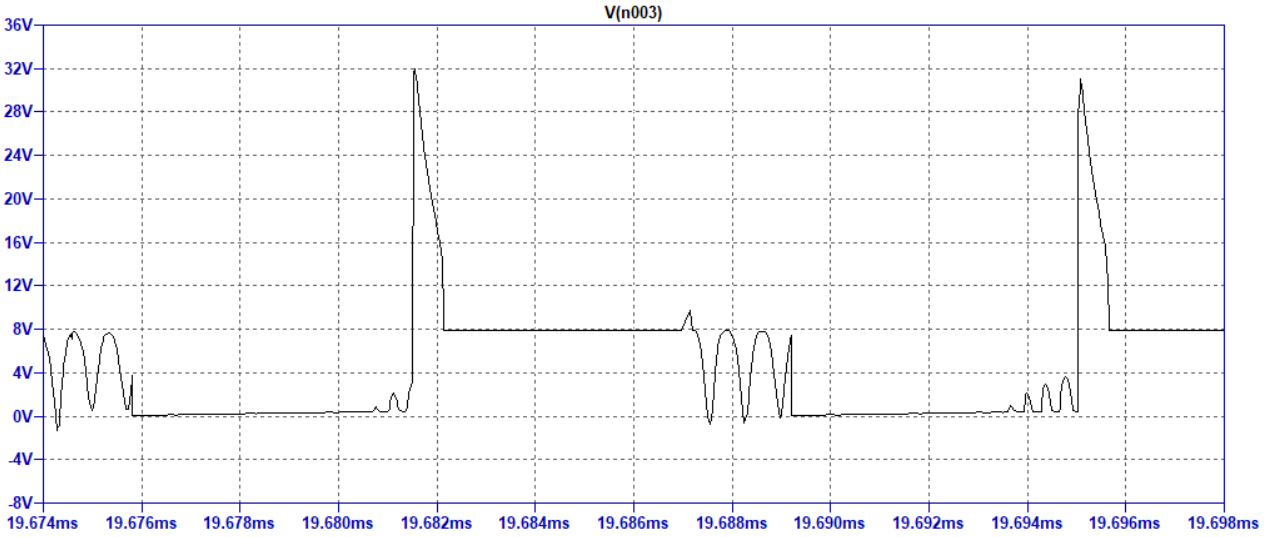
The output voltage startup transient of a 5V to 34V converter is shown below with an output capacitor of 1µF and a load resistor of 1.97KΩ. Note that the ripple frequency decreases as the output voltage reaches the steady-state value as there are fewer missing cycles. The efficiency of the converter is found as 44%.



The zoomed-in version of the output voltage is shown below for one ripple period. Since the output capacitor is small, the voltage drops significantly during the missing cycle. Individual cycles are also visible in this graph.



The switch voltage is a good indicator of a good design. The idle period should be a small fraction of the period, while its presence guarantees discontinuous mode operation. The graph below shows the switch voltage (at pin 1) with V_d=5V and V_{OR}=3V. You can make C_T smaller to reduce the idle period.



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