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EEE 419 – 01

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EEE 419 Experiment 1 Preliminary Report

Introduction

The aim of the experiment is to design a Buck Converter that converts a negative voltage to a smaller negative voltage.

A Buck Converter is a type of DC-DC power converter that steps down the input voltage to a lower output voltage. Step-down converters are commonly used in power supplies, battery management systems, and voltage regulation circuits.

The core principle of a buck converter is based on energy transfer and regulation using a switch device. In the given circuit, IRFZ44 nMOS is used for this purpose. The converter operates by rapidly switching the input voltage on and off, creating a series of voltage pulses that are filtered by the inductor and the capacitor to produce smooth, lower DC voltage.

Design and Methodology

In this experiment, V_d is 14V while V_o is 9.5V. Since $V_o > V_d/2$, in this case, the first circuit in the assignment is used. The given circuit in the assignment is shown in figure 1. Since the buck converter is a negative one, it converts $-V_d$ to a smaller voltage $-V_o$.

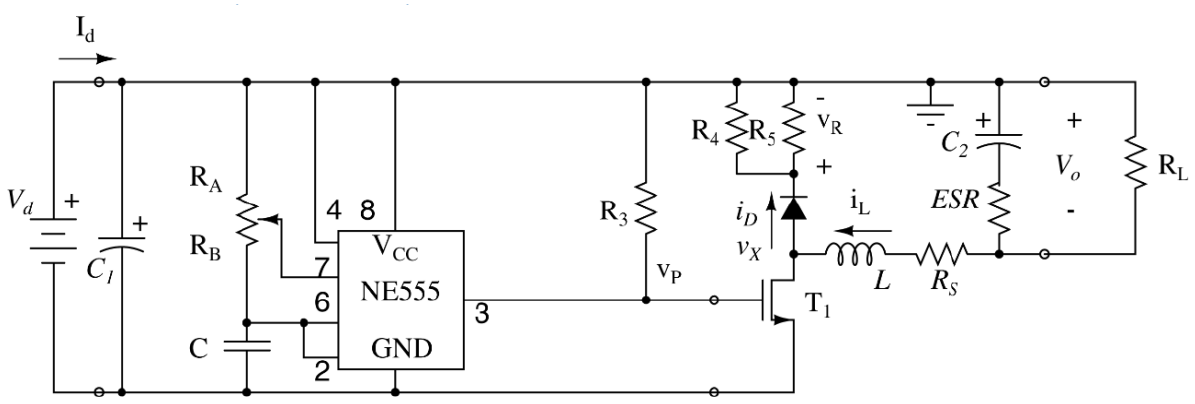

Figure 1: Given Design for Buck Converter

In this circuit, the NE555 pulse generator IC is used to generate a pulse width modulation signal that controls the switching of the nMOS. The frequency and duty cycle (D) of the square wave are determined by R_A, R_B and C. R_A and R_B resistors form a 10KΩ trimpot. Duty cycle of the pulse width modulation signal controls the average voltage applied to the inductor, hence regulating the output voltage. In this circuit, UF4007 fast diode and IRFZ44 switching transistor are used.

For C1, 100µF capacitor is used as instructed in the assignment. This capacitor acts like a power supply bypass capacitor. Which means it helps to stabilize the input voltage, reduce fluctuation and effectively filtering out unwanted noise.

R3 is a pull-up resistor connected between the output pin and the V_{cc} pin of the NE555 timer. This configuration is necessary because the NE555's output stage uses an open-collector (or open-drain) transistor, which means it can sink current but cannot source it on its own. R_3 ensures that when the internal open-collector transistor is not conducting, the voltage at the output pin is pulled up to V_{cc} This allows the output to swing between V_{cc} and 0V as needed. Without R_3, the output would be left floating when the transistor is off, resulting in unpredictable behavior or incorrect switching signals. The current through the resistor is about 20mA, so the value of it is found as

$$R_3 = \frac{V_d}{0.02} = \frac{14}{0.02} = 700\Omega$$

Since the resistors R_4 and R_5 are small and used to measure the voltage of the diode's current, their values are 1Ω.

The demonstration of the output voltage of NE555 is shown in figure 2.

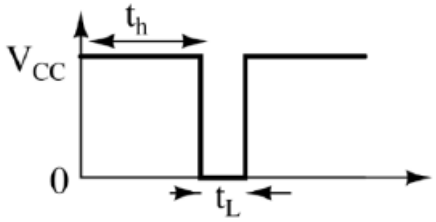

Figure 2: Output Voltage of NE555

The calculation of the duration of the high-level t_h is calculated as

$$t_h = 0.693C(R_A + R_B)$$

From the equation, the duration of the high-level is found as 15.25µs.

Hence from the equations

$$V_o = DV_d$$

$$D = \frac{t_h}{T_s}$$

The duration of the repetition period T_s is found as 22.47µs.

R_B value is calculated as

$$T_s = 0.693C(R_A + 2R_B) = 0.693C(R_A + R_B)\left(1 + \frac{R_B}{R_A + R_B}\right)$$

The value of R_B found as 4.9KΩ, so the value of R_A is 5.1KΩ

In this design, 326µH and 1.90Ω values are used for L and R_s. C value picked as 2.2nF.

Results

a) To find the maximum value of load resistance, inductor current should never be 0, hence the inductor current equation for continuous case is used for calculation as follows

$$i_L(0) = \frac{V_o}{R_L} - \frac{1}{2} \cdot \frac{V_d - V_o}{L} \cdot t_h > 0$$

$$\frac{9.5}{R_L} - \frac{1}{2} \cdot \frac{14 - 9.5}{326\,\mu H} \cdot 15.25\,\mu s > 0$$

$$9.5 - 0.105 > \frac{90.48}{R_L} \Rightarrow R_L < 90.48$$

$$\Rightarrow R_{max} \approx 90\Omega$$

Hence the maximum value of load resistance R_{max} is found as 90Ω.

$$i_{Lpeak} < 1.5A$$

$$i_{Lpeak} = i_L(0) + \frac{1}{2} \cdot \frac{V_d - V_o}{L} \cdot t_h < 1.5A$$

$$= i_L(0) + \frac{1}{2} \cdot \frac{(14V - 9.5V) \cdot 15.25\mu s}{326\mu H} < 1.5A$$

$$i_L(0) + 0.211 < 1.5A$$

$$i_L(0) < 1.29A$$

$$\frac{V_o}{R_L} - \frac{1}{2} \cdot \frac{V_d - V_o}{L} \cdot t_h < 1.29$$

$$R_L > 6.81$$

$$R_{min} \approx 7\Omega$$

Hence the minimum value of load resistance R_{min} is found as 7Ω.

b) For this part, between R_{max} and R_{min}, 68Ω is chosen for the load resistance value. The duty cycle, D, is calculated as

$$D = \frac{V_o}{V_d} = \frac{9.5V}{14V} = 0.68 = 68\%$$

c) The estimation of diode current and switch voltage is shown in figure 3.

When the switch is on, diode is off and when the switch is off, diode in on. Hence when the diode is off, it current is 0A while the voltage of the switch is equal to V_d, and when the diode is turned on and switch is off, the current through the diode came from the capacitor's storage, so it decreases linearly through time, while the voltage of the switch is 0V.

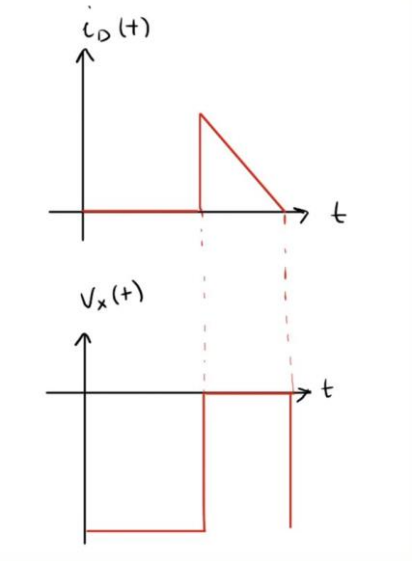

Figure 3: Estimated Plots of $i_D(t)$ and $V_x(t)$

d) The estimation of the ripple voltage dominated by ESR is calculated as follows

$$\Delta V_{ESR} = \Delta i_c \cdot R_{ESR}$$

$$\Delta i_c = \Delta i_L$$

$$\Delta V_{ESR} = (T_s - t_{on}) \cdot \frac{V_o}{L} \cdot R_{ESR}$$

$$= (22.47\mu s - 15.25\mu s) \cdot \frac{9.5V}{326\mu H} \cdot (0.25\Omega)$$

$$\Delta V_{ESR} = 0.0525V = 52.5mV$$

The plotting of the output ripple is shown in figure 4.

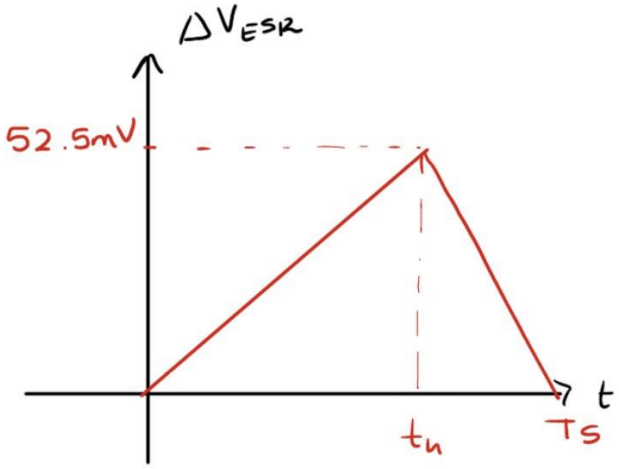

Figure 4: Estimated Plot of the Output Ripple Voltage

e) Load resistance is chosen as 150Ω. The calculation of Vo in discontinuous case is made with these equations

$$V_o = \frac{D^2}{D + \frac{I_o}{4 \cdot I_{OBmax}}} \cdot V_d$$

$$I_o = \frac{V_o}{R_L} = \frac{9.5V}{150\Omega} = 0.063A$$

$$I_{OBmax} = \frac{T_s \cdot V_d}{8L} = \frac{(22.47\mu s) \cdot (14V)}{8 \cdot (326\mu H)} = 0.121A$$

$$V_o = 10.92V$$

The estimated plot of inductor current and switch voltage is shown in figure 5. The difference between these plots and the plots from continuous case is that the switch's voltage increases to Vd before the period duration ends and the diode's current become 0A at the same time.

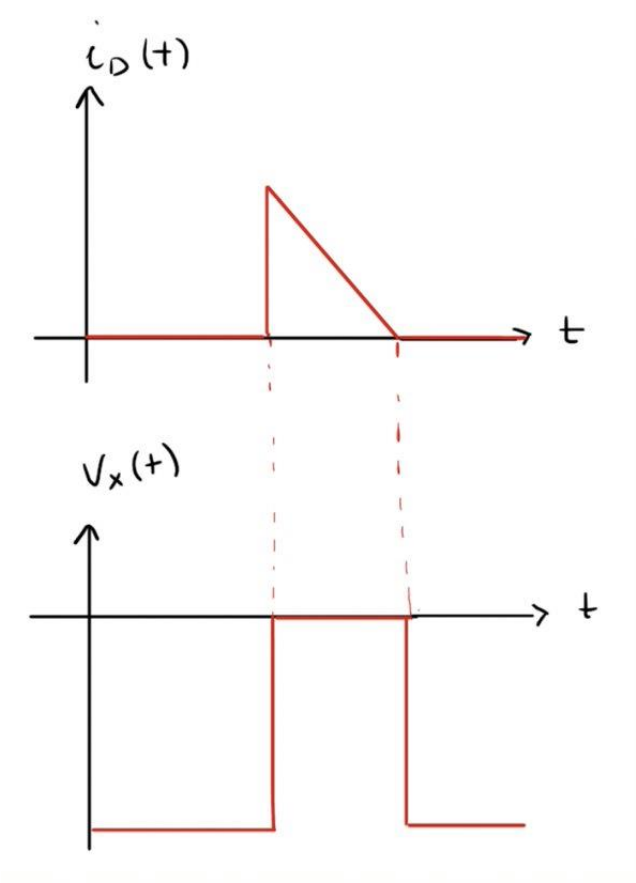

Figure 5: Estimated Plots of $i_D(t)$ and $V_x(t)$ in Discontinuous Case

f) With the same equations above which are

$$V_o = \frac{D^2}{D + \frac{I_o}{4 \cdot I_{\mathrm{OB}max}}} \cdot V_d$$

$$I_o = \frac{V_o}{R_L} = \frac{9.5V}{150\Omega} = 0.063A$$

$$I_{\mathrm{OB}max} = \frac{T_s \cdot V_d}{8L} = \frac{(22.47\mu s) \cdot (14V)}{8 \cdot (326\mu H)} = 0.121A$$

Duty cycle is found as

$$D = 0.52 = 52\%$$

The LTSpice of the buck converter circuit is shown in figure 6.

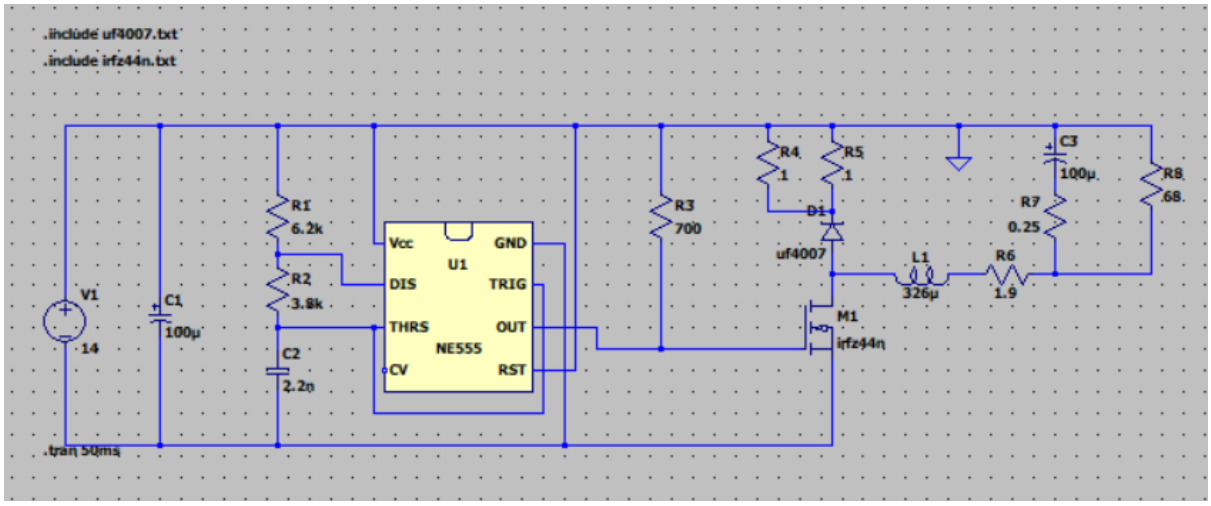

Figure 6: LTSpice Circuit of Buck Converter

g) When 68Ω is applied for load resistance and the duty cycle remains the same as found in b), the output voltage is approximately -8.7V as shown in figure 7.

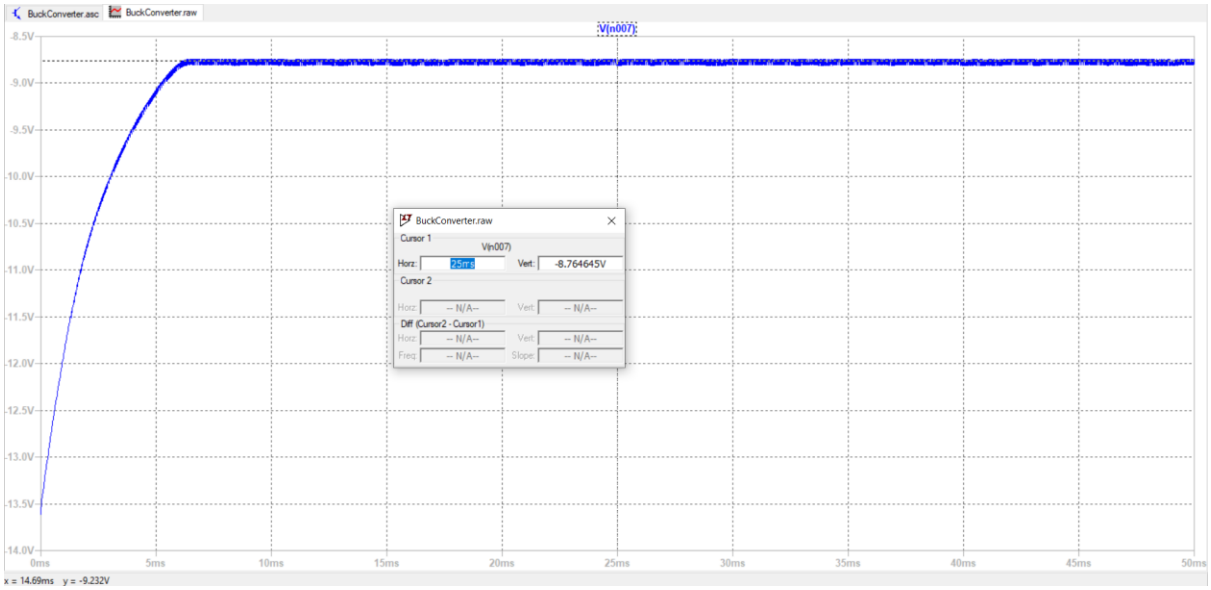

Figure 7: The Output Voltage when Duty Cycle is 0.68

The output voltage is less than required because of the voltage drop on the diodes and the resistances.

By changing the values of R_A and R_B, in other words, using the trimpot to adjust the duty cycle, the required output value is observed as shown in the figure 8. For this purpose, R_A is set to 6.2kΩ and R_B is set to 3.8kΩ.

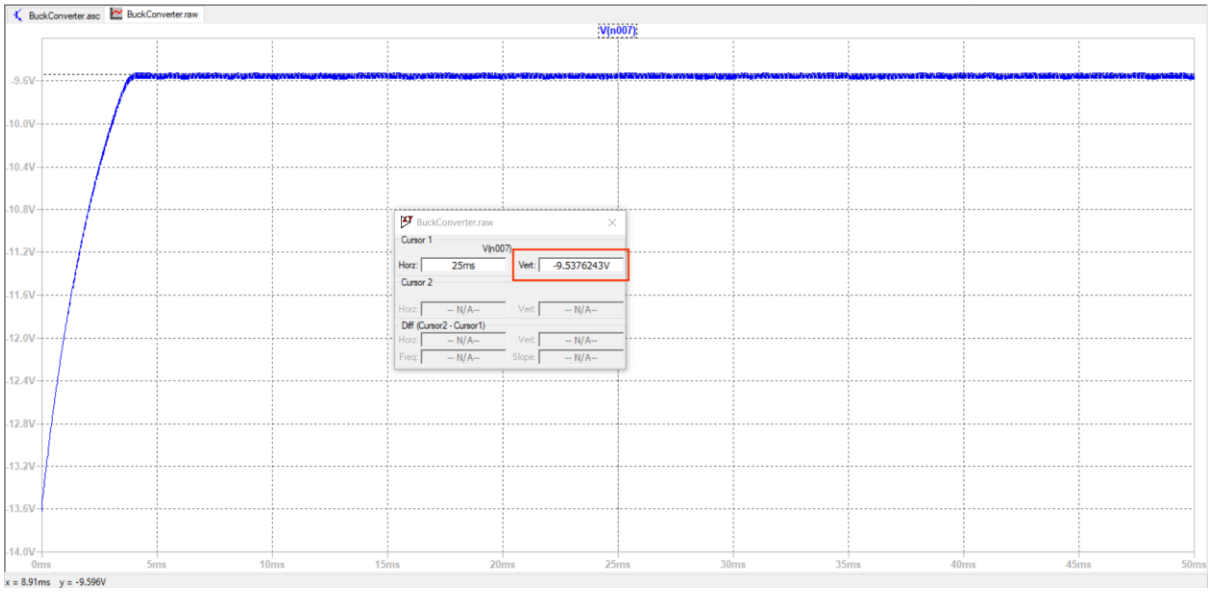

Figure 8: The Output Voltage when Duty Cycle is 0.71

The find the duty cycle the pulse graph of the NE555 is observed. From the simulation observations, T_s is found as 21.4µs which is shown in figure 9.

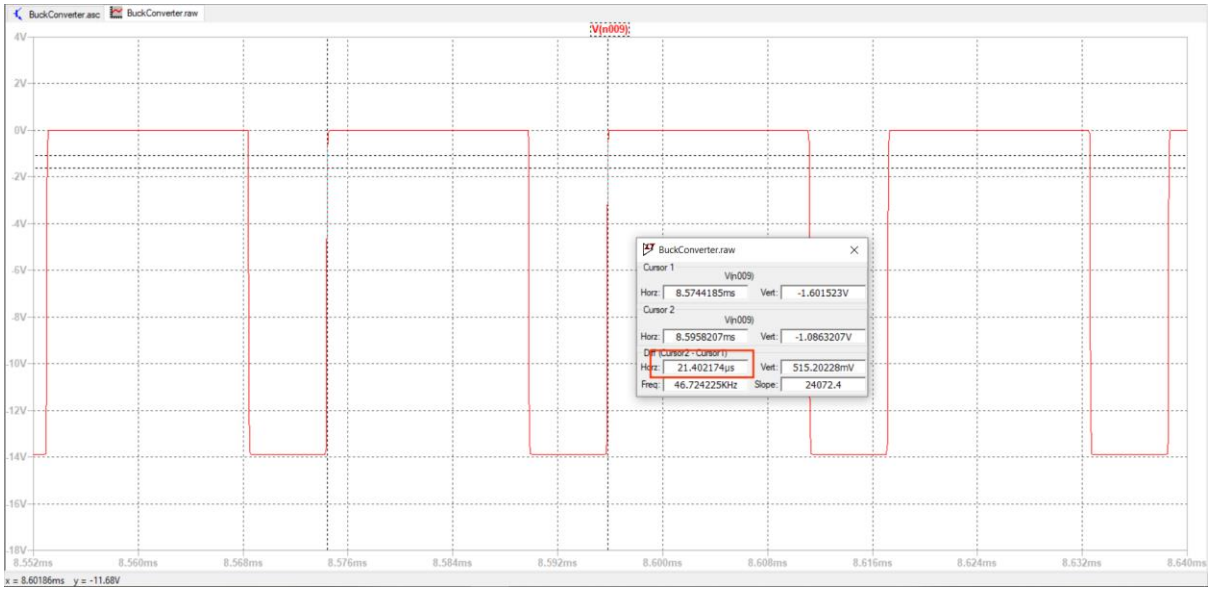

Figure 9: Simulation Value of T_s

With the same approach, t_h is found as 15.3µs which is shown in figure 10.

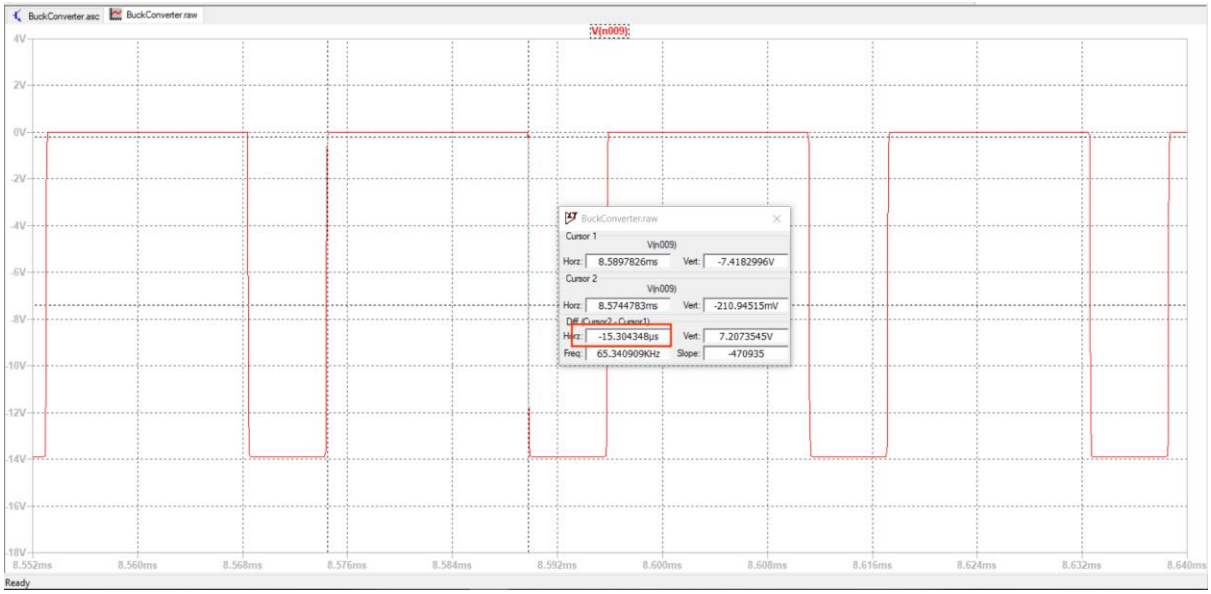

Figure 10: Simulation Value of t_h

Hence the duty cycle, D, is found as 71%.

h)

The diode current plotting, $i_D(t)$, is shown in figure 11.

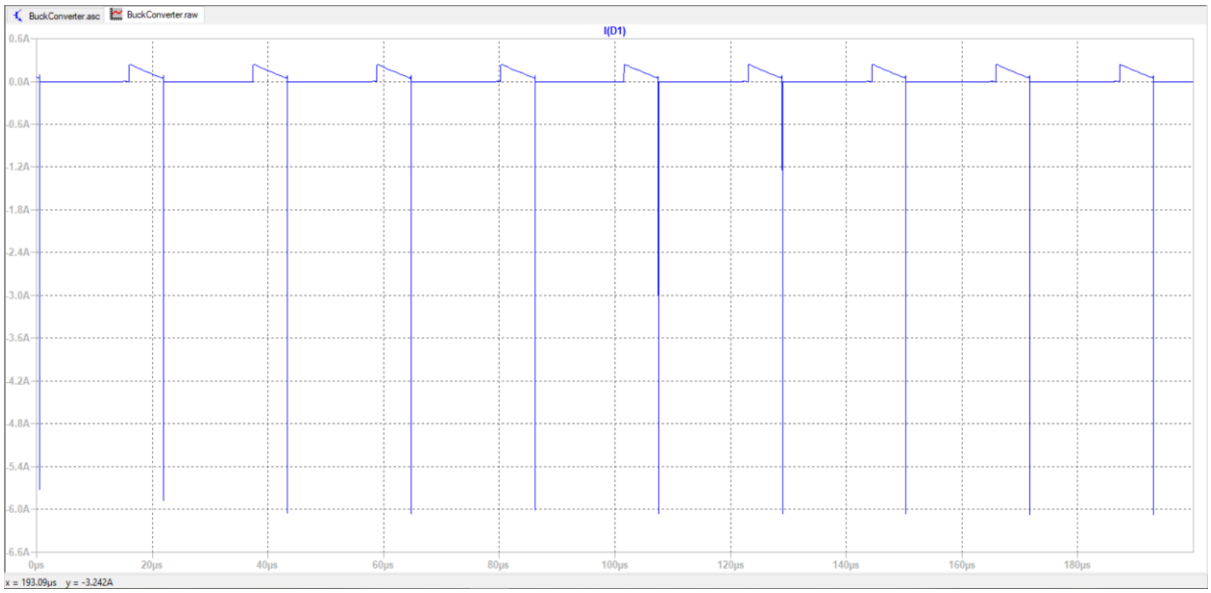

Figure 11: Plot of $i_D(t)$

The plotting of $v_X(t)$ is shown in figure 12.

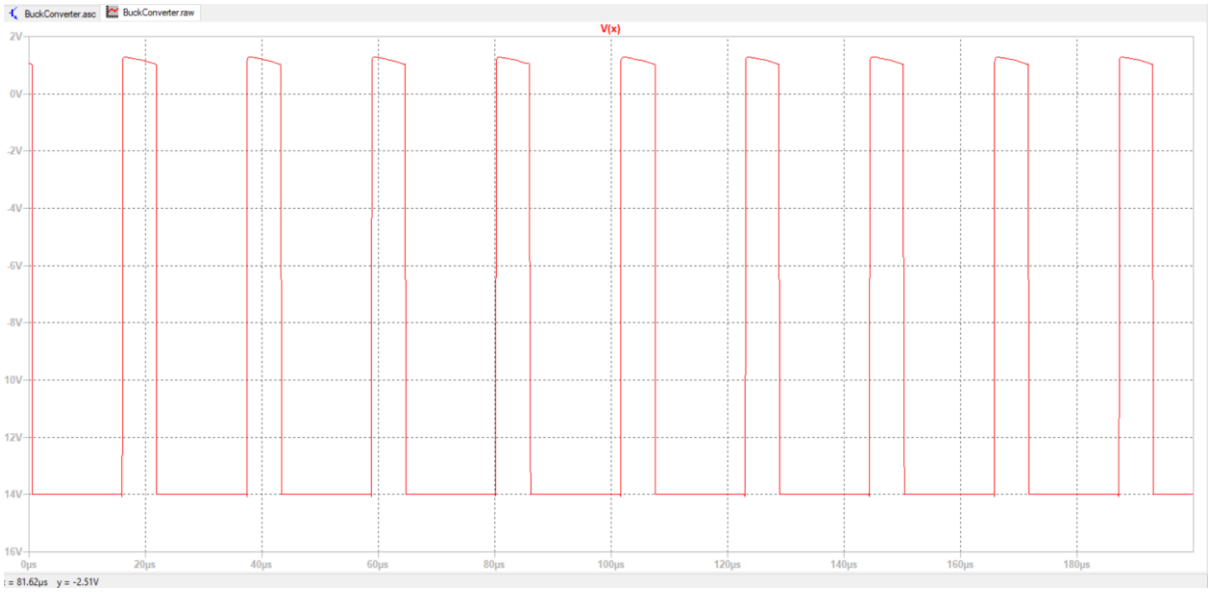

Figure 12: Plot of $v_X(t)$

i) The output voltage in PSS is shown in figure 13.

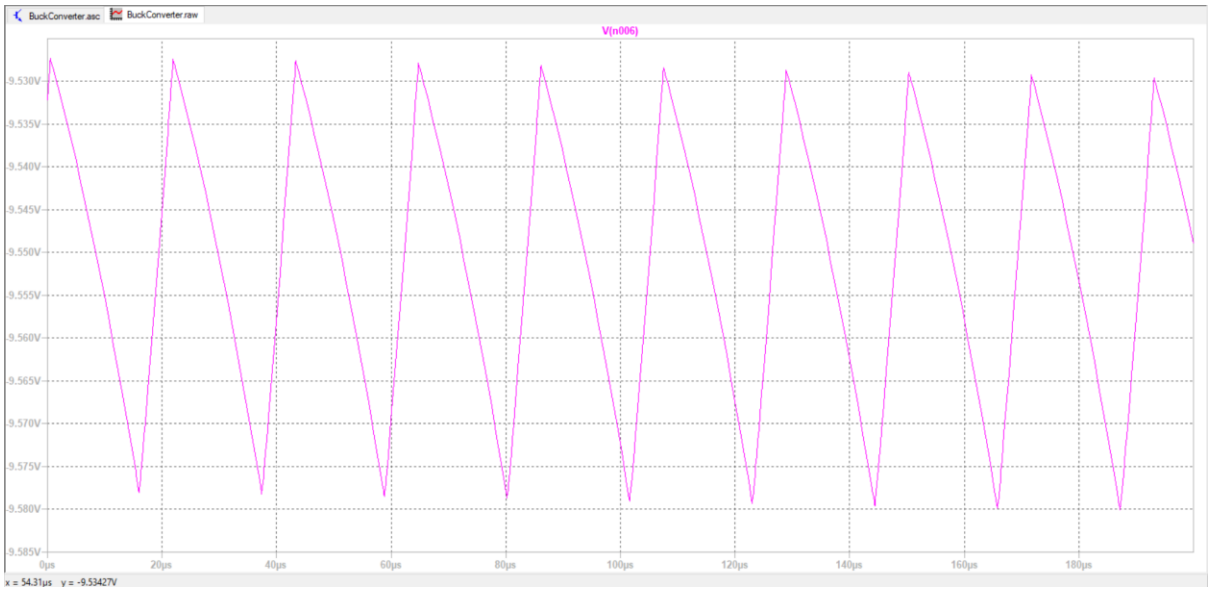

Figure 13: The Output Voltage in PSS

The ripple voltage value is shown in figure 14. The value is approximately 50.2mV

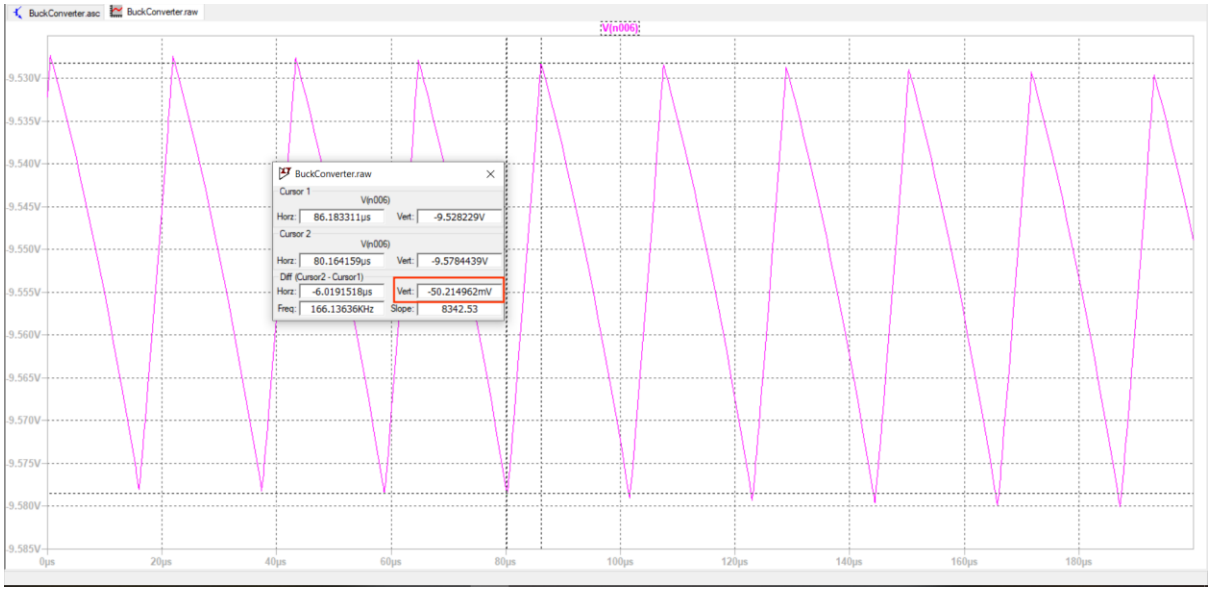

Figure 14: Peak to Peak Ripple Value

j) The value of the supply current is shown in figure 15.

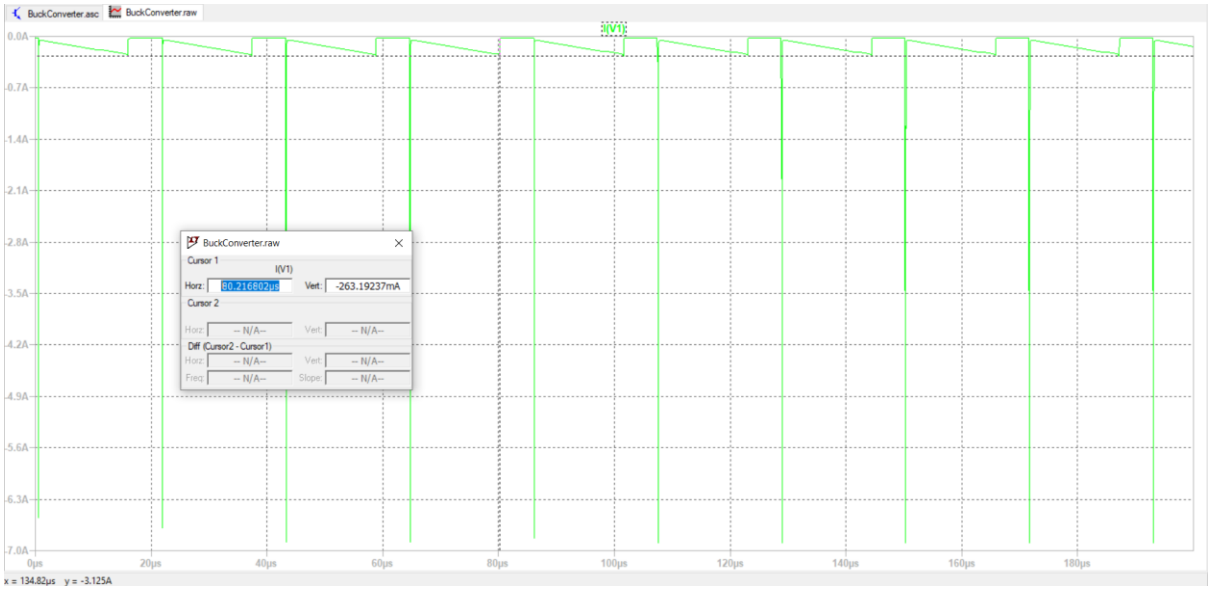

Figure 15: The Value of Supply Current

Hence P_{in} is found as 3.58W as shown in figure 16 and P_{out} is found as 1.34W as shown in figure 17.

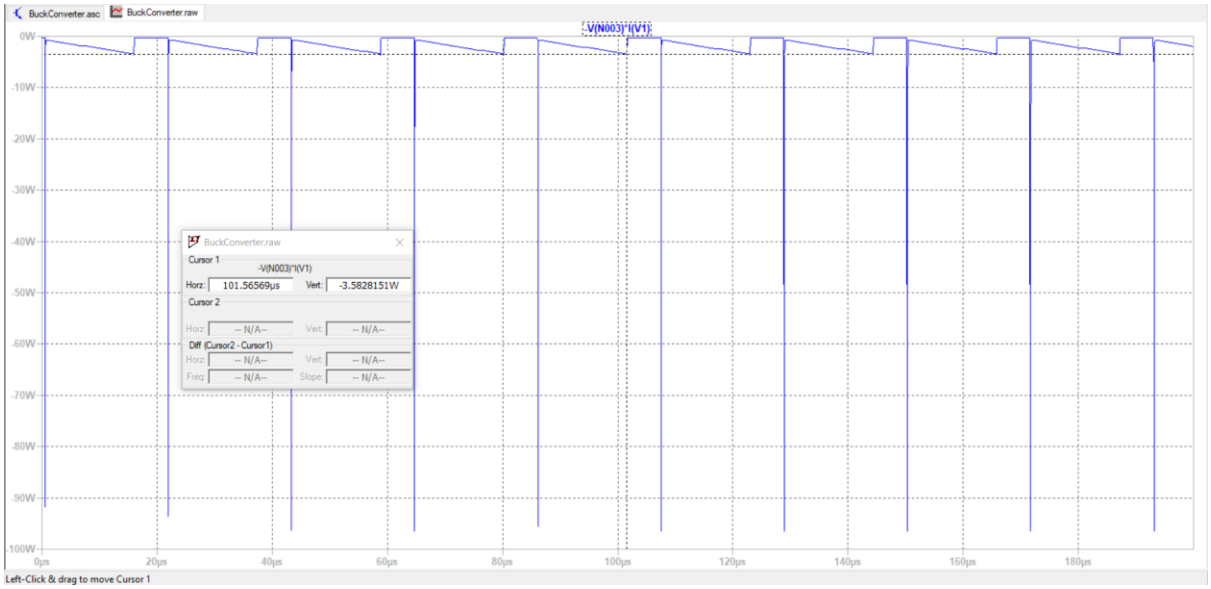

Figure 16: Plot of P_{in}

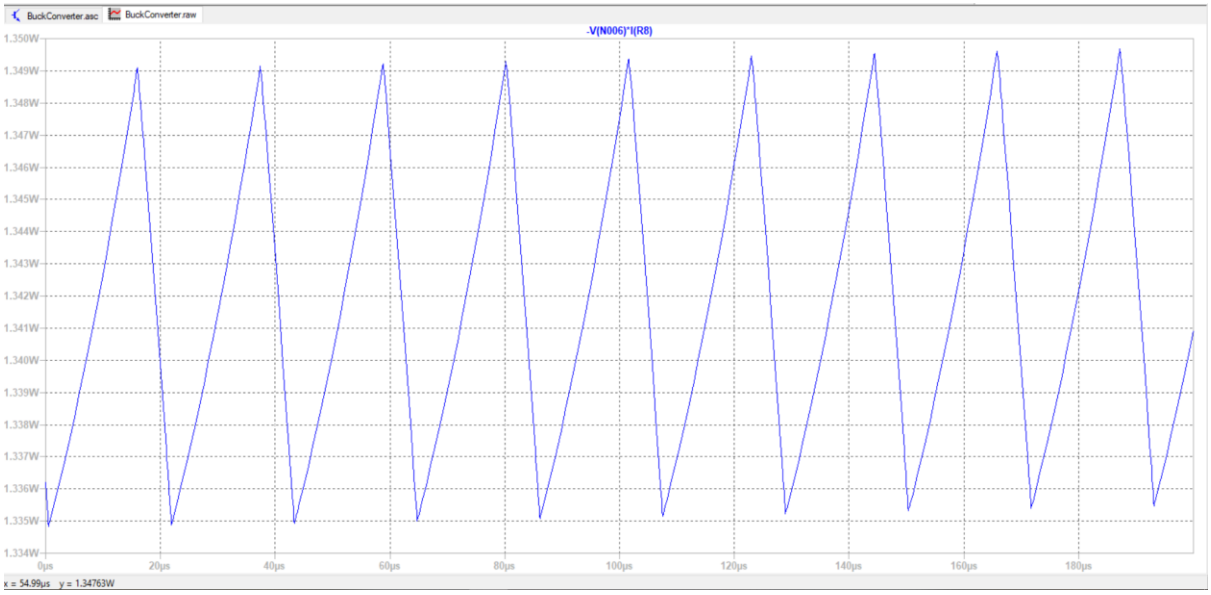

Figure 17: Plot of P_{out}

The efficiency, η, is found as 37.4%.

k) The output voltage when R_L is 150Ω is shown in figure 18. The value is approximately -10.4V which is higher than normal value in magnitude.

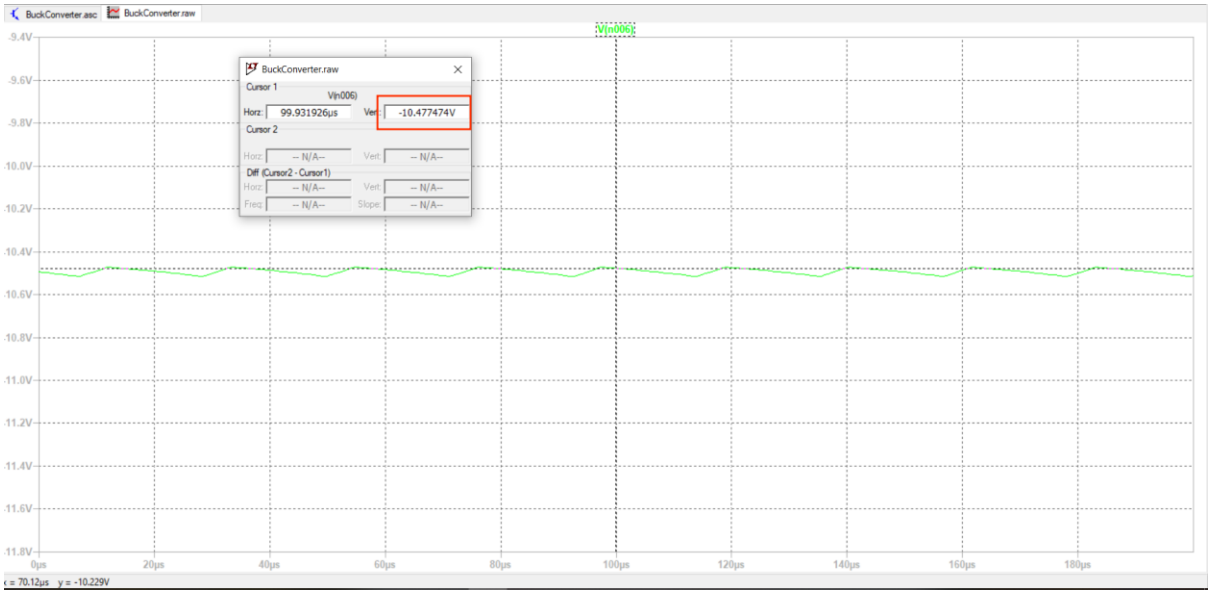

Figure 18: Plot of the Output Voltage for $R_L = 150\Omega$

I) When the resistance values are adjusted by using trimpot, R_A is set to 200Ω and R_B is set to 9.8kΩ for -9.5V output. At this duty cycle, the output plot of NE555 is shown in figure 19. T_s is shown in the same figure which has the value of 31µs.

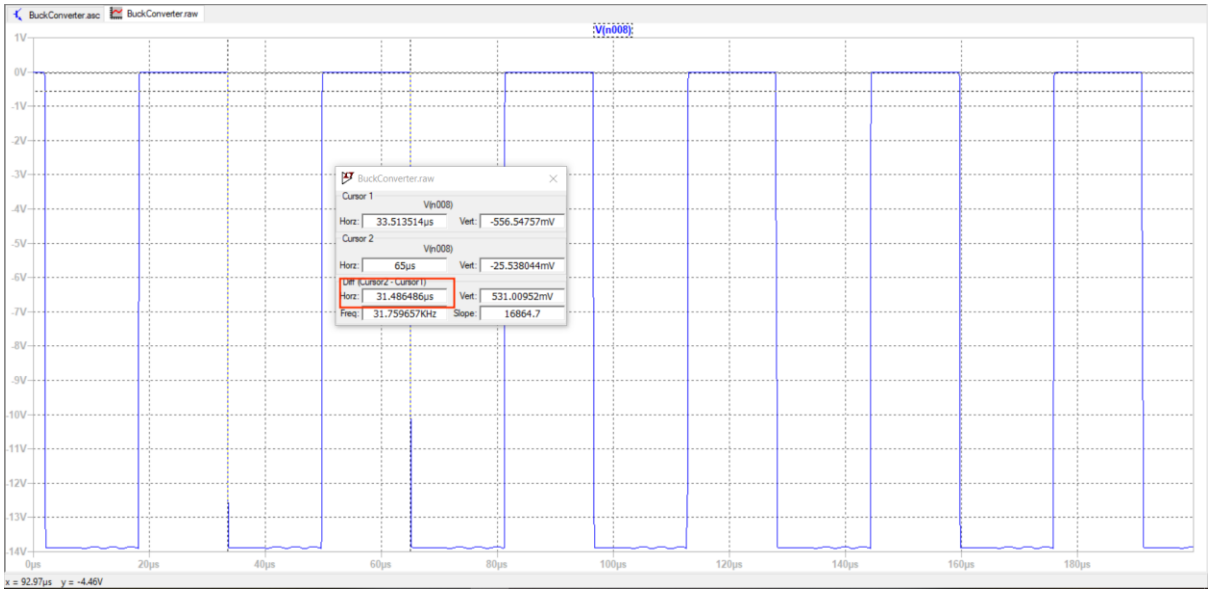

Figure 19: Output Voltage of NE555 for 150Ω Load Resistance

High level duration is shown in figure 20 which has the value of 16.2µs

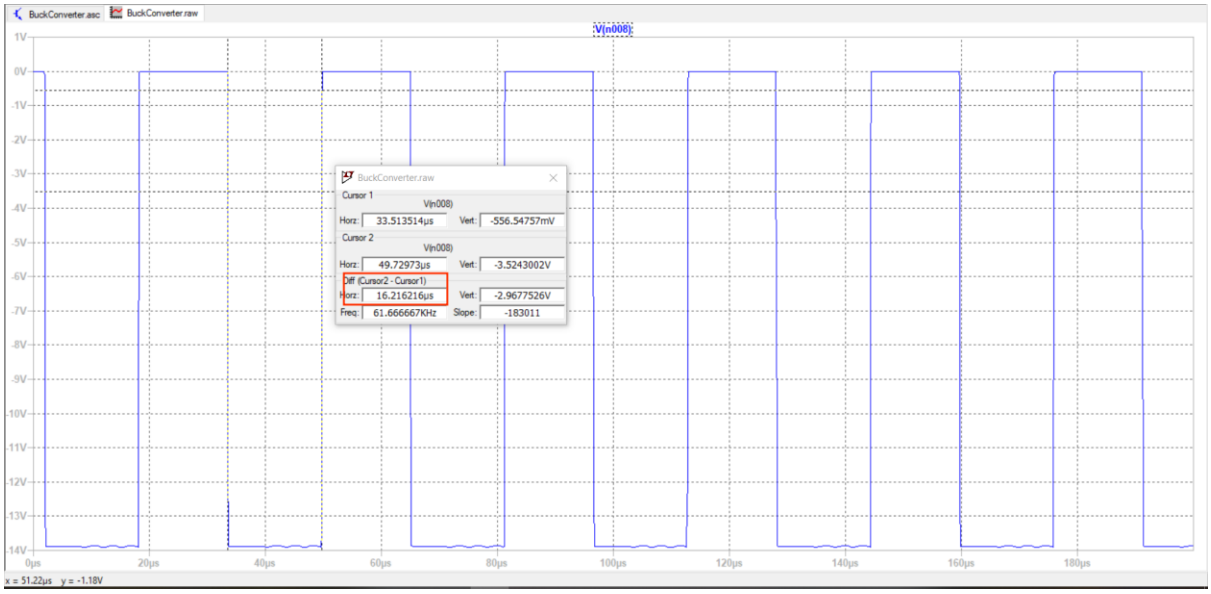

Figure 20: High Level Duration for 150Ω Load Resistance

Hence the duty cycle is found as 52.25%. This value is nearly same as the value that is found in b).

Conclusion

The preliminary part of this assignment involved analyzing the behavior of a buck converter circuit that converts a negative input voltage (\(-V_d\)) to a smaller negative output voltage (\(-V_o\)). Using theoretical calculations and component selection, the expected output voltage and circuit behavior were predicted for different load conditions. Important parameters such as the duty cycle, maximum and minimum load resistance, and component values were determined to ensure the converter operates efficiently within continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

Additionally, various configurations were explored using the NE555 timer as a pulse generator with a suitable pull-up resistor and external components to control the switching of the transistor. Theoretical calculations were used to set up the repetition frequency and the duty cycle needed to achieve the desired output voltage under different load conditions.

This preliminary work laid the foundation for understanding the behavior of the buck converter and established a reference for the experimental setup. Future experiments will verify these theoretical predictions and further investigate the converter's performance under varying load conditions using simulation and practical measurements.