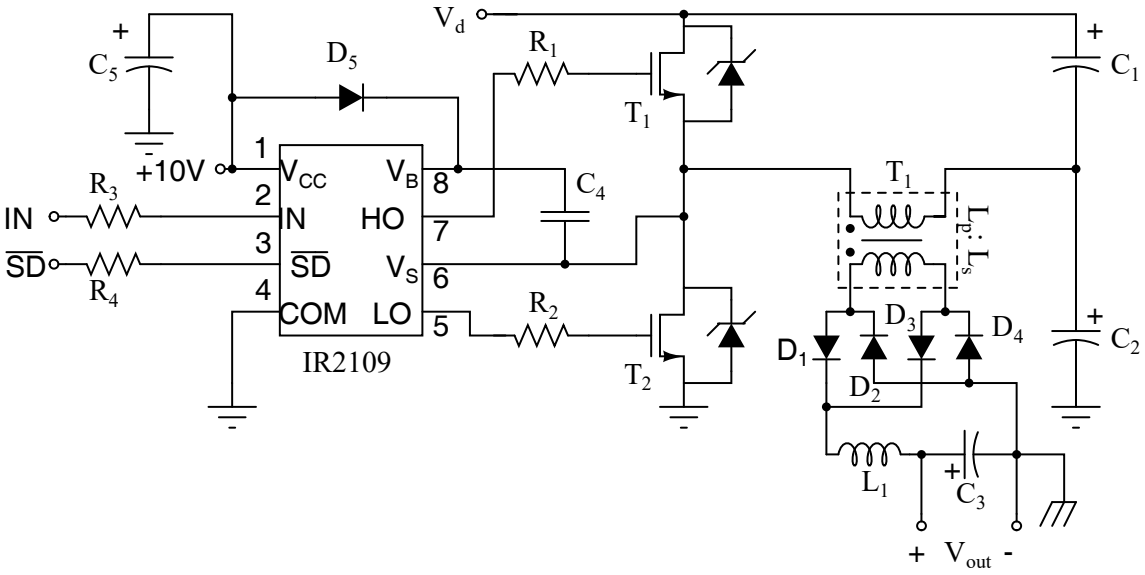
EE419/519 Experiment #2 (v2)

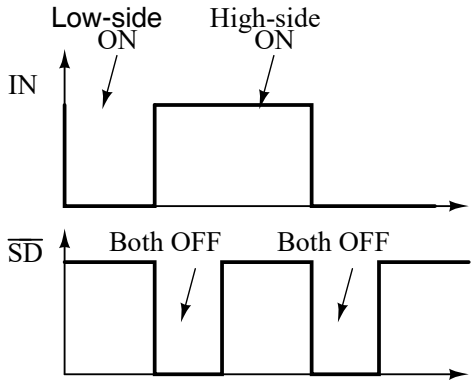
All work should be done independently

Consider the following half-bridge isolated DC-DC converter with an input voltage of V_d less than 30V. We would like to generate an isolated output voltage of V_{out} (less than 50V), delivering 2W to a selected load resistor.



MOSFET transistors T_1 and T_2 need at least 10V gate-to-source voltage to turn on well. Gate-to-source voltage of T_2 can be easily obtained, but we need a floating gate-to-source voltage to drive T_1. For example, to keep T_1 on, the gate voltage needs to be at least 25+10=35V. IR2109 is a half-bridge driver that generates both gate voltages using a separate supply voltage of +10V. With this supply voltage, it is able to generate 10V gate-to-source voltages using a bootstrap circuit consisting of D_5 and C_4. When the IRF2109 input voltage IN is less than 0.8V, its LO output becomes high (+10V) turning on the low-side MOSFET; when the input voltage is larger than 2.9V, the HO output becomes high (V_s+10V=35V) turning on the high-side MOSFET. A floating supply voltage is generated by the capacitor C4, which has a voltage of +10V. Note that for HO output to be operating properly, the input signal should be switching at every cycle. Otherwise, C4 cannot be charged in every cycle, and IR2109 is not able to turn on the high-side transistor. When the shutdown input (SD\) is smaller than 0.8V, both transistors stay off. Note that IR2109 allows the use of an input V_d voltage of up to 600V. In this experiment, V_d is kept intentionally low for safety reasons.

We need the following two signals varying between 0 to 10V to drive IR2109:



You can use NE555 and a pnp BJT to invert the signal to generate SD\ varying between 0 to 10V. The duty cycle can be adjusted using the ratio of two resistors. The duty cycle at the inverted output is given by $R_B/(R_A+2R_B)$, where R_A and R_B are timing resistors. The duty cycle at the inverted output can be adjusted between 0 to 0.5.

Design a simple digital circuit (e.g., use a negative edge triggered counter) to generate IN signal for IR2019 from SD\ signal. A negative edge-triggered CMOS counter (CD4020), which can operate from a +10V supply voltage, is available.

Component list:

C_1, C_2	150µF, 35V
C_3	100µF, 50V
C_4	50nF
C_5	10µF, 16V
R_1, R_2	33Ω
R_3, R_4	100Ω
T_1, T_2	IRFZ44N
D_1, D_2, D_3, D_4, D_5	UF2003
Load resistor	33, 47, 68, 100, 150, 220, or 470Ω
Timer	NE555
Logic	CD4020
Half-bridge driver	IR2109

Datasheets of components can be found in Moodle. As L_1, use the assigned inductor in the Lab Group 1 and Lab Group 2 documents in Moodle. The properties of the inductors are listed below. For the transformer, use the transformer you wound and characterized for the course project.

LTSpice has a model of NE555 (under the Misc directory). The model of the IRFZ44N transistor is also available in LTSpice (with the nmos symbol). The models of IR2109 and CD4020 can be found in Moodle. To set the supply voltage of CD4020, right-click on the symbol and set the VDD parameter to 10. For a successful simulation of IR2109 use the alternate solver: Tools→ Control Panel → SPICE → Engine: Solver → Alternate. For a faster

simulation, a small output capacitor (C3) and the spice initial condition directive (.IC V(Vout)=xx) should be used to set the capacitor voltages near the expected values.

Inductors:

Inductor #	L_1 (µH)	R_s (Ω) (@ 50 KHz)
1	502	0.96
2	446	1.06
3	131	0.50
4	119	0.41
5	347	0.91
7	652	1.11
8	173	0.61
9	169	0.56
11	326	0.52
12	337	0.55
13	169	1.14
14	119	0.43
17	201	0.53
18	315	0.43
24	408	0.55
25	108	1.39
26	326	1.90
27	155	0.80
28	147	1.09
29	174	0.92
30	137	0.49
31	482	1.91
33	160	0.60
34	319	0.55
35	278	0.55
36	258	0.42
37	459	1.22
40	245	1.23
41	245	1.06
45	356	0.61
47	435	1.25

Design Hints:

1. Choose a repetition period in the range of 15 to 30µs.
2. Choose a load resistor R_L suitable for your transformer. If the transformer has a turn ratio close to unity, choose a smaller load resistor from the list. If the transformer has a higher turn ratio, choose a larger load resistor from the list. Set V_{out} so that 2W is delivered to the chosen load resistor (V_{out}^2/R_L=2W) . Choose V_d and D such that V_{out} is obtained at the output. Note that you can adjust D between 0 to 0.25. Note that since $L_1 \gg L_S$, the simple formula $V_{out}=V_dD\,(N_2/N_1)-1.7$ (1.7V is the forward voltage drop of two diodes of full wave rectifier) does not apply. The output voltage will be higher than the voltage expected from the formula.

Preliminary work: (Due November 22, 2024):

A. Model NE555 oscillator in LTSpice. Set its duty cycle and operation frequency at the intended values by choosing the timing resistors and the capacitor of NE555. Note that the duty cycle and repetition frequency of the NE555 should be chosen twice the calculated values. Plot the output waveform for SD\ signal for a few cycles.

B. Add the circuit for CD4020 to LTSpice. Plot the output waveform for IN signal for a few cycles.

C. Add LT2109 and half-bridge transistors. Plot the voltages at the gates and bridge midpoint for a few cycles.

D. Add the transformer and the capacitors of the half-bridge. Set the coupling coefficient between the primary and secondary inductances of the transformer as the measured value. Insert the measured coil resistors in the model. Plot the current in the primary and secondary of the transformer for a few cycles in PSS. Increase the repetition frequency if the current peak in the primary exceeds 2A in PSS. Insert a 22K resistor in parallel with the output of the transformer to reduce oscillations.

E. Add the remaining parts of the circuit (D_1-D_4, L_1, C_3, and load resistor). Insert the series resistor R_S of L_1 in the model. Set the input voltage V_d to the calculated value so that you get the intended output voltage. You may need to increase the input voltage and/or the duty cycle to compensate for the losses. Plot the L_1 current and the output voltage in PSS for a few cycles.

F. Determine the efficiency of the converter while it is delivering 3W to the chosen load resistor. Measure the efficiency while the plot window shows an integer number of cycles.

Experimental work (Report due November 29, 2024):

Extreme care should be used with power electronics circuits. Since high currents or high voltages may be involved, power dissipation in components may occur. Overvoltages or reverse voltages may cause dangerous explosions of electrolytic capacitors. Follow the steps below carefully.

A. Set up the circuit for NE555 on a breadboard. You may use the upper supply bar of the breadboard for +10V and GND. Make sure that you have a decoupling capacitor (0.1µF) between the supply voltage (10V) and GND. Check the output voltage using the oscilloscope. Test its operation before the next step.
B. Add the pnp transistor inverter circuit. Check its output voltage using the oscilloscope.
C. Add the circuit for CD4020. Add another decoupling capacitor close to its supply voltage. Check that the output of CD4020 is as expected.
D. Set up the circuit for IR2109 and the half-bridge transistors. You need another power supply decoupling capacitor near its supply voltage. The total current from the +10V supply should be less than 30mA.
   Use the bottom supply bar of the breadboard for V_d and GND. Make sure that the upper and lower GND lines are connected to each other. Increase the input voltage V_d slowly up to the value found in the preliminary while observing the current (no current should be flowing). Observe the voltages at transistor gates and the half-bridge midpoint. Use SD\ signal as external sync of the oscilloscope.
E. Add the transformer and the capacitors of the half-bridge. Increase the input voltage V_d starting from zero while observing the current. A small current (less than 30mA) must be flowing. Record the secondary voltage of the transformer. Note that without the load resistor, the voltage at the secondary may be high if V_d is increased.
F. Add the diodes (D_1-D_4). Observe the rectified voltage as you increase the input voltage V_d. Since the load is not yet connected, a small current must flow.
G. Connect L_1, C_3, and the load resistor. As you increase the input voltage V_d, a significant current begins to flow. Set V_d to the simulated value. Measure the output voltage.
H. Change the input voltage so the output voltage is at the intended value. Record the input voltage and the efficiency.