Bengisu Münteha Koç

21801974

EEE 419 – 01

23.11.2024

EEE 419 Experiment 2: Half-Bridge Isolated DC-DC Converter

Introduction

The objective of this experiment is to design a half-bridge isolated DC-DC converter.

The half-bridge isolated DC-DC converter is a widely utilized topology in power electronics due to its ability to provide electrical isolation and efficient voltage conversion. This experiment focuses on designing and analyzing a half-bridge isolated DC-DC converter with an input voltage (V_d) less than 30V, delivering an isolated output voltage (V_{out}) less than 50V while supplying 2W of power to a selected load resistor.

A critical aspect of the experiment is the use of a half-bridge driver (IR2109) to generate the gate drive voltages for the two MOSFET transistors (T1 and T2), enabling efficient switching and power transfer. The circuit incorporates a bootstrap mechanism to provide the floating gate drive voltage required for the high-side transistor. Additionally, a digital signal generator is employed to control the operation of the driver, ensuring proper timing and functionality.

The objective of the experiment is to evaluate the design, implementation, and efficiency of the converter under varying load and input conditions. Key components include NE555 as a signal generator, a CD4020 CMOS counter for signal processing, and an IR2109 driver to manage the switching. Simulation and experimental results are compared to theoretical expectations, with a focus on determining the efficiency and operational stability of the system.

This report details the design considerations, circuit implementation, and analysis of the half-bridge isolated DC-DC converter, emphasizing the interplay between theory and practical performance. Safety precautions are highlighted throughout the experiment to mitigate risks associated with high voltages and currents in power electronics circuits.

Design and Measurements

Repetition period of the converter, T_s, is chosen as 20μs. The ratio $\frac{N2}{N1}$ is not close to unity, hence the load resistance value is chosen as 220Ω.

The output voltage value is calculated as

$$P = \frac{V^2}{R} = 2W$$

Since the required power dissipation on load resistor is this. The output voltage value is found as

$$\mathrm{V_{out}} = 21V$$

With this value, input voltage and duty cycle will be determined as follows

$$\frac{V_d \cdot D \cdot T_S}{2 \cdot L_M} = \mathrm{i_{Mpeak}}$$

$$V_o = V_d \cdot \frac{N_2}{N_1} \cdot D\left(2 - \frac{I_o \cdot \frac{N_2}{N_1}}{I_{M\mathrm{peak}}}\right)$$

Since the primary part of the transformer value is 37.87µH and k is 0.92, L_M value is found as

$$L_M = L_1 \cdot k = 34.84\mu H$$

With these values the DV_d value is calculated as 8.04. Then the duty cycle value is chosen as 0.4. Hence the input voltage value, V_d, is found as 20.1V.

NE555 is used as a signal generator in this converter. Since the inverted output is used as input for the CMOS counter, the repetition period and the duty cycle is double of the chosen values. Since the first output pin of the counter will be used for IR2109 and this pin is dividing the input frequency by 2, repetition period and duty cycle of NE555 is doubled.

NE555 is used in Astable Operation mode. Hence, by referring to the datasheet of the component, these equations are used for obtaining the values of timing resistors and timing capacitor.

$$t_H = 0.693 \cdot (R_A + R_B) \cdot C$$

$$t_L = 0.693 \cdot R_B \cdot C$$

R_A is found as 5.6KΩ R_B is found as 10KΩ and C is found as 2.2nF.

With these values, the output signal of NE555 is observed as shown in Figure 1.

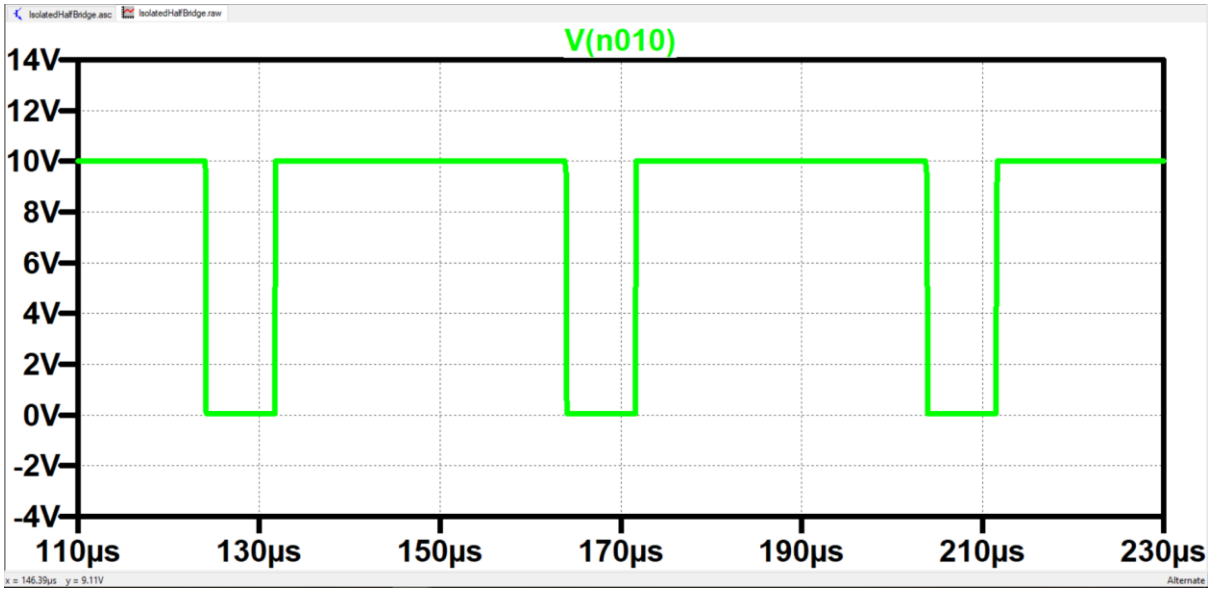

Figure 1: Output Signal of NE555

The repetition period and t_{on} of NE555 are shown in figures 2 and 3, respectively.

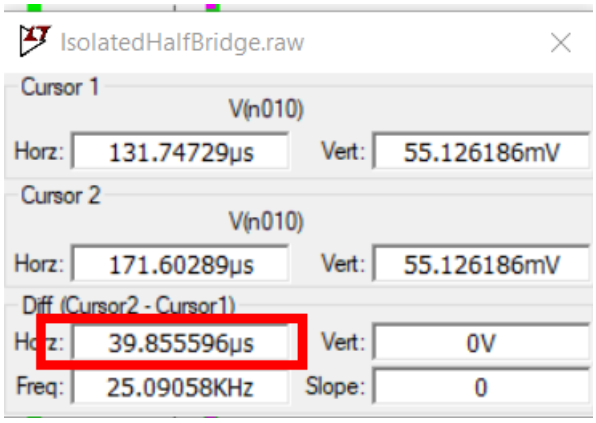

Figure 2: Repetition Period of NE555

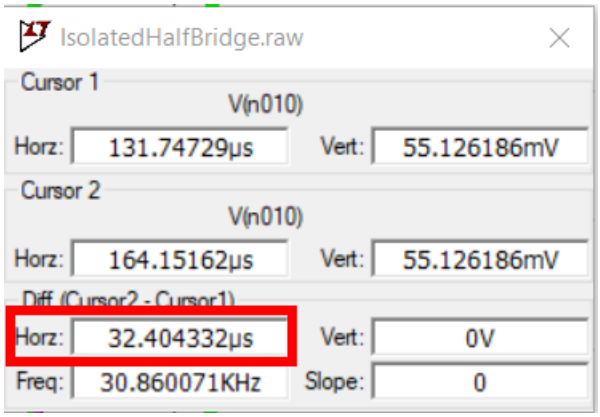

Figure 3: t_{on} of NE555

Hence the duty cycle of signal generator is found to be 0.81. This the double of the chosen duty cycle for converter. This signal is connected to the base of a PNP transistor (BC308) to invert the signal. This transistor is used as a switch. The signal is inverted because CD4020B counter is the negative edge triggered.

The inverted output signal is connected to the counter and the output of the first pin is observed as shown in Figure 4.

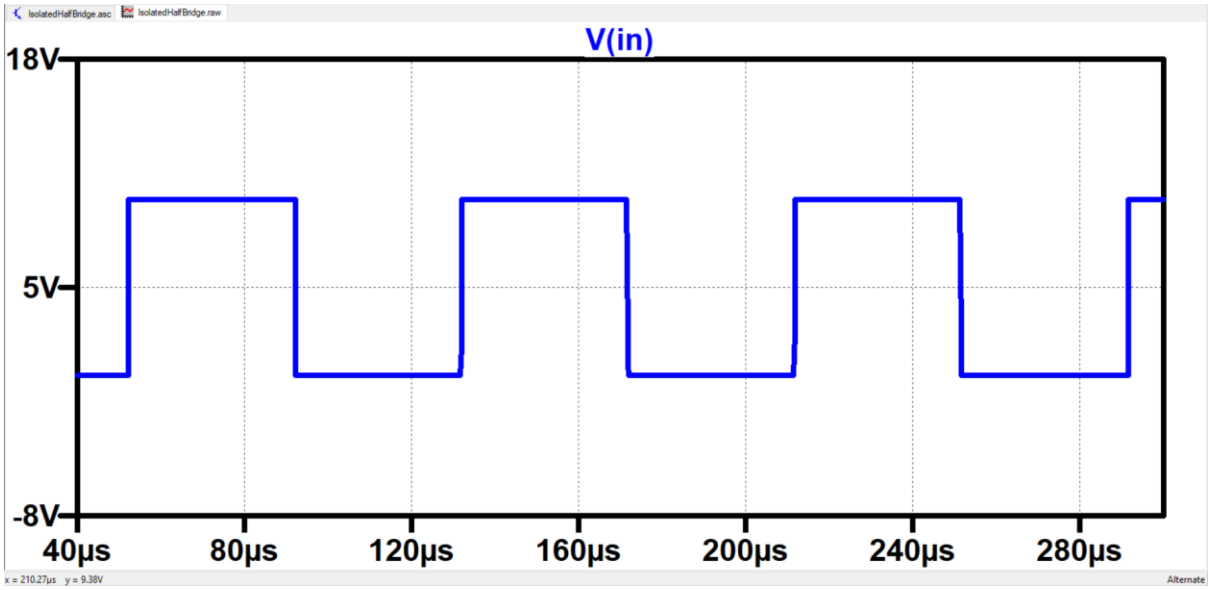

Figure 4: Output of the Counter CD4020B

The repetition period and ON duration of the signal are shown in figures 5 and 6, respectively.

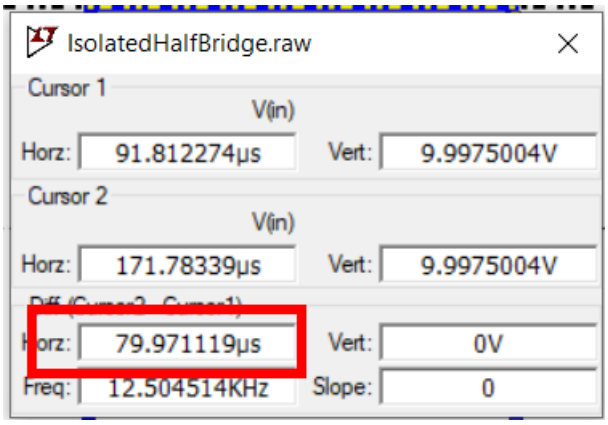

Figure 5: Repetition Period of the Counter

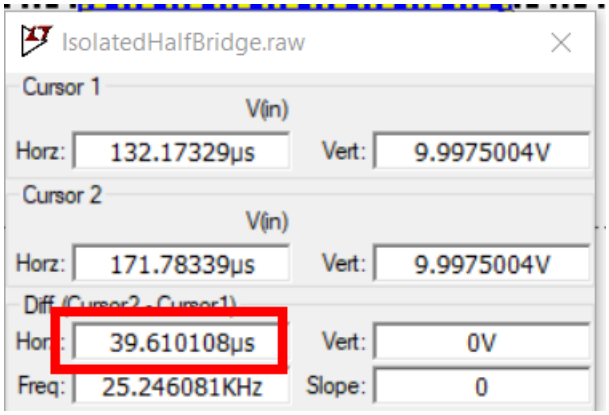

Figure 6: ON Period of the Counter

The observation of both SD\ and IN is shown in Figure 7.

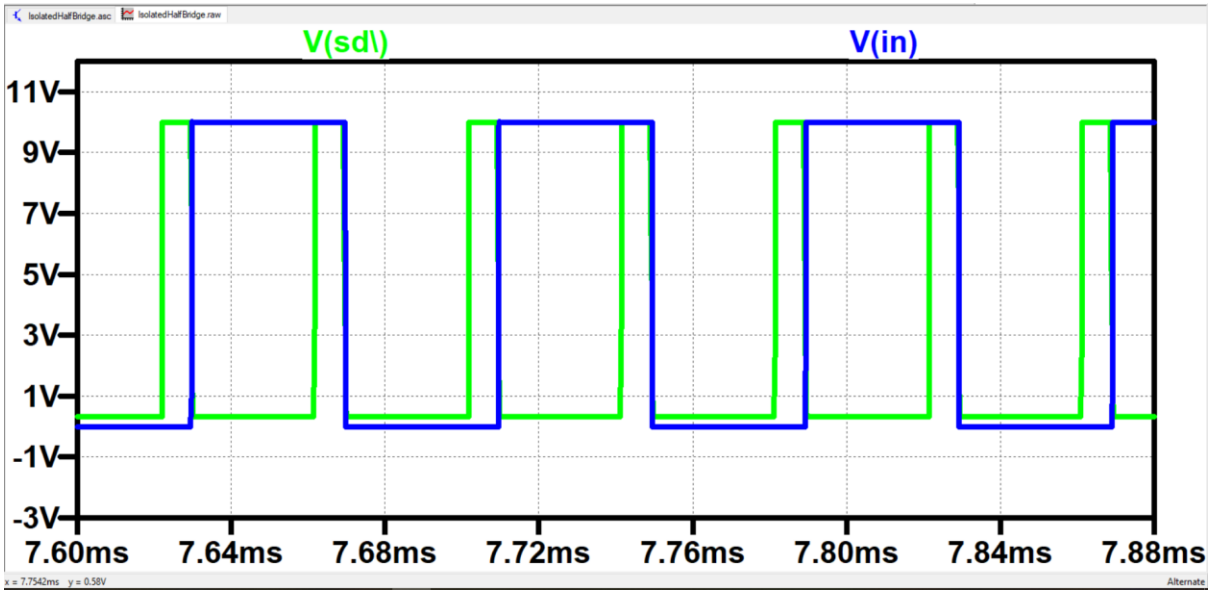

Figure 7: SD\ and IN Signals

The driver and the other components are added to the circuit with suggested values. The circuit of the converter is shown in Figure 8.

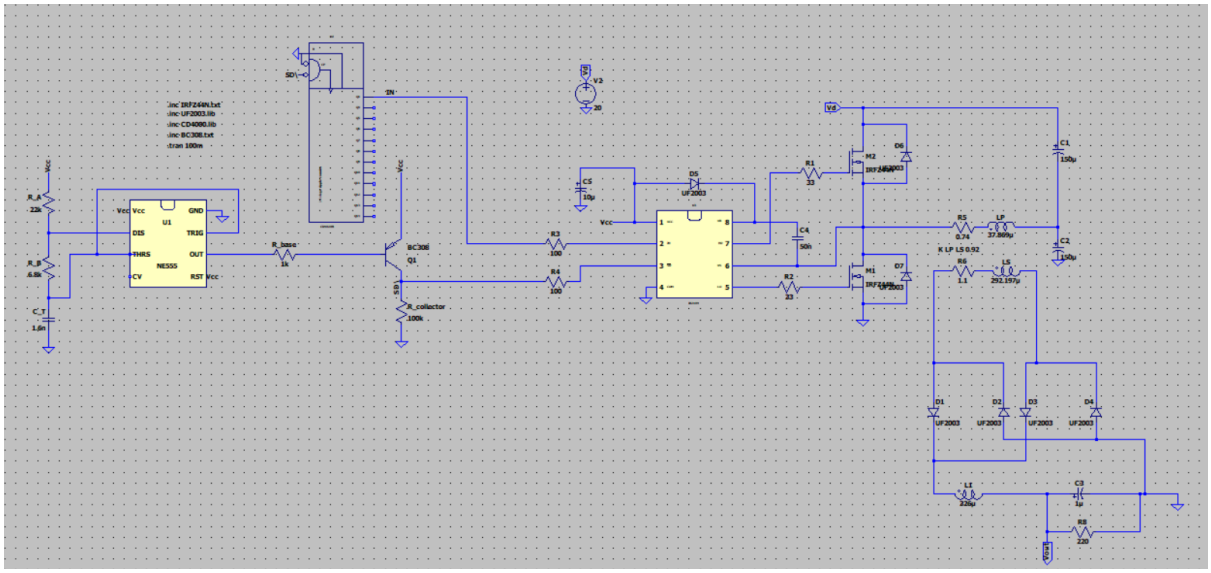

Figure 8: Half-Bridge Isolated DC-DC Converter Circuit

Gate voltage of the first MOSFET is shown in Figure 9.

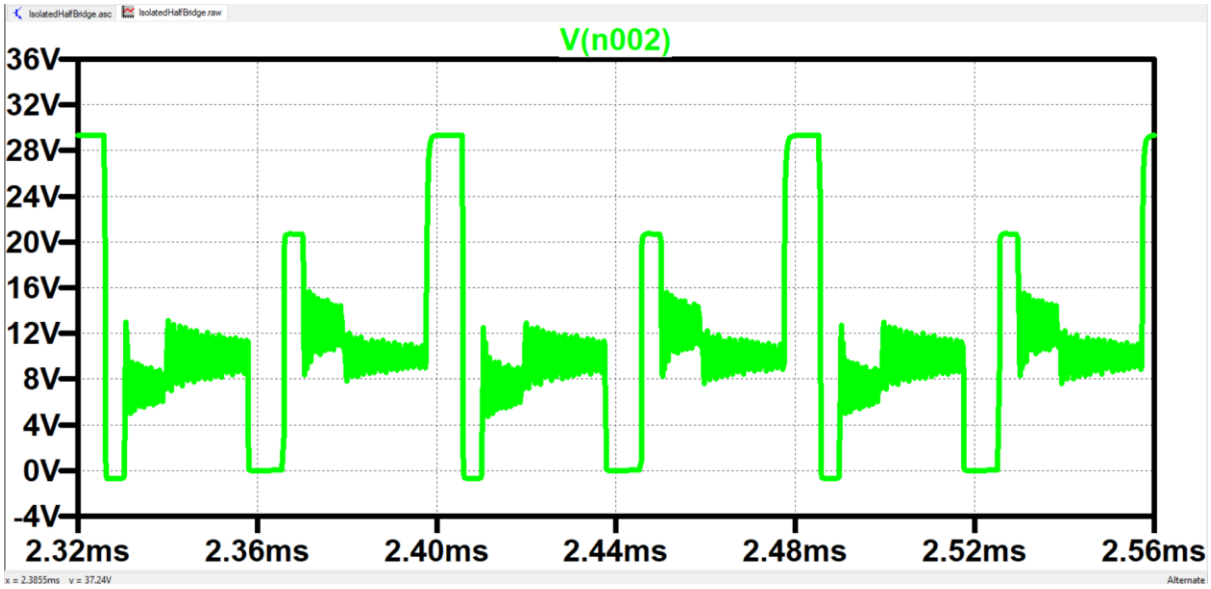

Figure 9: Gate Voltage of the T1

Gate voltage of the second MOSFET is shown in Figure 10.

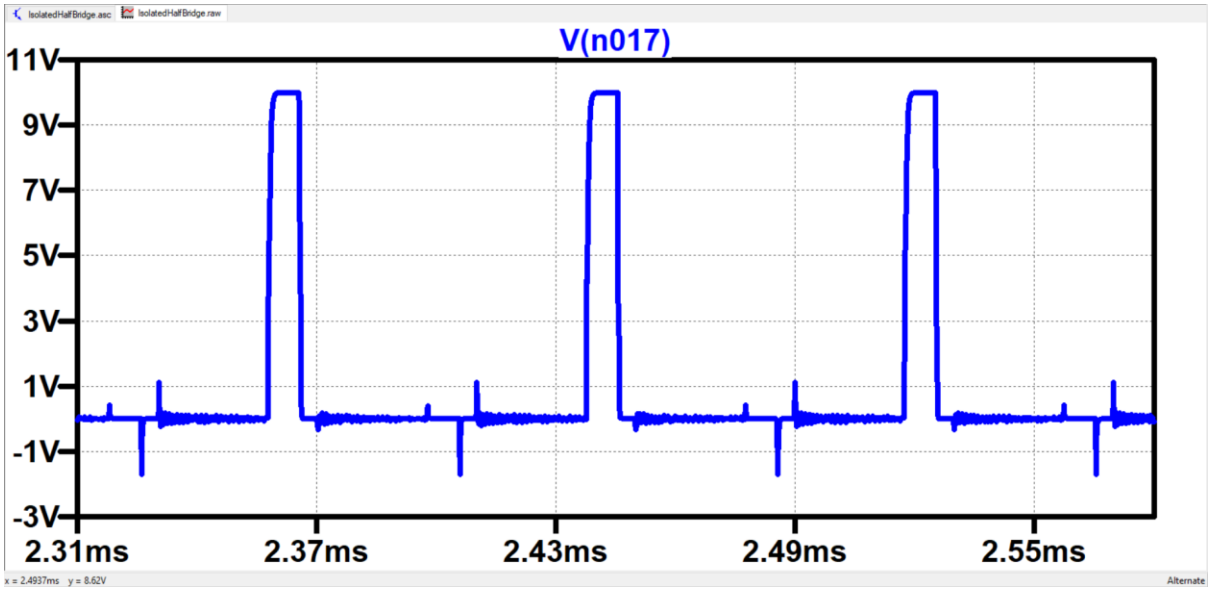

Figure 10: Gate Voltage of T2

The voltage graph of the bridge midpoint is shown in Figure 11.

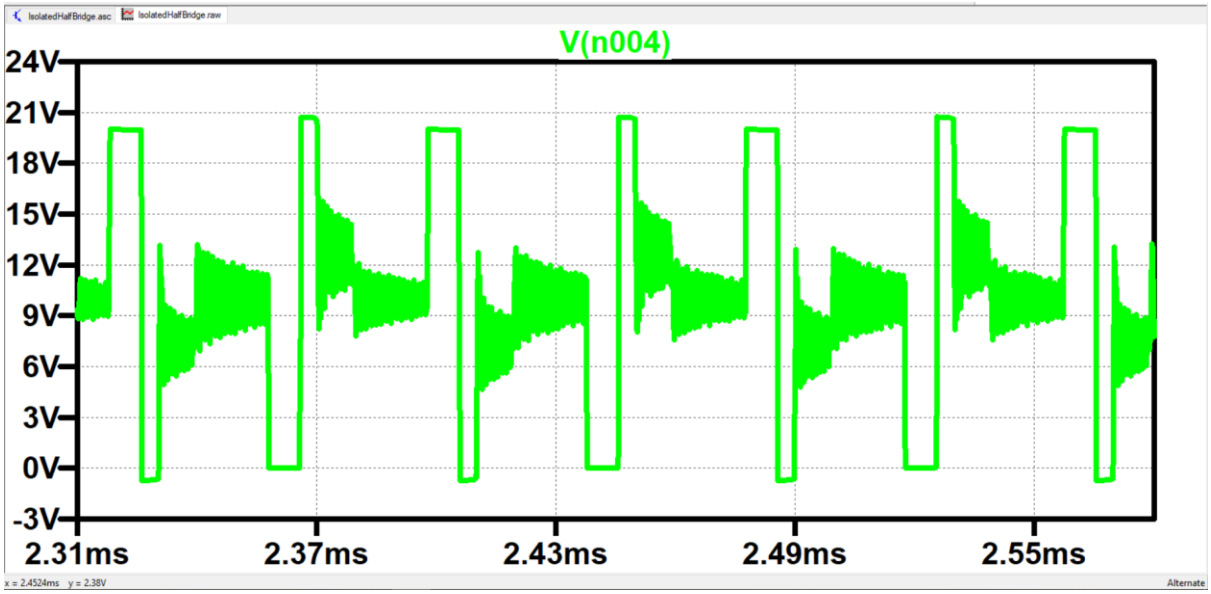

Figure 11: Voltage of the Bridge Midpoint

The current graph of the primary part of the transformer is shown in Figure 11.

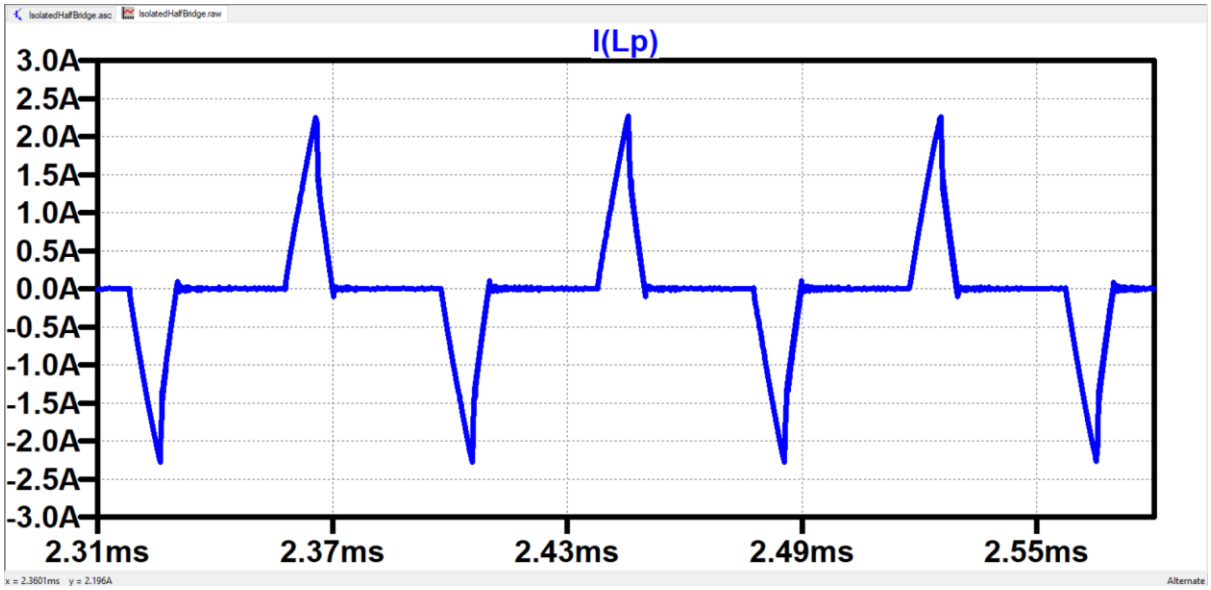

Figure 11: Current of the Primary of the Transformer

The current graph of the secondary of the transformer is shown in Figure 12.

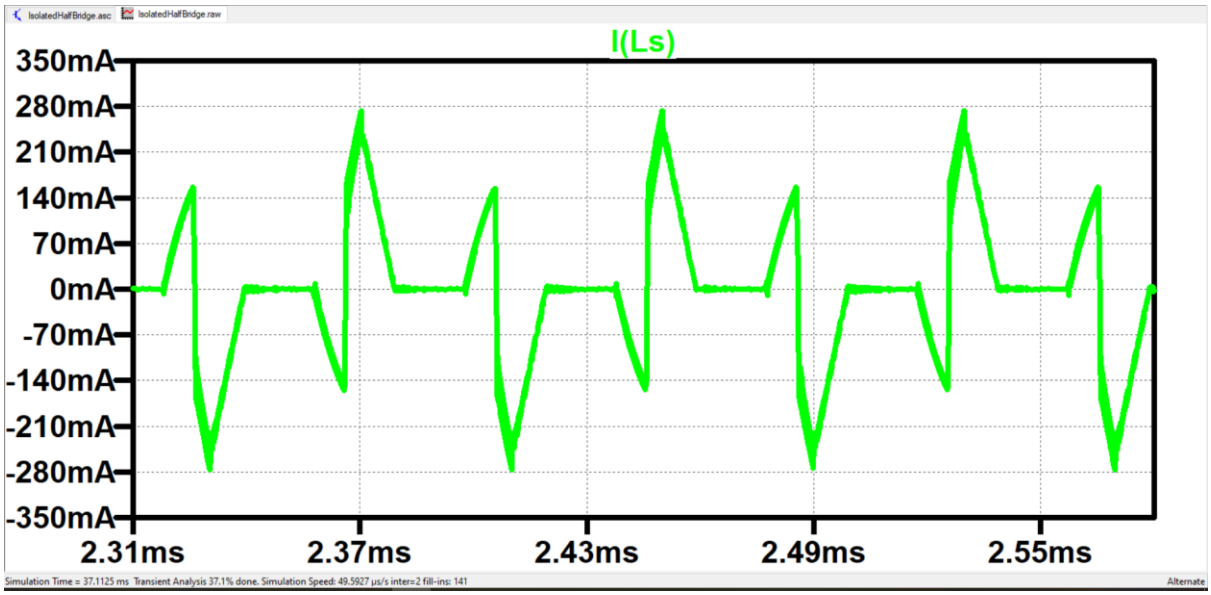

Figure 12: Current of the Secondary of the Transformer

Since the output of the converter is lower than expected, the input value is increased by 2V, duty cycle is decreased to 0.3 and the repetition period is dropped to 15µs to compensate the losses.

Simulated value of the output voltage is shown in Figure 13.

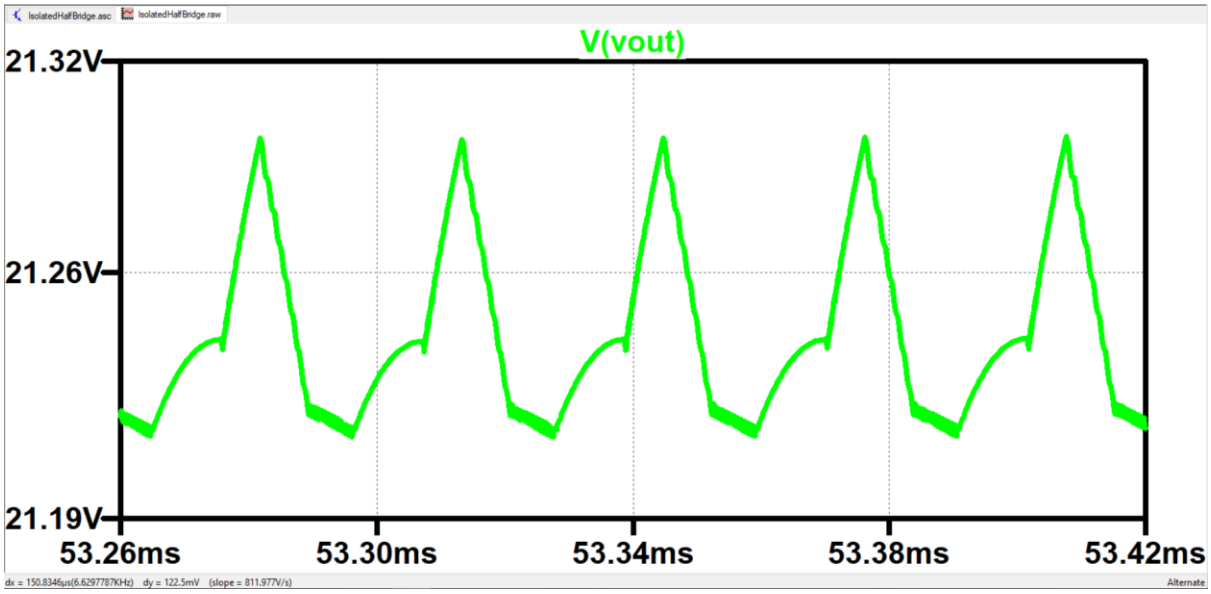

Figure 13: Output Voltage Graph

As can be seen from the above figure, the output voltage is 21V, as calculated.

The current of L_1 is shown in Figure 14.

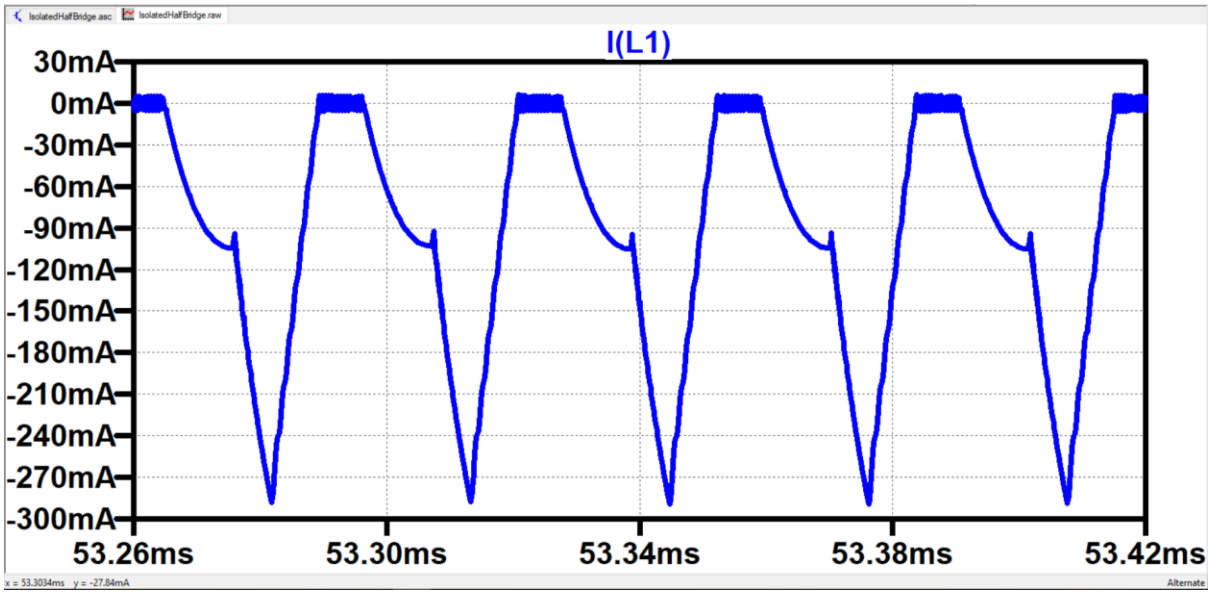

Figure 14: Current Graph of L_1

The output power graph of the converter is shown in Figure 15.

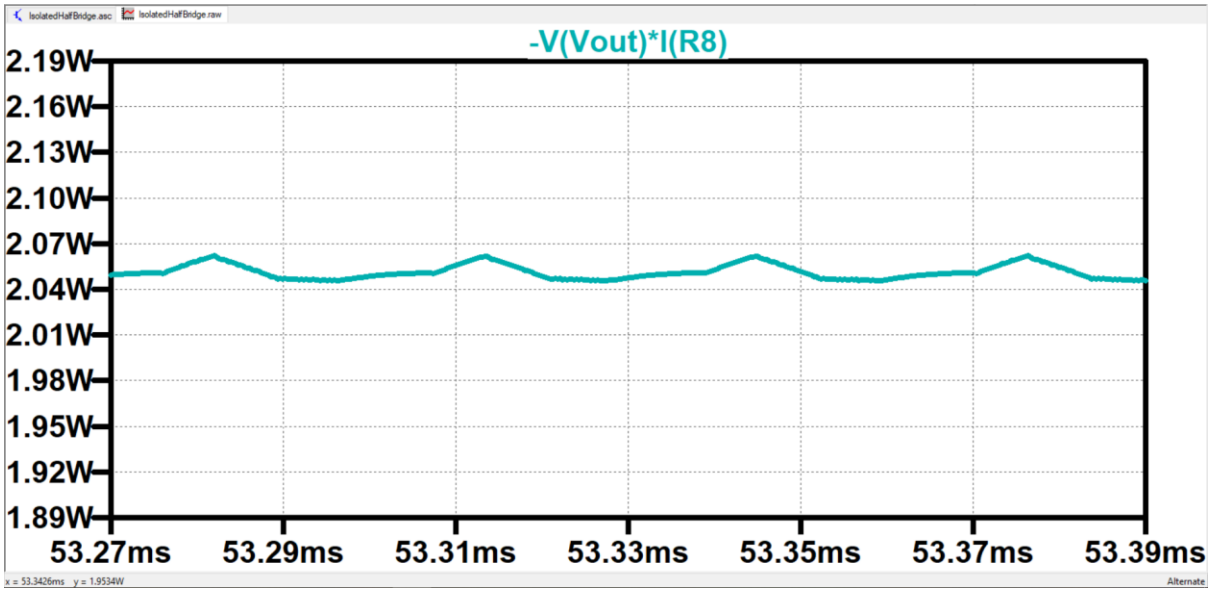

Figure 15: Output Power of the Converter

Average value of the converter output power is shown in Figure 16.

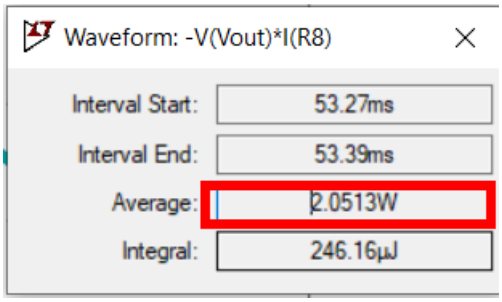

Figure 16: Average Output Power

Average value of the input power is shown in Figure 17.

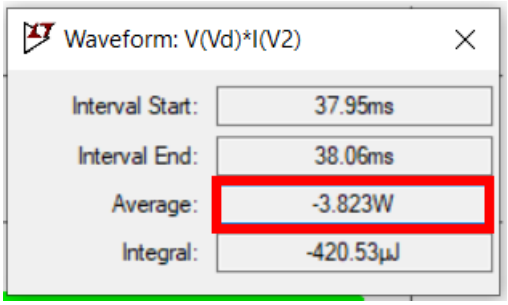

Figure 17: Average Input Power

Hence the efficiency of the converter is 54%.

Conclusion

In this experiment, a half-bridge isolated DC-DC converter was successfully designed and analyzed using key components, including the NE555 timer, CD4024 counter, and IR2109 driver. The NE555 timer generated the required PWM signal, controlling the duty cycle and frequency of the circuit. The counter synchronized the switching elements, enabling proper transformer operation and energy transfer. The theoretical equations for output voltage and peak magnetizing current were validated, showing good alignment with practical measurements.

Adjustments to the load resistor and duty cycle demonstrated the critical relationship between circuit parameters, output voltage, and load conditions. The experiment highlighted the importance of proper transformer design, inductor sizing, and output filtering in achieving stable and efficient operation. Overall, the assignment provided valuable insights into the design and functionality of DC-DC converters.