A novel method for the fabrication of a high-density carbon nanotube microelectrode array

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A B S T R A C T

We present a novel method for fabricating a high-density carbon nanotube microelectrode array (MEA) chip. Vertically aligned carbon nanotubes (VACNTs) were synthesized by microwave plasma-enhanced chemical vapor deposition and thermal chemical vapor deposition. The device was characterized using electrochemical experiments such as cyclic voltammetry, impedance spectroscopy and potential transient measurements. Through-silicon vias (TSVs) were fabricated and partially filled with polycrystalline silicon to allow electrical connection from the high-density electrodes to a stimulator microchip. In response to the demand for higher resolution implants, we have developed a unique process to obtain a high-density electrode array by making the microelectrodes smaller in size and designing new ways of routing the electrodes to current sources.

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A R T I C L E   I N F O

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Through-silicon via interconnects
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1. Introduction

Over the last few decades, with the help of miniaturized neural circuits, a lot of effort have been put into understanding the nervous system and developing prostheses. Biocompatibility and high resolution are one of the most important requirements for state-of-the-art medical implants.

A good example is the epiretinal prosthesis, a device that is able to electrically stimulate surviving retinal cells of patients suffering from diseases such as retinitis pigmentosa (RP) and age-related macular degeneration (AMD). A large percentage of patients with AMD retain good peripheral vision. In contrast, many patients with advanced RP retain their central vision. Thus, implantation of a retinal prosthesis would be justified for such patients only if it provided a substantial improvement in visual acuity; otherwise they would not benefit from it. Studies show that a retinal prosthesis must have about 1000 pixels/electrodes to restore functions such as face recognition, reading and unaided mobility [1]. Unfortunately, most of the epiretinal prostheses currently under development comprise arrays of as few as 60 electrodes, each with diameters of 100 micrometers or more [2–5]. These implants provide very limited vision, allowing patients to only see spots of light and high-contrast edges.

The design of high density microelectrode arrays presents several engineering and biological challenges. For instance, having 1000 electrodes confined in an area of 30 mm^2 (area of the macula) leads to two major issues: (1) at least 10 conducting lines would need to pass between electrodes, which would produce large capacitive coupling and be very difficult to fabricate and (2) the center-to-center distance between electrodes cannot exceed 150 μm, thus the electrode diameter has to be made small enough in order to avoid cross-talk, and most electrodes with a diameter that small (usually <100 μm) cannot deliver enough charge to exceed the stimulation threshold of nerve cells without conflicting with the electrochemical safety requirements.

The first challenging issue, which is the routing of signals from the current sources to the stimulating electrodes, has been addressed by patterning the conducting lines on different planes and using vias to connect the planes to each other [6,7]. However this increases the thickness of the device (leading to large stiffness) and greatly complicates the fabrication process flow. Some researchers have overcome the interconnect limitation by designing novel MEA systems and making use of multi-microchip architectures, which consist of multiple chips, each comprising several electrodes and a control circuit [8,9]. This approach offers the possibility of connecting several microchips via a bus system, which enables a decrease in the number of connection lines. However this
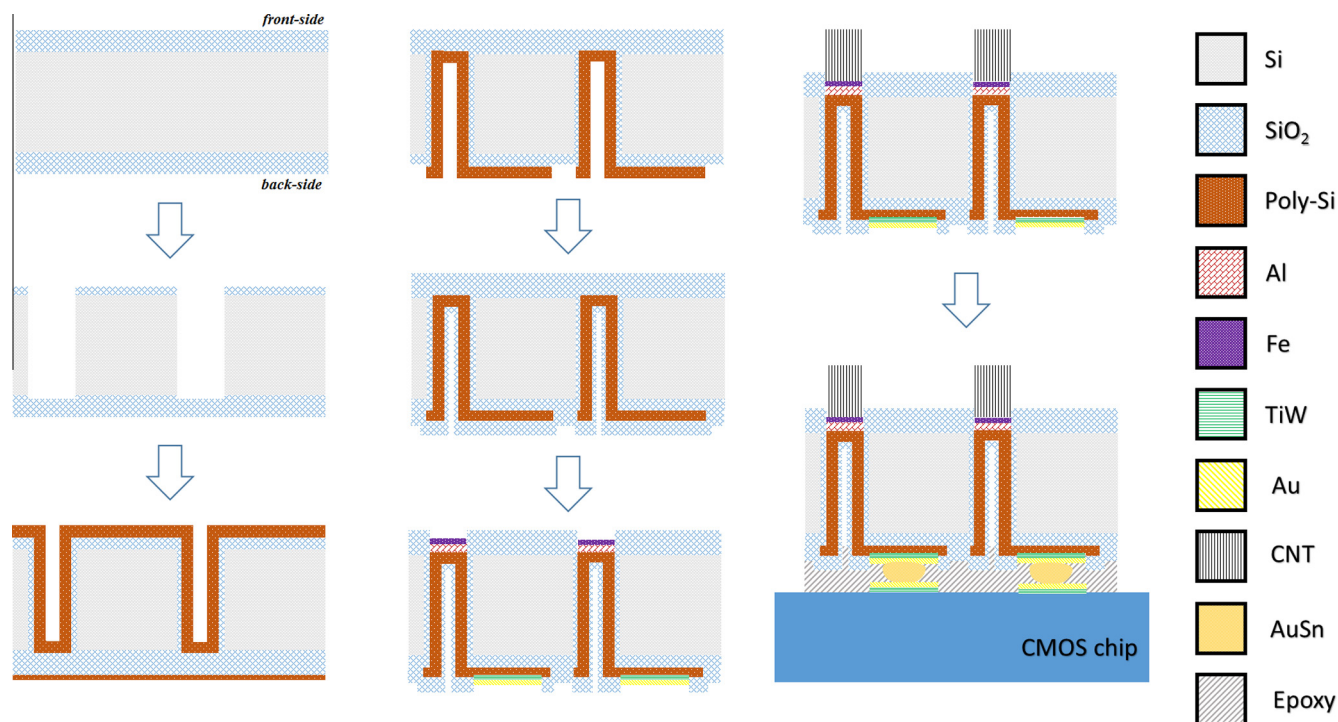
Fig. 1. Process flow diagram of the MEA designed to be integrated into the CMOS implant.

does not result in a significant increase in electrode density as some space has to be dedicated to each control circuit and to the spacing between microchips. While fabricating small electrodes is technologically possible, using them to safely and efficiently stimulate neurons is the second challenging issue. Nevertheless, a great number of metals and metal alloys have been fabricated and used as microelectrodes for neural stimulation. Iridium oxide (IrOx) is considered to be one of the best neural electrode materials because of its very high charge injection capacity and its reversible faradic reaction. However, because IrOx delaminates under high current pulsing, it leaves traces in the tissue which would lead to harmful effects in the long run [10].

Clearly, new micro fabrication processes are needed for developing the future generation of high-resolution neural implants that are fully functional and safe. To tackle the two mentioned issues, in this paper we propose a neural implant that (1) employs TSV polycrystalline silicon interconnects with flip-chip technology to solve the problem of routing for high-density microelectrode arrays and (2) uses VACNT microelectrodes that are efficient, safe and small.

The paper is organized as follows. Section II outlines the material selection as well as the microelectrode design and fabrication. Section III reports the electrochemical characterization and the measurement results. Finally, the conclusion is provided in section IV.

2. Materials and methods

2.1. Material selection

When in contact with human neural tissue, a stimulating microelectrode must be biocompatible, mechanically safe,
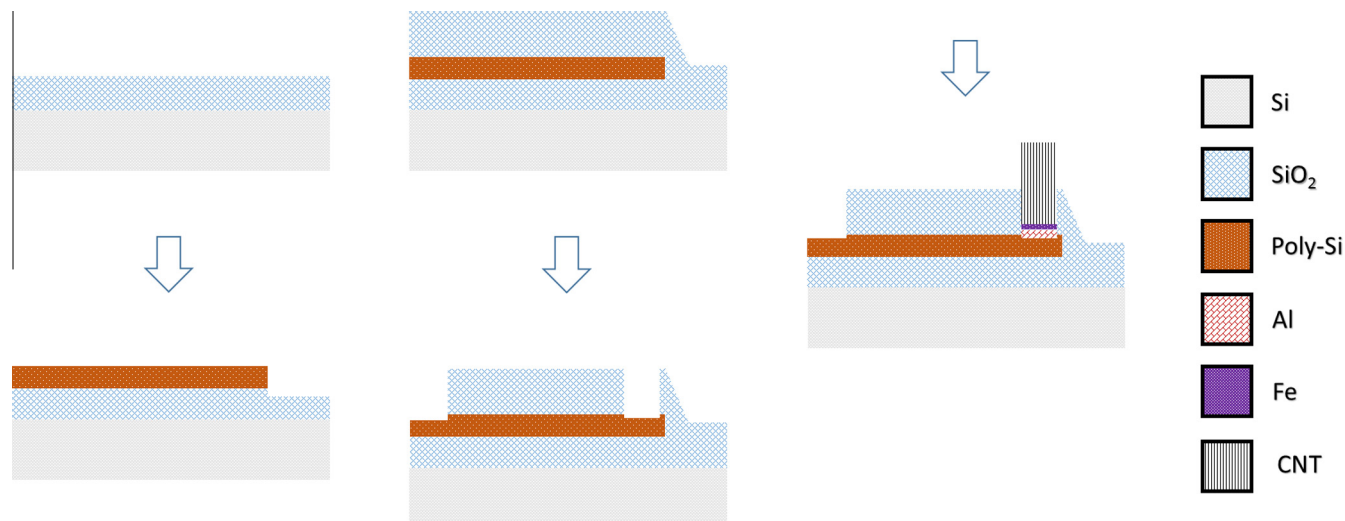

Fig. 2. Process flow diagram of the MEA designed for CNT characterization.

electrochemically safe and stable. One candidate that can operate under these demanding conditions when miniaturized is CNTs. They have shown a combination of flexibility and mechanical stability with Young's modulus in the range of 1–1.8 TPa, making them capable of penetrating neural tissue without inducing any damage to themselves. Experiment evidence shows that CNTs are not only biocompatible but also chemically inert [11,12] and that charge transfer of CNTs in an electrolytic medium is mostly non-faradaic, thus preventing the formation of reduction and oxidation species [13]. CNTs are highly porous and because of this feature the electrolytes should be able to penetrate through the surface to gain access to the interior surface. However CNTs are also hydrophobic materials [14]; hence most of their large interior surface area is inaccessible in aqueous solution and thus cannot contribute to charge injection. Thus, it is essential to modify the CNTs' surfaces to become hydrophilic.

CNTs have mainly been grown on insulating materials such as SiO_2 because metal catalysts tend to form alloys with conducting substrates at high temperatures. To prevent intermixing of catalyst and substrate, a conducting buffer layer can be used. In order to have a good adhesion to the catalyst and the interconnect, the right underlayer material with the right thickness must be carefully chosen [15,16]. Most importantly, it is crucial for the diffusion barrier not to react with the catalyst so that the catalyst film can easily form uniform and discrete nanoparticles. In this study aluminum (Al) and titanium (Ti) have been used (separately) as underlayers.

Metals are not used as our electrical conducting lead material since most metals would not survive the high process temperature of the microwave plasma enhanced chemical vapor deposition machine (900 °C). Those who do have high melting points show a very high chance of forming microscopic cracks due to a much higher thermal expansion than that of silicon dioxide ($0.5 \times 10^{-6}\,K^{-1}$). For instance, titanium nitride has a thermal expansion coefficient of $9.35 \times 10^{-6}\,K^{-1}$. Furthermore, unlike CVD, it is difficult to grow a conformal film in high aspect ratio trenches by sputter deposition. Sputtering into these features results in poor step coverage and large overhang, which leads to void formation. Given the harsh fabrication requirements, heavily doped polycrystalline silicon (poly-Si) is used as metal interconnects. It has a good interface with silicon dioxide and most importantly it keeps the fabrication process at a "Clean CMOS" state which allows, for example, the deposition of silicon dioxide of higher quality.
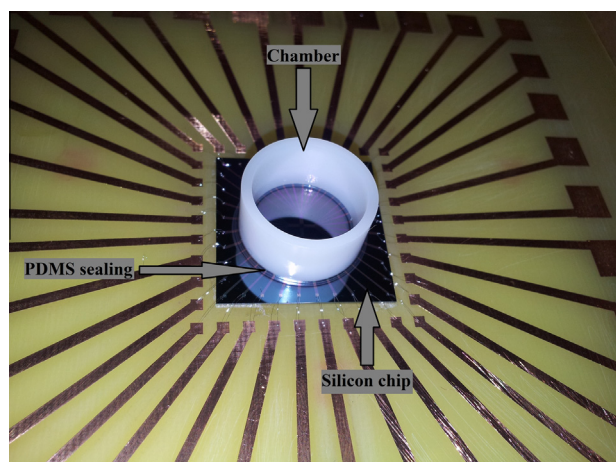

Fig. 3. The MEA-chip on the customized PCB, ready for electrochemical experiments.

2.2. Microelectrode array chip design and fabrication

Two microelectrode array chips have been designed and manufactured. The first is the CNT MEA chip to be integrated with the CMOS implant, the second is the CNT MEA assembly that was employed to characterize the electrochemical properties of the electrodes.

The fabrication process flow for the first chip is depicted in Fig. 1. We used 200 μm thick 4-inch double polished <100> p-type silicon wafers. A 3 μm layer of low-temperature oxide (LTO) was deposited using low pressure chemical vapor deposition (LPCVD) at 425 °C. Standard UV photolithography defined the layout of the vias. The backside was coated with photoresist using a manual photoresist coater. The exposed LTO on the front side was then removed in buffered oxide etch (BOE) and the photoresist was stripped in a mixture of H_2SO_4 and H_2O_2. Through-silicon deep reactive ion etching (DRIE) with a customized Bosch process was performed to form 200 μm deep vias. Since the wafer was thin and tended to easily break from stresses generated by the etcher machine (surface technology systems inductively coupled plasma), a dummy wafer had to be placed underneath it. Following DRIE, a 0.5 μm layer of thermal oxide (wet oxidation) was formed to provide electrical insulation of the interconnect vias from the bulk silicon. The vias were then partially filled (3 μm deposition) with heavily doped amorphous-silicon by LPCVD. To obtain poly-Si of $9.9 \times 10^{-4}\,\Omega$ cm, amorphous-silicon was annealed at 900 °C for 2 hours. To pattern the poly-Si layer on the front side of the wafers, a spray coating system (EVG 101) was used so that the photoresist could reach and deposit uniformly deep down the vias. To develop the resist, the wafers were inserted into a container with AZ 400K developer, which was diluted in deionized water at a 1:4 ratio. Poly-Si in undesired areas was then removed by reactive ion etching (RIE) with HBr gas and a blanket etch was performed on the backside of the wafers to completely remove the poly-Si. The photoresist was stripped off and a 4 μm thick layer of LTO was deposited. The third mask was used to pattern the LTO in order to expose the electrodes on the bottom side of the wafers. Rather than using the HPR-504 photoresist that has been used previously for photolithography, the more heat resistant HPR-6500L photoresist was used since the wafers were going to be exposed to higher temperatures. The spray coating system was used once again to coat photoresist on the top side of the wafers and the fourth mask was then used to pattern the LTO in order to expose the contact pads. The exposed LTO on both sides of the wafers was removed in BOE. A 15 nm layer of Al and a 5 nm layer of Fe were then deposited on the back side of the wafers by electron beam evaporation. A 200 nm layer of titanium tungsten (TiW) and a 300 nm layer of gold (Au) were sputtered on the front side of the wafers. Afterwards, lift-off was performed by soaking the wafers in acetone while agitating them in an ultrasonic bath for 10 min. Finally, the wafers were diced and CNTs were grown on each die.

The flip-chip assembly consists of three standard major steps: (i) bumping of the CMOS chip, (ii) flipped chip attachment and (iii) under-filling. During the attachment, the MEA-chip would be held by a customized substrate holder which is designed and

Table 1
Process parameters of the customized Bosch etch process.

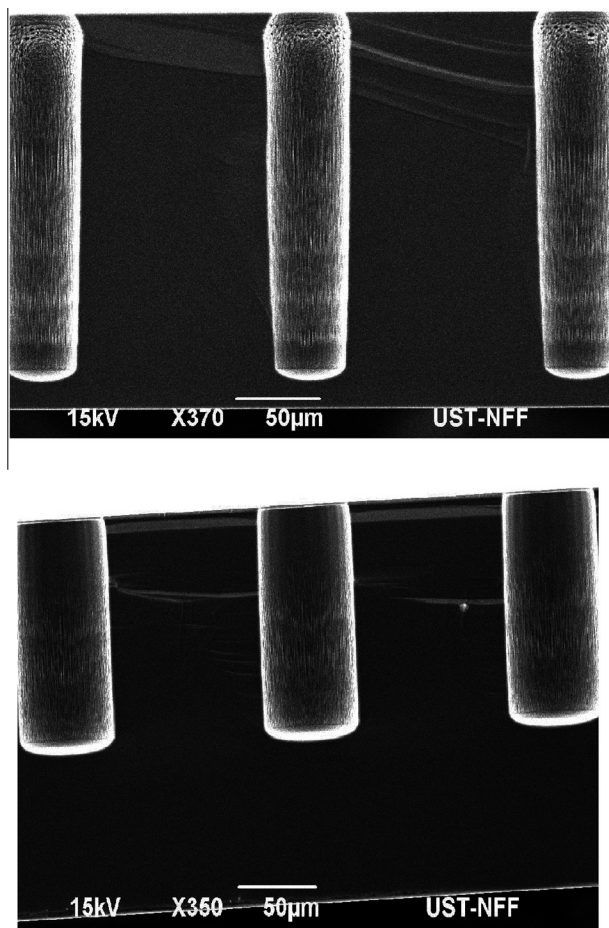| Process parameters	Etching/Passivation cycle
Coil Power (W)	600/400
Platen Bias (W)	10/0
Pressure (mTorr)	34/18
SF_6 (sccm)	140/50
C_4F_8 (sccm)	30/95
O_2 (sccm)	12/0

Fig. 4. SEM image of a cross-section of vias holes before (top image) and after (bottom image) customizing the Bosch process.

fabricated to protect the CNT electrodes. The electrical connection between the MEA-chip and the CMOS substrate can be achieved using gold tin (AuSn) bumps, the under-bump-metallization (UBM) would consist of a sputter deposited TiW/Au thin film stack and the underfill material chosen is a biocompatible epoxy. The execution of the flip-chip bonding is yet to be done due to the lack of the CMOS chip (which just entered tape-out stage).

The fabrication process flow of the second chip is depicted in Fig. 2. We used 525 μm thick 4-inch single polished <100> p-type silicon wafers. The wafers already had 1 μm of silicon dioxide coated on them. A 540 nm layer of poly-Si was deposited using LPCVD at 620 °C (300 mTorr, SiH_4 30 sccm). The poly-Si was then doped to achieve a resistivity of $4.71 \times 10^{-4} \, \Omega$ cm in a furnace for 30 min at 1000 °C. The formed phosphorus silicon glass (PSG) layer was later removed in BOE. Standard UV lithography defined the layouts of the electrodes, interconnects and contact pads. Poly-Si in undesired areas was removed by plasma etching with HBr gas and the photoresist was stripped. A 1 μm layer of LTO was deposited using LPCVD at 425 °C. The second mask was then used to pattern the LTO in order to expose the contact pads. LTO was removed by plasma etching with C_4F_8 gas. After stripping off the photoresist, the third mask was used to pattern the LTO once more in order to expose the electrodes. A 2 min O_2 plasma descum followed to improve lift-off, and the LTO was then removed by plasma etching. A 15 nm layer of Al and a 5 nm layer of Fe were deposited by electron beam evaporation. Afterwards, the wafers were soaked in acetone and agitated in an ultrasonic bath for 10 min.

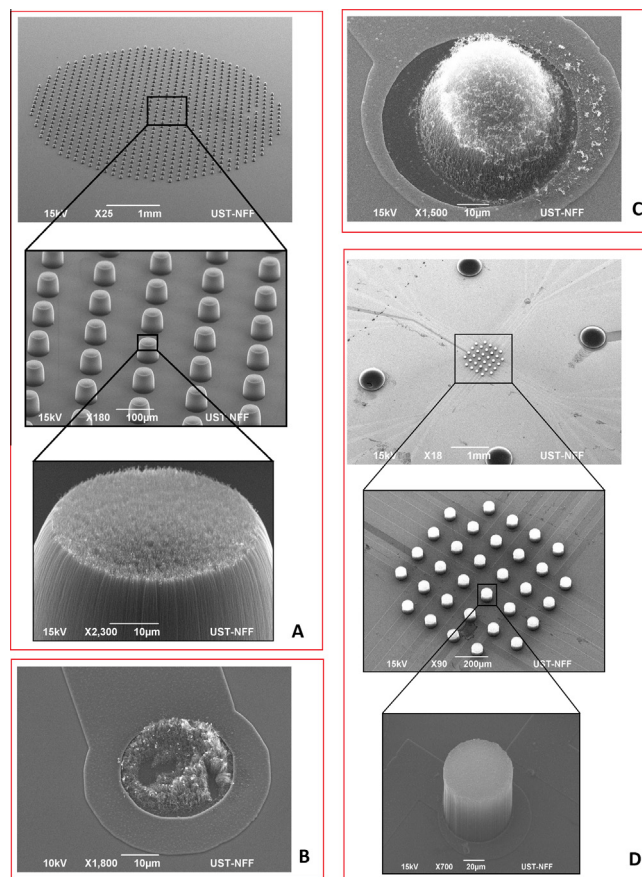**Fig. 5.** TEM photograph of CNT tips. Each MWCNT measures about 7 nm in diameter.

Fig. 6. SEM images of CNTs grown directly on (a) SiO, (b) poly-Si, (c) a Ti-barrier layer and (d) an Al-barrier layer.

Each wafer was then diced into 4 dies. The die size is 27 mm × 27 mm and has a total of 36 electrodes with a center-to-center distance of 150 μm. Instead of having 1000 electrodes, a die containing 36 electrodes was fabricated to

demonstrate the electrochemical properties of the CNT electrodes. After CNT growth, each chip was mounted and glued to a custom PCB. Wire bonding was used for making interconnections between the MEA-chip and the PCB. A chamber for electrochemical measurements was formed by bonding a polyoxymethylene (POM) ring onto the MEA–CNT chip using polydimethylsiloxane (PDMS). PDMS was prepared in a 10:1 ratio of PDMS base with curing agent and was stirred for 5 minutes. It was then used to attach the ring onto the chip and cured for one hour at 90 °C. The ring had a height of 10 mm, an inner diameter of 17 mm, and an outer diameter of 20 mm. Thus, the chamber volume was about 2270 μ l, which was large enough to hold two external electrodes and enough solution for electrochemical measurements. The pads on the MEA chip were left outside the chamber for electrical connections. The assembly is shown in Fig. 3.

2.3. Carbon nanotube growth

In this paper, VACNTs were synthesized using microwave plasma enhanced chemical vapor deposition (MPECVD) and thermal chemical vapor deposition (TCVD).

For the MPECVD process, samples were loaded into the reaction chamber (ASTEX 5200M, Seki) and the pressure was pumped down to 2 Torr. Then hydrogen and nitrogen were introduced with a flow rate of 20 sccm and 5 sccm, respectively. The temperature was ramped up to 800 °C and the pressure stabilized to 8 Torr. As soon as the plasma was ignited, a 30 sccm methane gas was introduced for 90 seconds. Then the RF heater and the microwave-generated plasma were switched off. All the gases were switched off except for hydrogen, which was increased to 80 sccm to allow the substrate to cool down at a faster rate until it reached room temperature.

For the TCVD process, after raising the reactor chamber (CARBOLITE CTF) temperature to 520 °C, the samples were placed inside the quartz tube furnace. The chamber was then pumped to a base pressure of 0.02 Torr, followed by the introduction of H_2 at 490 sccm. The temperature of the furnace was maintained at 520 °C for 3 min to pretreat the catalyst. It was then raised to 600 °C at a rate of 20 °C min^{-1}. C_2H_2 was introduced at a flow rate of 10 sccm for 10–90 minutes (depending on the desired CNT height). Afterwards, H_2 and C_2H_2 were turned off, and the reactor was cooled to room temperature with Ar gas at 400 sccm.

2.4. Electrochemical tests

A three-electrode system was used for the cyclic voltammetry (CV) and the electrochemical impedance spectroscopy (EIS). In our experiment, the CNT electrode served as the working electrode, Ag/AgCl as the reference electrode and Pt as the counter electrode. The three electrodes were submerged in a 22.7 cm^3 phosphate buffer saline (PBS) solution. The PBS is composed of 10.59 mM KH_2PO_4, 1151.72 mM NaCl, 29.66 mM $Na_2HPO_4 \cdot 7H_2O$ and has a pH of 7.4. Measurements were conducted using a potentiostat (Reference 600, Gamry Instruments, Warminster, PA) and Gamry software. The voltage range was increased step by step until the H_2 and O_2 evolution limits were reached. Once the potential limits were found, all CV tests were conducted at a scan rate of 100 mV s^{-1} and a voltage range between −0.3 and 0.8 V (vs Ag/AgCl). The EIS measurements were made over a 1–10^5 Hz frequency range using a 50 mV sinusoidal excitation voltage. The impedance spectrum is presented as Bode plots. A two-electrode system was used for the potential transient measurement (PTM). A cathodic-first symmetric biphasic current pulse was applied between a CNT electrode and the counter electrode. The electrode potential was monitored on a digital oscilloscope.

3. Results and discussion

3.1. Device fabrication and carbon nanotube synthesis

The reason for using TSV and flip-chip technology is to enable the fabrication of a high electrode density implant. TSVs not only accommodates the interconnect density demands but also offer a reduction in interconnect lengths (connection lengths are reduced to the thickness of the chip). The latter not only results in reduced power consumption (the average resistance of each poly-Si lead is about 140 Ω), but also reduces parasitic capacitance.

As mentioned in the fabrication process flow, vias were created by the Bosch process. The process parameters of the standard Bosch etch process has been modified (Table 1) to obtain vias with smaller local bowing and reduced sidewall roughness, as can be noticed in Fig. 4. Complete filling of high aspect ratio TSVs can be both costly and challenging. One common type of failure is voids, which are formed due to premature closing during the via-filling step. A few of solutions have been proposed in order to obtain void-free poly-Si vias, such as changing the trench design in order to get tapered vias [17] or carefully optimizing the CVD process parameters [18]. However, these suggested solutions are very challenging to implement. Furthermore having the vias fully filled with poly-Si would require an impossibly long deposition time. That is why a process was developed that allowed us to electrically connect both sides of the wafer without having to completely fill the via holes. In [19] signals recorded from probes were also transferred by TSVs through the chip to the CMOS circuits, however in their work, an array of TSVs is assigned to an array of probes (and thus control of a single electrode is not possible), the via is completely filled with Cu and the electrode material chosen is Pt (which is known to have very limited charge injection ability).
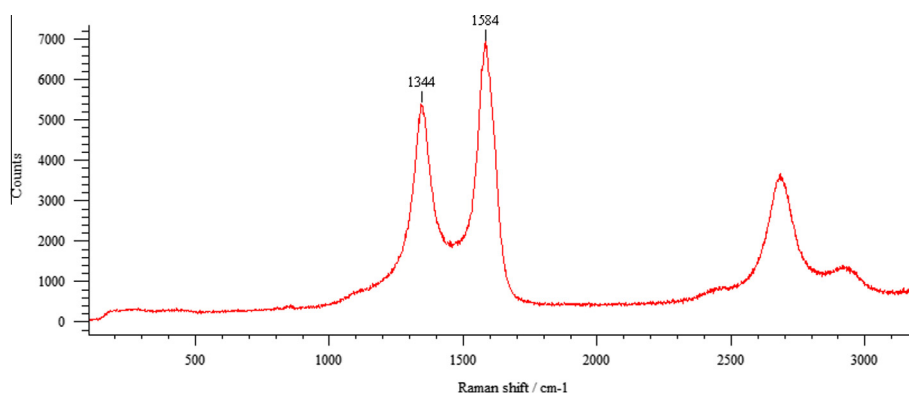

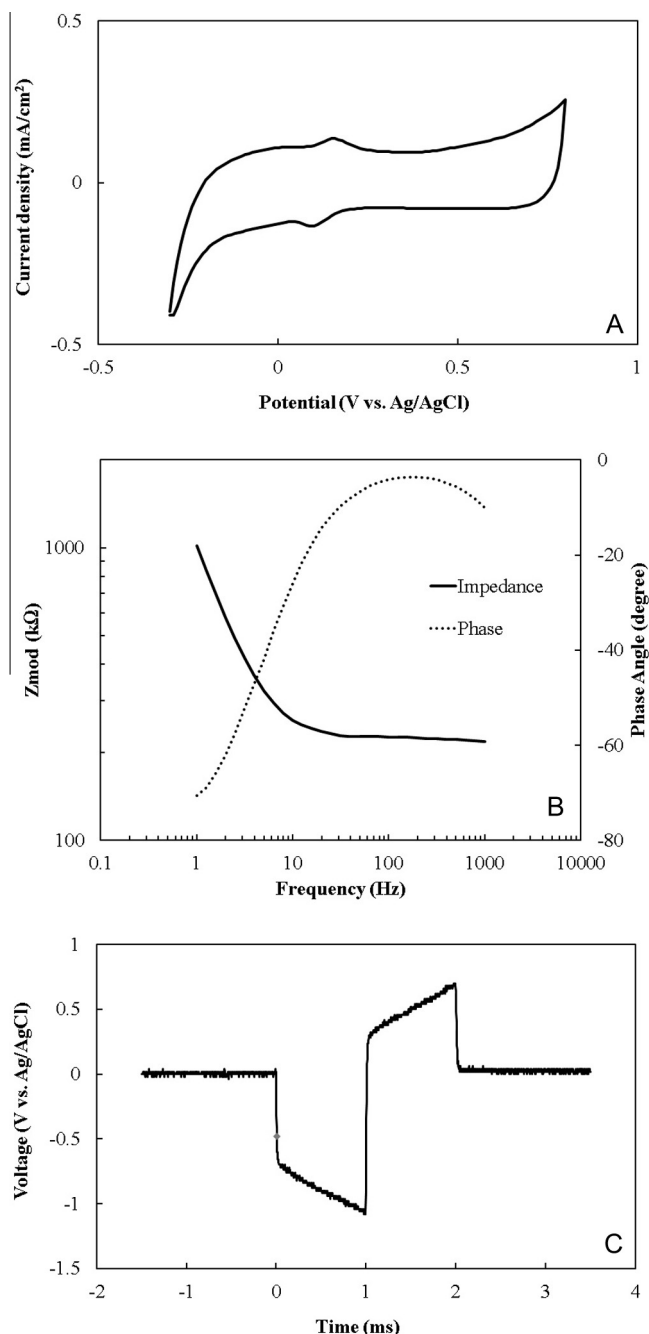**Fig. 7.** Raman spectrum of MWCNTs grown by TCVD.

Fig. 8. Electrochemical measurements of an untreated CNT electrode with a geometrical area of 10^{-4} cm². (a) The cyclic voltammogram, (b) the bode plot representation of its impedance and (c) the potential transient after 15 min of pulsing in PBS.

All of the grown multi-walled carbon nanotubes (MWCNTs) used the base-growth mode, as can be noted by the absence of a catalyst at the tip of the tubes (Fig. 5). When using a "forest" of

CNTs as a neural stimulating electrode, base-growth mode is preferable since the metallic catalyst is toxic to neurons [20]. During the base growth mode, the catalysts partially diffuse into the underlayers leading to a strong interaction which stabilizes them and prevents them from escaping. Thus, it was not necessary to employ harsh purification methods to remove the metal catalysts. Nevertheless, further research is needed to know if non-biocompatible materials would cause long-term complications even when they are not directly exposed to the tissue.

Initially CNTs were grown on SiO_2 using MPECVD. Our investigation showed that well aligned CNT (Fig. 6a) can be obtained when the $CH_4:H_2$ gas flow ratio is kept at 3:2. CNTs were then grown on poly-Si, and poor-quality CNTs were obtained (Fig. 6b). It was noticed that at high temperatures (>800 °C), Fe interacted with Si to form silicides ($FeSi_2$), which led to the deactivation of the catalyst and hindered the growth of CNTs. A 15 nm thick Ti-barrier layer was thus used and average-quality CNTs were obtained (Fig. 6c). This suggested that Fe continues to diffuse into the voids of the diffusion barrier. In order to use materials with lower melting points, CNTs were then synthesized using TCVD and VACNTs were successfully grown on a 15 nm thick Al layer (Fig. 6d). Unfortunately, including a photograph of the completed chip showing a cross-section of TSVs with CNTs was not possible since during dicing the CNTs would detach itself from the chip because of the mechanical force from the deionized water jet.

The chemical bonding of VACNTs were then quantified using Raman spectroscopy (Fig. 7). The most prominent Raman features in MWCNTs are the high frequency D (1344 cm^{-1}), G (1584 cm^{-1}) and G′ (2690 cm^{-1}) modes. There is a very small peak at 850 cm^{-1}, which is associated with armchair SWCNTs [21]. Since all armchair nanotubes are metallic we can conclude that the grown MWCNTs are mainly made of metallic nanotubes (the best possible structure for an electrode CNT). The quality of the sample can be evaluated using the ratio of intensities of the G band to the D band; the larger its value, the smaller the structural defects in CNTs would be. The I_g/I_d for the measured sample is 1.46 which suggests good crystallinity.

3.2. Electrochemical characterization

The CV curve (Fig. 8a) obtained from our grown VACNTs displays, except for the small peaks at 100 mV and 150 mV (presumably due to the reduction of absorbed oxygen), a rectangular shape within the potential window. The lack of distinct peaks within the water window indicates that the current flow is dominated by the capacitive charging-discharging mechanism. It has become common practice to characterize electrodes by their charge storage capacity (CSC) which is calculated by integrating the current density enclosed by the CV curve and dividing it by two times the scan rate. It is important to note that only the electrode's geometric surface area has been measured and used to calculate the CSC, not the real surface area that is involved in microscopic processes. The geometrical area of a CNT electrode includes both the top and the sidewalls of the pillar. The calculated CSC for an untreated 60 µm diameter electrode is about 1.2 mC cm^{-2}. The EIS spectra for the same electrode is shown in

Table 2
CSC, Impedance and CIC of a variety of materials considered for use as neural stimulating electrodes.

Paper	[22]	[23]	[24]	[25]	[26]	Our work
Material	Platinum	Iridium Oxide	Untreated CNT	Untreated CNT	Untreated CNT	Untreated CNT
Geometrical area (cm²)	9.5×10^{-3}	3×10^{-4}	5×10^{-4}	6.7×10^{-5}	2.8×10^{-5}	10^{-4}
CSC (mC cm^{-2})	NA	4.91	NA	0.02	0.5	1.2
Impedance at 1 kHz ($k\Omega$)	NA	14	NA	NA	51	230
CIC (mC cm^{-2})	0.050–0.15	NA	0.02	NA	NA	0.5

"NA" denotes the parameters are not available in the content of the publication.

Fig. 8b, the measured impedance is 230 kΩ at 1 kHz. It's voltage transient in response to a 50 μA, 1 ms biphasic symmetric current pulse is shown in Fig. 8c. The smallest hydrolysis limit (which is −0.3 V vs Ag/AgCl) was reached when the amplitude was increased to 50 μA. Thus by dividing the injected charge by the geometric area, the charge injection capacity (CIC) of the measured CNT electrode is equal to 0.5 mC cm^{-2}.

Table 2 summarizes the main findings related to electrode electrochemical properties. The electrochemical experimental results (CSC, CIC and impedance) do not only depend on the electrode material but also on many other parameters such as the size, shape and roughness of the electrode, the equation used to obtain the electrochemical results (e.g. whether the values are normalized to the geometric area or the real surface area), the different kinds of treatments performed on the electrode, and the electrochemical experimental setup itself (e.g. PBS composition, pH used). The impedance of our untreated CNT electrode is too high to be used as a neural stimulating electrode. Thus, in order to fully exploit CNTs' full potential, future work needs to be done to decrease the impedance by changing the surface from superhydrophobic to hydrophilic. To improve the capacitance and impedance value of CNTs, several methods have been proposed; they include (a) coating the nanotubes with a conducting polymer such as polypyrrole [25,26]; (b) wet chemical functionalization using HNO$_3$ or KOH [27]; and (c) plasma functionalization such as an oxygen and steam plasma treatment [28]. All of them consist of chemically modifying the surface of the nanotube by functionalization, but only approach (a) maintains the CNTs' vertical alignment.

4. Conclusion

There is an increasing need for high electrode density implants. While the electrode size continues to scale down, the stimulating neural microelectrode array has to remain efficient and safe. Furthermore, while the number of electrodes increases, new ways of routing the electrodes to current sources has to be found. This is not an easy task and arising problems can be solved or at least alleviated through intelligent design of the microelectrode chip. In this study, a new class of microelectrode chip was designed, fabricated and tested. Carbon Nanotubes have been used as the electrode material, with the objective of satisfying the size, efficiency and safety requirements; and TSV poly-Si interconnects were employed to solve the problem of routing for large microelectrode arrays. We are the first to combine these two technologies into a single chip. With the use of CNTs, TSV and Flip-Chip technology, the next generation of neural implants could easily incorporate at least 1000 microelectrodes.

Conflict of interest

The authors declare no conflict of interest.

Acknowledgment

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