

## ECE 385 TTL Logic Wiring Guidelines

- Unit test all of your chips
  - Try hardcoding inputs to all gates on a chip, and make sure the output matches what you expect
  - This will save you lots of headache in the future if a chip ends up not working.
- Build in modules
  - If you have a “memory” block, make an effort to physically locate the chips that comprise it together on the board
  - Once the chips are in place for a module, hardcode some inputs and test to make sure it works as expected.
- Keep your wires as short as possible
  - Instead of the medium length red and black to short pins to Vcc or ground, use the short yellow and orange wires
  - Pick the shortest wire possible to do the job, only using the long ones where absolutely necessary (eg bridging signals between modules)
- Keep your wires as far as possible from the pins of the TTL chip
  - Every row on the breadboard is entirely shorted, so instead of placing wires right next to the chip, give the chip some space.
  - This keeps your layout clean, and if you burn a chip, you’ll be able to replace it easily.
  - This also makes it easy to directly probe the pins of the TTL chip, which are all that matter in terms of the logic actually being propagated
- Where possible, route wires around, instead of over, the TTL chips.
  - Again, this makes it easier to probe the chips, and replace them if you need to.
- Create “lanes” for common signals
  - Signals like the clock will be used all over the place, so instead of leapfrogging it between different chips, decide on a few specific places on the board that get the clock, and route the wires that need it to these places.
  - Ideally, lanes allow you to make direct, straight, connections to places that need them, and allow you to easily follow which signals go where
- If possible, get a pair of pliers
  - They’re \$5-8 in the ECE store, and will save you lots of time during labs 2 and 3, which each take between 10 and 20 hours to build and debug.
  - A mechanical pencil or pen can be used to extract wires and chips in absence of pliers