ECE 385

Fall 2021

Experiment #1

Lab 1
Introductory Experiment

Name: Guanshujie Fu
Student ID: 3190110666
Lab Section D231 18:00 – 21:00
TA: Yuchuan Zhu

Purpose of the Circuit
The purpose of Lab1 is to understand how delay and glitch occur and how to avoid them when design the circuit.

Description of the Circuit
The original logic design of the circuit based on Boolean function $Z = BA + B'C$ is shown in Figure 1. A slight modification can be done to make the circuit use only NAND gates, as shown in Figure 2.

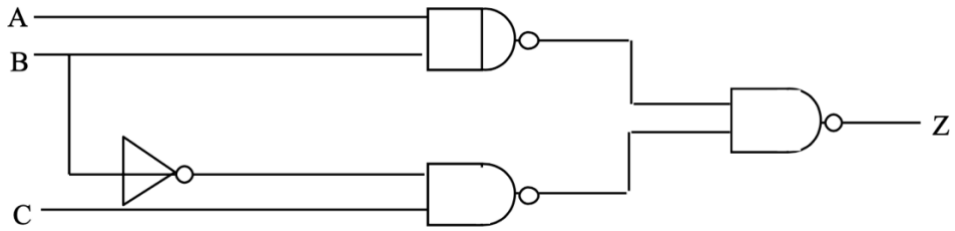

Figure 1

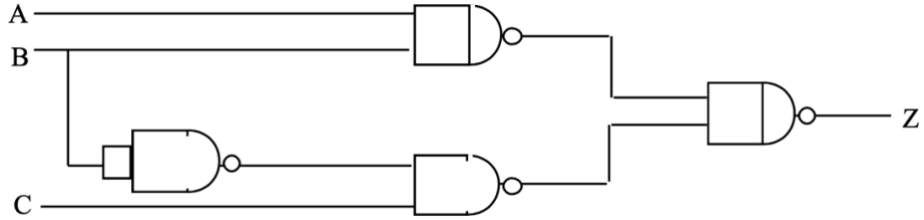

Figure 2

For Boolean function $Z = BA + B'C$, we can indicate following truth table as shown in Table 1.

ABC	*Z*
000	1
001	1
010	0
011	0
100	0
101	1
110	1
111	1

Table 1

Clearly, as we can observe from the truth table, when we keep $AB = 1$, the output Z will always be 1 regardless of the value of C. Also, when we keep $AC = 1$, the output Z will also keep 1 regardless of the value of B. To further explore the circuit, I then use Quartus to construct schematic diagram for simulation and construct the circuit layout. The schematic diagram and layout are shown in Figure 3 and 4.

For prelab Part B, with more inverters added, the truth table does not change. The logic circuit is not shown as it just adds several inverters in Figure 2.
For prelab Part C, the improved circuit is shown in Figure 4.

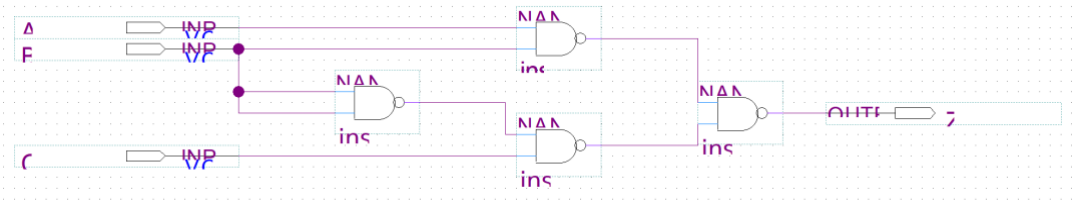

Figure 3

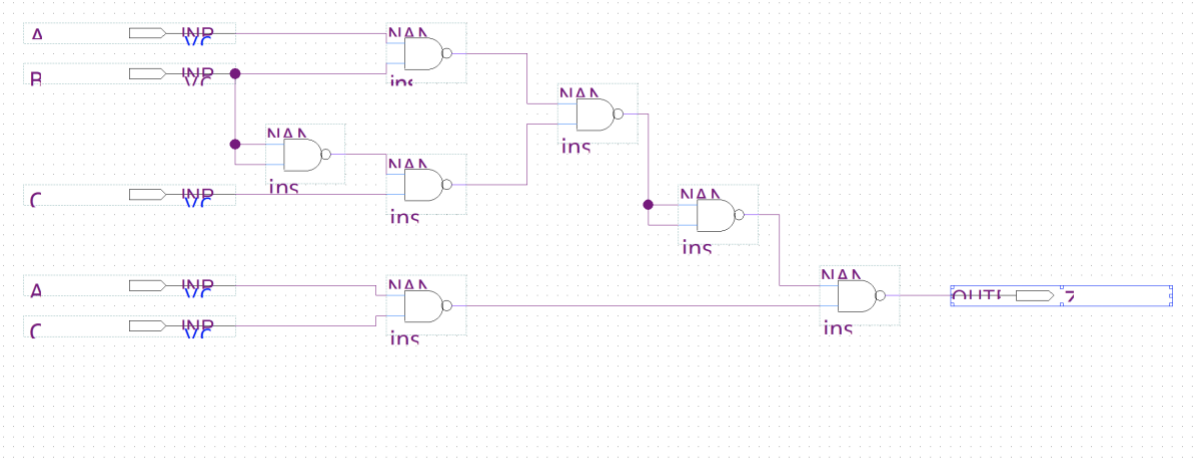

Figure 4

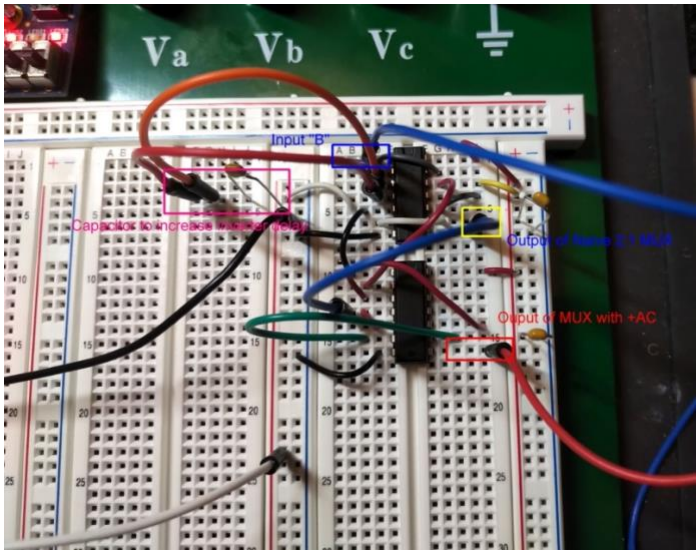

Figure 5

High Level Block Diagram
As the circuit for Lab1 is not complex, I omit this part.

Logic Diagram
The needed logic diagram of the circuits has been shown in **Description of the Circuit**.

State Diagrams and Tables
No need for Lab1.

Component Layout
No need for Lab1.

Answer for Pre-Lab Questions

A. *Chain an odd number of inverters together in place of the single inverter. But no static hazard is find, why?*
By compiling and doing the simulation with the wave form showing in Figure 6, no static hazards were observed. The output *Z* remains 1 all the time. It is because the simulation using Quartus will simplify the Boolean function for the circuit and hence no hazard will be observed. With more inverters added, the truth table does not change and there does not exist hazard. It would be the same as Part A.

B. *Redesign the circuit of part A to eliminate all static-1 hazards (glitches) at the output.*
To avoid possible hazard, we could add one more term without affecting the truth table. We can observe from the K-map of Z that we can add one more *AC* while keep the output unchanged as shown in Figure 6. Hence, we can design an improved circuit presented in Figure 4.

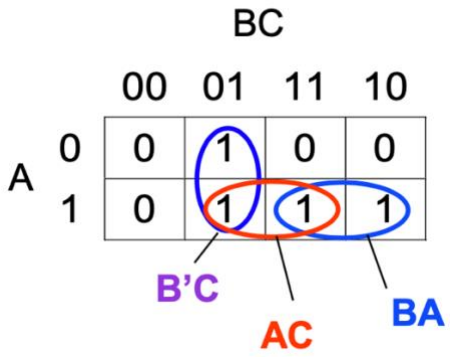

Figure 6

Answer for Lab Questions

1. The truth table has been shown in Table 1. By compiling and doing the simulation with the wave form in Figure 6, no static hazards were observed. However, the test using real layout with the same input indicates obvious glitch as shown in the Figure 7. There exists an obvious drop from 1 to 0 in the wave, which is a hazard.

2. *For the circuit in Part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?*

It is more likely to observe a glitch at the falling edge of the input *B*. We can see from the circuit in Figure 2 that the term *AB* will change faster than the term *B'C*. Hence, at the falling edge of input *B*, the term *B'C* will remain 0 for a short time while the term *AB* is already changed to 0, which lead to the static hazard for a short time. This can be seen from the Figure 7.

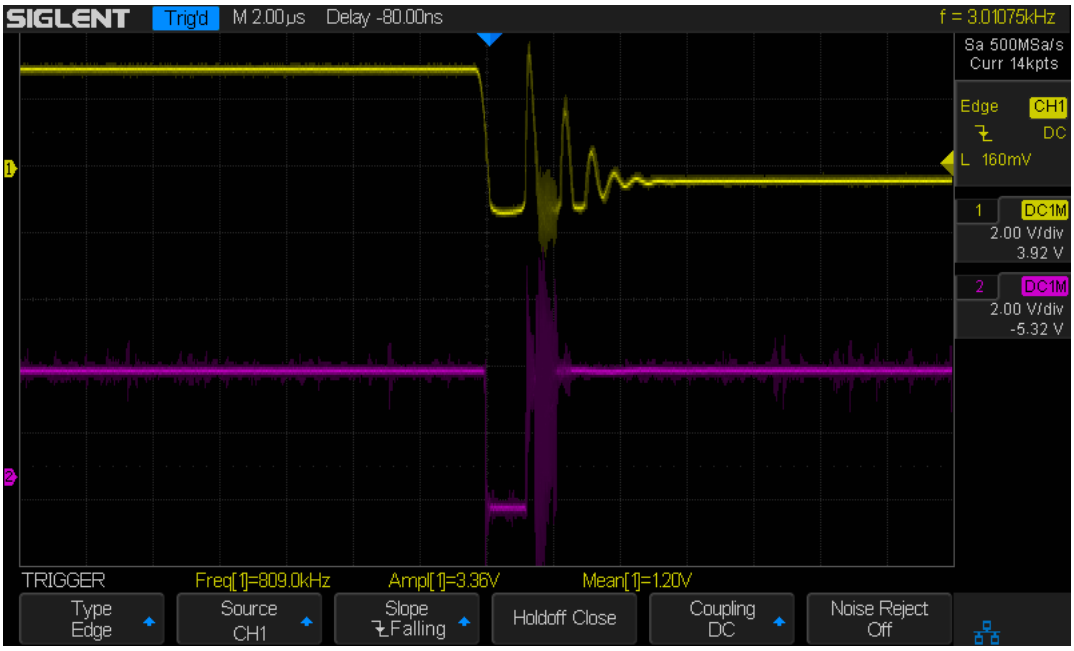

Figure 7

Answer for General Guide

1. *What is the advantage of a larger noise immunity?*
   Larger noise immunity will make the circuit stable because the output will not change easily.
2. *Why is the last inverter observed rather than simply the first?*
   Because more inverters could rule out the occasional situation. If one of them has a filp between low and high, the output will sense it.
3. *How would you calculate the noise immunity for the inverter?*
   The overall noise immunity of the gate is the smallest of the ranges X and Y. In this case, 0.8 < 2.15, so 0.8 V is the noise immunity for this gate.
4. *If we have two or more LEDs to monitor several signals, why is it a bad practice to share resistors?*
   Because if LEDs are connected in parallel.The current is divided into several small ones as the total current remains the same.

Conclusions

For the Lab 1, it is about possible hazard and glitch that will occur during the design of the circuit. We observe the glitch and learn how to eliminate the glitch by redesign the circuit. I could not observe glitch in Pre-Lab Part A because the simulation in Quartus will automatically simplify the circuit. However, with the real layout, I successfully observe the glitch in the wave

generated by the output. To avoid the glitch, I then use K-map to include all adjacent terms and redesign the circuit.