ECE 385

Fall 2021

Experiment #2

Lab 2
Data Storage

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Lab Section D231 18:00 – 21:00
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1. Introduction

a. In this experiment, we design and construct a simple 2-bit, four-word shift-register storage unit. The circuit could read from the register or store into the register with specific instructions. Our memory contains 4 words, and the bit width of each word is 2.

2. Operation of the memory circuit

a. Describe how the addressing is implemented: A counter is used to simulate the change of the address in the register, it shifts one position every clock cycle. Only when the address outputted by the counter equal to the address inputted by SAR, the circuit may commit read or write. // The circuit will commit a read from the input switches when the FETCH signal is high, the STORE signal is low, the address SAR matched, LDSBR signal is low. The circuit will commit a write to output register when the FETCH signal is low, the STORE signal is high, the address SAR matched, LDSBR signal is low.

b. Describe how a write operation is performed on the memory: 1. First clock cycle: As the STORE signal is high, the COMPARATOR will determine whether the current position of words in the REGISTER recorded by the COUNTER and SAR match, if so, the 1-bit SELECT signal will be set to 0 and input into the 2-to-1 MUX. At the same time, the 2-bit SELECT signal would be set to 10 and inputted into 3-to-1 MUX. 2. Second clock cycle: With two select signals, the data in SBR(FLIP_FLOPS) would transform through two MUX, one of those data will be store into SBR(FLIP_FLOPS) again through 3-to-1 MUX, another will be store into the SHIFT REGISTER through 2-to-1 MUX. Thus, the data in SBR won't change and will be write into the SHIFT REGISTER.
From the description, we flip the Ripple Counter (SN7493) to match the address by using Magnitude Comparator (SN7485). When the comparator generates signal EQUAL, the STORE and EQUAL will flip the 2-to-1 Multiplexer (SN74157) such that the data in the SBR will be chosen to store in the Shift Register (SN74LS194A), which is activated at the last step. Intuitively, the signal flows in this order: 2-to-1 MUX → 3-to-1 MUX → D_FLIP_FLOP → Shift Register.

c. Describe how a read operation is performed on the memory: 1. First clock cycle: As the FETCH signal is high, the COMPARATOR will determine whether the current position of words in the REGISTER recorded by the COUNTER and SAR match, if so, the 1bit-SELECT signal will be set to 1 and inputted into the 2-to-1 MUX. At the same time, the 2-bit SELECT signal would be set to 00 and inputted into 3-to-1 MUX. 2. Second clock cycle: With two select signals, the data stored in SHIFT REGISTER will transform through the 3-to-1 MUX and then be stored into SBR. Thus, the data in SBR(FLIP-FLOPS) will be replace by the data of words in SHIFT REGISTER. 3. Third cycle: DATA in SBR(FLIP-FLOPS) will be outputted.
From the description above, we flip the Ripple Counter to match the address by using Comparator similar to the write operation. After the EQUAL signal is generated, it will flip into the 2-to-1 MUX and be fetched into the Control Logic to generate signals for 3-to-1 MUX which will activate the SBR at the final step. Intuitively, the signal flows in this order: 2-to-1 MUX and Control Logic → 3-to-1 MUX → D_FLIP_FLOP.

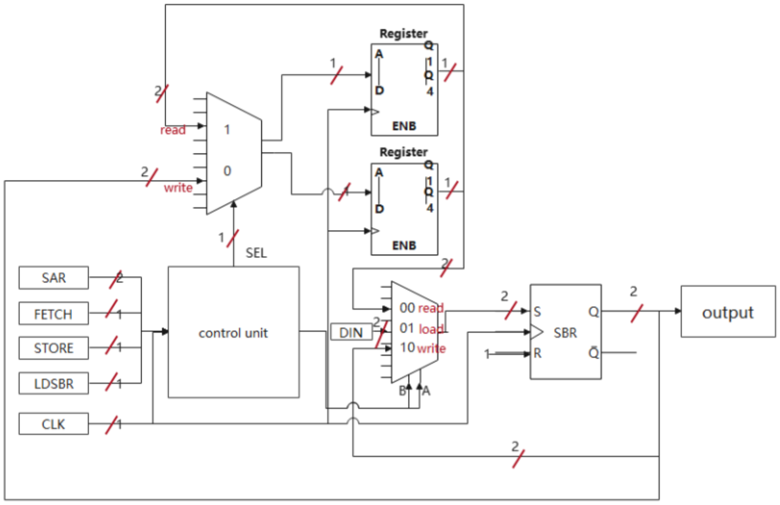
3. Description and block diagram of memory circuit implementation

a. High-level description

   i. The components we used to perform the operations are SHIFT REGISTER (SN74194), 2-to-1 MULTIPLEXER (SN74157), 4-to-1 MULTIPLEXER (SN74153), RIPPLE

COUNTER (SN7493), COMPARATOR (SN7485), FLIP-FLOPS (SN7474) and some Logic Gates.
There are six kinds of input signals, including SAR, FETCH, STORE, LDSBR, CLK and DIN. Through the CONTROL UNIT, these signals will be transmitted to two SELECT signals to MUX to commit read, write and load operations. MULTIPLEXERs here act as switches, FLIP-FLOPS act as SBR, two 4-bits SHIFT REGISTERs store 4 2-bits words and continue to shift right.

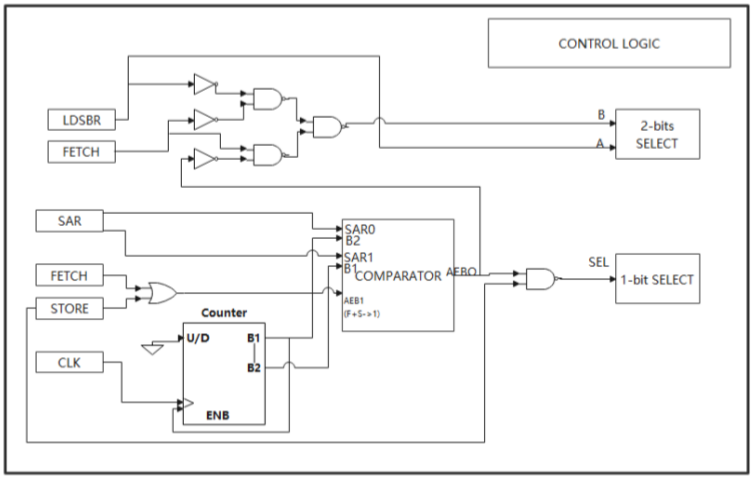
b.



4. Control Unit

a. Provide an intuitive written description of your control unit: The Control Unit will output two SELECT signals to the MULTIPLEXERs. It is implemented with three kinds of major components: COMPARATOR, COUNTER, and GATES. As shown in the figure, the function of A signal is LDSBR, the function of B signal is $\overline{LD + FETCH} + \overline{FETCH + COMP}$ and the function of SEL signal is STORE+COMP. The COMPARATOR will determine whether the current position of words in the REGISTER recorded by the COUNTER and SAR match, if so, it will output high COMP signal when FETCH or STORE signal is high.

b.

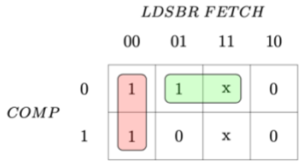


5. Design steps taken and detailed circuit schematic

a. We construct a truth table to indicate how the Control Logic operates as shown below. The EQUAL signal represents the output of COMPARATOR while the SELECT represents the select signal for 2-to-1 MUX. We only consider the situation that only one instruction is fetched each time according to the requirement of the experiment.

FETCH	STORE	LOAD	EQUAL	SELECT	BA
0	0	0	0	1	10
1	0	0	0	1	10
1	0	0	1	1	00
0	1	0	0	1	10
0	1	0	1	0	10
0	0	1	0	1	01
0	0	1	1	1	01

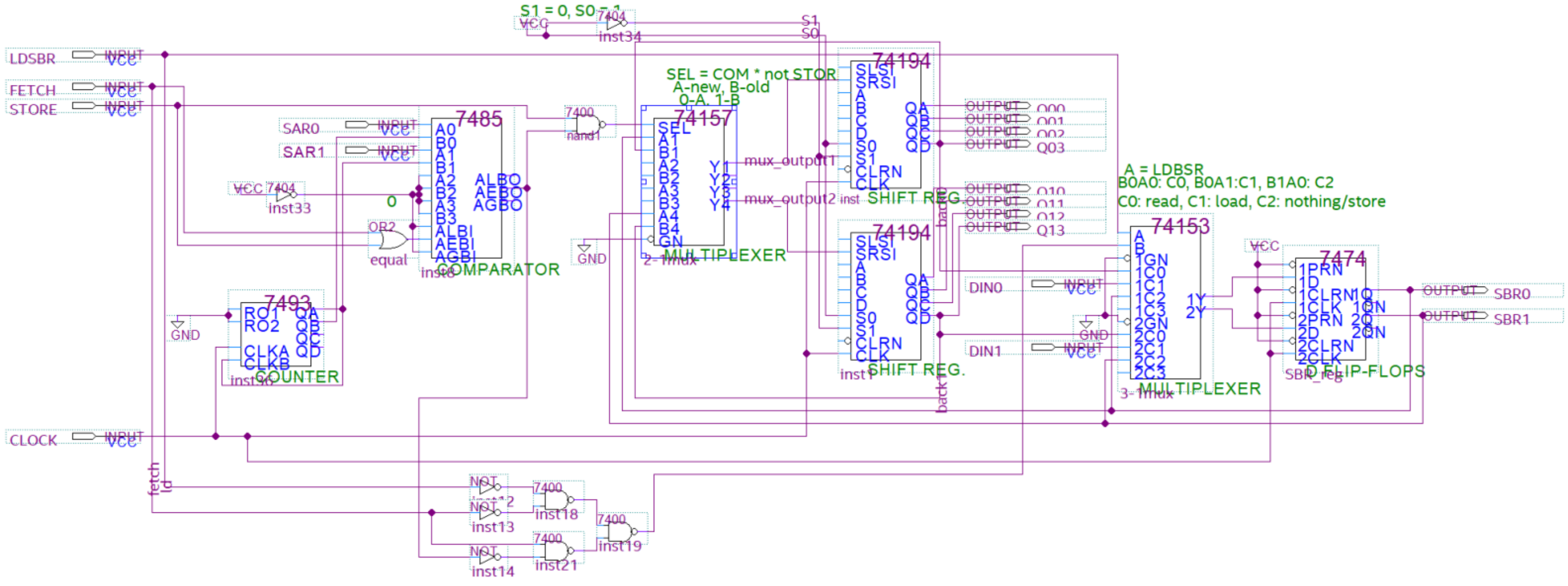
From the table showing above, it is obvious that SELECT is only related to STORE signal and we can hence derive SELECT = $\overline{STORE \cdot EQUAL}$. As for the signal BA, we can also indicate easily that A is only related to the signal LOAD and we can omit the effect of EQUAL when LOAD is performed since no address is needed. Hence, A =$LOAD$. For signal B, we can obtain that B = $\overline{LD + FETCH} + \overline{FETCH + COMP}$ from the Karnaugh Map showing below.



COMP \ *LDSBR FETCH*	00	01	11	10
0	1	1	x	0
1	1	0	x	0

b. Written description of the design considerations taken (did you consider multiple implementations of the same circuit and the tradeoffs of each?)
Most part of the circuit do not take many considerations due to the function of each component. The part of circuit that could have multiple designs should be the Control Logic.

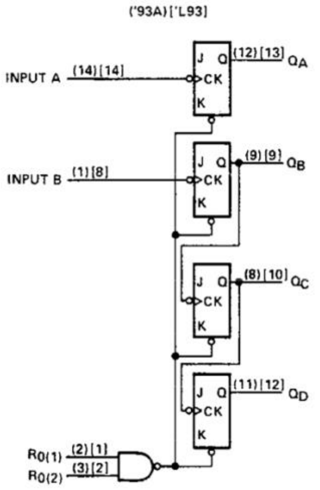
c. Detailed Circuit Schematic (in section 3 and 4)



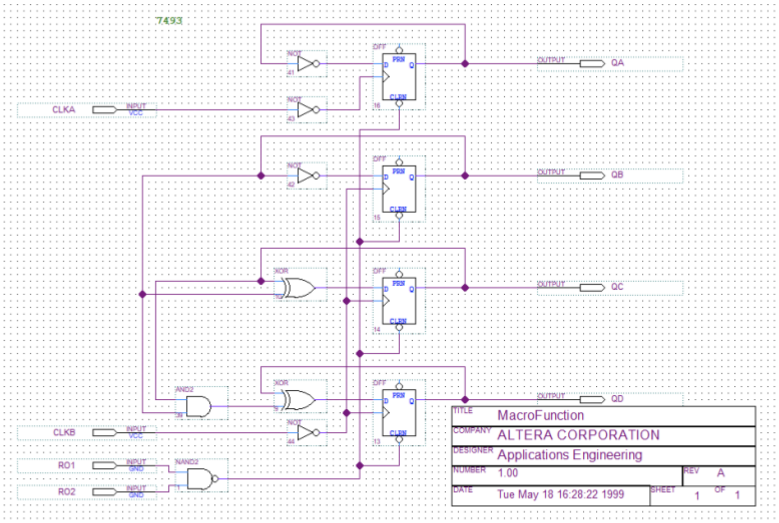
Circuit Schematic of our lab

6. Description of all bugs encountered, and corrective measures taken

The first bug occurred at the counter part where it cannot count up successfully. In order to find out the reason, we check the inner logical diagram of the SN7493 Ripple Counter. The inner design logical diagram and simulation circuit have been shown below.



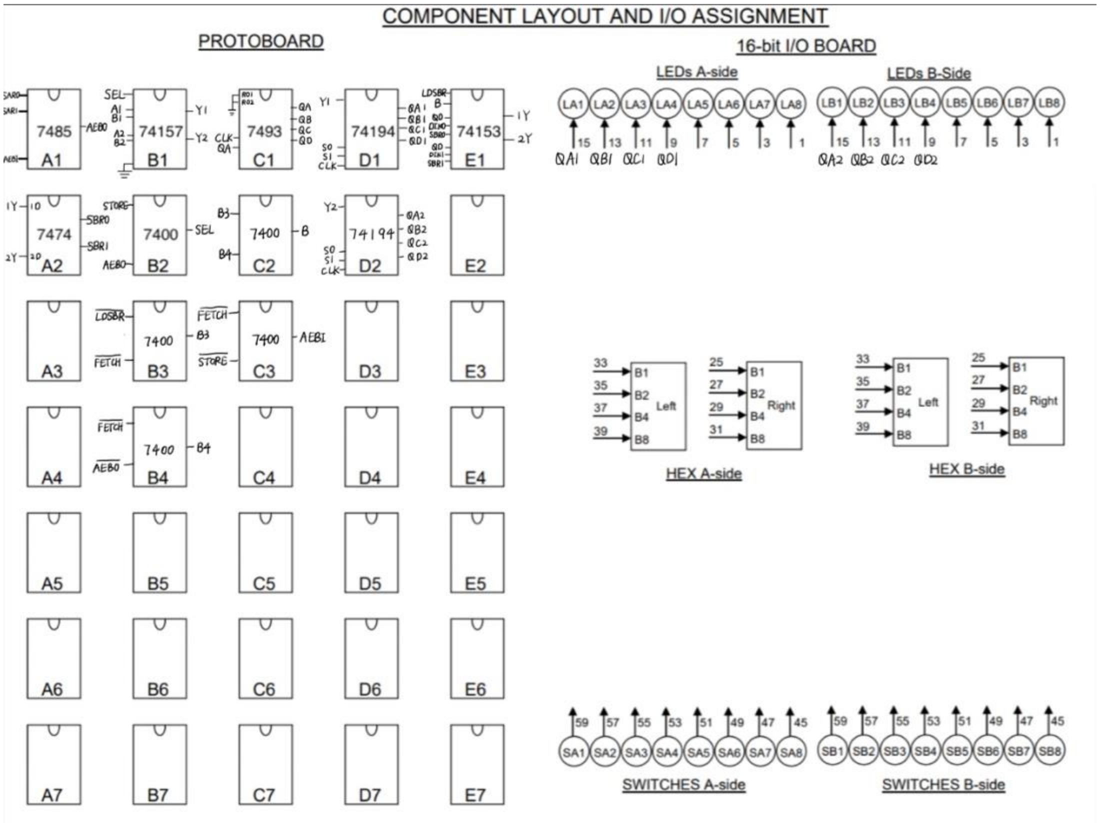
Logical Diagram of SN7493



Design File of SN7493

From the design file I notice that pin *CLKB* and *CLKA* are two different *CLK* pins compared to the original logical diagram, which has only one *CLK* pin. Hence, we connect the pin *QA* to the pin *CLKB* on the Ripple Counter according to the design file which successfully solve the bug.\

7. Component Layout Sheet



8. Answers to Lab Questions

A．Pre-lab:

1. The clock must run continuously – do not gate the clock (this is bad practice in digital design, why?

In the practical design of circuit, if we gate the clock with other signal, the possible noise exist in the signal would cause glitch and hence result in error and damage.

B. Post-lab:

1. What are the performance implications of your shift register memory as compared to a standard SRAM of the same size?

Compared to the standard SRAM, the shift register memory has mainly three advantages. Firstly, it cannot access random address immediately since it needs to wait for the counter to match the address wanted. For shift register of small size, the effect of counter could be omitted. However, for shift register memory of large size, it would be much slower to access data using counter compared to SRAM, which could read sequence of data in one access. Secondly, the shift register memory uses serial output due to the design of the registers, which significantly influence the speed of access when read large data. Moreover, the shift registers memory use flip-flops to store data while the standard SRAM use paired inverters to store bits, which result in less energy consumption for SRAM.

2.What are the implications of the different counters and shift register chips, what was your reasoning in choosing the parts you did?

There are three types of counters listed in available components list, which are *SN7493 4-bit Ripple Counter, SN74LS169A 4-bit UP/DOWN Counter* and *SN74LS193 4-bit UP/DOWN Counter*. We use *SN7493 4-bit Ripple Counter* for this lab. The second and third counters are basically the same. They can be initialized using *LOAD* or be paused by ourselves. For this lab, we thought that the ripple counter is enough for us to implement the circuit. Also, it is synchronous such that we only need one clock to control the whole circuit, which could greatly simplify the design and make it easier to debug.

9. Conclusion

In Lab2, we design and construct a simple 2-bit, four-word shift-register storage unit. All functions of our simulated circuit work successfully and we have the proper waveform generated. We have some insights into the design of circuit using Quartus during the experiment. Also, this experiment helps us on learnning how to design a control logic according to the instructions and output needed, which might have significant effect on our future work.