Guanshujie Fu

8700 Küsnacht,
Switzerland

Personal Web
fuguan@student.ethz.ch

EDUCATIONS

ETH Zürich (ETHz) Zürich, Switzerland
M.S. in Information Technology and Electrical Engineering-EEIT 2023.09 - Present
- Specialized in *Computers and Networks*

University of Illinois, Urbana Champaign (UIUC) Illinois, USA
B.S. in Computer Engineering-ECE (GPA: 3.85/4.00) 2019.09 - 2023.06
- Graduated with *High Honors*
- Dean's List (2020&2021&2022)

Zhejiang University (ZJU) Hangzhou, China
B.E. in Computer Engineering-ECE (GPA: 3.97/4.00) 2019.09 - 2023.06
- Graduated as *Outstanding Graduates of Zhejiang University*
- ZJU-UIUC scholarship (2020&2021)

SKILLS

Programming:
Proficient in *C/C++, Golang, Python, Java, Assembly, SystemVerilog*
Intermediate in *CUDA-C, RTL, P4, Haskell, MATLAB.*
Knowledge of *Linux Kernel, Network Protocols, Distributed System, Frontend Design*
Frameworks/Tools: *Docker, Kubernetes, Redis, Altera Quartus, Vitis/Vivado, Git*
Cloud/Database: *AWS, Spark, MySQL*

EXPERIENCES

Backend Engineer Intern | Hangzhou Houqi Tech Co. Ltd | *Kubernetes, Docker, Golang, C++* 2023.02 - 2023.05
- Worked in the develop group, my duty mainly includes deploying high performance vector database *Milvus* on ***Kubernetes*** *cluster*, developing vector store/search/query APIs in ***Golang*** based on *Milvus*, and developing/maintaining ***Docker*** containers to provide low-latency vector operations as a microservice in a larger picture
- Used *ffmpeg* and *Hikvision* ***C++*** *SDK* to develop a *rtsp* video stream pulling/pushing scheme. The pulled stream data is decoded and converted into *OpenCV Mat* format to fetch into a self-developed face detection algorithm within *30ms*

Undergraduate Researcher | UIUC | *Xilinx FPGA, High Level Synthesis, C++, P4* 2022.02 - 2023.02
Advisor: Professor Nam Sung Kim
- Worked in the F.A.S.T lab, I explored the application of *Samsung SmartSSD* and *Xilinx FPGA* on Edge Computing.
- Implemented benchmark program to test bandwidth performance of *SmartSSD*, designed data encryption algorithm (Run Length Encoding and LZ77) using ***HLS C++*** in SmartSSD
- Offloaded database filter operations to *SmartSSD* to provide database operations using ***HLS C++***, and tested the performance to verify the potential application of *SmartSSD* in database operations at data center
- Worked with a Ph.D. candidate, I implemented a *Vitis* ***P4*** *module* and deployed it into *Corundum* high-performance FPGA-based NIC. The module will receive incoming network packets to split based head data and perform simple process tasks

Research Assistantship | National University of Singapore | *DPU, TCP/IP, Doca, C++* 2022.08 - 2022.11
Advisor: Professor Jialin Li
- Designed and implemented network application on *NVIDIA BlueField-2 DPU* with *DOCA Flow* acceleration
- We explored the potential of offloading the main TCP stacks from Host *CPU* to *DPU* based on DOCA Flow framework, proposed potential offloading scheme and made presentation to industry group

Teaching Assistantship | ZJU
Course: ECE385, Digital Laboratory 2023.02 - 2023.05
Advisor: Professor Chushan Li and Zuofu Chen
- Hosted weekly lab session and office hours, grading weekly programming tasks (SystemVerilog/C++) in computer lab

Course: MATH213, Discrete Mathematics 2021.09 - 2022.01
Advisor: Professor Klaus-dieter Schewe
- Hosted tutorials and Q&A sessions for sophomores, prepared exam materials, graded homework, and exam papers

PROJECTS

Flask-based Movie Recommendation Website [Repo] | UIUC 2022.06 - 2022.08
- Worked in a team to develop a website for movie collection and recommendation
- Used ***HTML*** and ***JavaScript*** to construct web pages, ***Python***-based Flask to render web pages
- Implemented the movie recommendation system using *Euclidean Algorithm*

Unix-like OS Kernel Design [Repo] | UIUC 2022.03 - 2022.05

- Led a team to design and implement an OS kernel resembling Linux with basic and advanced features in ***C*** and ***Assembly***
- The kernel includes disk read/write, file system support, virtual memory, scheduling, interrupts & exceptions and etc.
- Designed a high-resolution (60fps, 800*600 resolution) graphic user interface with standard VGA capable

FPGA-based Graphic Design [Repo] | UIUC 2021.09 - 2021.12

- Developed an *FPGA-based* version of video game using ***SystemVerilog*** along with SoC, capable of processing and outputting complex graphics (60fps, 640*480 resolution) to *VGA* in a high frame rate and enabling keyboard control
- Used a *NIOS II SOC* to run the software game loop FPGA and communicate to the graphics system through the *Avalon Bus*
- Designed a complex finite state machine (FSM) on the FPGA board to optimize user interaction and collision detection

Representation and Extraction of Diesel Engine Maintenance Knowledge Graph | ZJU 2020.06 - 2021.02

Advisor: Professor Hongwei Wang

- Designed a framework in ***Python*** to extract bidirectional relations through a novel combination of reports preprocessing, *BERT* model and *Bi-LSTM-CRF* model
- Enabled the framework to construct diesel engine maintenance knowledge graph based on data set collected from power plants, automatically extract key information from the unstructured text in maintenance reports, transfer the extracted results into a structured knowledge graph using *Neo4j*, and construct bidirectional relations in the graph using *Protégé*

PUBLICATION

Jin Y., **Fu G.**, Qian L., Liu H., Wang H. "Representation and Extraction of Diesel Engine Maintenance Knowledge Graph with Bidirectional Relations Based on BERT and Bi-LSTM-CRF Model", in 2021 IEEE International Conference on e-Business Engineering (ICEBE 2021), pp 126-133, Nov. 2021. [Paper]