

Microeletrônica

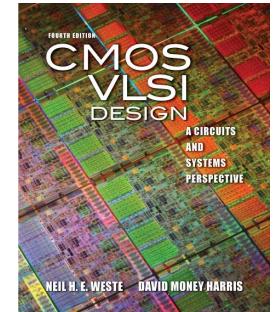
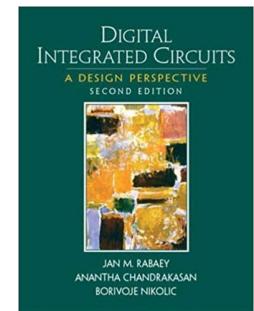
Aula #3 → Portas lógicas estáticas

□ Professor: Fernando Gehm Moraes

□ Livro texto:

Digital Integrated Circuits a Design Perspective - Rabaey

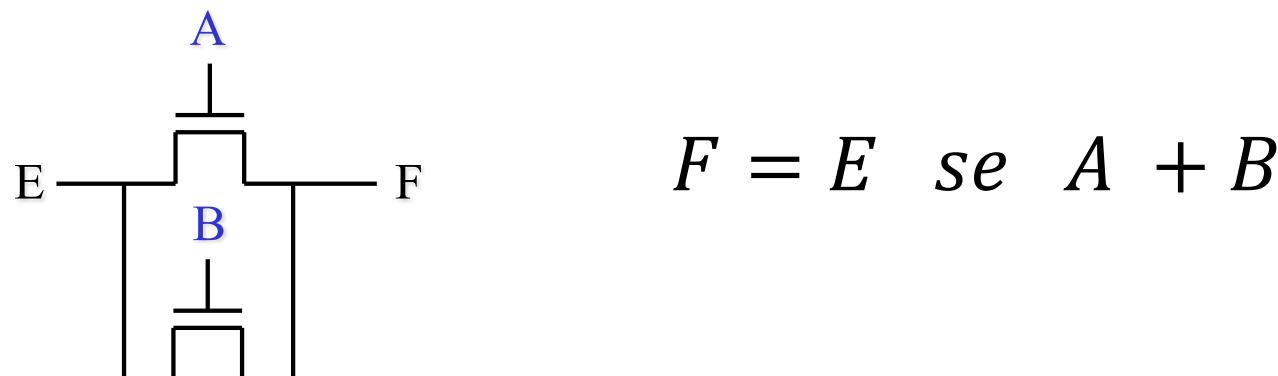
C MOS VLSI Design - Weste



Revisão das lâminas: 28/março/2025

Lógica de chaves

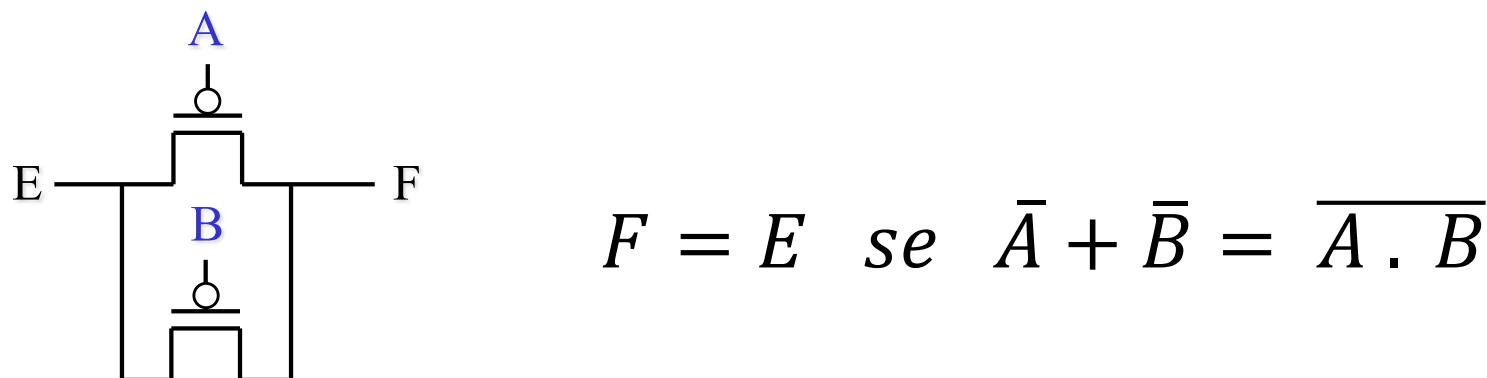
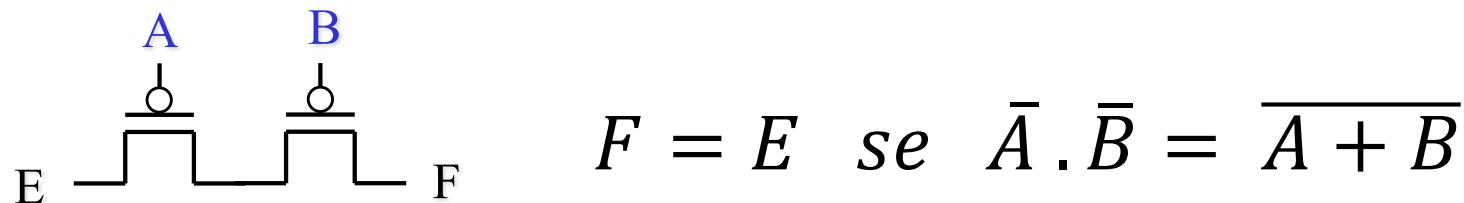
- Transistores podem ser vistos como uma chave controlada pelo sinal de gate
- Uma chave NMOS fecha quando o sinal de controle for VCC (1 lógico), desde que $VGS > VT$



O transistor NMOS passa um 0 forte e um 1 fraco

Lógica de chaves

Uma **chave PMOS** fecha quando o sinal de controle for GND (0 lógico), desde que $|VGS| > |VT|$



O Transistor PMOS passa um 0 fraco e um 1 forte

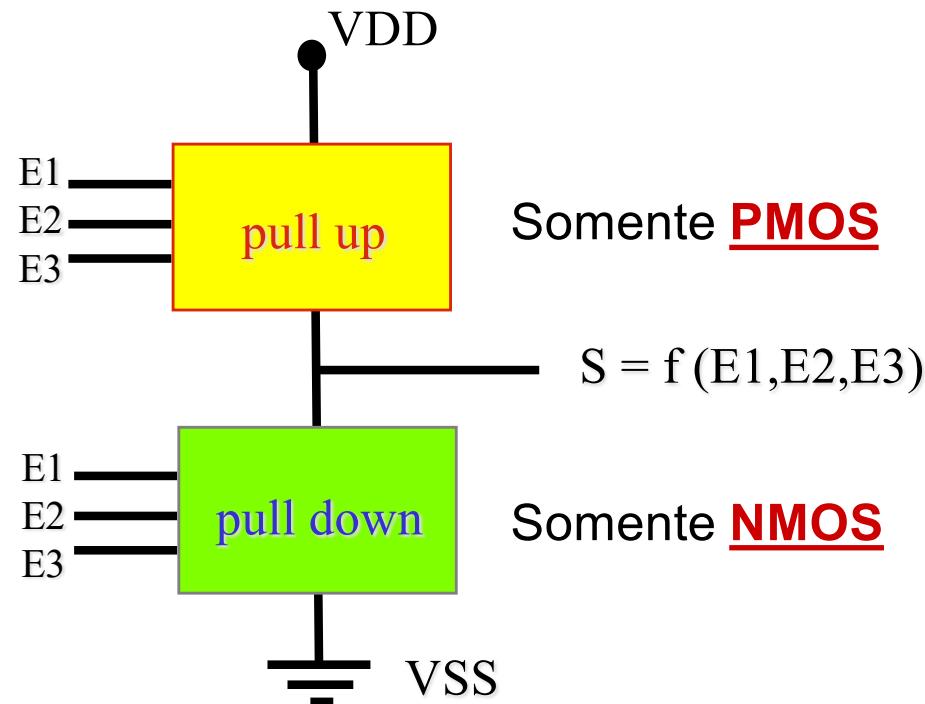
Portas Lógicas

Circuitos CMOS Estáticos

- Exceto durante o período de transição, a saída de uma **porta CMOS estática** está ligada a **VDD** ou **GND** através de um caminho com baixa resistividade.
 - Isto faz com que uma porta CMOS estática consuma muito menos que uma porta NMOS.
- A saída de uma porta CMOS assume sempre o valor da função booleana implementada pelo circuito (ignorando novamente os efeitos de transição durante o período de chaveamento).
- O colocado acima difere da classe de circuitos **dinâmicos**, que baseia-se no armazenamento temporário de valores de sinais em capacitâncias de nodos do circuito com alta impedância.

Portas Lógicas

Circuitos CMOS Estáticos



As redes PUP (pull up) e PDN (pull down) são duais

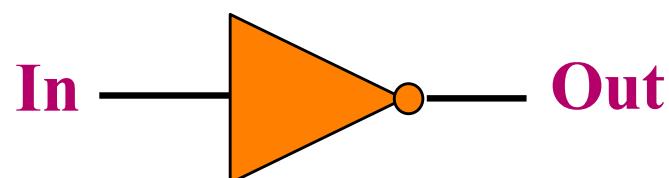
Portas Lógicas

INVERSOR CMOS

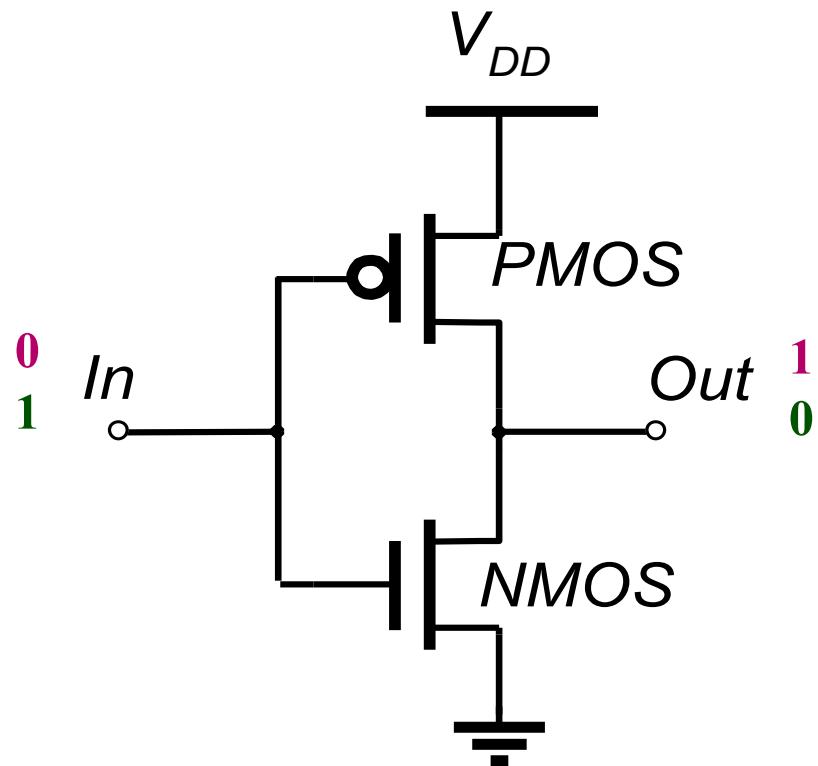
- Equação:

$$Out = \overline{In}$$

Esquema Lógico



- Esquema Elétrico CMOS

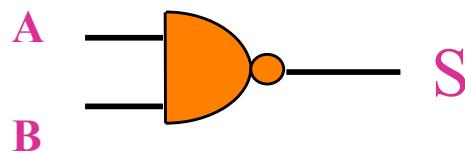


Example Gate: NAND

Equação Lógica:

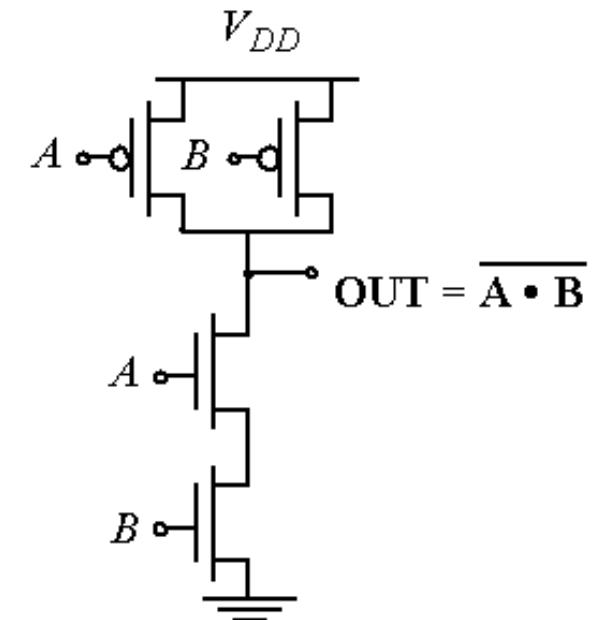
$$S = \overline{A \cdot B}$$

Esquema Lógico :



A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: $G = A \cdot B \Rightarrow$ Conduction to GND

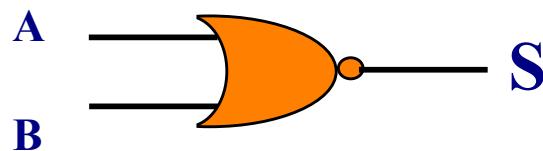
PUN: $F = \overline{\overline{A} + \overline{B}} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(\overline{In}_1, \overline{In}_2, \overline{In}_3, \dots)} \equiv F(\overline{In}_1, \overline{In}_2, \overline{In}_3, \dots)$$

Example Gate: NOR

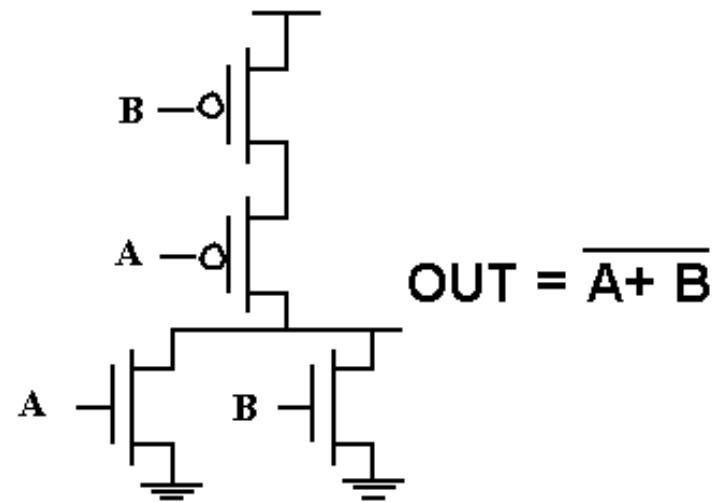
Equação: $S = \overline{A + B}$

Esquema Lógico:



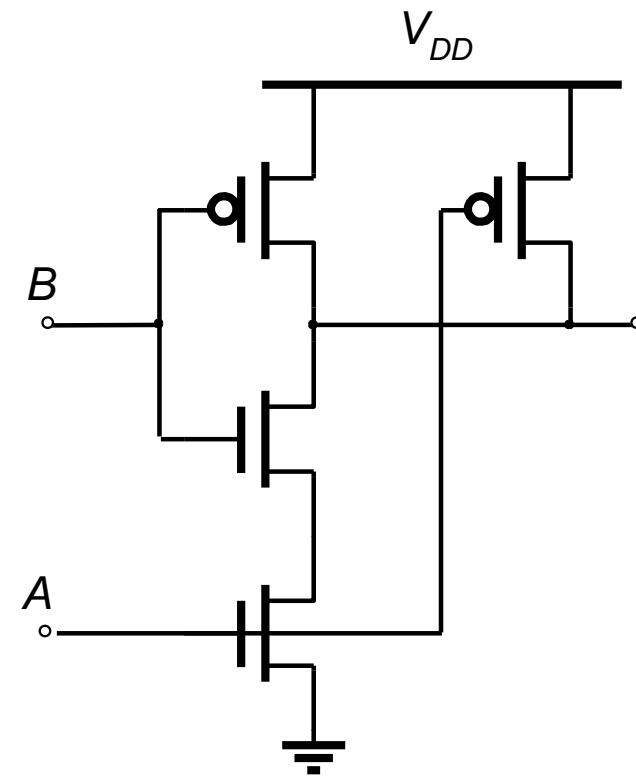
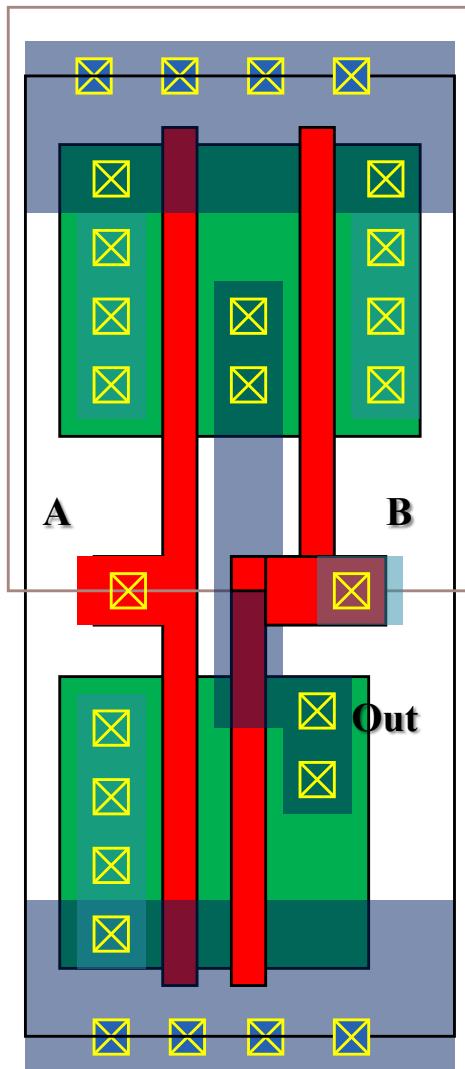
Truth Table of a 2 input NOR gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0



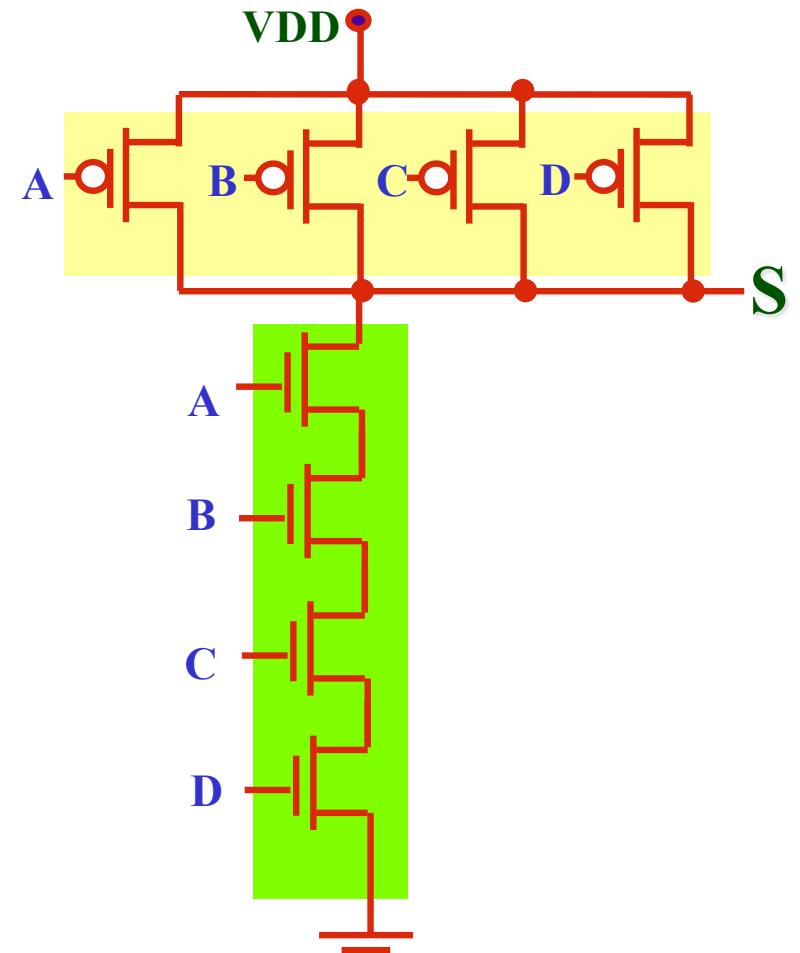
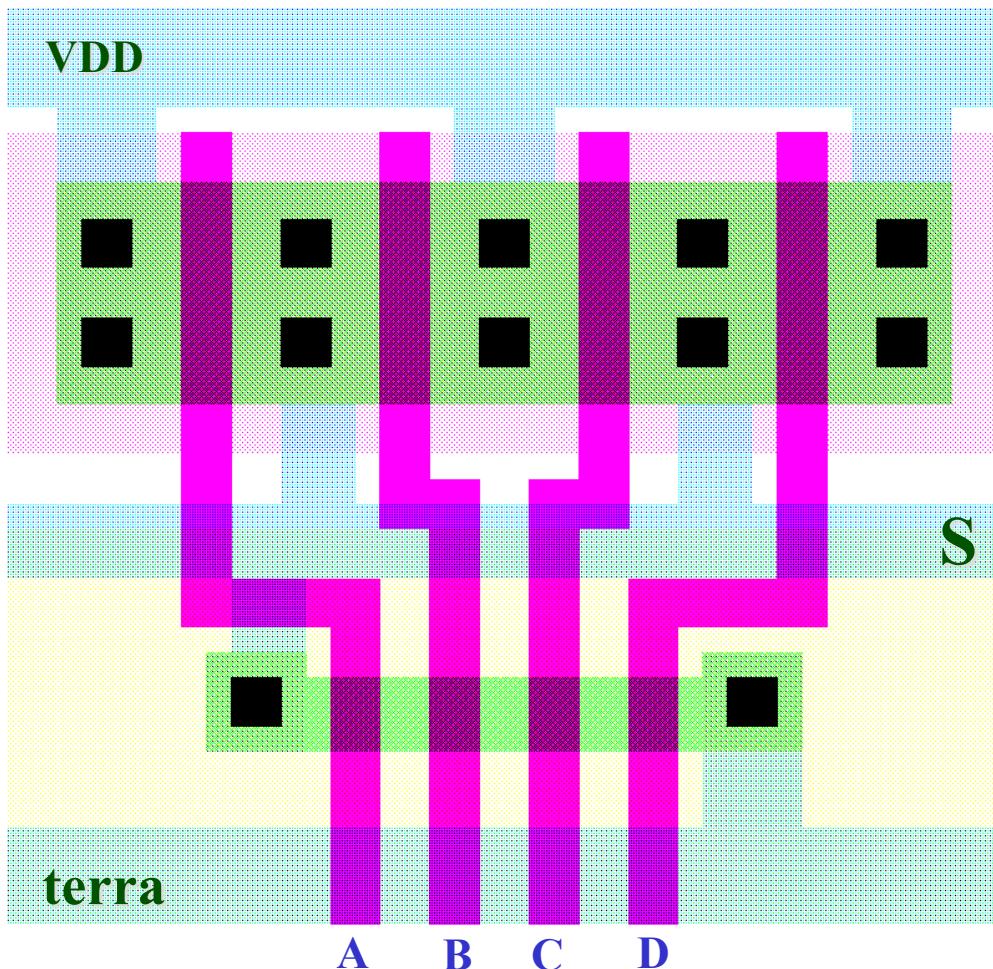
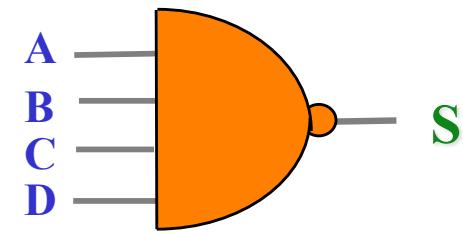
Portas Lógicas

Porta NAND CMOS



Portas Lógicas

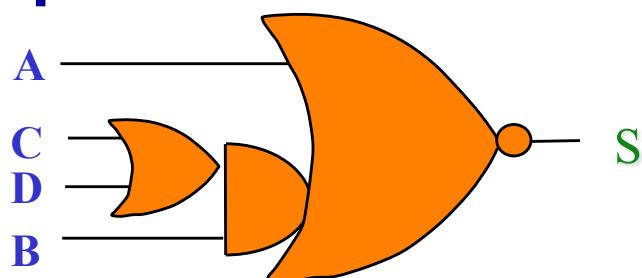
Porta NAND CMOS



Portas Lógicas

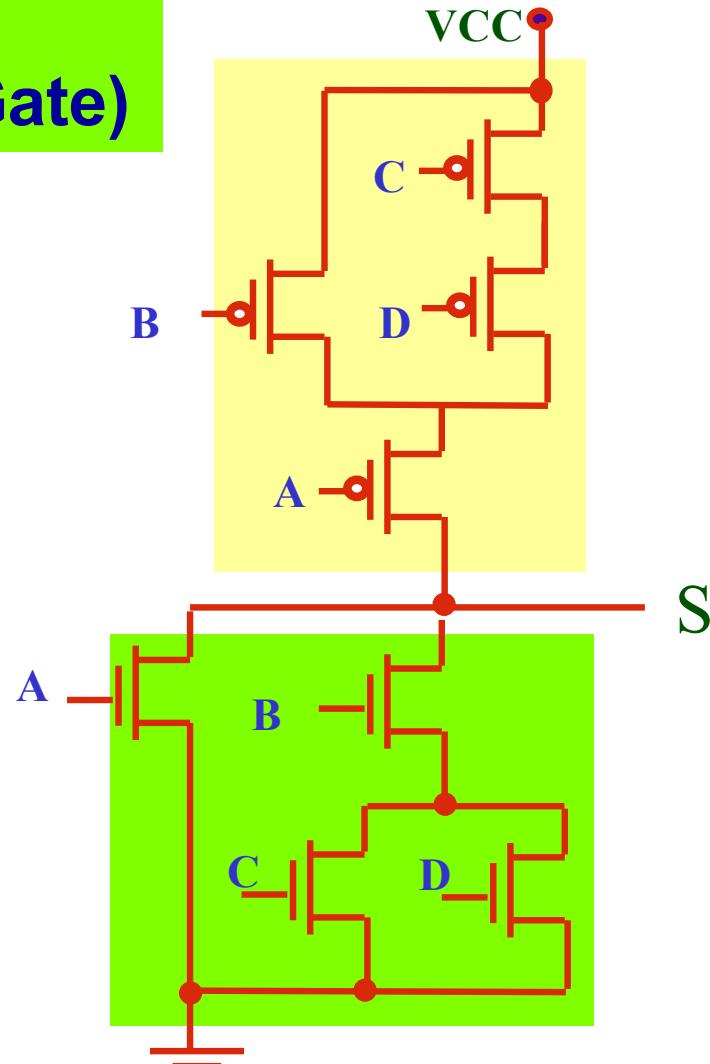
Portas CMOS Complexas
SCCG (Static CMOS Complex Gate)

Exemplo:

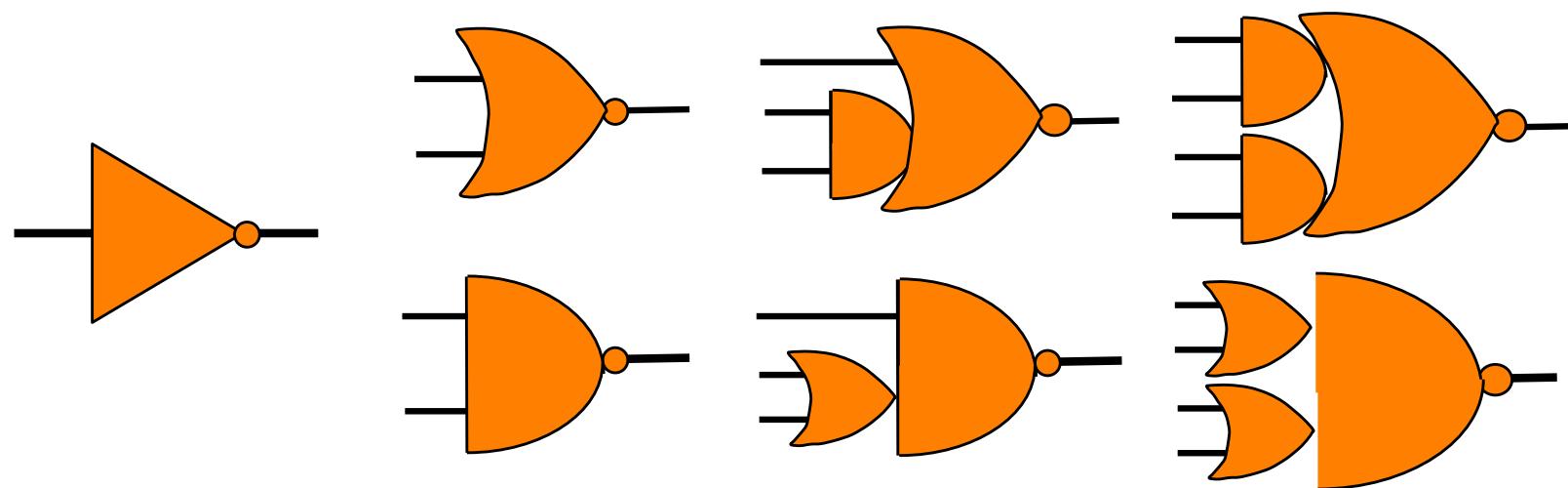


$$S = \overline{A} + (\overline{B} \cdot (\overline{C} + \overline{D}))$$

A lógica da porta é definida pelos transistores de pull down



Exemplo de funções com até 2 transistores em série



(3,3) → 87 funções diferentes

(4,4) → mais de 4000 funções diferentes

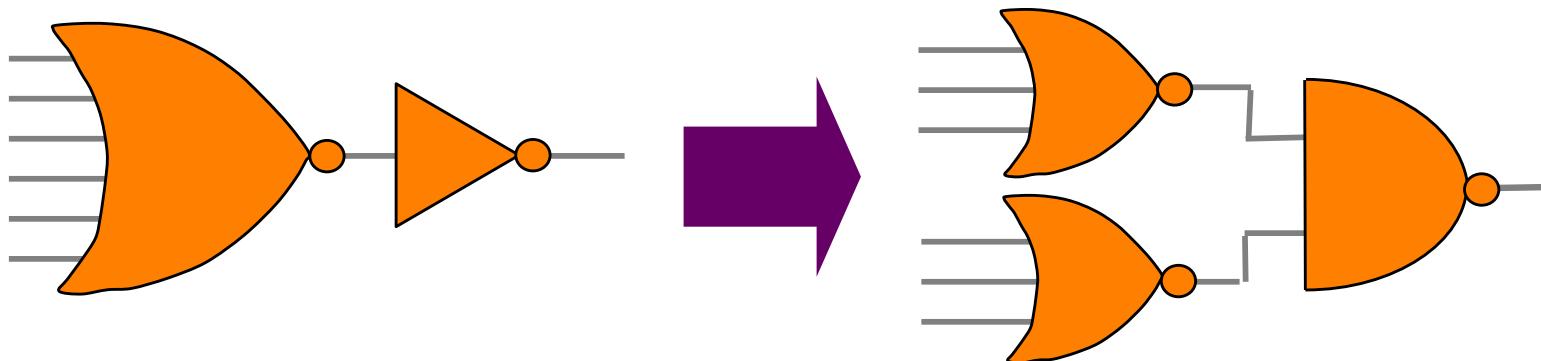
Portas Lógicas

Lógica CMOS

Restruturação lógica para redução do fanin



redução do atraso da porta

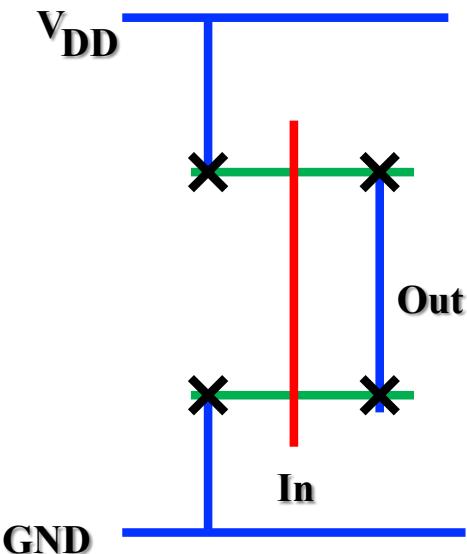


Layout de portas lógicas

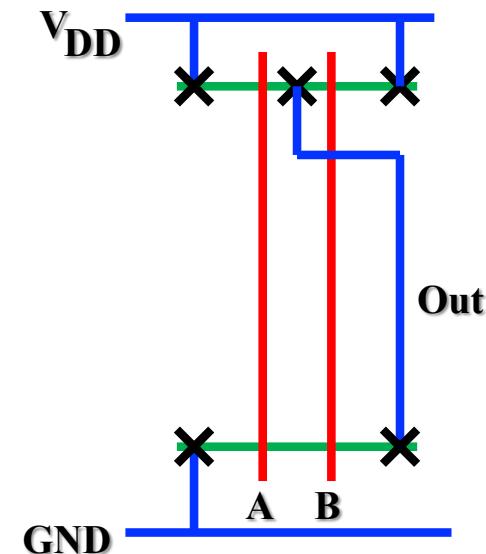
Stick Diagrams

- Não contém dimensões
- Representa as posições relativas dos transistores

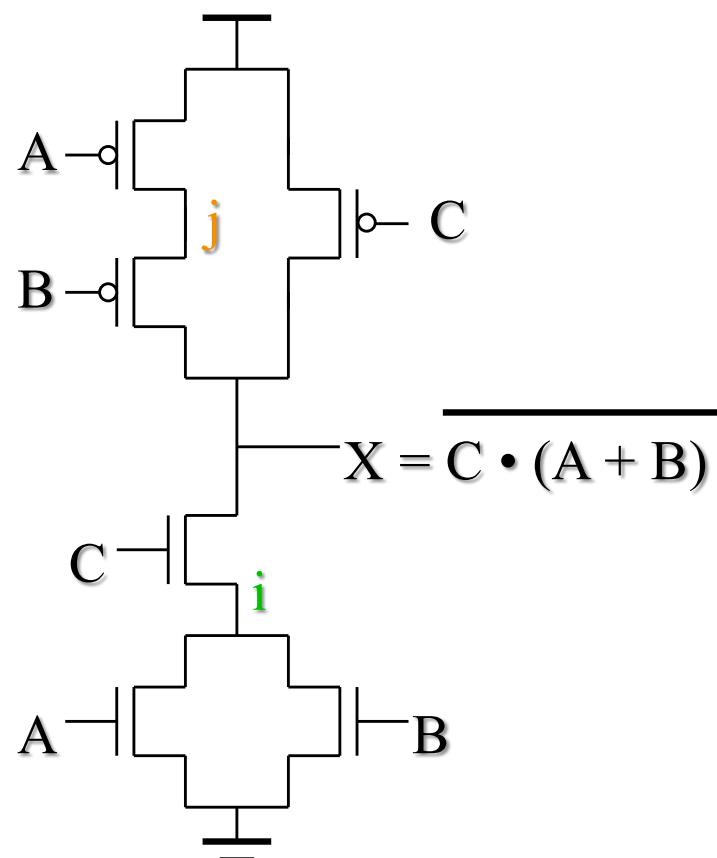
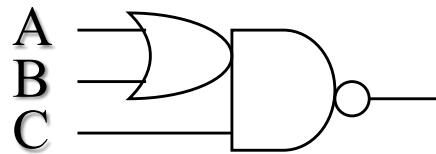
Inverter



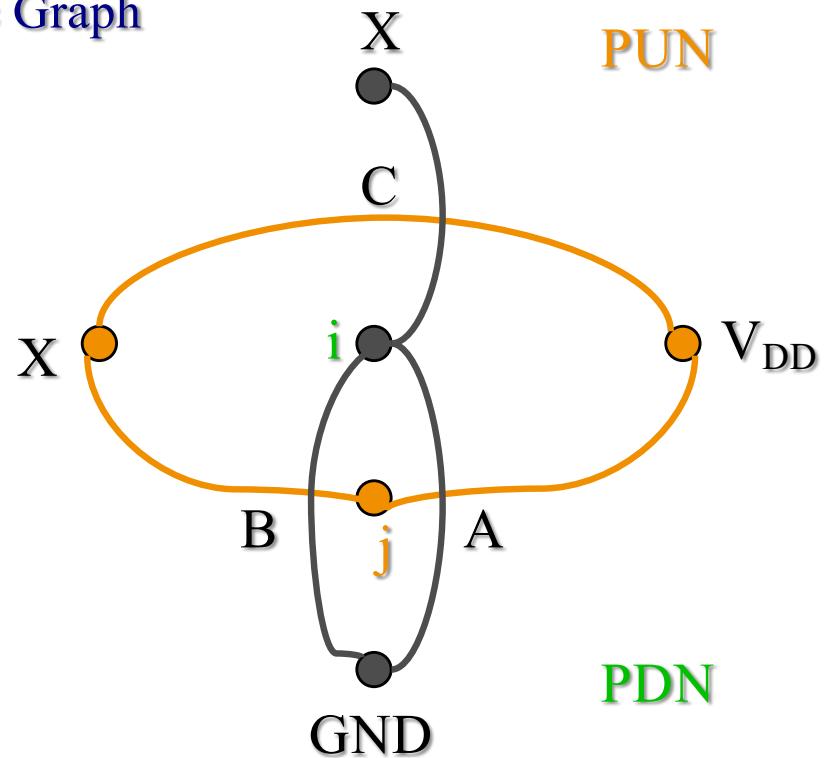
NAND2



Stick Diagrams



Logic Graph

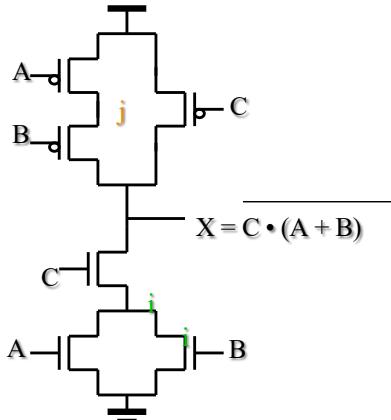


PUN

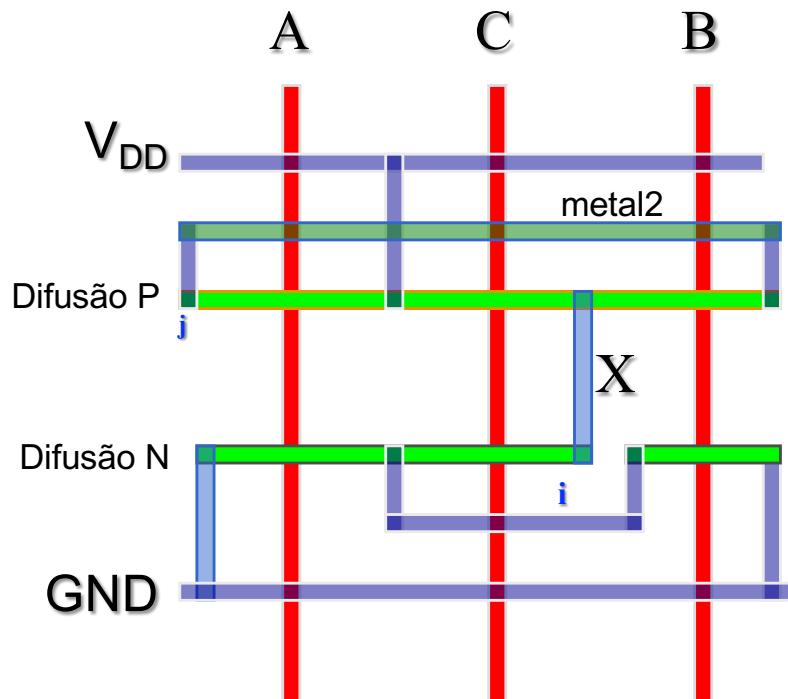
PDN

*Na teoria dos grafos, um **caminho Euleriano** é um caminho em um grafo onde se visita cada aresta exatamente uma vez.*

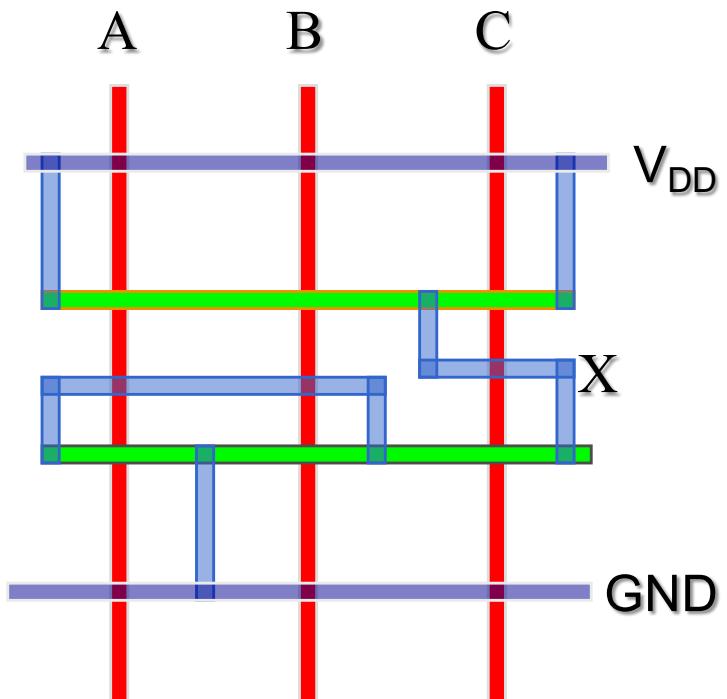
Two Versions of $C \cdot (A + B)$



- Não utilizando o mesmo caminho de Euler gera **quebra** nas linhas de difusão (gap), o que deteriora o desempenho da célula devido à capacidades parasitas

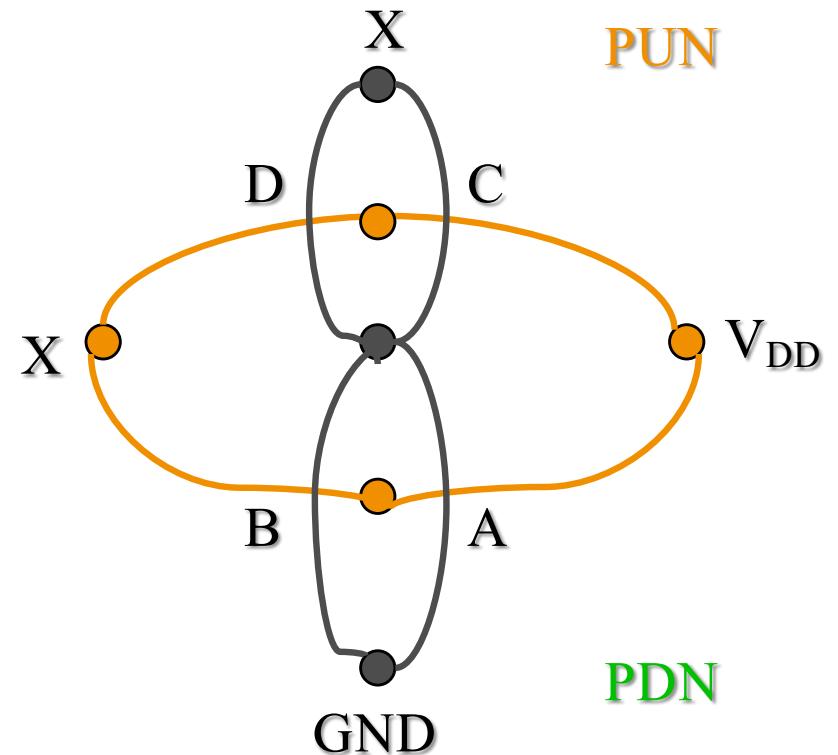
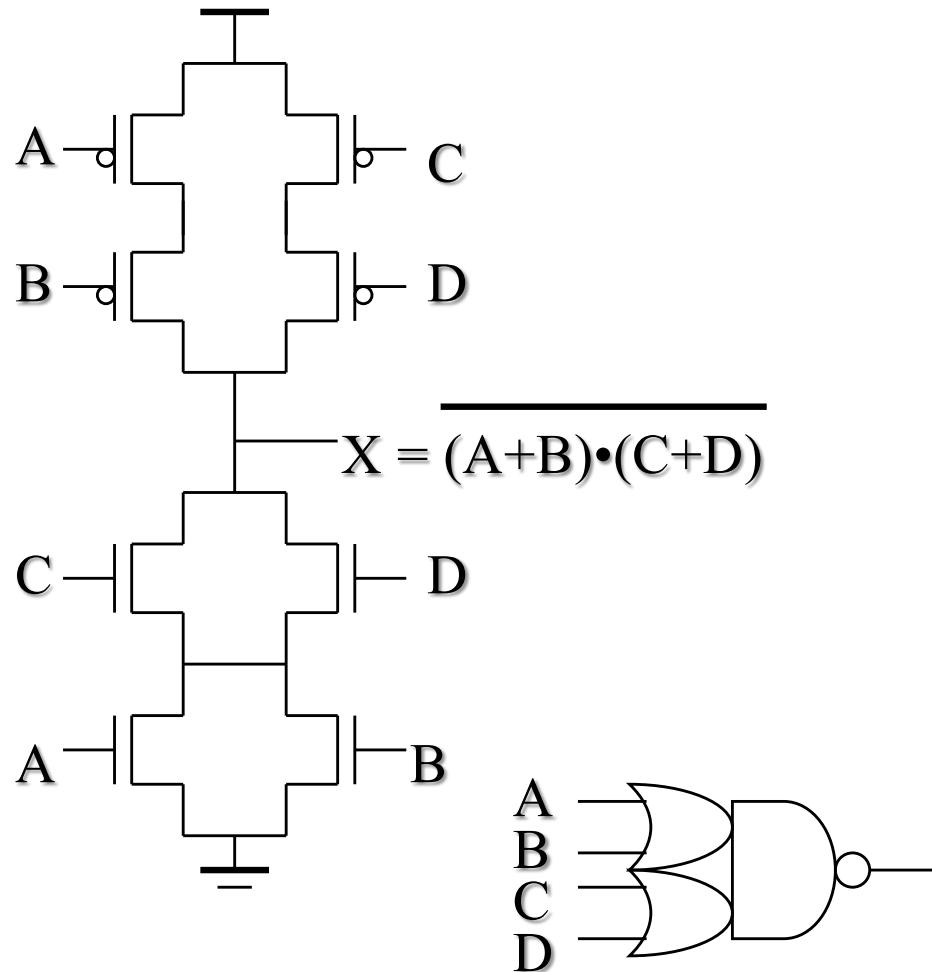


Layout com quebra na linha de difusão N entre os transistores C e B



Layout com caminhos de Euler iguais

OAI22 Logic Graph

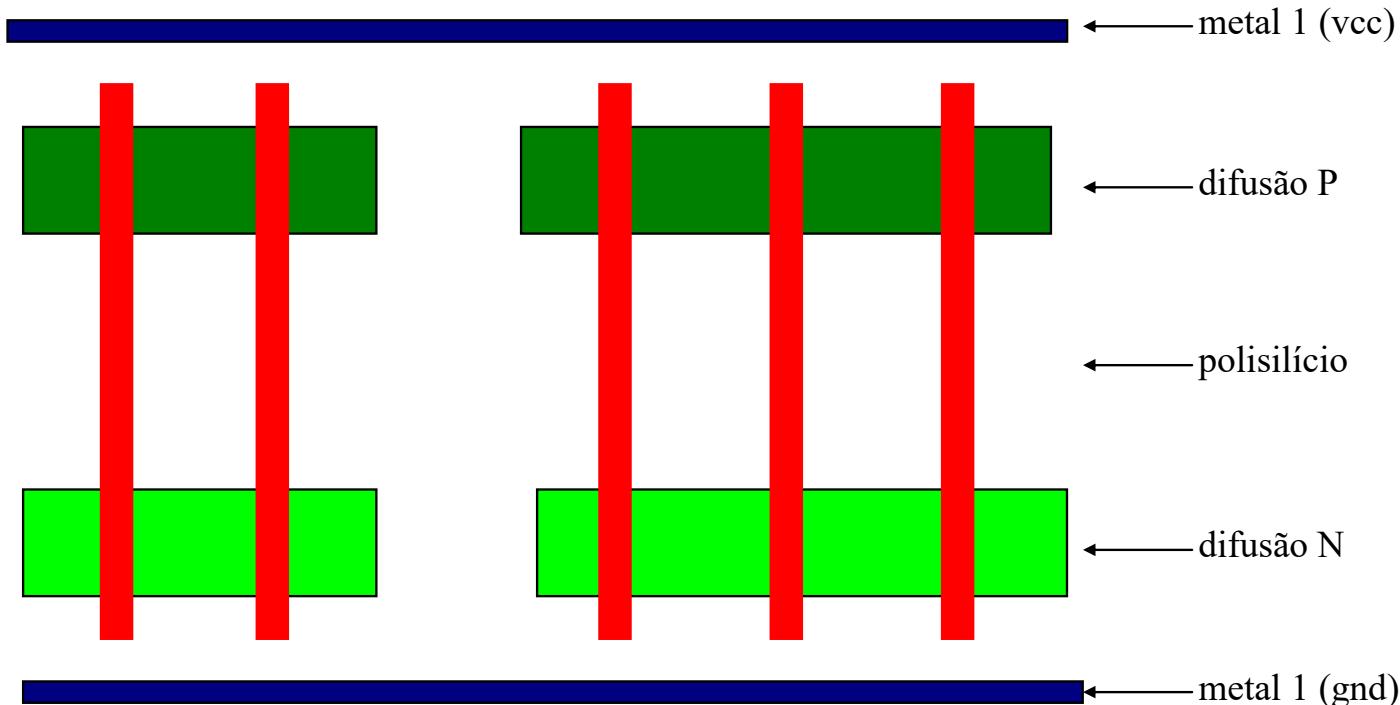
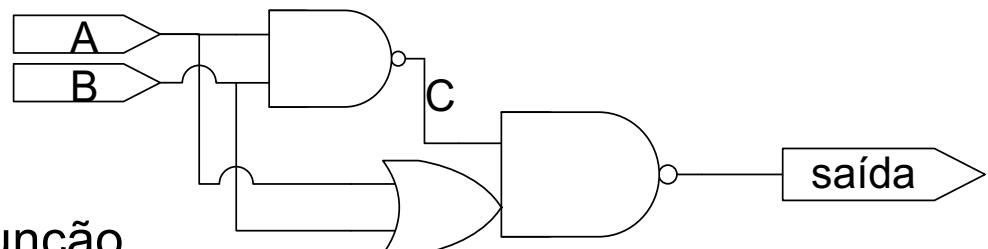


Passos para fazer o stick de uma porta complexa

1. Fazer o diagrama de transistores da porta lógica
2. Determinar um caminho de Euler **comum** aos planos N e P
3. No *template* do diagrama de stick anotar os nodos internos da célula sobre a difusão
4. Fazer as conexões de metal1/metal2 necessárias para conectar os nodos internos da célula

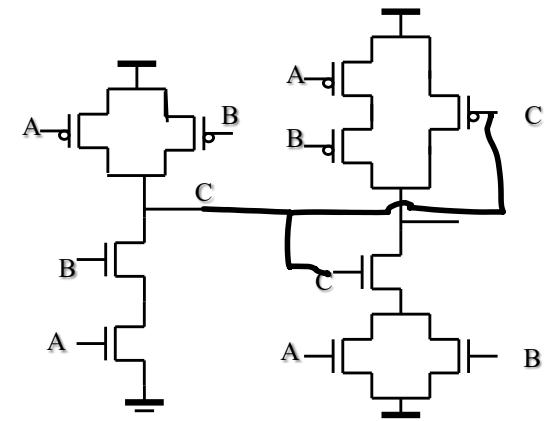
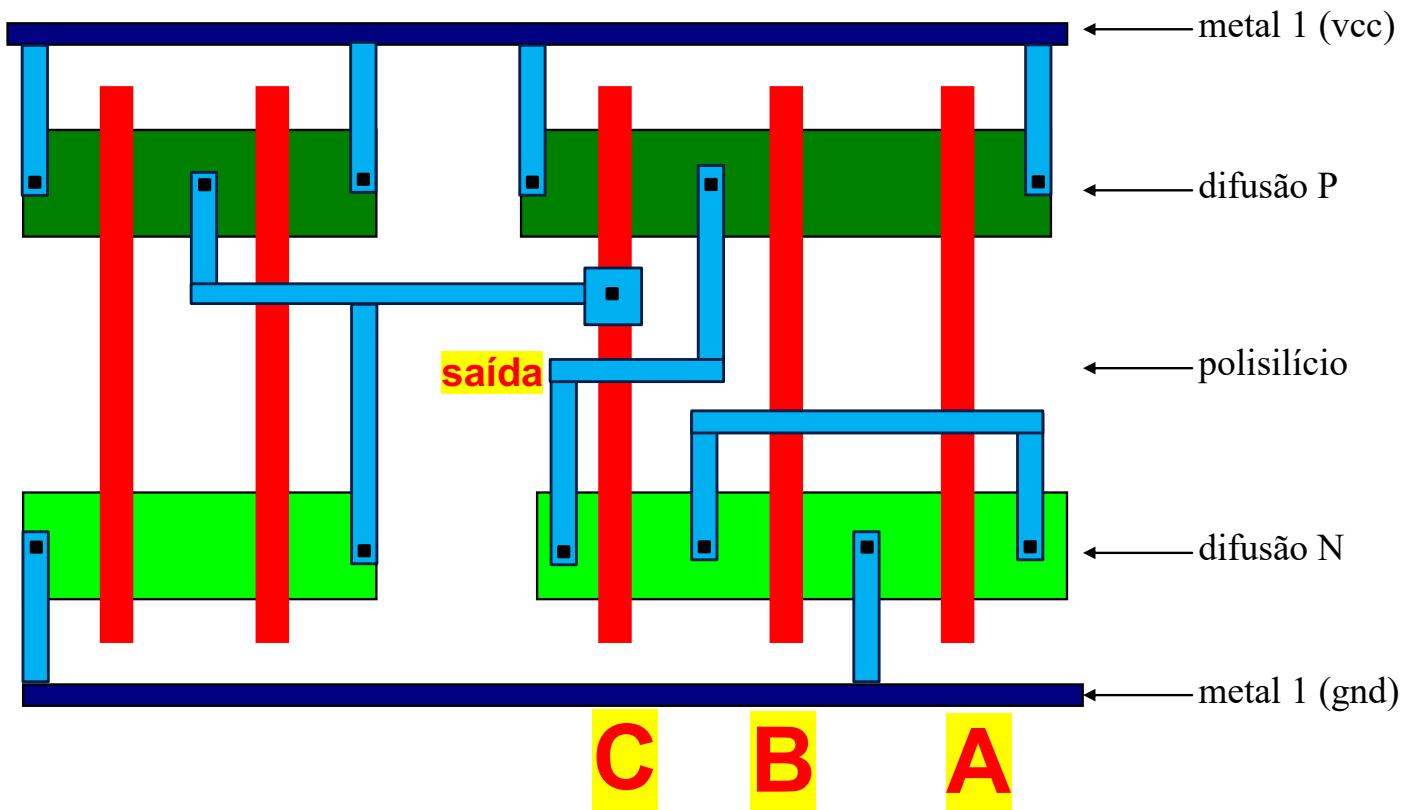
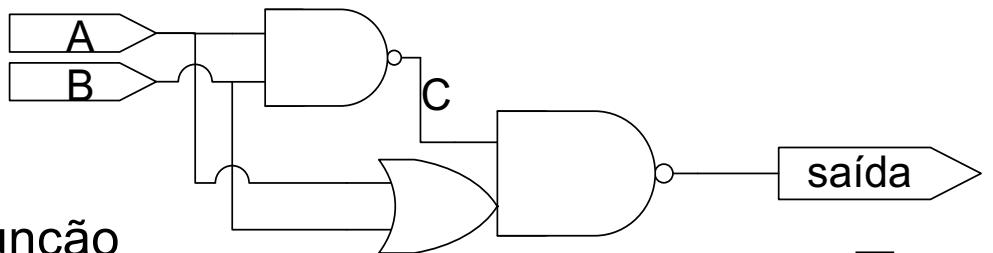
Exercício 1/8

- a) Diagrama de transistores
- b) Número de transistores
- c) Função lógica da porta
(faça a tabela verdade e diga à qual função corresponde)
- d) Diagrama stick, da função



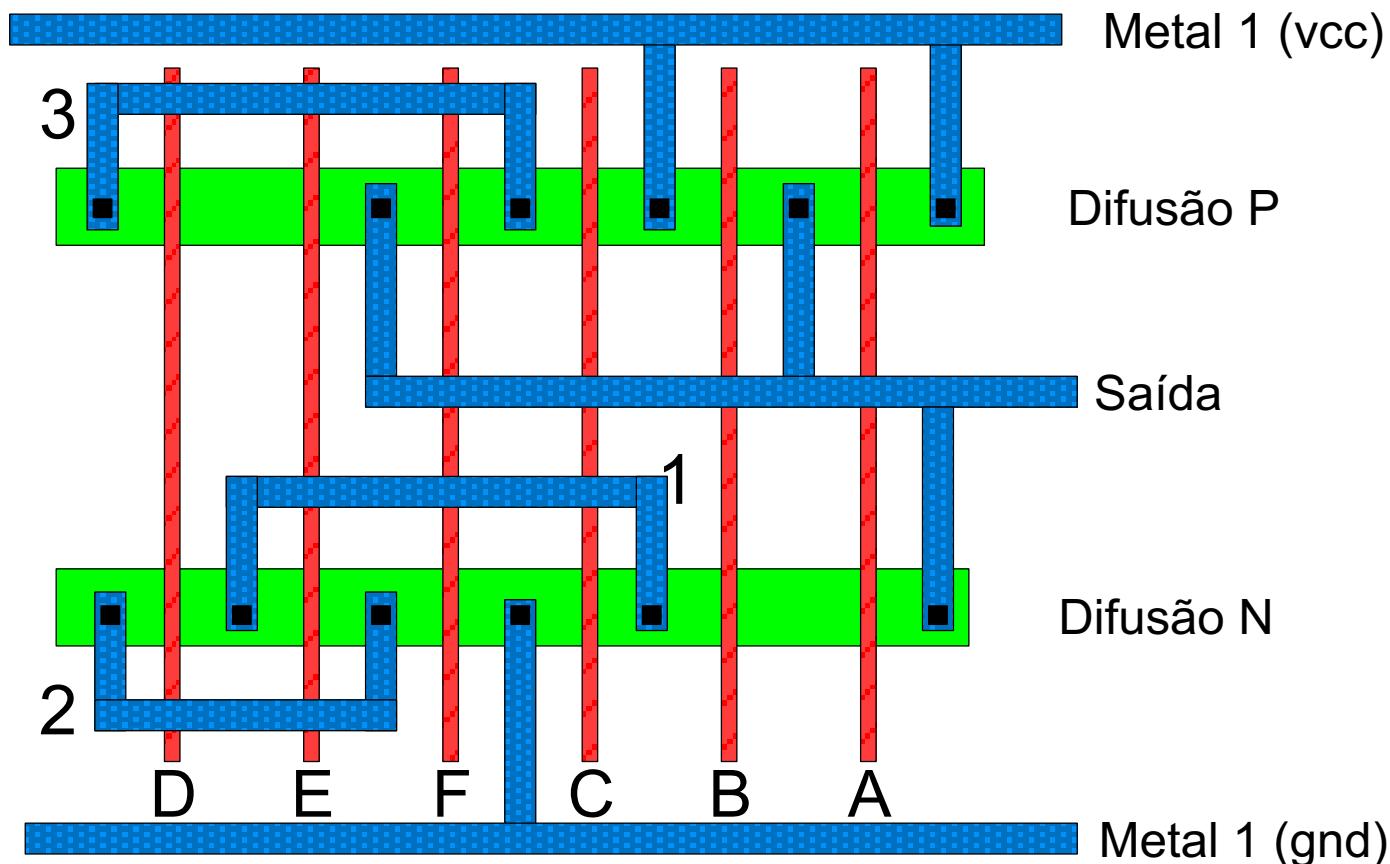
Exercício 1/8 - Solução

- a) Diagrama de transistores
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- c) Função lógica da porta
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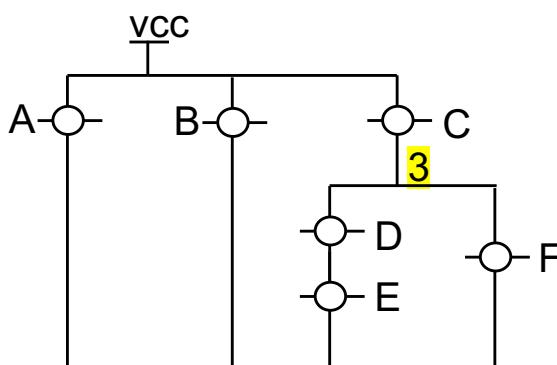
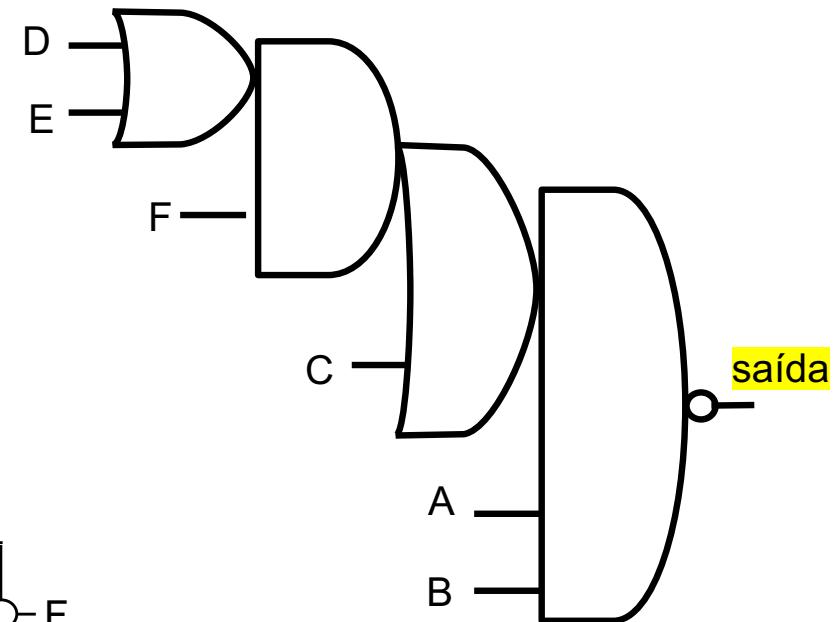
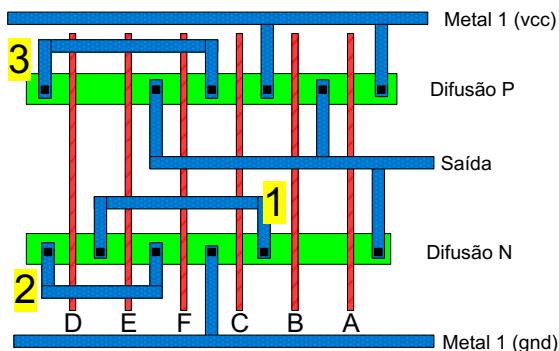


Exercício 2/8

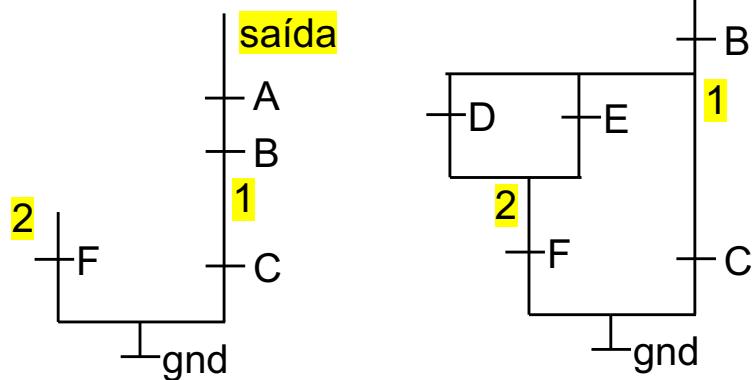
1. Número de transistores total, número de transistores N, número de transistores P
2. Diagrama de transistores
3. Diagrama lógico
4. Qual o número máximo de transistores há em série no plano N (conjunto de transistores N) e no plano P?
5. Se esta mesma função fosse implementada com portas simples (*nand*, *nor*, *inversor*) quantos transistores seriam necessários? Justifique.



Exercício 2/8 - Solução



$$\text{Saída} = \text{not}(A \cdot B \cdot (C + ((D+E) \cdot F)))$$



Exercício 3/8

$$F_2 = \overline{(a + b) \cdot (c \cdot d \cdot e + f)}$$

$$F_3 = \overline{(a \cdot b) + (c \cdot (d + (e \cdot f)))}$$

$$F_4 = \overline{a \cdot (b + (c \cdot d) + (e \cdot f))}$$

$$F_5 = \overline{((a + b) \cdot c) + (d \cdot e \cdot f)) \cdot g}$$

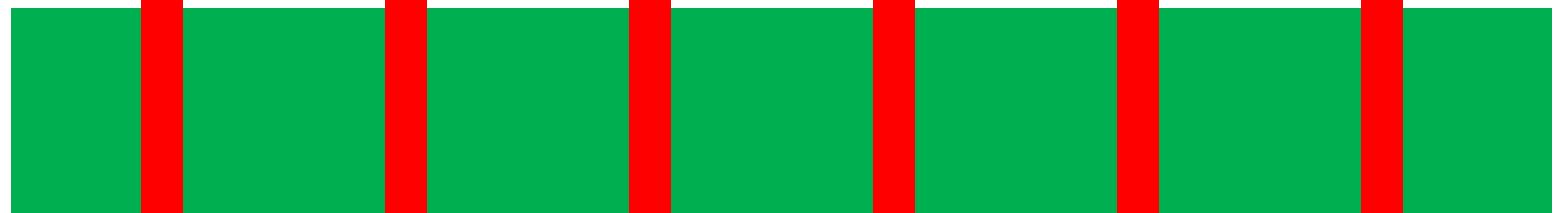
Pede-se:

- Diagrama lógico
- Diagrama de transistores
- Número de transistores, quantos transistores há em série no plano N (conjunto de transistores N) e no plano P?
- Diagrama de stick (F_4 pode ter quebras na linha de difusão P)

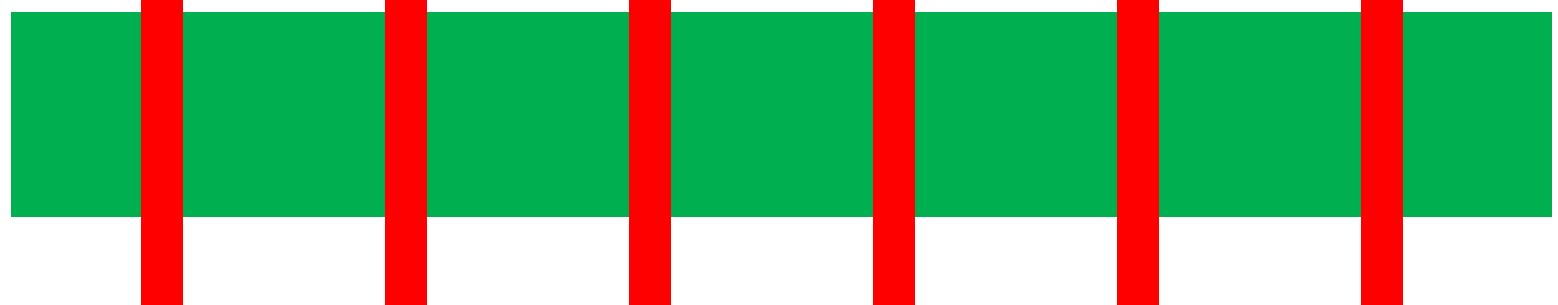
$$F_2 = \overline{(a + b) \cdot (c.d.e + f)}$$



vcc



dif. P



dif. N

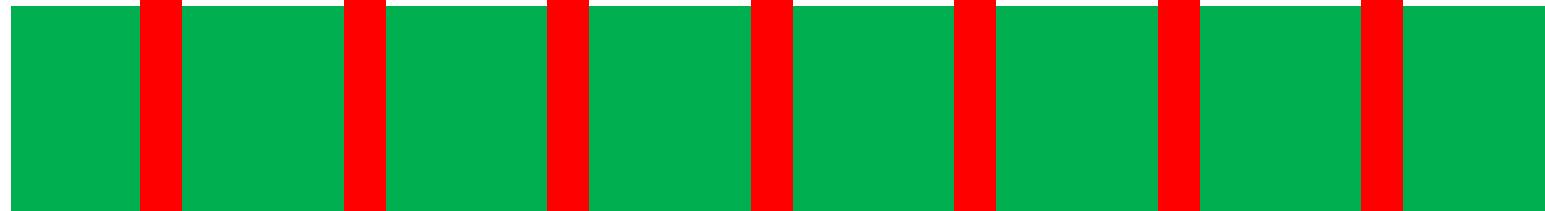


gnd

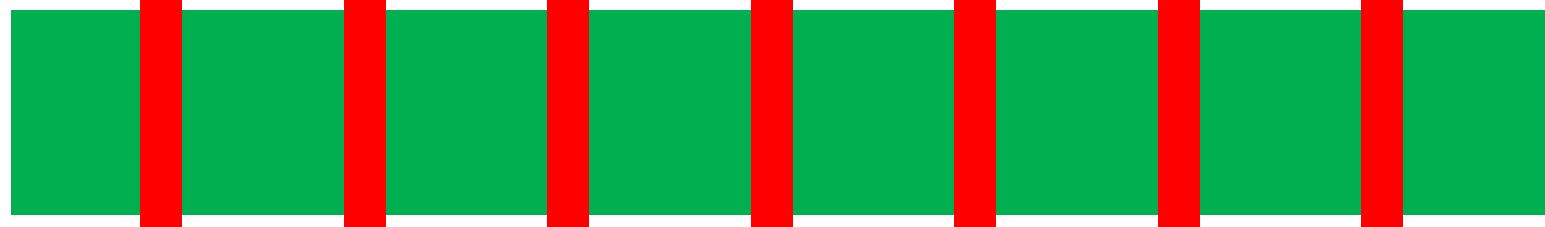
$$F_5 = \overline{(((a+b).c.) + (d.e.f)).g}$$



vcc



dif. P



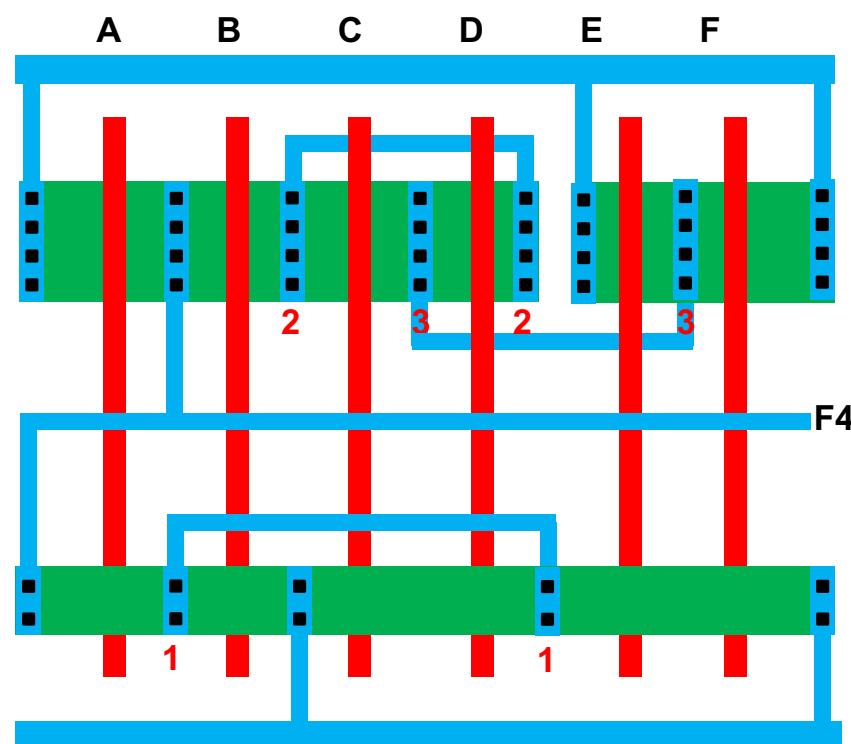
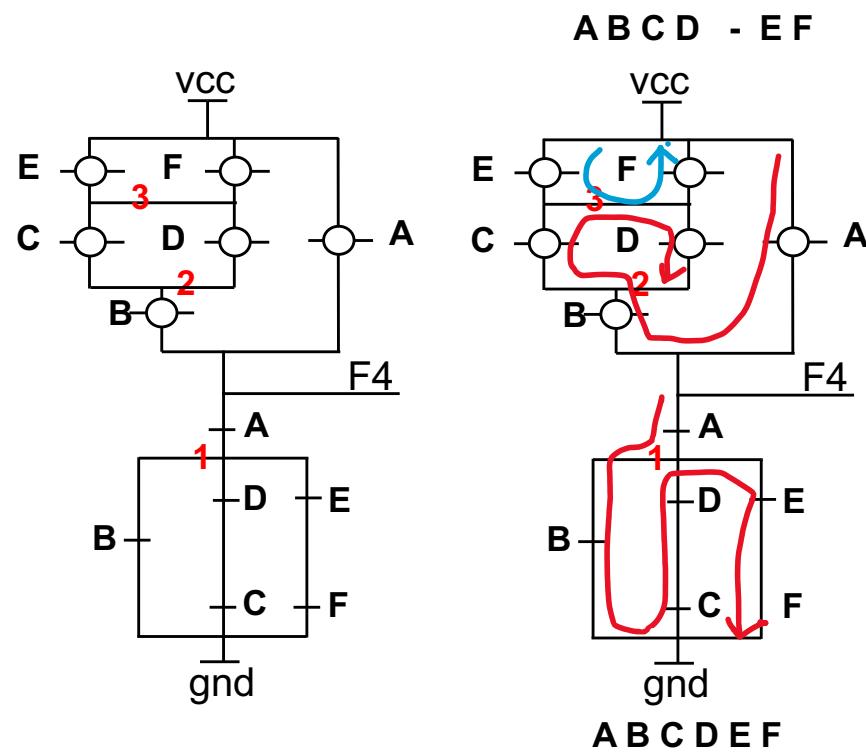
dif. N



gnd

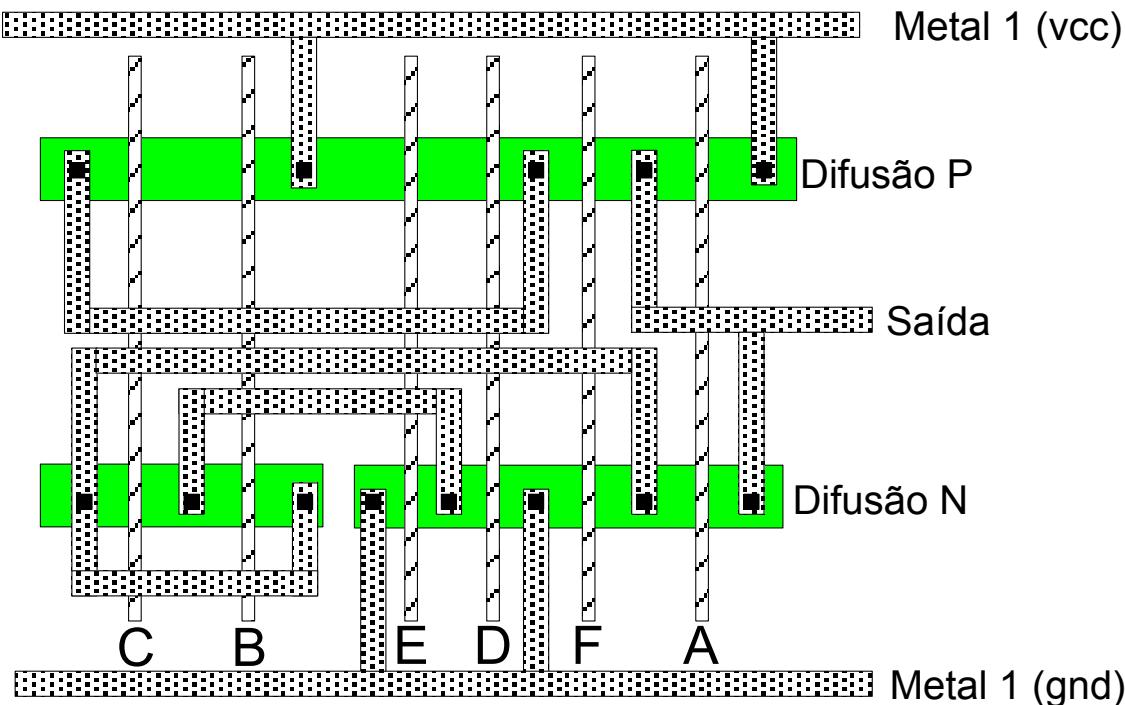
$$F_4 = \overline{a \cdot (b + (c \cdot d) + (e \cdot f))}$$

Exemplo de diagrama stick com quebra de difusão

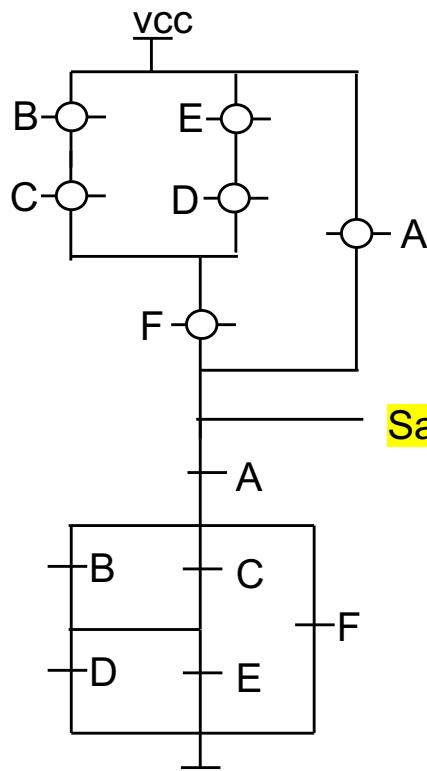
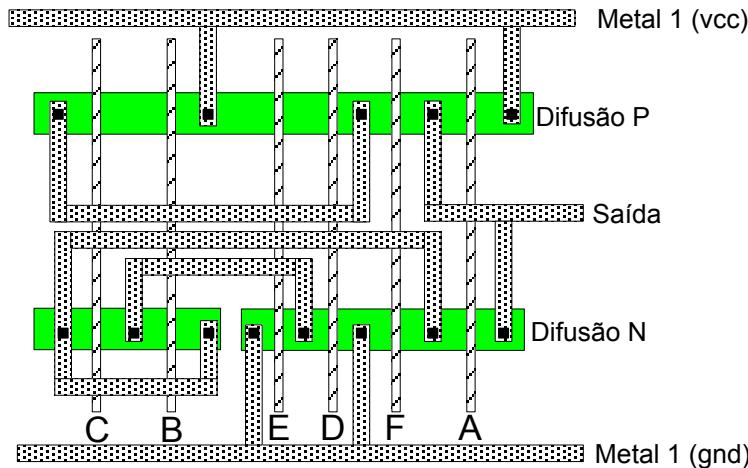


Exercício 4/8

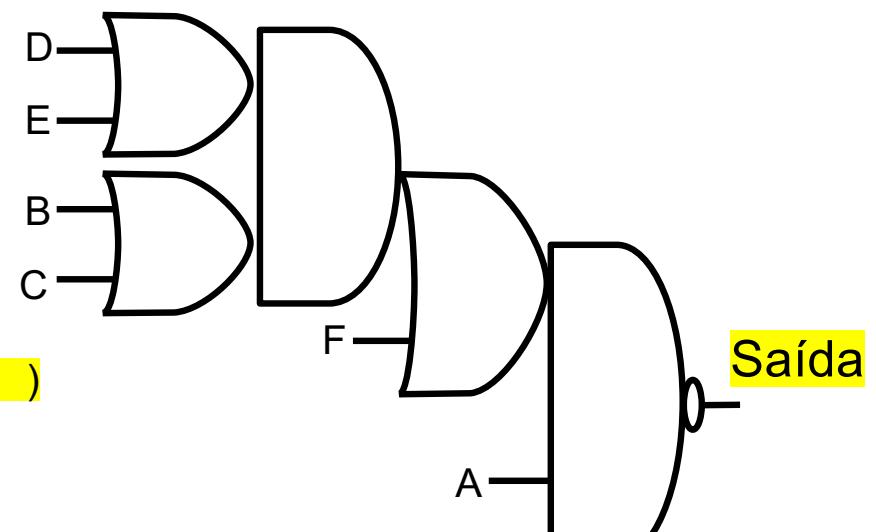
1. Número de transistores total, número de transistores N, número de transistores P
2. Diagrama de transistores
3. Diagrama lógico
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5. Se esta mesma função fosse implementada com portas simples (*nand*, *nor*, *inversor*) quantos transistores seriam necessários? Justifique.



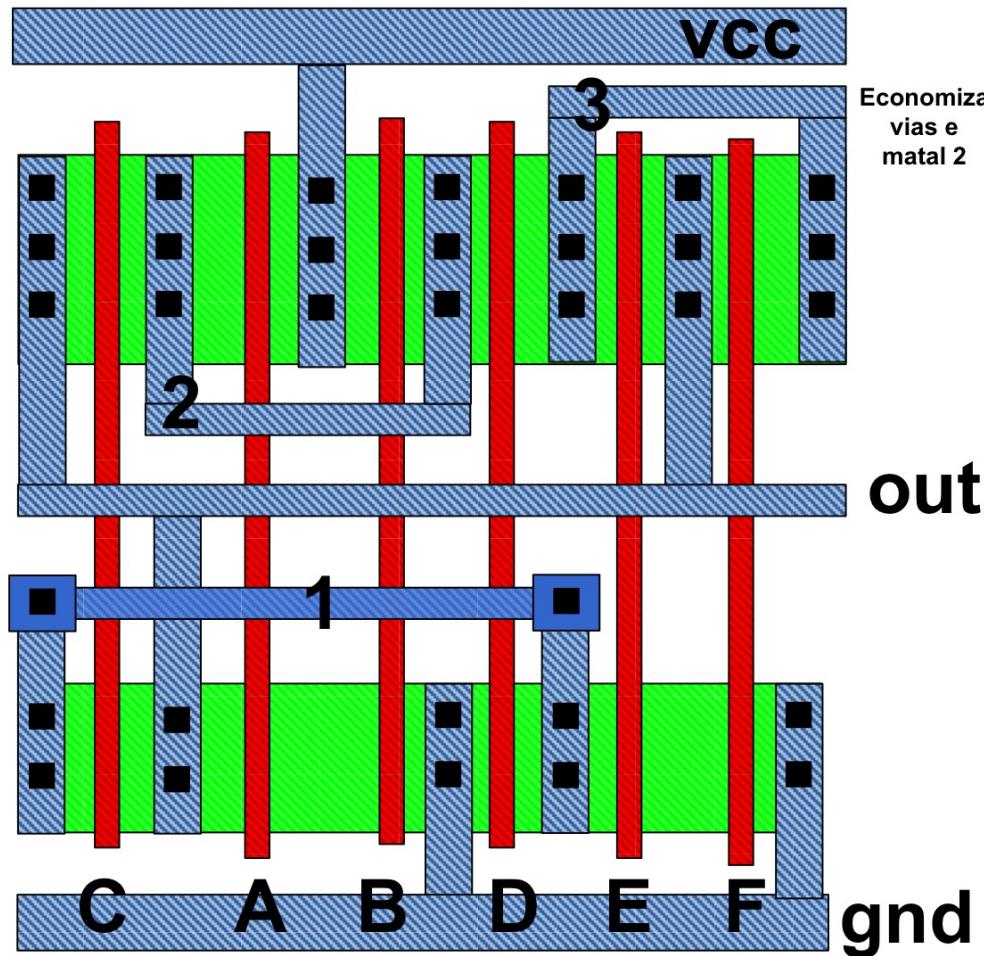
Exercício 4/8 - solução



$$\text{Saída} = \text{not}(((D+E).(B+C)) + F) . A$$



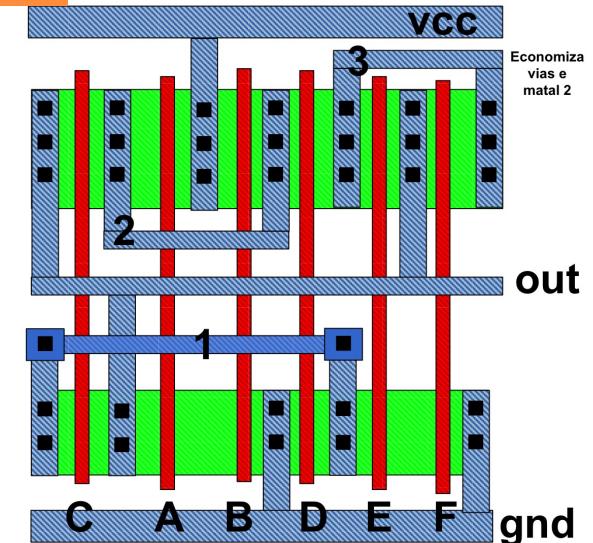
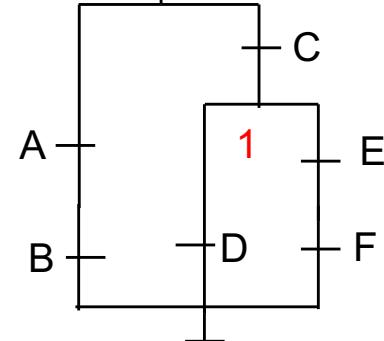
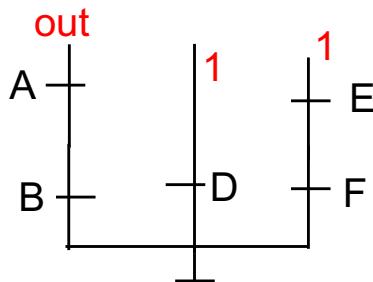
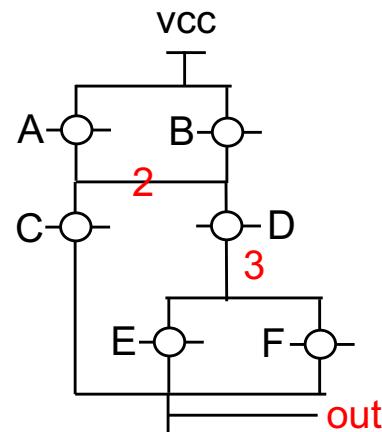
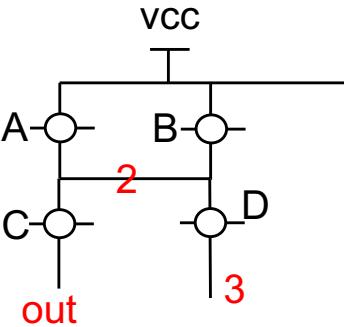
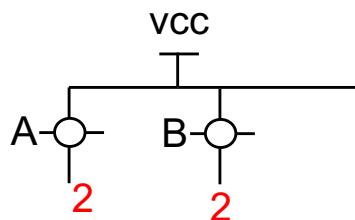
Exercício 5/8



Pede-se:

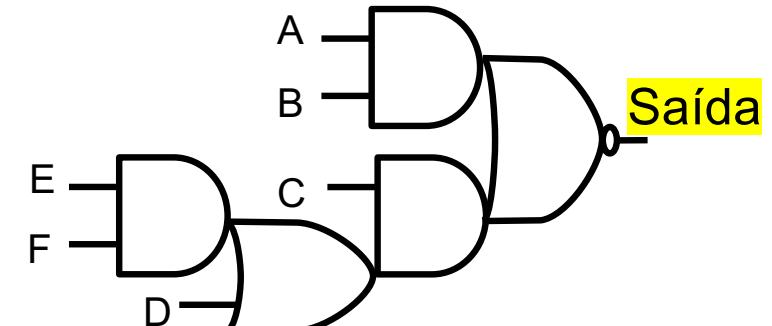
- Identifique no layout acima em um transistor qualquer os parâmetros W e o L.
- Desenhe o diagrama de transistores (N e P) desta porta lógica
- Qual é a função lógica desta porta? (no formato $F = \overline{((a.b + c.d) . (e.f + g.(h + i)))}$)

Exercício 5/8 - solução



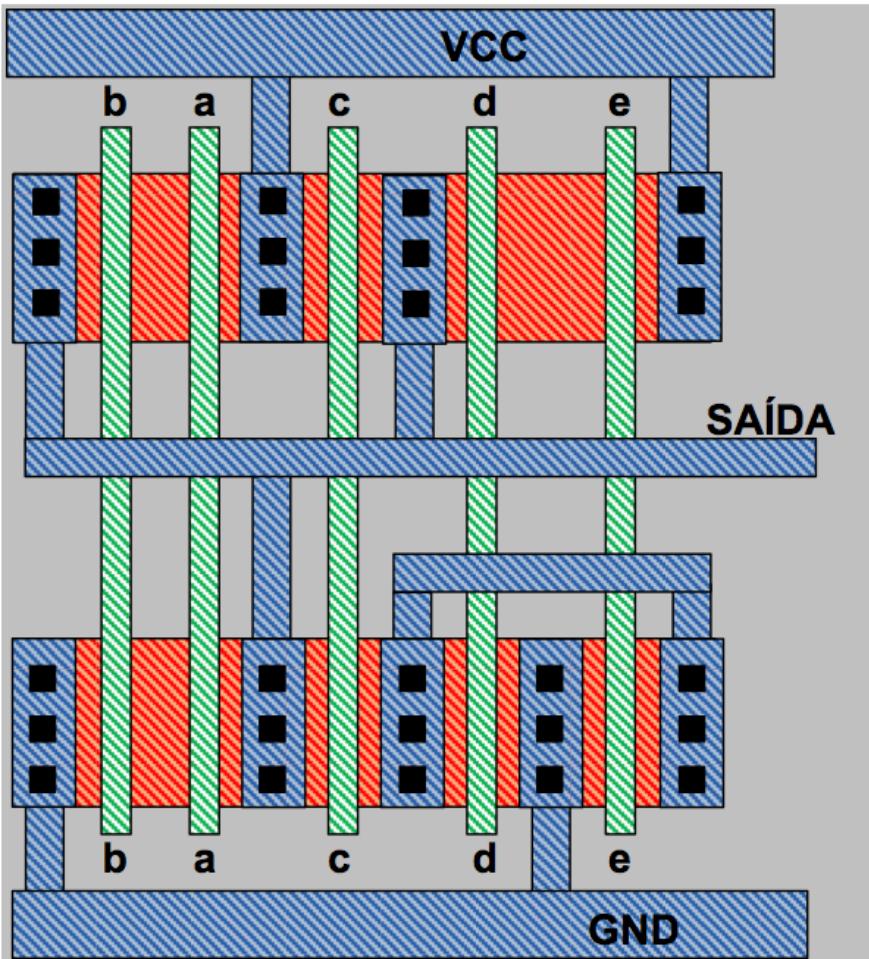
Pede-se:

- Identifique no layout acima em um transistor qualquer os parâmetros W e o L.
- Desenhe o diagrama de transistores (N e P) desta porta lógica
- Qual é a função lógica desta porta? (no formato $F = \overline{((a.b + c.d) . (e.f + g.(h+i)))}$)

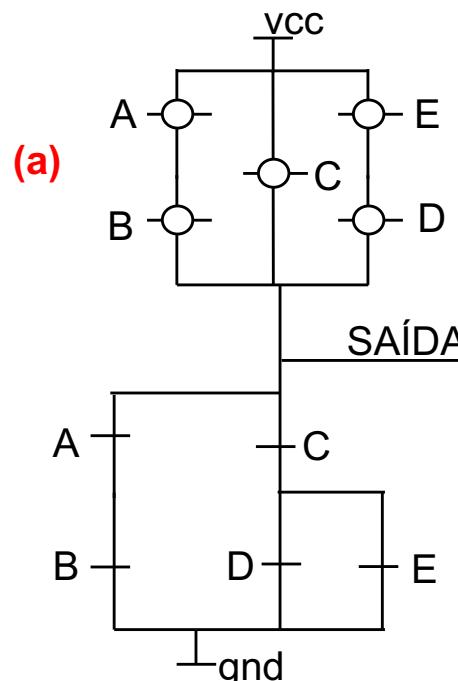


Exercício 6/8

Considere o layout abaixo:



- Determine o diagrama de transistores desta porta lógica (fazer desenho comprehensível)
- Para o vetor de entrada $ABCDE = \{11011\}$ determine o valor lógico da saída.
- Esta porta lógica está corretamente projetada? Tanto em caso afirmativo como negativo, justificar a resposta.



(b) Curto-circuito

(c) Não está corretamente projetada pois não respeita o princípio da dualidade

Exercício 7/8

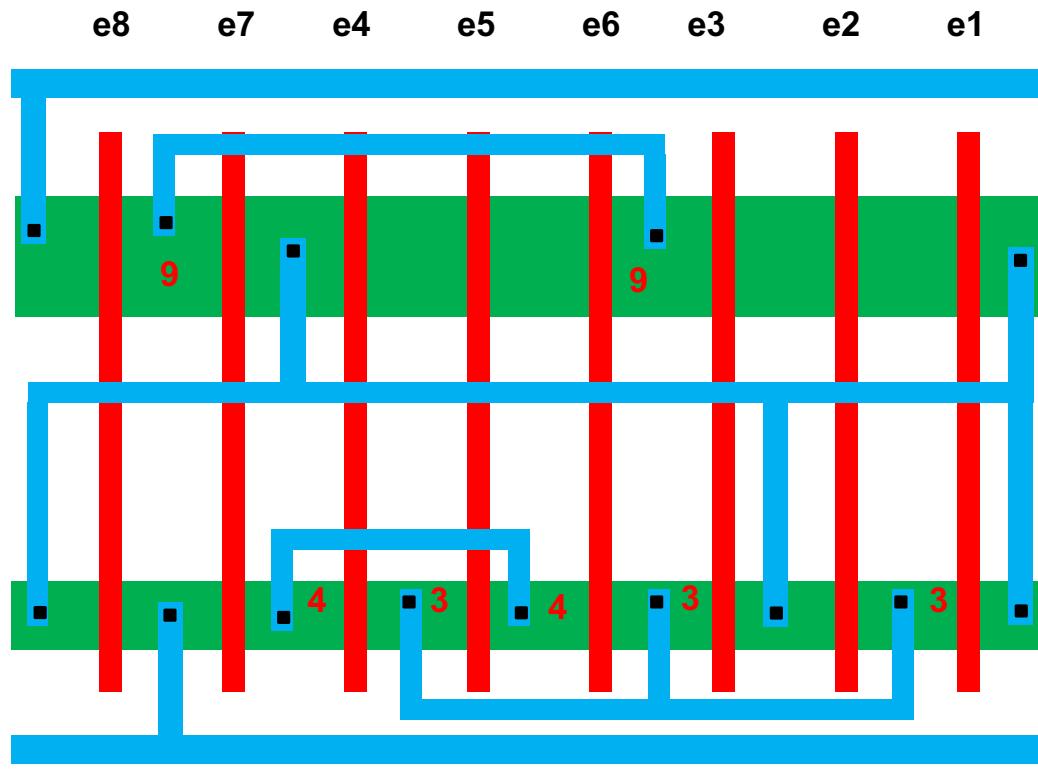
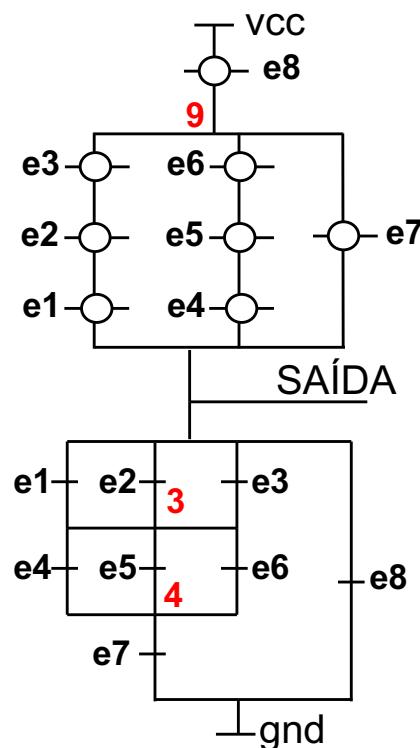
Considere o netlist spice abaixo :

MN1	out	e1	3	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN2	out	e2	3	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN3	out	e3	3	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN4	3	e4	4	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN5	3	e5	4	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN6	3	e6	4	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN7	4	e7	<u>gnd</u>	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN8	out	e8	<u>gnd</u>	<u>gnd</u>	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP9	out	e1	5	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP10	5	e2	6	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP11	6	e3	9	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP12	out	e4	7	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP13	7	e5	8	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP14	8	e6	9	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP15	out	e7	9	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP16	9	e8	<u>vcc</u>	<u>vcc</u>	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U

- Diagrama de transistores (compreensível)
- Diagrama lógico
- Número de transistores total, número máximo de transistores em série no plano N, e número máximo de transistores em série no plano P.
- Desenhar o diagrama stick da célula.
- Se esta mesma função fosse implementada com portas simples (*nand*, *nor*, *inversor*) quantos transistores seriam necessários? Justifique.

Exercício 7/8 - solução

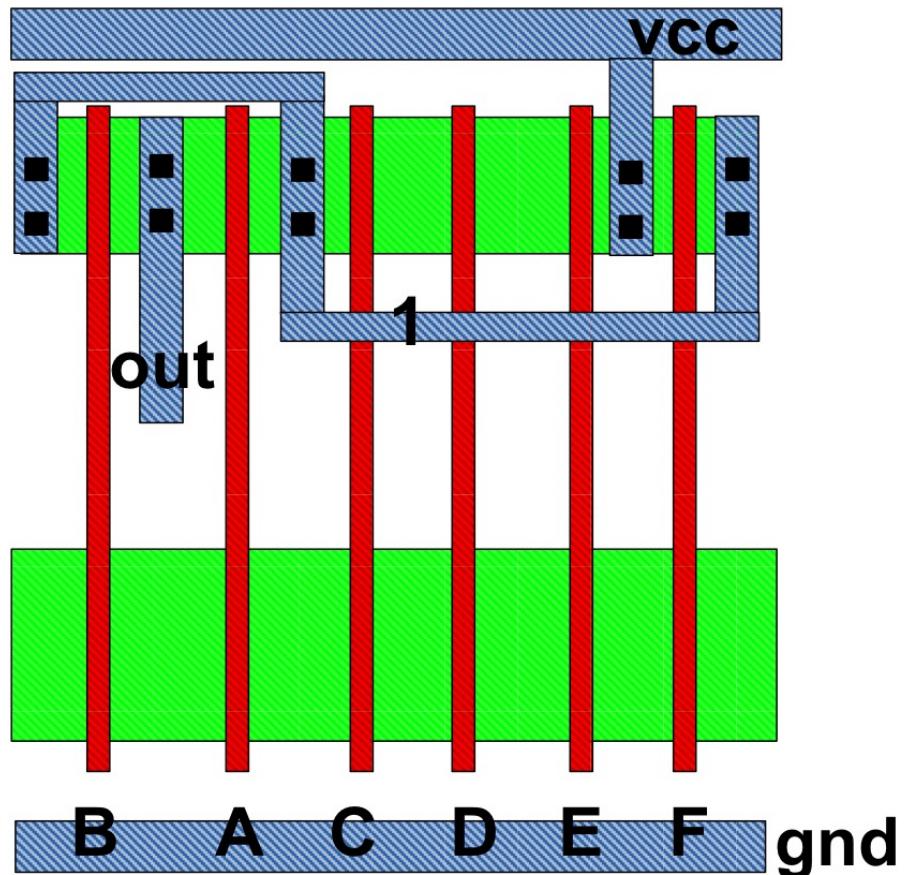
MN1	out	e1	3	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN2	out	e2	3	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN3	out	e3	3	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN4	3	e4	4	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN5	3	e5	4	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN6	3	e6	4	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN7	4	e7	gnd	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MN8	out	e8	gnd	gnd	NMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP9	out	e1	5	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP10	5	e2	6	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP11	6	e3	9	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP12	out	e4	7	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP13	7	e5	8	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP14	8	e6	9	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP15	out	e7	9	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U
MP16	9	e8	vcc	vcc	PMOS	L=0.8U W=8U AD=17.6P AS=17.6P PD=20.4U PS=20.4U



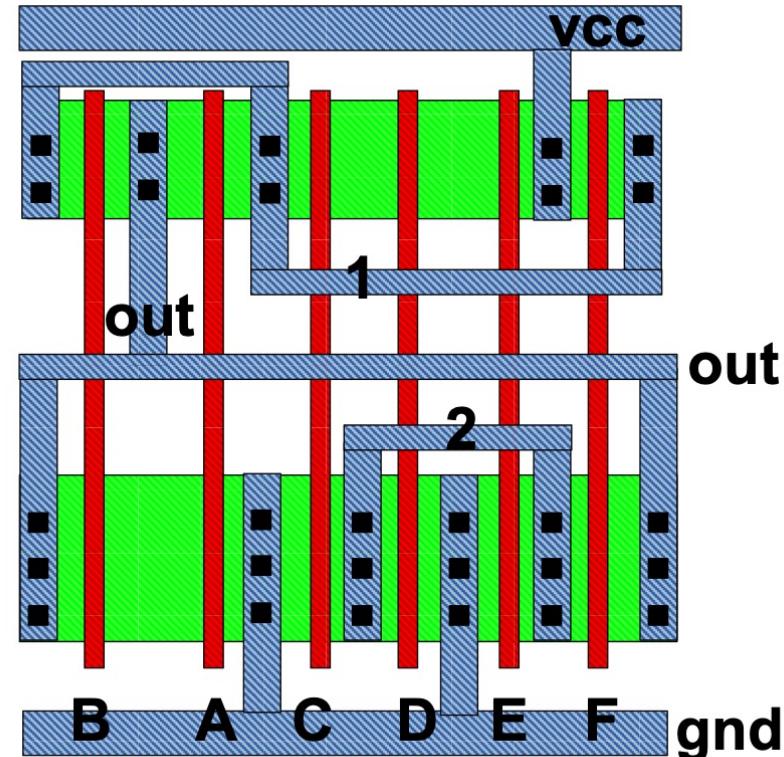
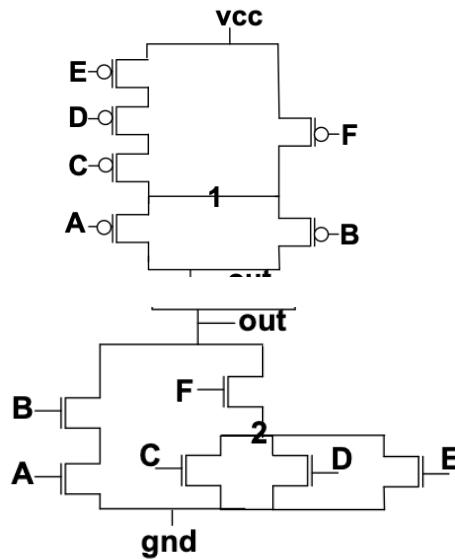
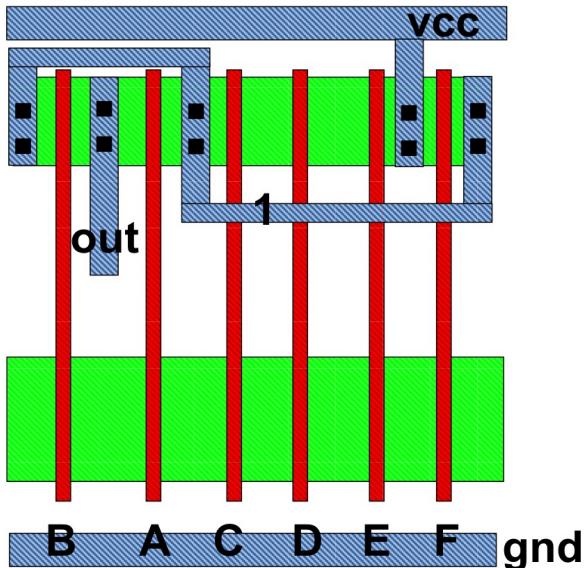
Exercício 8/8

Complete o plano N do layout abaixo

- Determine o diagrama de transistores P
- Fazer o diagrama dos transistores N
- Completar o layout

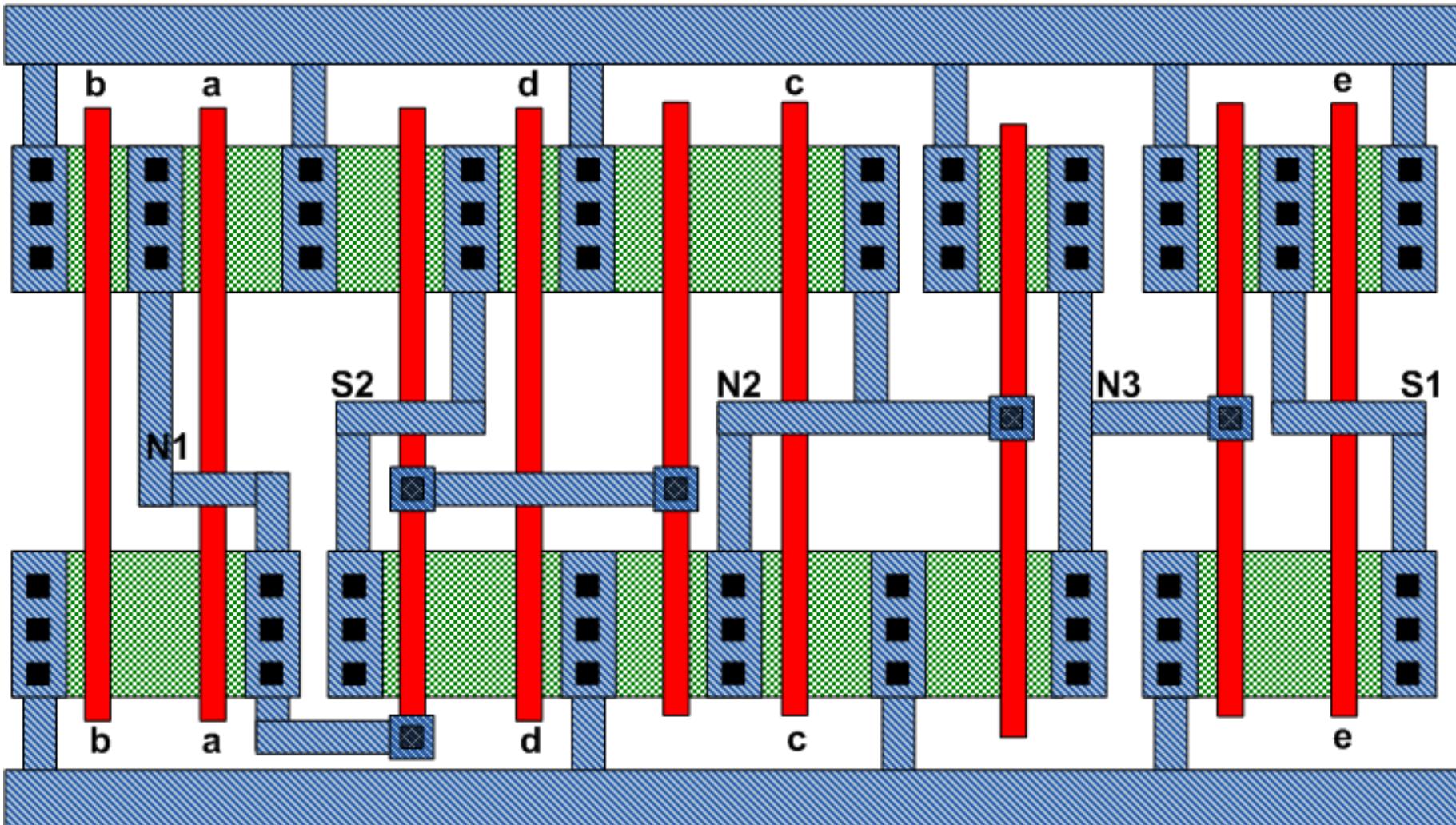


Exercício 8/8 - solução

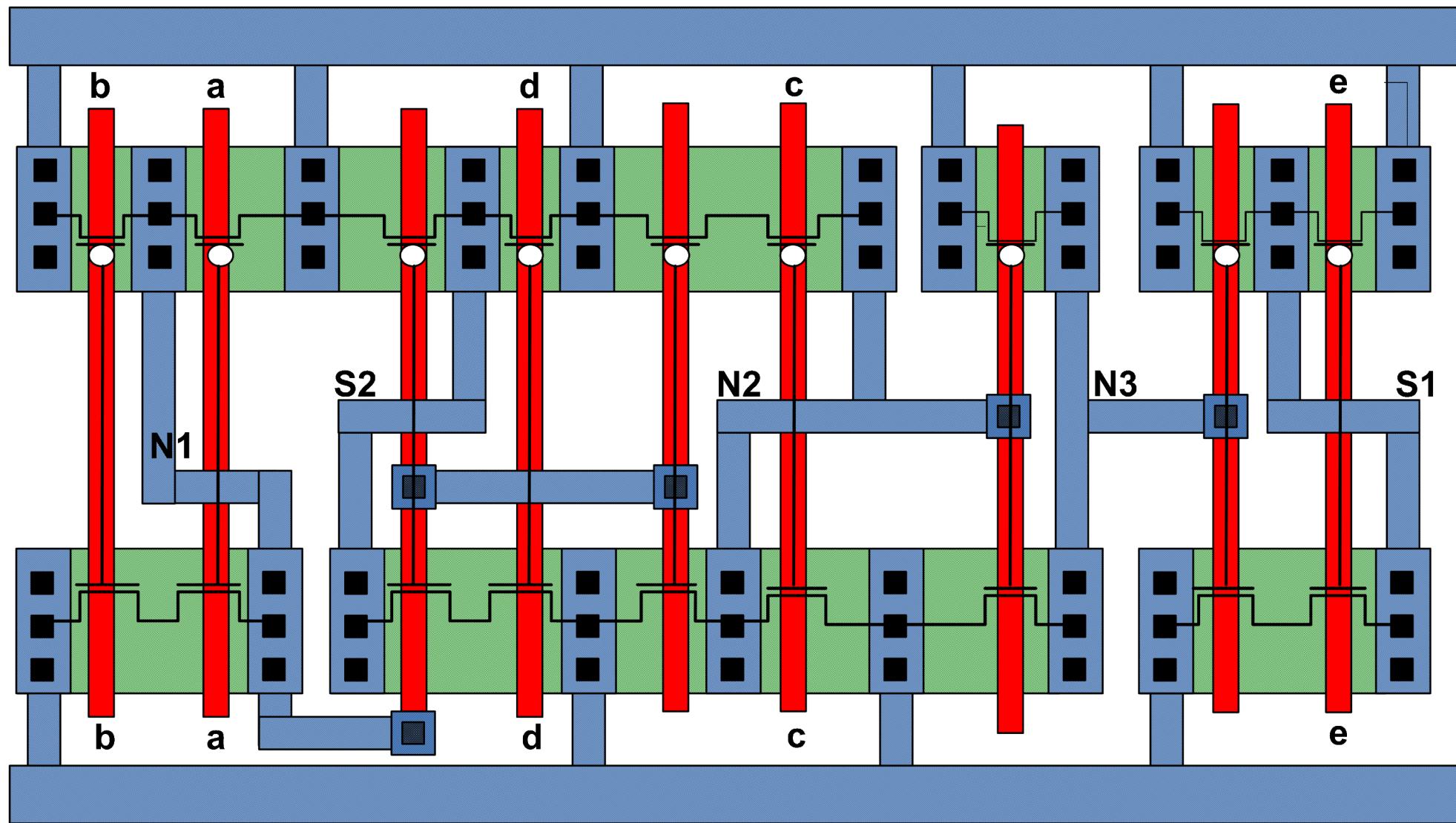


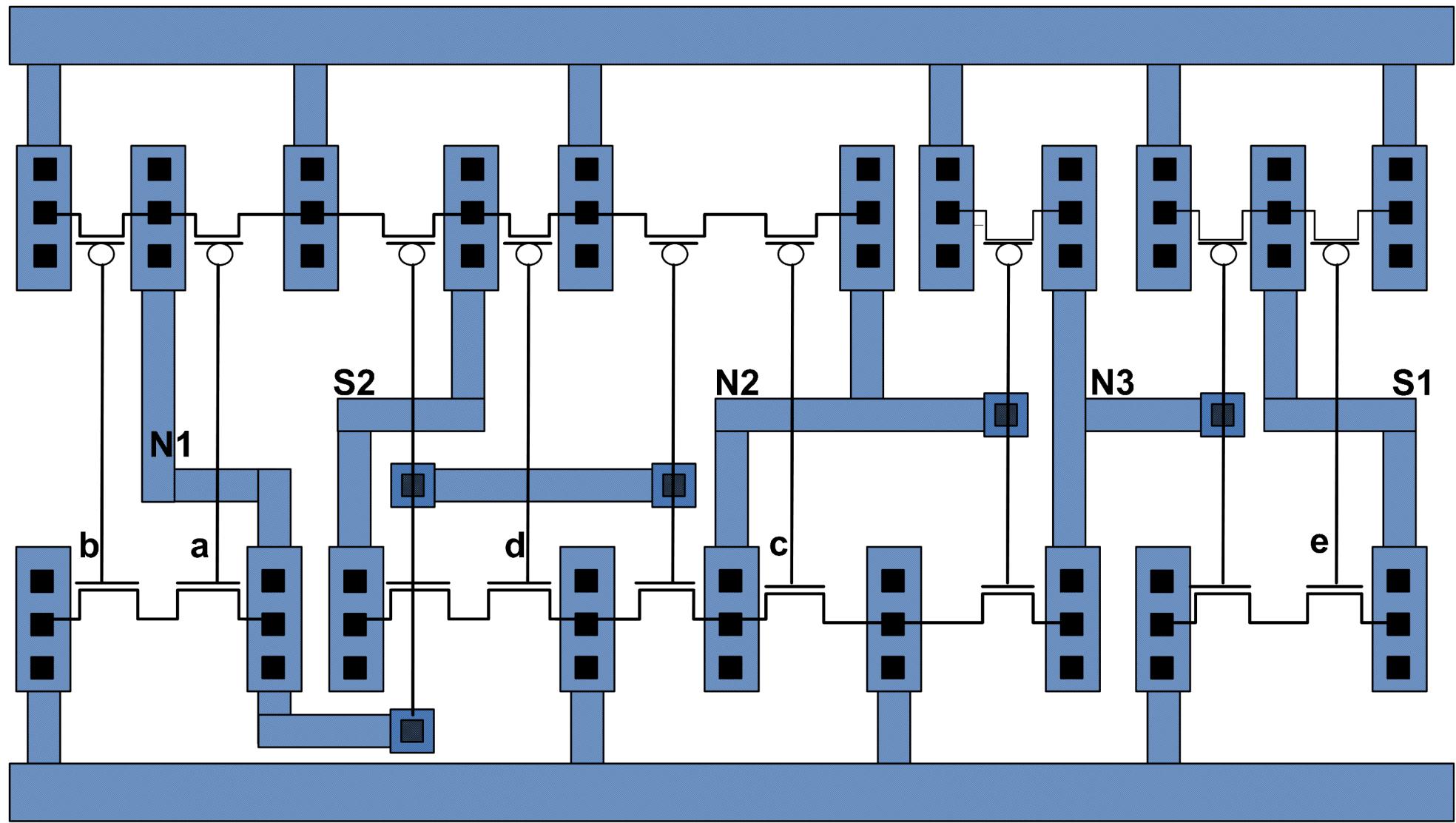
Múltiplas portas lógicas

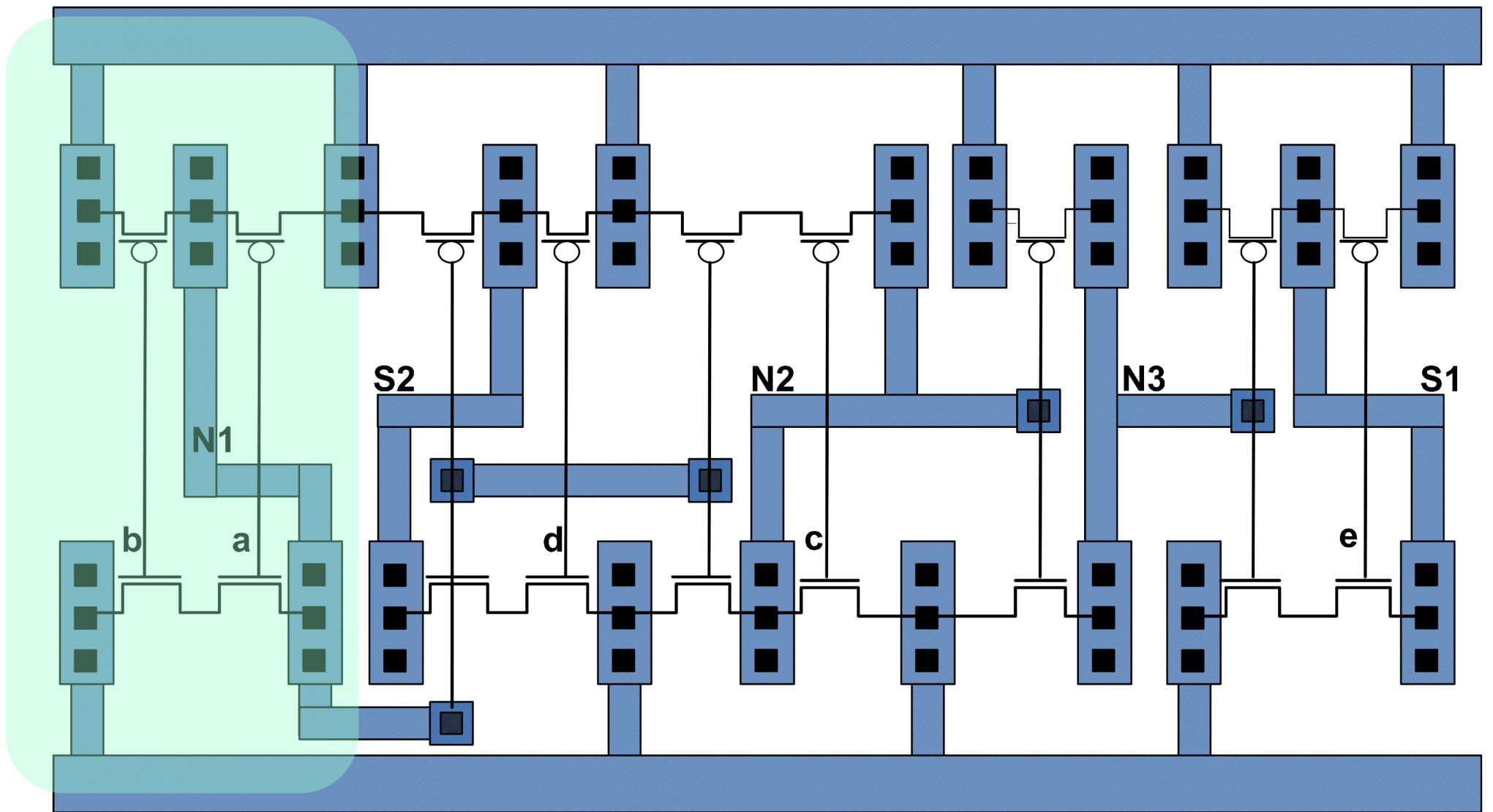
1. Faça o diagrama de portas lógicas do layout abaixo. Para cada porta lógica, indicar as entradas e saídas com o *labels* do layout ($a, b, c, d, e, N1, N2, N3, S1, S2\}$).



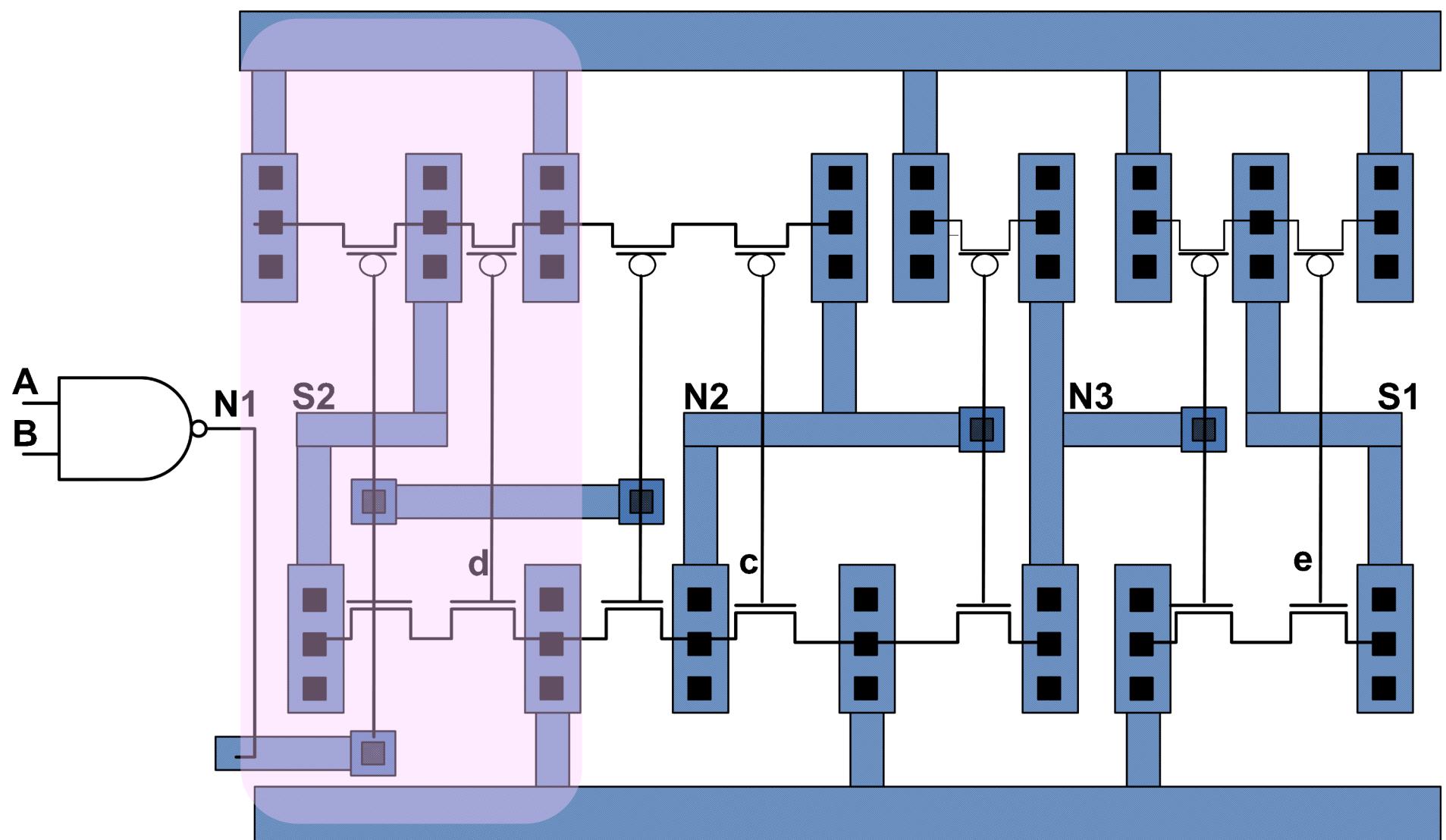
Este circuito contém 18 transistores



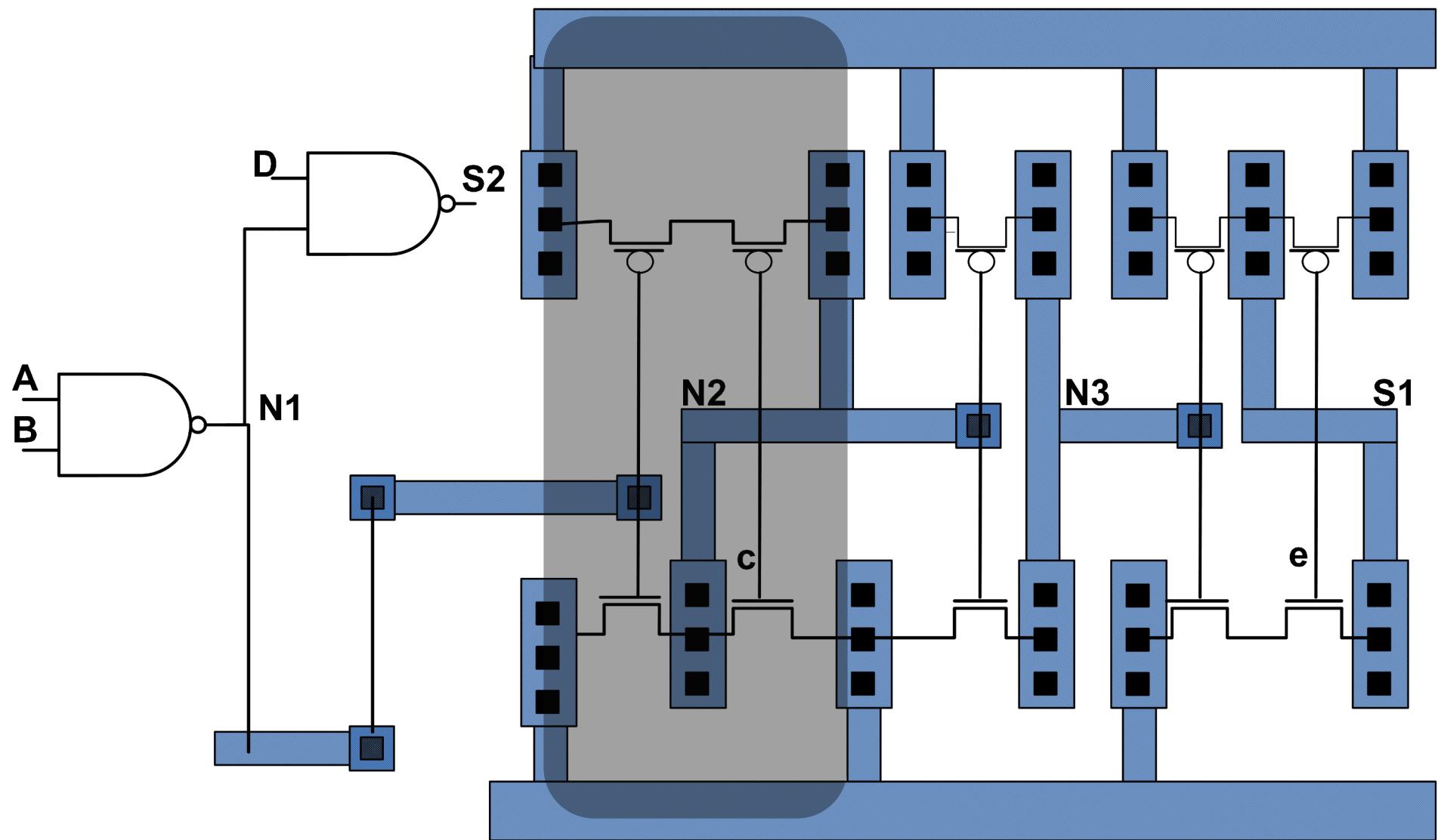




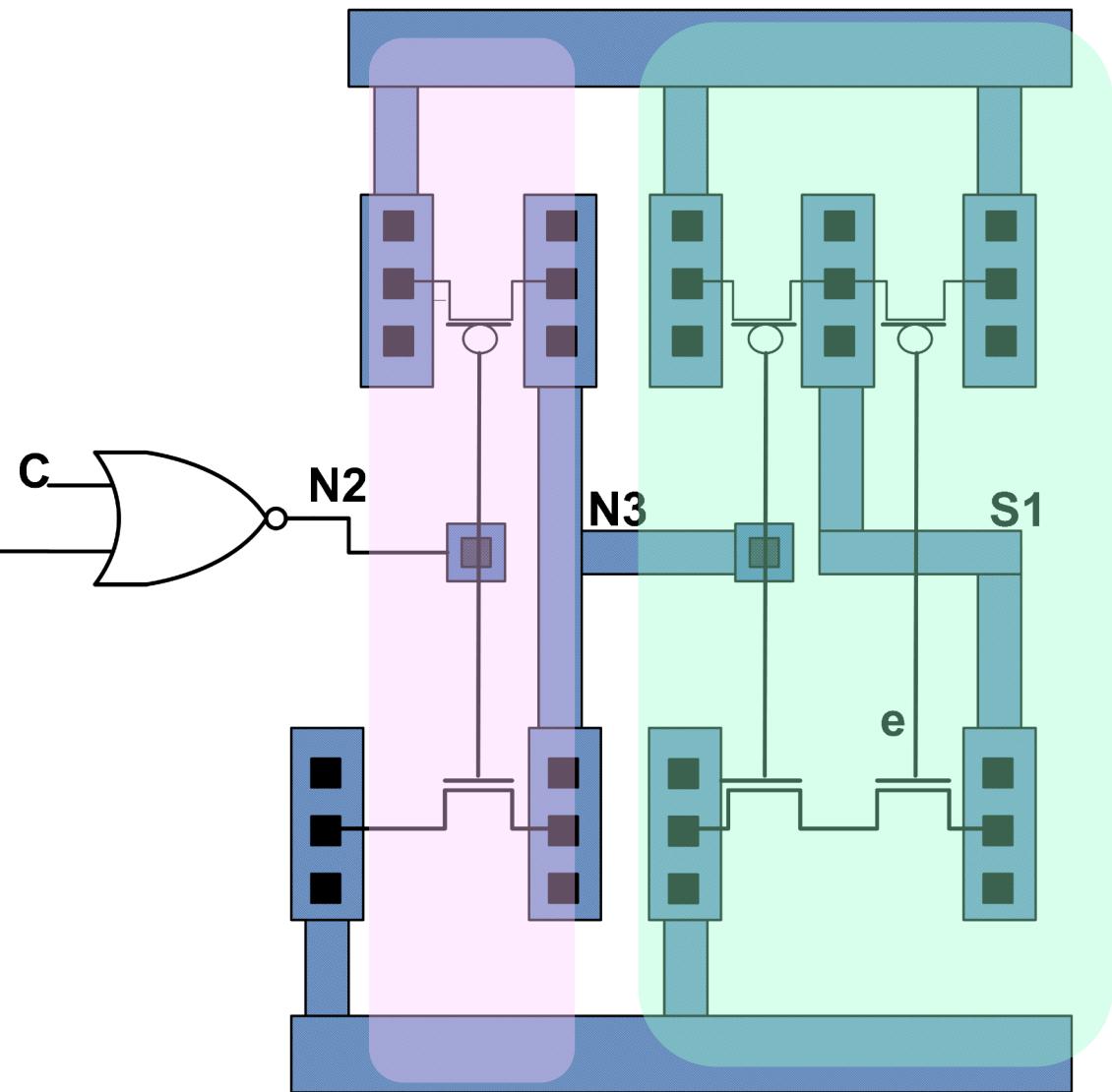
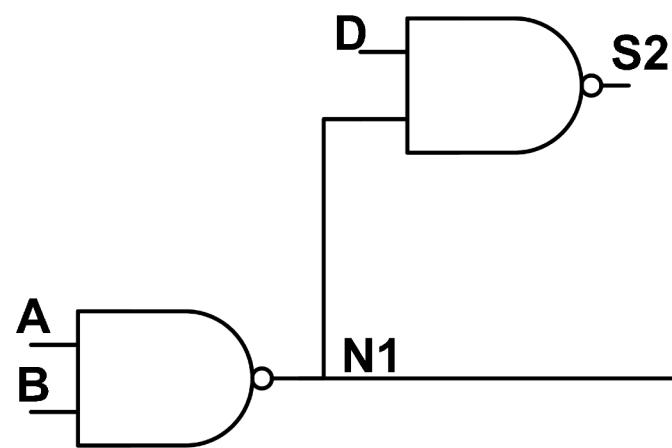
NAND 2



NAND 2

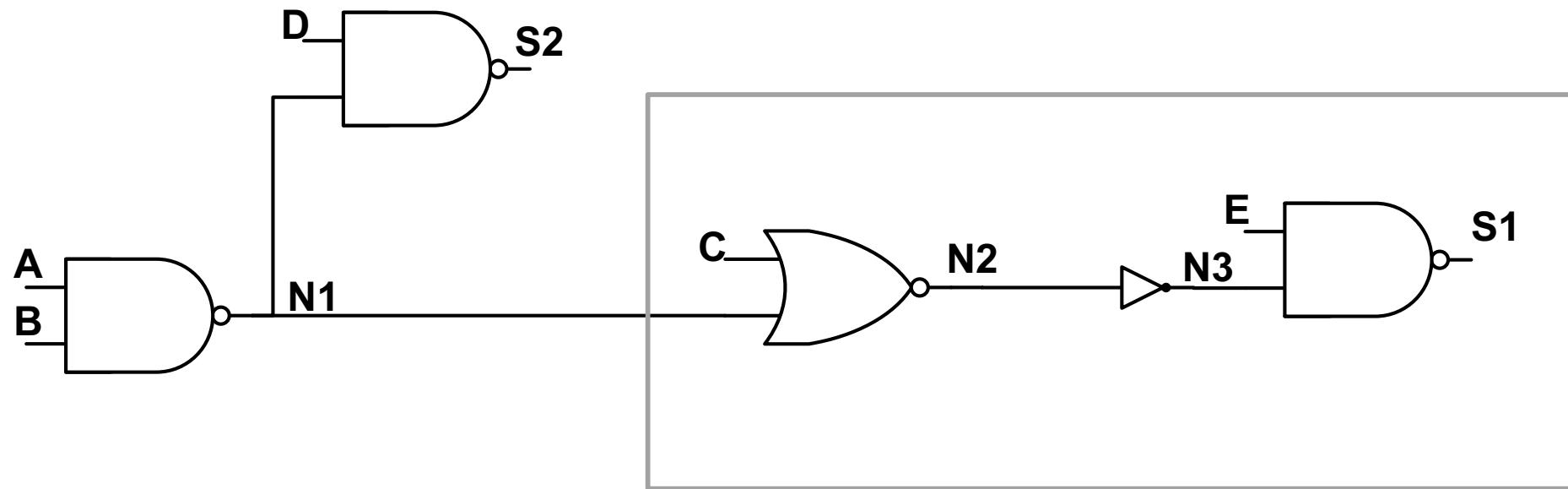


NOR 2



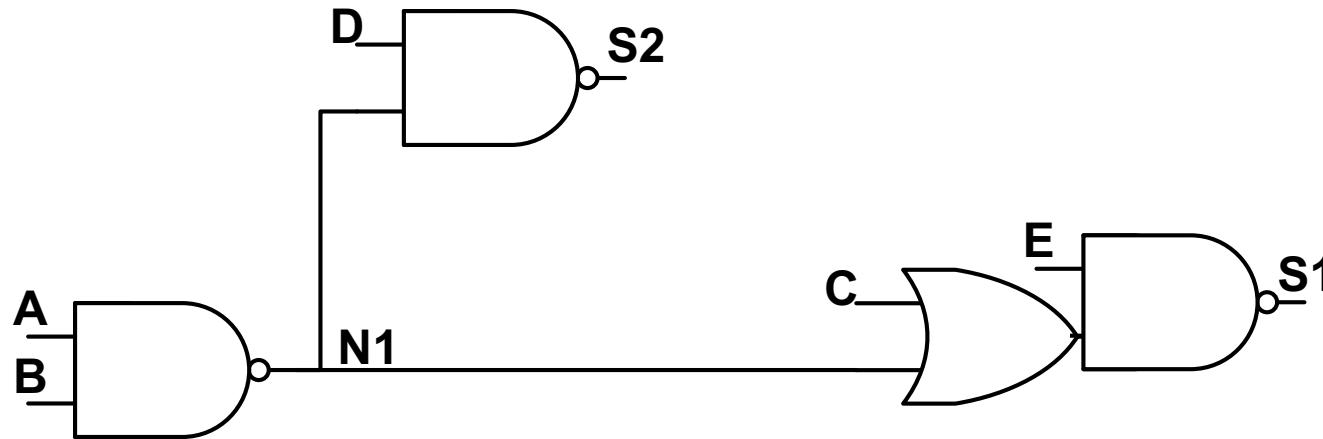
inversor

NAND 2

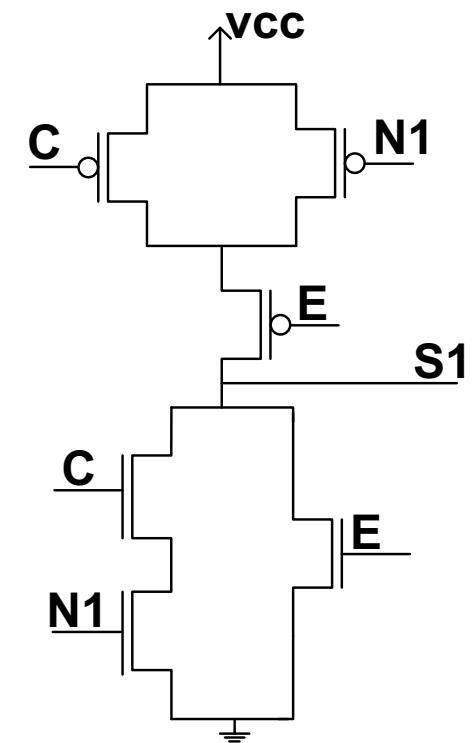
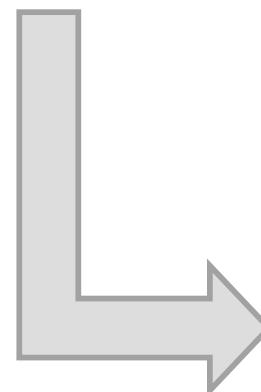


*Esta parte do circuito pode virar
uma porta complexa*

Novo circuito com porta complexa:



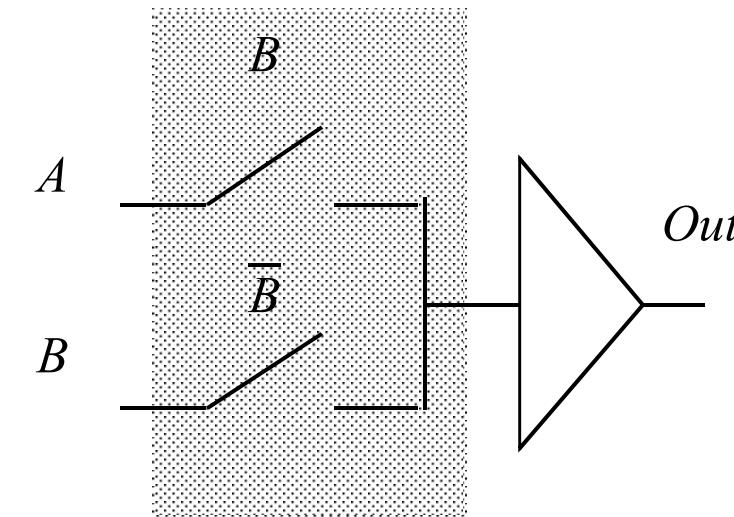
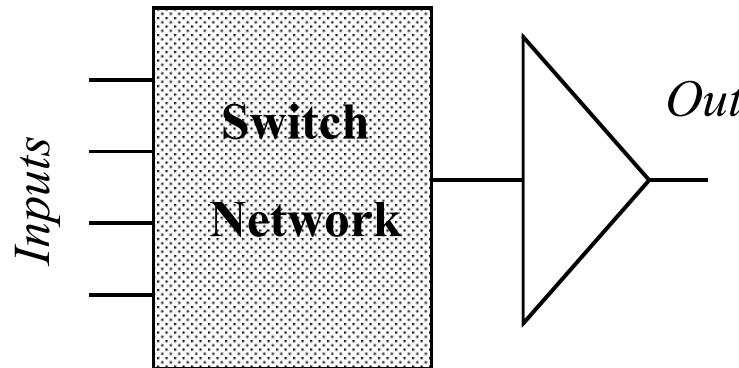
De 18 transistores passamos para 14 transistores



Lógica com transistores

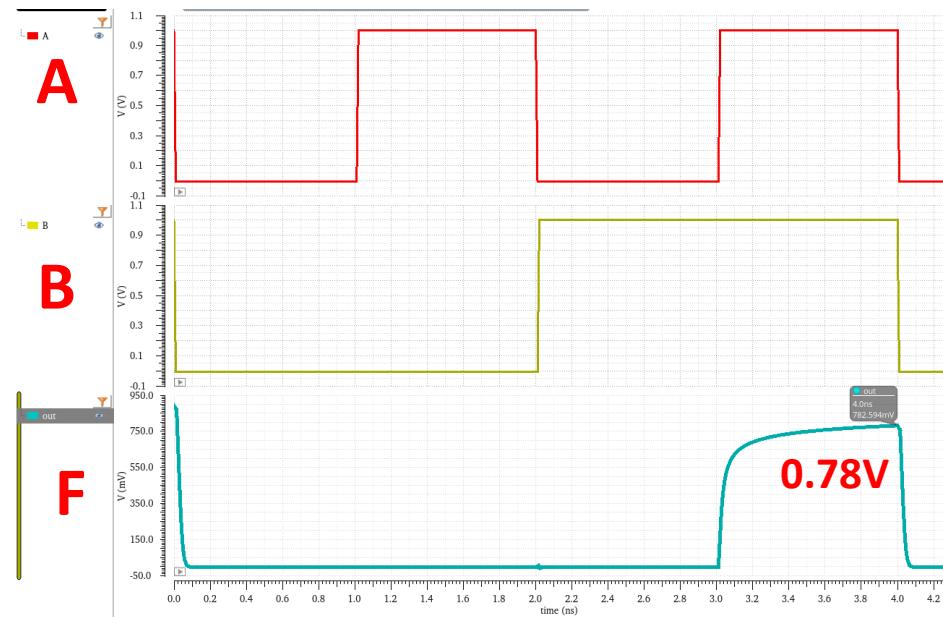
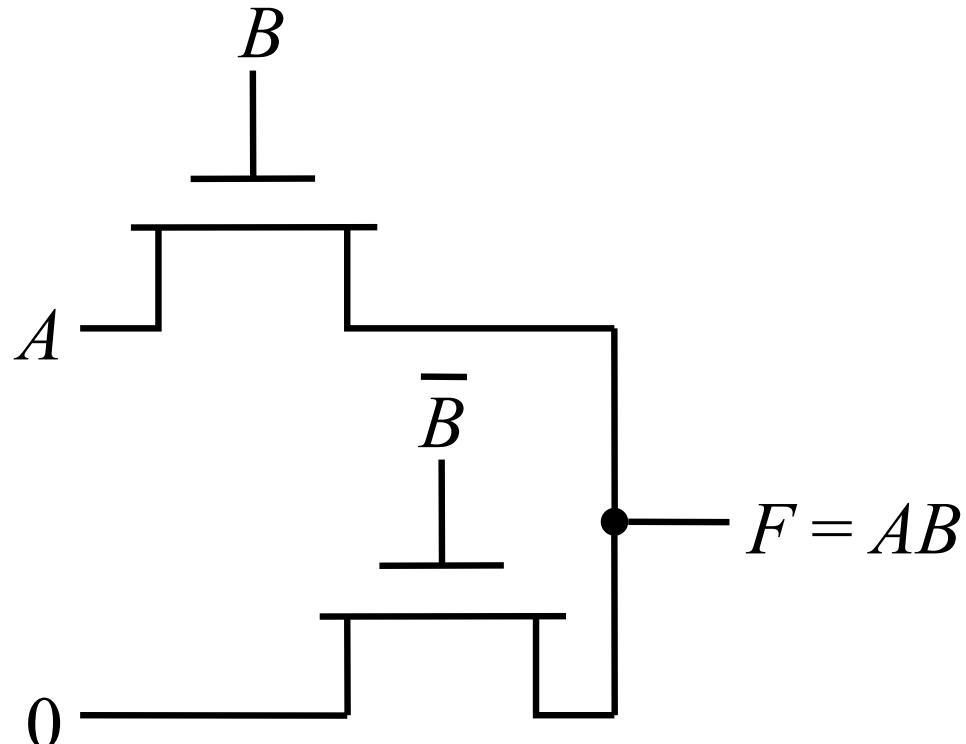
Pass-transistor

Pass-Transistor Logic



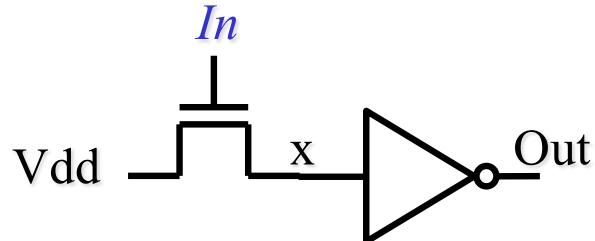
- N transistores, ao invés de $2N$ como nas portas complementares
- Não há consumo estático, devido à isolação dos gates

Example: AND Gate

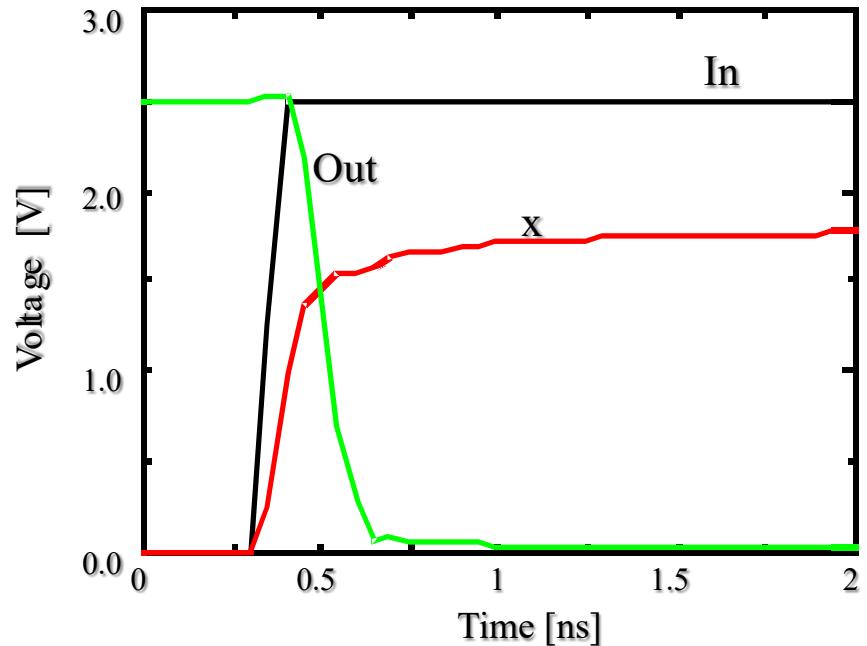


Transistor N: passa bem o zero lógico

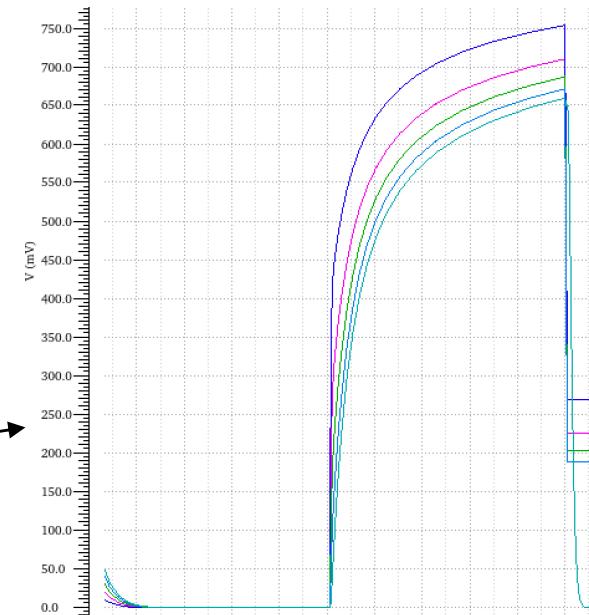
NMOS-Only Logic



Out (curva verde): regenera o valor de x



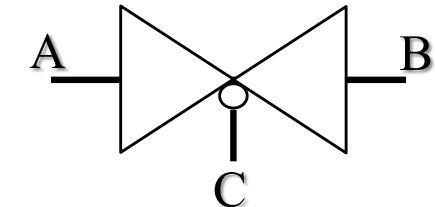
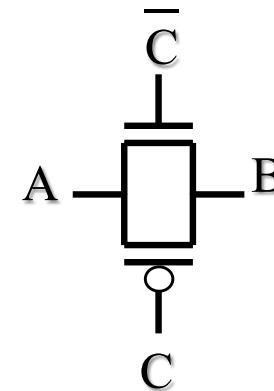
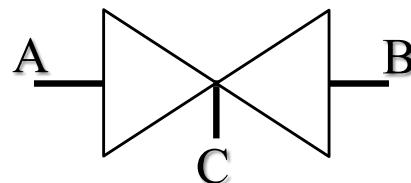
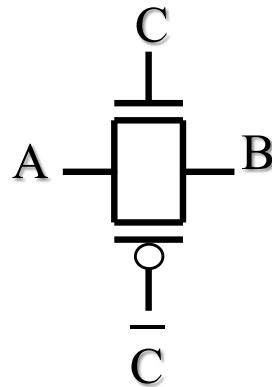
- Problema: o transistor N não passa bem o nível 1
 - Lembrando: se a entrada for '1' e o sinal In também for '1' temos $V_{gs}=0$, ou seja, não há condução – **olhar o sinal x**
 - Por esta razão o inverter: regenera o sinal x para gerar um sinal out que excursiona de 0 a vcc
- O segundo problema é que vários transistores em série também degradam o sinal em x



Transmission Gate

Solução:

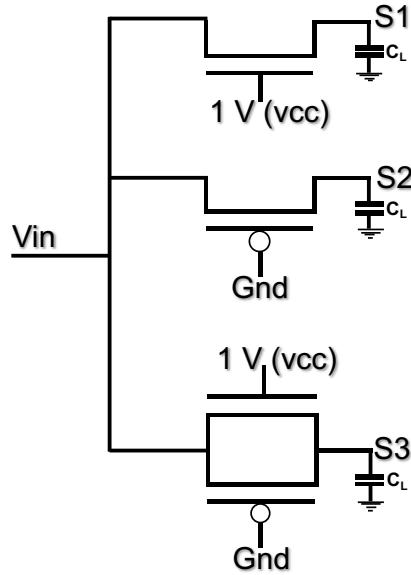
- Um transistor N em paralelo com o transistor P
- Passa corretamente os níveis '0' e '1'



$B = A$ quando **$C=1$**

$B = A$ quando **$C=0$**

Caminho de baixa impedância
(direção da corrente depende do *driver*)



V_{in}

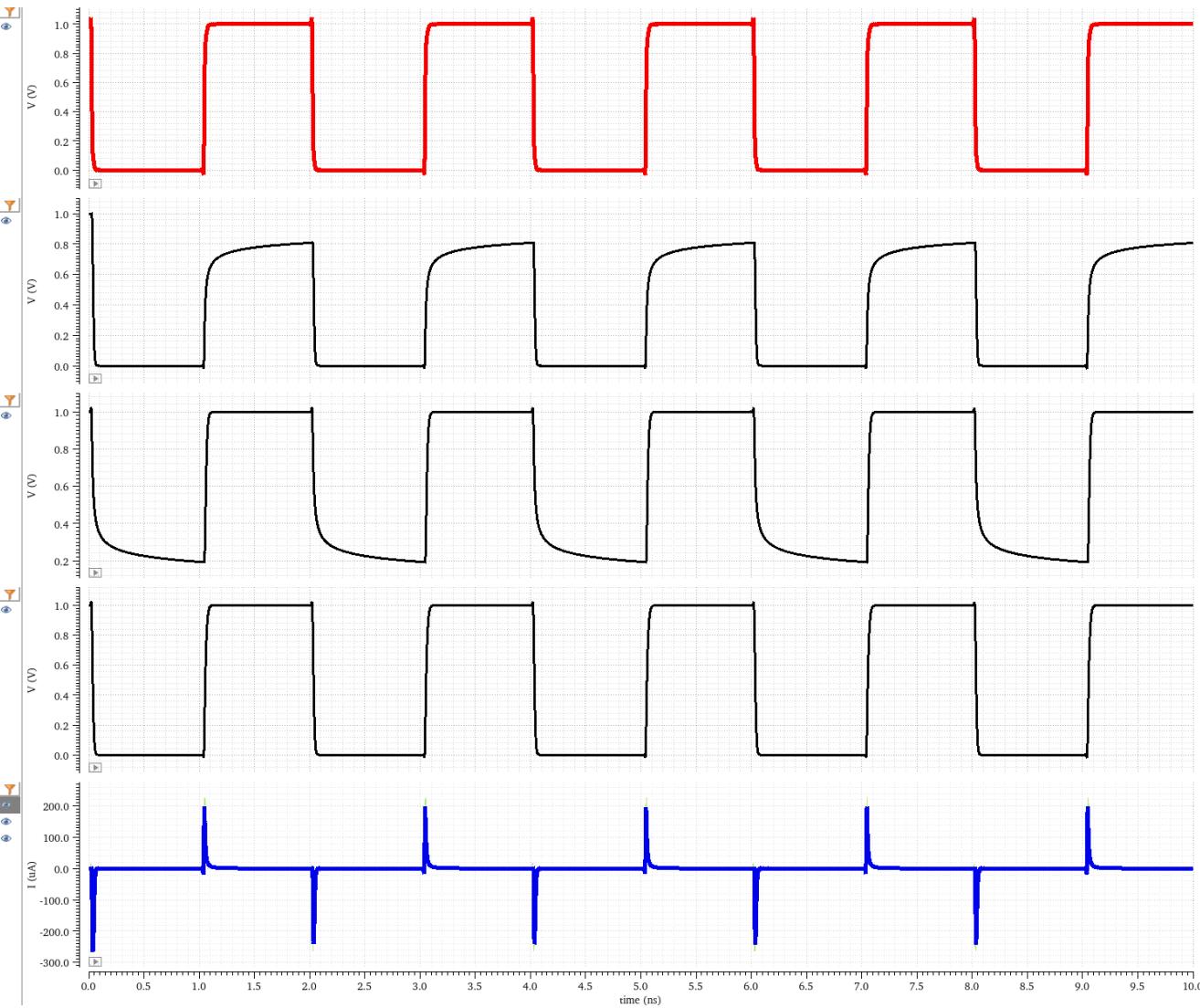
N: '1' ruim

S₂

P: '0' ruim

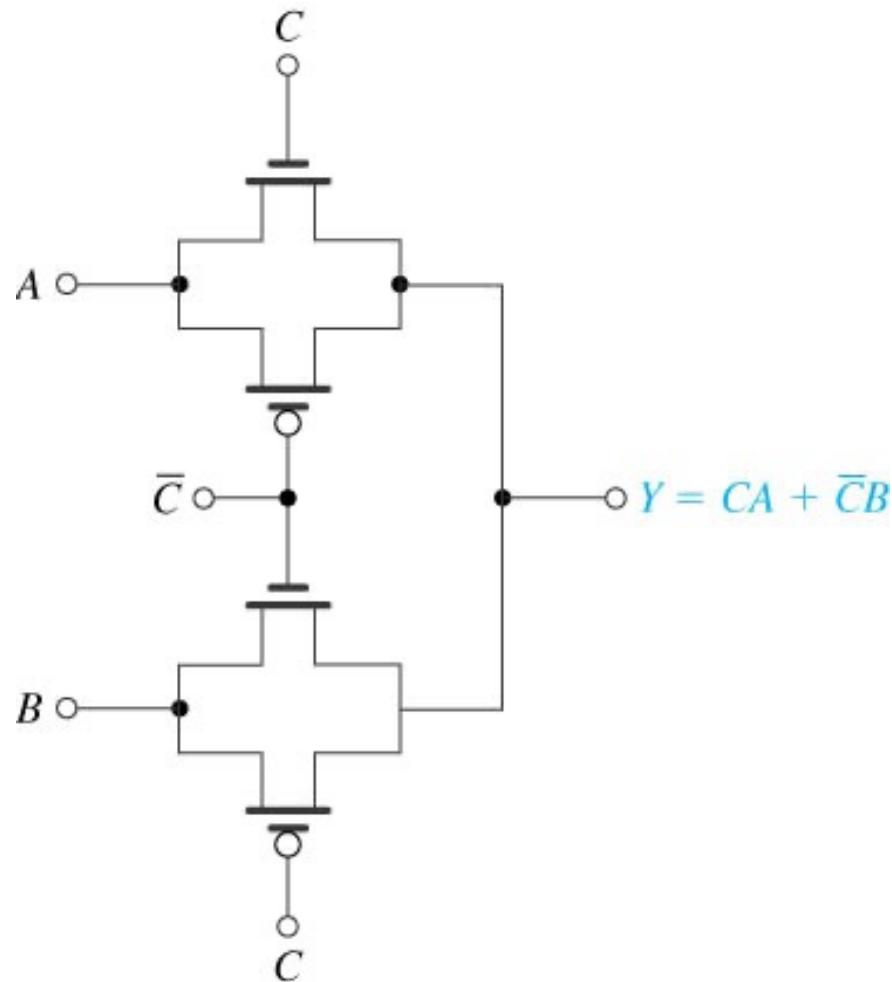
TG: 2 níveis OK S₃

corrente

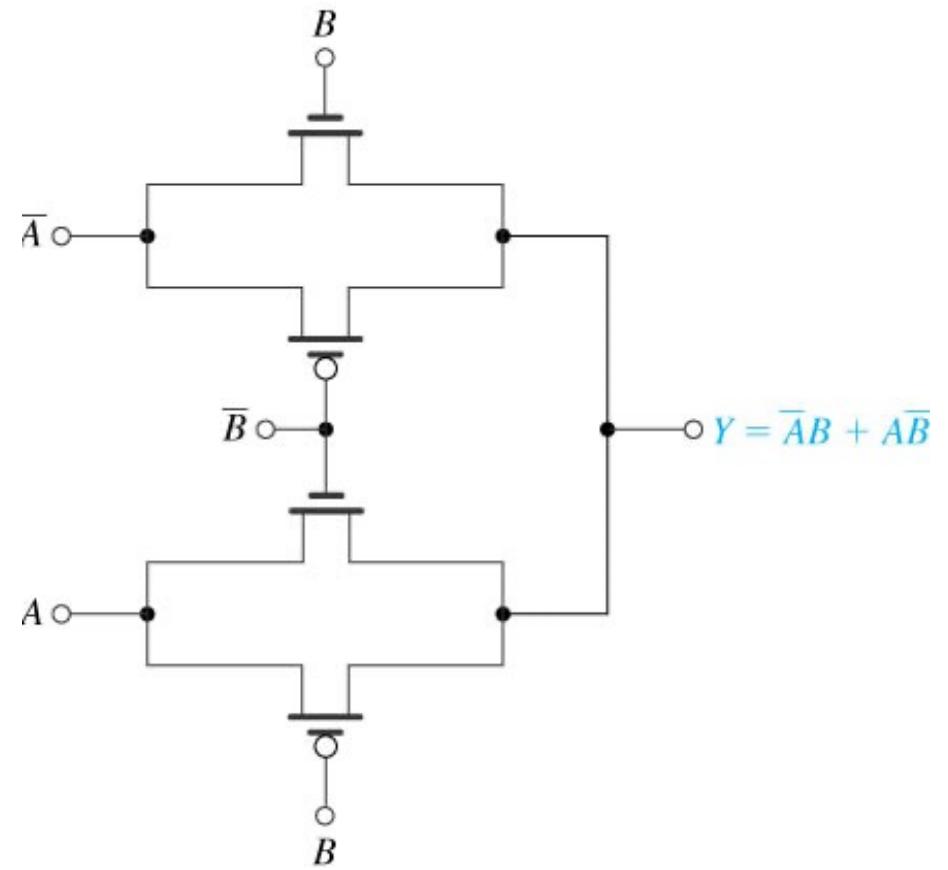


Pass-Transistor Logic

- Multiplexador 2 x 1



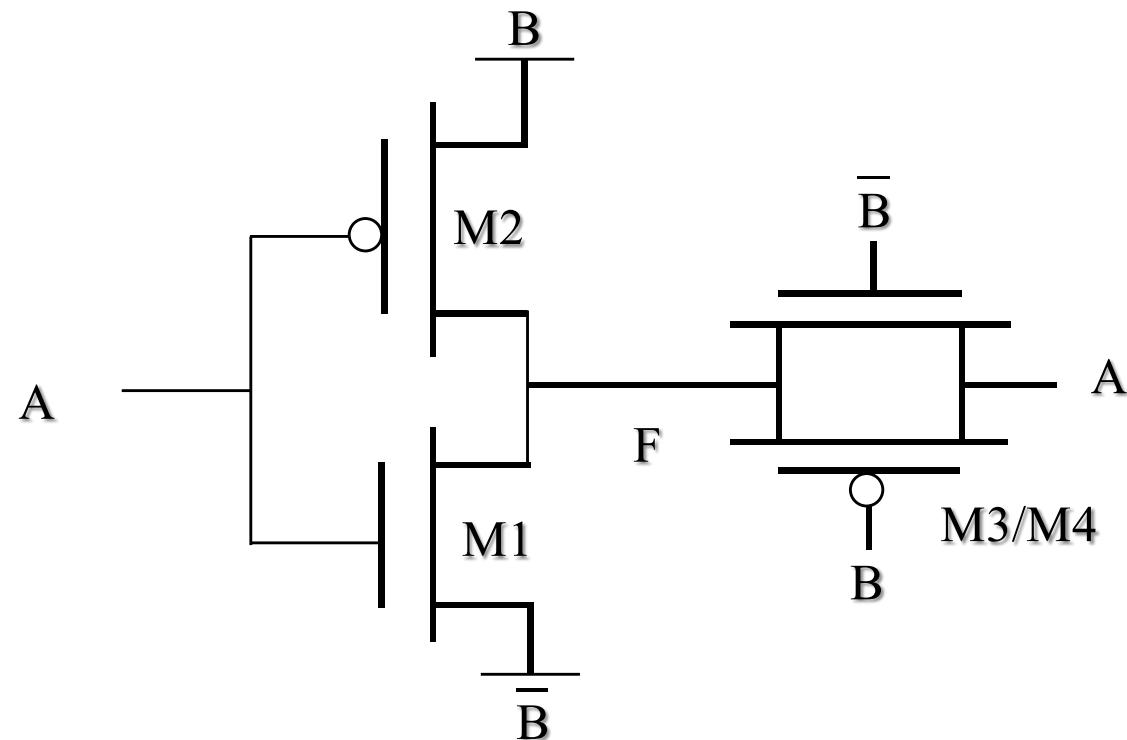
- Xor



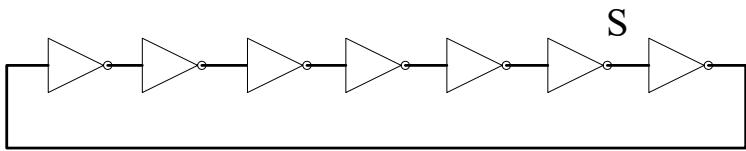
Transmission Gate XOR

- Exemplo de aplicação (2):
 - Porta xor, com um transmission gate e um inverter com a tensão de alimentação controlada pelo sinal B
 - Quando temos $B=0'$ o transmission gate deixa passar o A e temos na saída $F=A$
 - Quando temos $B=1'$ é o inverter que opera, fazendo: $F = \text{not } A$

B	A	F
0	0	0
0	1	1
1	0	1
1	1	0



6) A figura abaixo ilustra um oscilador em anel.



Pede-se:

- (a) Dado que $tr=1.0$ ns (tempo de propagação de subida de um inverter) e $tf=0.5$ ns (tempo de propagação de descida de um inverter), qual o período (unidade: ns) e a frequência (unidade: MHz) resultante no nodo S?
- (b) A figura abaixo ilustra a saída do oscilador. Determine os tempos t_A , t_B , t_C , t_D , mostrando como os mesmos foram obtidos. Como os tempos de subida e descida são diferentes, o duty cycle não é 50%.

