Exploring Soft Error Susceptibility in FET Devices via Geant4 Simulation

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***Abstract*—In recent years, there have been significant advancements in electronic device technology. However, these devices remain vulnerable to Single-Event Effects (SEEs), caused by the interaction of cosmic rays with sensitive regions, potentially leading to processing errors. Thus, it is interesting to investigate the correlation between cosmic ray events and the likelihood of processing errors, particularly concerning the interactions between specific particles and the sensitive areas of the devices. This work presents a study using the Geant4 tool to simulate the interaction of cosmic rays with FET devices and their potentially associated effects. Simulations involve hitting particles such as protons, alpha particles, positive and negative pions, as well as positive and negative muons. These are injected with energies ranging from 0.5 MeV to 100 TeV and at various angles of incidence. Simulations demonstrate that alpha particles generate the most electrons, which is especially relevant in outer space environments. Protons, which constitute the majority of cosmic rays, significantly affect SEEs not only in outer space and low Earth orbit but also at ground level. Although positive muons and pions have a lesser effect, they become prominent at lower altitudes, including at ground level. The angle of incidence is critical in evaluating SEEs, with planar technologies showing a higher occurrence of electron generation. In contrast, finFETs, although producing fewer electrons, exhibit a greater potential for generating bit flip currents.**

***Index Terms*—Soft Errors, Cosmic Rays, FET, finFET, Geant4.**

I. Introduction

Cosmic rays consist of high-energy particles, primarily protons, alpha particles, and heavy ions atomic nuclei [1], that continuously enter Earth's atmosphere. Upon entering the atmosphere, they interact with it, creating a cascade of many secondary particles such as muons, protons, neutrons, and pions, forming an extensive air shower [2]. These secondary particles interact with materials in the atmosphere and on Earth's surface. This interaction can have several consequences, including specific effects on electronic devices such as high electric charge doses [3] and atoms ionization [4].

The composition, energy, and quantity of secondary particles produced by cosmic ray interactions depend on factors such as the primary cosmic ray's energy, its composition, and the altitude of the interactions. Each level of the atmosphere is characterized by the following flux and particles [5]:

- Deep Space: in deep space, there can be up to $300,000\,particles/cm^2/h$, mainly protons (90%), with some alpha particles (9%) and heavy ions (1%);
- Geosynchronous Orbit: up to $500,000\,particles/cm^2/h$, mainly electrons and protons. However, as shown in [6], there are also pions and neutrons generated from the interaction of primary particles with the atmosphere;
- Low Earth Orbit: Up to $100,000\,particles/cm^2/h$, mainly electrons and protons. As in geosynchronous orbit, this region also contains pions, neutrons, and muons;
- Airplane Altitudes: there are about $6,000 - 9,000\,neutrons/cm^2/h$ and muons present;
- Ground Level: the flux is about $10-15\,neutrons/cm^2/h$, and approximately $60\,muons/cm^2/h$ and neutrinos.

Several works have explored the impact of radiation-induced errors in electronic devices, ranging from cryptography hardware implementations on SRAM-based FPGAs [7, 8] to the execution of modern machine learning algorithms [9]–[11]. For instance, Zhang and Li [12] suggest that smaller devices or those operating under reduced voltage supplies are more susceptible to radiation-induced errors.

To address this issue, it is crucial to examine key parameters influencing Single Event Effects (SEEs) and their manifestations. This paper *proposes* a simulation study using Geant4 [13]–[16] to model the impact of particles from cosmic cascades, such as protons, muons, pions, and alpha particles. The focus is on simulating the ionization process responsible for electron generation in structures like planar and finFET transistors. Simulation outcomes are validated through memory bit simulations for five technological nodes (65, 28, 22, 14 and 7 nm), showing that the modeled current reliably induces bit flips. This Geant4-based approach for simulating FET devices enables precise evaluation across technological nodes, making it a valuable tool for assessing susceptibility to cosmic-ray-induced particles across different technologies.

II. Geant4 and Related Work

Geant4 (Geometry and Tracking 4) [13]–[16] is an open-source toolkit designed to simulate the trajectory of particles or radiation as they traverse different materials. Its application areas include high-energy physics, technology transfer, space and radiation studies, and medical physics (e.g., X-rays, proton therapy). Geant4 is used by many research institutions, including the European Organization for Nuclear Research (CERN).

Geant4 can replicate experimental setups, simulate radiation sources, and capture specific physical quantities resulting from the interaction of source particles and secondary particles with the material. This toolkit supports a large spectrum of particle transport simulations, allowing users to model geometries, navigate tracks, apply physics interactions, generate secondary particles, record relevant information, visualize setups, and interact with the application through a flexible interface. Geant4

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also encompasses a comprehensive set of physics processes, spanning electromagnetic, strong, and weak interactions across a broad energy range. Its open-source nature, readable source code, and example applications make it adaptable for various domains, facilitating the creation of custom applications or the utilization of existing configurations.

Examples of Geant4 applications in MOS device research include: (i) radiation environment simulation, (ii) particle interaction modeling, (iii) damage and degradation analysis, (iv) shielding and mitigation strategies, and (v) testing and validation.

A. Related Work Using Geant4 in FET Devices

Takashi *et al.* [17] show that negative muons induce significant multiple-cell upsets (MCUs) in 65 nm and 28 nm bulk planar SRAMs. In contrast, positive muons do not result in such upsets [18, 19]. Their research notices that the susceptibility to MCUs increases as SRAM cells shrink. Also, they observe that due to transistor miniaturization, the MCU mechanism becomes more complex, including the induction of parasitic bipolar effects (PBEs) due to the well potential perturbation [20, 21]. In conclusion, these authors infer that it is necessary to investigate the muon-induced MCUs in more advanced devices.

Deng *et al.* [22] propose a method based on a proton acceleration test using Geant4 simulation to predict single event upsets (SEUs) caused by positive muons in 65 nm bulk SRAM. They compare experimental data on muon-induced SEUs with simulation results for proton-induced ones, and conclude that the fluxes of incident particles reaching the semiconductor devices differ between protons and positive muons, due to energy straggling within the device. The authors emphasize the following assertion: *"...neutron indirectly induces soft errors through the nuclear interaction with atomic nuclei in the device, while the muon can deposit the energy directly through the ionization process in the device and cause SEUs."*

Hubert *et al.* [23] demonstrate that both protons and muons need to be considered in ground environments. They also report significant differences among bulk CMOS, FDSOI, and finFET technologies, noting that downscaling increases the susceptibility to radiation-induced SEUs. Consequently, muon-induced SEE rates are expected to rise as the critical charge decreases with the miniaturization of semiconductors.

Additionally, Hao *et al.* [24] investigate the differences in gamma-ray radiation effects between planar and finFET devices. Their study concludes that finFETs exhibit lower sensitivity to transient radiation than planar FETs.

III. Simulation Methodology

This work adopts Geant4 version 11.2.1 (2024) as simulation framework, using the FTFP_BERT physics list [25]. The selection includes five technologies: two planar ones (65 and 28 nm) and three finFET ones (22, 14, and 7 nm). The construction process involves incrementally building each component of the structure. Fig. 1 and Table I detail the selected technologies' main geometrical representation.

Simulations follow the geometries modeling. When preparing simulations, the incident particles, their angles of incidence, energies, and the number of initial particles per run

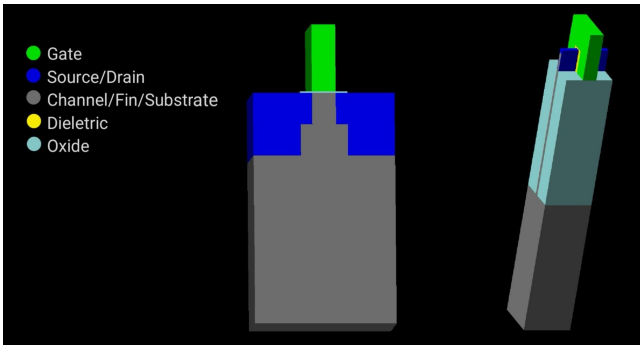

Fig. 1. FET architecture designs, planar (left) and finFET (right).

TABLE I
FET architecture dimensions for 65 nm, 28 nm, and 7nm technologies, displayed with XYZ position and values in nm.

Material	65 nm	28 nm	7 nm
Gate	35, 110, 100	32, 56.25, 57.15	24.1, 9, 57 (sides) 8.8, 9, 3.6 (superior)
Source/Drain	70, 110, 99.3	38.25, 56.25, 48	0.56, 24, 62.88 (sides) 6, 24, 10.88 (superior)
Substrate	210, 110, 250	112.5, 56.25, 250	57, 57, 250
Dielectric	——	——	1.4, 9, 53.4 (sides) 6, 9, 1.4 (superior)
Oxide	70, 110, 2.5	36, 56.25, 2.5	25.5, 57, 250

are specified. Protons, muons, alpha particles, and pions are chosen targets here. The initial particle energy range spans from 0.5 MeV to 100 TeV, as to cover the particles flux in the atmosphere presented in Chapter I. The initial particle angles of incidence are chosen trying to cover most of the ranges witch the particle may come, and are depicted in Fig. 2, which illustrates four distinct angular measurement groups:

- **Planar a**: angles range from perpendicular to the gate to lateral orientations that pass through the source and drain regions;
- **Planar b**: angles vary from above and perpendicular to the gate to a 90° angle that directly traverses the pure silicon channel;
- **FinFET a**: angles range from perpendicular to the gate to those that pass through the entire fin structure;
- **FinFET b**: angles range from above the gate to lateral orientations relative to the gate.

In each simulation, 10,000 strikes involving identical particles with the same initial energy and angle of incidence are performed to ensure statistically representative data. Results reflect what occurs within the sensitive area, defined as the silicon region below the gate. For finFETs, this includes the region below the gate and between the source and drain, whereas for planar FETs, it covers the area between the source and drain. While the simulation provides abundant physical data, the focus here is on electrons and the energy deposited by the detected particles. Table II summarizes the target parameters and conditions used in the work.

To compute the total number of electrons contributing to the particle-induced current, two simulation factors from must be considered: the number of detected electrons in the sensitive area and those generated by the energy deposited by particles passing through the sensitive area. This computation

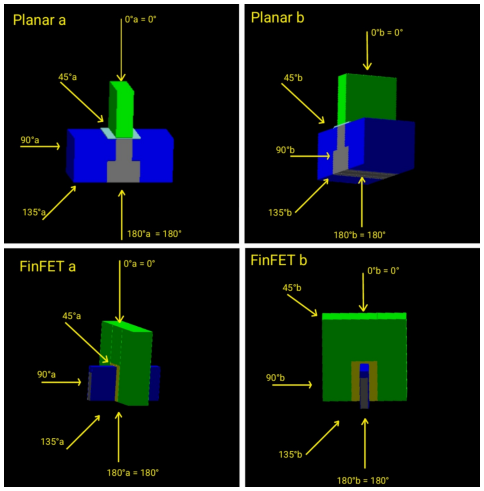

Fig. 2. Geant4-based simulation templates for 65 and 22 nm technology nodes. For clarity, the substrate area is not drawn. The selected four distinct angular measurement groups are highlighted.

TABLE II
SUMMARY OF EMPLOYED EXPERIMENTAL PARAMETERS/CONDITIONS.

Parameter	**Description**
Particles	Protons, positive muons, negative muons, alpha particles, positive pions, negative pions, neutral pions
Technology	Two planar (65 nm and 28 nm) and three finFETs (22 nm, 14 nm, and 7 nm)
Initial Particle Energy	0.5 MeV, 1 MeV, 2 MeV, 5 MeV, 10 MeV, 100 MeV, 500 MeV, 1 GeV, 500 GeV, 1 TeV, 10 TeV, 100 TeV
Incident Angles in Technology	0°, 45°a, 90°a, 135°a, 180°a, 45°b, 90°b, 135°b (Figure 2)
Number of Particles per Simulation	10,000 incidents of identical particles

is necessary because Geant4's standard libraries only account for electrons generated by ionization with energies above 10 eV [26], while low-energy electrons also contribute. Electrons are included if the deposited energy exceeds the pair creation threshold. The number of generated electrons is computed by dividing the initial energy by the 3.6 eV, required to create pairs in silicon [27]. The total number of electrons is then divided by 10,000 to determine the number per incident particle. With this information, the drain current can be computed.

Eq. (1) presents the current computation as a function of the number of electrons obtained from the Geant4 simulation, based on the technological parameters [28]–[30].

$$I = \frac{N\, q_0\, \mu\, V}{L^2} \tag{1}$$

In Eq. (1), N is the number of produced electrons, q_0 is the elementary charge of the electron [28], μ is the electron mobility in $\frac{m^2}{V \cdot s}$, V is the supply voltage, and L the effective channel length. It is thus possible to use the current equation and technology definitions to compute the current induced in each simulation. This approach allows assessing and compare the results with Spice (using e.g. Cadence Spectre) simulations and tabulated values to determine whether the device is susceptible to inducing bit flips.

IV. RESULTS

The first part of the results, Section IV-A, evaluates the number of electrons each particle produces, as a function of its energy. Section IV-B determines the current required to induce bit flips, through electrical simulation. Section IV-C presents the electric current produced by the charges obtained from the Geant4 simulation, for different angles of incidence. This Section compares the current from the Geant4 simulation with that obtained from electrical simulations, which allows assessing when bit flips do occur, based on technology, particle type, and angle of incidence.

A. Energy versus Average Number of Electrons

Fig. 3 shows the average number of electrons (y-axis) produced at different energy levels (x-axis). Due to paper size limitations, only protons and alpha particles data are presented, though simulations were also performed for pions, positive muons, and negative muons. This Figure demonstrates that the number of generated electrons decreases as energy increases. At higher energies, particles tend to traverse the material more quickly, resulting in fewer collisions and, consequently implying a lower production of secondary electrons. This behavior is associated to the *stopping power* in silicon material [31], which explains why, in this case, the number of produced electrons decreases as the particle's energy increases. The Figure also shows that planar technologies, especially the 65 nm technology, produce more electrons due to their larger sensitive area. However, this does not necessarily imply a higher number of SEUs, as the current required to induce a bit flip varies among different technologies.

In the conducted experiments, since higher-energy particles interact less with the medium, the 0.5 MeV energy is used for all results below.

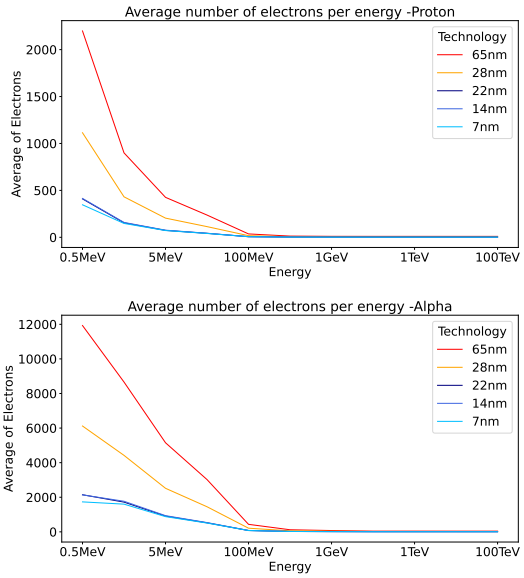

Fig. 3. Energy versus Average Number of Electrons per Particle: protons (top), alpha particles (bottom).

B. Memory Cell Simulation

This section details the electrical stimulation of a memory cell across 65 nm (planar), 28 nm (planar), and 7 nm (finFET) technology nodes to determine the current needed to induce a bit flip. A current source is connected to the memory cell outputs, Q and $\overline{Q}$, simulating the current generated by particle interactions.

Fig. 4 provides a close-up view of the moments when bit flips occur in the simulation. Table III presents the current required to induce a bit flip, as measured using commands from the Cadence Spectre simulator. A lower current value was expected for the 28 nm technology. This value presented by Spectre is probably due to differences in transistor sizing and type. *A key finding of this work is the quantification of the current that particles must induce in real technologies for bit flips to occur.*

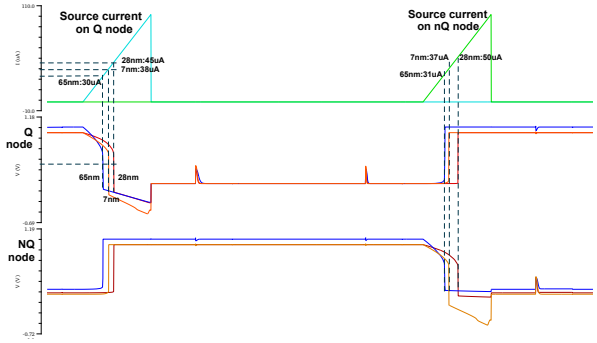

Fig. 4. Simulation of bit flips on 65 nm, 28 nm, and 7 nm. The simulation highlights the current inducing the bit flips on signals Q and NQ (cell memory outputs), for each technology.

TABLE III
CURRENT, IN μA, TO INDUCE A BIT FLIP.

Technology node	65 nm	28 nm	7 nm
bit flip 1 $\rightarrow$ 0	**30**	**45**	38
bit flip 0 $\rightarrow$ 1	31	50	**37**

C. Angle of Incidence versus Current

Fig. 5 presents the maximum current achieved for each particle strike incidence angle, based on angles from Fig. 2 and an energy of 0.5 MeV. The graphs span various technologies, though only results for the 65 nm and 7 nm nodes are shown. The y-axis maximum current (I) is determined by the electron count generated by each particle, calculated using Eq. (1).

In Fig. 5, the dashed golden line represents the minimum current required to induce a bit flip in the technology at hand. This current value, obtained from Spectre electrical simulation (as presented in Section IV-B), indicates the bit flip threshold.

From Fig. 5, it is possible to observe (due to page limitations, we present graphs only for 65 nm and 7 nm):

- **65 nm**: Protons generate currents above the bit flip threshold at all incidence angles, experimental findings have been reported in previous studies, where low-energy protons were shown to upset circuits in different angles [32]. Positive pions and muons can also induce bit flips at $90°a$, particularly when passing through the source/drain area;
- **28 nm**: This technology demonstrates strong resilience to bit flips, with only protons causing issues at $90°a$ through the source/drain area;
- **22 nm**: Protons can induce bit flips at various angles, while positive pions approach the bit flip threshold at $45°a$ and $135°a$;
- **14 nm**: Both protons and positive pions can induce bit flips, with positive muons also capable of causing bit flips at $0°$. That result agrees with the statement that proton and muon effects must be considered for ground environments, with increased SEU susceptibility in smaller technologies [23].
- **7 nm**: All particles can induce bit flips at $0°$. However, due to the specific angle and small affected region, fewer events may occur despite the increased sensitivity. At other angles, protons are the main contributors to bit flips.

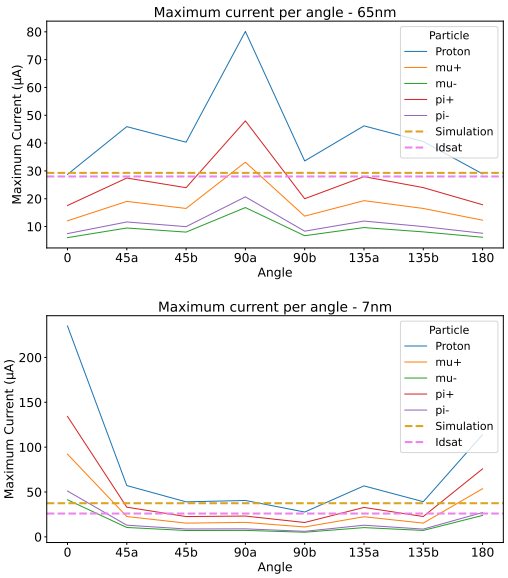

Fig. 5. Current per incidence angle for different particles. The golden dashed line is the minimum current needed to cause a bit flip, obtained from electrical simulation (Section 4). the violet dashed line is the minimum current using I_{ON}.

V. CONCLUSIONS AND FUTURE WORK

This work investigated the impact of various cosmic ray particles on different transistor technologies. Simulations using Geant4 were conducted to investigate electron generation and the potential for SEEs in FET technologies.

Although alpha particles constitute only 9% of cosmic rays, they generate a significant number of electrons. Protons, which account for 90% of cosmic rays, also produce many electrons and are prominent in experimental studies. While positive pions and muons generate fewer electrons, they remain relevant due to their presence at lower atmospheric and ground levels.

The current induced by electron generation varies with the angle of particle incidence. Planar technologies are at a higher risk of SEEs when particles pass through the source and drain at an angle of $90°$. FinFET technologies, in contrast, are more vulnerable when particles strike from above the fin and pass through the gate at $0°$. Simulations highlight the importance of considering angular dependence when evaluating SEE risks and demonstrate that positive pions and muons can induce bit flips in finFET technologies.

This work provided an initial approach to assess the effects of cosmic ray particles on FET devices. Future research can expand this approach to include a broader range of particles (such as neutrons) and investigate newer technology nodes beyond 7 nm. This would help assess how further miniaturization impacts SEE susceptibility and explore mitigation strategies.

ACKNOWLEDGMENTS

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