An IR-UWB Pulse Generator using PAM Modulation with Adaptive PSD in 130nm CMOS Process

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ABSTRACT

This paper proposes an adaptive pulse generator using Pulse Amplitude Modulation (PAM). The circuit was implemented with eight Pulse Generator Units (PGUs) to produce up to eight monocycles per pulse. The number of monocycles per pulse is inversely proportional to the Power Spectrum Density (PSD) bandwidth in the Impulse Radio Ultra-Wide Band (IR-UWB). The complete circuit contains two pulse generator blocks, each one composed by eight PGUs to build a rectangular waveform at the output. The PGU has been implemented with Edge Combiners High (ECH) and Edge Combiners Low (ECL) to encode the information. Each Edge Combiner has a high impedance circuit that is selected by digital control signals. The circuit has been simulated, showing an output pulse amplitude of ≈70mV for the high logic level and an amplitude of ≈35mV for the low logic level, both at 100 MHz Pulse Repetition Frequency (PRF). This produces a mean pulse duration of ≈270ps, a mean central frequency of ≈3.7GHz and a power consumption less than 0,22μW. The pulse generator block occupies an area of $0.54mm^2$.

CCS CONCEPTS

• **Hardware → Radio frequency and wireless interconnect**;

KEYWORDS

IR-UWB, PAM modulation, Microwave transmitters, IoT, CMOS.

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1 INTRODUCTION

The global communications market shows that innovations in wireless connectivity have enormous potential for the Internet of Things (IoT) [1], [2] and [3]. This potential is due to the demand of short-range circuits, such as wireless sensor networks [4], wearable devices and mobile health applications [5]). These advancements are possible because there had been an evolution in silicon technologies allowing the development of the Systems-on-Chip (SoC) and wireless technologies on the same silicon wafer. In communications area many researchers believe that Impulse-Radio Ultra-Wideband (IR-UWB) is an excellent alternative for IoT applications. It has excellent wireless connectivity, low power consumption, high transfer rates, simple architecture at low cost. The basic architecture of an IR-UWB transmitter can be implemented using four building blocks: (*i*) a modulator that encodes the binary input data using an external clock; (*ii*) a pulse generator with pulse output for sub-nanosecond range; (*iii*) amplifier circuits; (*iv*) a driver for 50 Ω antennas [6], as shown in Figure 1. The IR-UWB devices can support many applications in environments where distances between devices are very small [5]. For instance, at home and commercial environments the IR-UWB is more effective, allowing unique communication channels with low power. Other advantages of IR-UWB devices include rejection of multipath fading and security against interception and jamming.

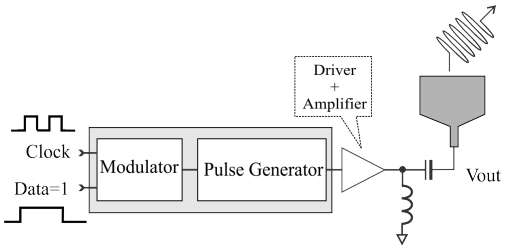

Figure 1: The basic architecture of an IR-UWB transmitter.

Moreover, there are various carrierless modulation schemes developed for UWB systems for data transmission, including Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM) [7], Binary Phase Shift Keying (BPSK) [8], On-Off-Keying (OOK) [9]. Theses pulse modulations can be designed in different ways. For instance, references [9] and [10] proposed an edge combiner circuit to produce a pulse at the integrated bandpass filter to generate UWB pulses. This technique is straightforward, but it has limitations to generate pulses with different waveforms. Besides, this is expensive, due to the large area occupied by the on-die planar inductors and capacitors. Reference [11] proposes a pulse generator using a single NAND gate to generate a voltage pulse that is applied across an on-chip nMOS-type capacitor and produces a current-voltage relationship like the first derivative (i. e. monocycle pulse). A transmitter based on the pulse synthesizing technique was implemented in [12]. This technique is very simple to apply but depends on the time control provided by a chain of inverters, composed by a voltage-controlled delay line (VCDL) circuit where a rising edge is propagated through tunable delay cells. Reference [13] suggests implementing an all-digital transmitter with dual capacitively-coupled pulse-shaping drivers.

This paper proposes an IR-UWB pulse generator that can change the range of the bandwidth in the Power Spectral Density (PSD) of the emissions mask, using just a variable using up to 8 monocycles per pulse at the output. In this design, the variations of monocycles inside the pulse change the bandwidth, being that just one monocycles per pulse produces a wideband on the power mask. However, if the pulse has eight monocycles tend a produces a narrowband on the power mask, as shown Figure 2. The main goal is to make a transmitter circuit using this concept to fit the signal in the emission mask [14]. The principle of operation is explained in Section 2. Section 3 discusses architecture description of the adaptive PSD pulse generator circuit design in detail. The layout and simulations results are the target of Section 4, followed by a set of conclusions, drawn in Section 5.

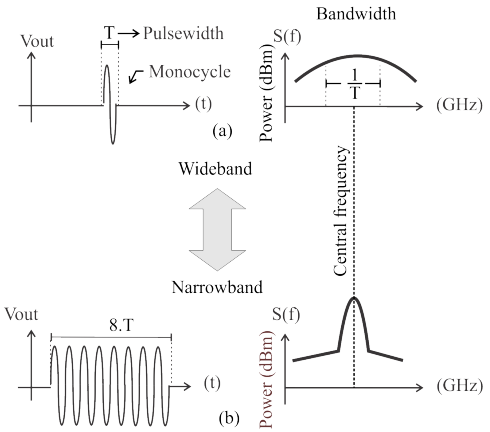

Figure 2: Signal forms of PSD in the emissions mask: (a) Wideband; (b) Narrowband.

2 PRINCIPLE OF OPERATION

The IR-UWB pulse generator, proposed in this paper, uses a simple PAM modulation scheme to produce two pulse amplitude variations at the output to represent either the high logic level or low logic level at input. In other words, the pulse requires only a single polarity to represent a data signal: high amplitude represents high logic level and the low amplitude represents low logic level. Besides, each pulse at output of the pulse generator can generates up to 8 monocycles per pulse to adapt in the PSD emission mask, as shown in Figure 2. This circuit was implemented with four main blocks: a demultiplexer circuit to select the clock forward between Edge Combiner High (ECH) and Edge Combiner Low (ECL).This circuit was implemented with two AND gates (G1 and G2) connected to an inverter circuit to select the edge combiner into a PGU and to encode the data signal in the PAM modulation; eight PGUs connected in parallel and each PGU uses two edge combiner circuits(e.g. ECH and ECL), each one generating up to 8 eight monocycles per pulse; a digital selector block composed by static logic gates to select the PGUs; a polarized filter at the output connected to all PGUs, as shown in Figure 3.

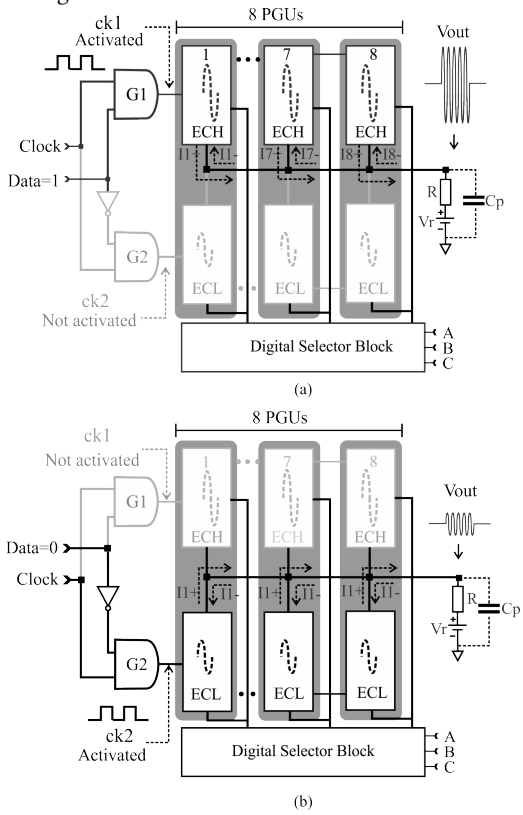

Figure 3: The operation mode of pulse generator. (a) when Data=1 the ck1and ECH are actived; (b) when Data=0 the ck2 and ECL are actived.

The principle of operation of the pulse generator using the PAM modulation is relatively simple. It can use two values of the signal amplitude as described above. When the data signal is set to high, the logic AND gate G1 of the Demultiplex (DEMUX) circuit is activated and the clock signal of the input goes to the output of the logic gate. This output signal is called "Ck1" and is connected to ECH PGUs, as shown in Figure 3(a). Then, the digital circuit block will select the number of oscillations of the output pulse. This pulse selection defines the number of PGUs that will be used to generate

the pulse at high amplitude output. This pulse is connected to the filter and to properly form the output pulse oscillations. When the data signal is set to low, the logic AND gate G2 of the demultiplex circuit is activated and the clock signal of the input goes to the output of the logic gate. This output signal is called "Ck2" and is connected to ECL PGUs, as shown in Figure 3(b). The digital circuitry at the digital block will select the quantity of monocycles per pulse at the output of PGUs. This monocycles will be sent to the filter to correctly waveform at output of pulse generator.

3 ARCHITECTURE DESCRIPTION

The proposed IR-UWB circuit generates rectangular pulses that can be adjusted up to eight monocycles, using a PAM modulation scheme. It consists of three main blocks: a demultiplex circuit block; PGU blocks generates monocycles; Digital Selector Block (DSB) to select number of PGUs. The main blocks are explained in detail as follows.

3.1 Demultiplex Block

The decision circuit, in this design, was implemented with a 1:2 Demultiplex (DEMUX) circuit using two static CMOS NAND gates, and an inverter circuit to select output, as shown in Figure 3(a, b).

3.2 Pulse Generator Unit (PGU)

Many techniques can be used to design of edge combiner circuits in the PGU. In the proposed design, we implement both edge combiners were modified from previous publications [4]. Under these circumstances, each PGU was implemented with ECH and ECL techniques using pMOS and nMOS transistors connected in series, as shown in Figure 4. Thus, each PGU behaves like a charge pump circuit to control charge and discharge current on the polarized filter to generate the output voltage. In other words, the PGU controls the current flow from VDD to Vout and Vout to GND to form one monocycle. When the PGU is not selected, transistors Mp13, Mn11, Mp23 and Mn21 are off, and as a result the node output is in high impedance state. Thus, there is no output voltage peak in the polarized filter. However, when the PGU is selected, the ECH as well as the ECL are selected through transistors Mp13, Mn11, Mp23 and Mn21, which are on. When the data signal is high, just the ECH is selected to generates high amplitude monocycles at Vout as shown Figure 4(a), conversely when the data signal is low, just the ECL is selected to generates low amplitude monocycles at Vout as shown Figure 4(b). In this block, the monocycle is generated at the output, due the phase difference among delay signals V(a), V(b) and V(c), as shown in Figure5 (b). This delay signals generate a positive peak amplitude of the monocycle in 3 states:

(1) First state, before transition: suppose that signals V(a)=1 and V(b)=0, then signal (I+)='0' (at high impedance condition). In this condition, Mp11 is on and Mp12 is off;
(2) Second state, when V(a) goes from high to low , and V(b) goes from low to high , Mp11 and Mp12 goes on, generating a narrow pulse of current with a width of the phase difference, then the electric current flows from VDD to polarized filter;
(3) Third state: after the transition, suppose that signals V(a)=0 and V(b)=1, then pulse current (I-)='0' (at high impedance condition). In this condition, Mp11 is off, Mp12 is on.

The negative peak amplitude of the monocycle is generated similarly, as follows:

(1) First state, before transition: suppose that signals V(b)=0 and V(c)=1, then signal (I-)='0' (at high impedance condition). In this condition, Mn11 is on, Mn12 is off;
(2) Second state, when V(b) goes from high to low , and V(c) goes from low to high , Mn11 and Mn12 goes on, generating a narrow pulse of current with a width of the phase difference, then the electric current flows from polarized filter to GND.
(3) Third state: after the transition, suppose that signals V(a)=0 and V(b)=1, then pulse current (I-)='0' (at high impedance condition). In this condition, Mn11 is off, Mn12 is on.

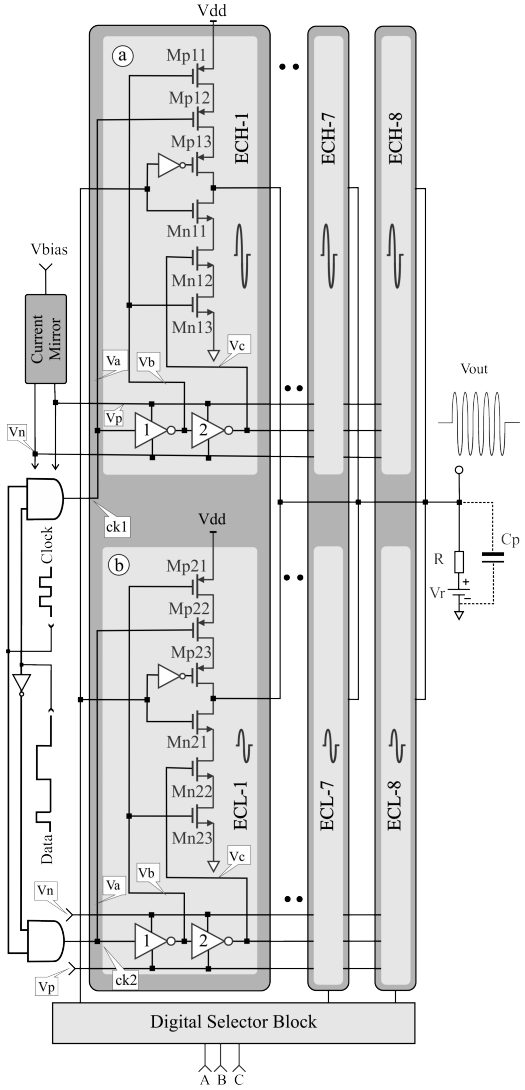

Figure 4: Block diagram of reconfigurable pulse generator with 8 PGUs using PAM modulation scheme: (a) ECH circuit – top part of the Figure; (b) ECL circuit – lower part of the Figure.

The delay circuit was implemented with three cascaded inverters to control the delay time in the PGUs. Thus, was chosen a current starved, a conventional static inverter, and a pseudo-nMOS inverter

[15] [16], to enhance the control of the delay between the inverter input and outputs, as shown in the Figure 5(a). When compared, these inverters represent a trade-off among them. For example, the current starved is often used to control delay in the ring oscillator, because current sources limit the current available to the inverter. In the static inverter there is no DC current flow through it and consequently the power consumption is smaller. As a result, the design takes advantage of the fact that the current starved and pseudo-nMOS circuits need a current mirror to control the current at the output of the inverter. This justifies the configuration choice here, to operate as delay circuits, given its simplicity to keep a fixed frequency. Besides, it presents an excellent delay response, resulting in a better IR-UWB output pulse frequency. This signal voltage will be produced on the edge combiner output. It presents a satisfactory delay response, making possible a better IR-UWB output pulse frequency.

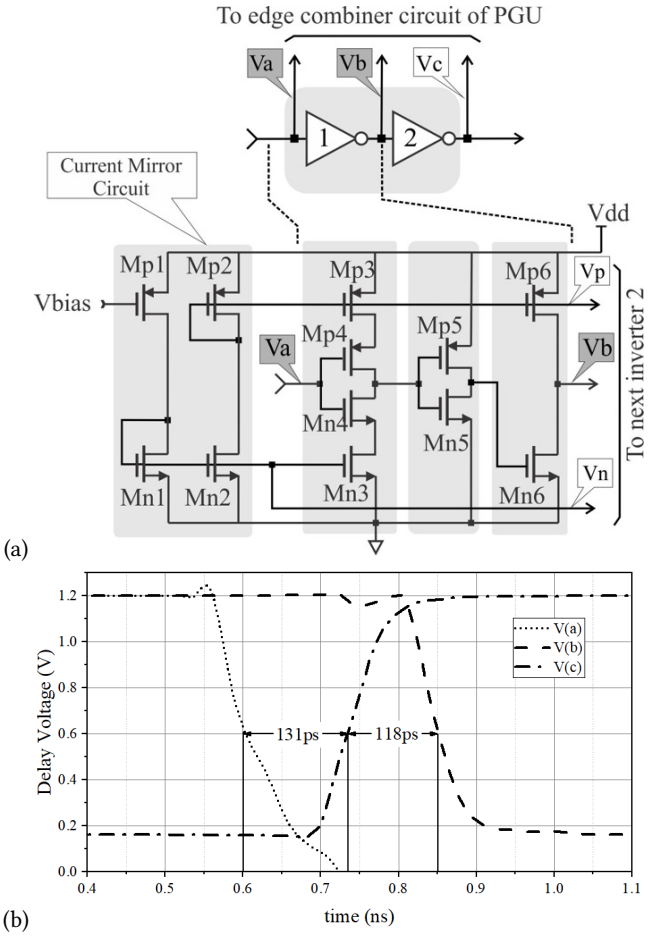

Figure 5: Delay circuits schematic: (a) Delay circuit; (b) Delay voltage phase difference.

3.3 Digital Selector Block

The digital selector block was implemented to select eight PGUs, generating up to eight monocycles per pulse. It was implemented using a simple circuit with AND and OR static gates. Each PGU has been designed with a high impedance circuit that is activated when a logic level at input goes to high, as shown in Figure 3(a,b). In this condition, the transistor mp13 and mn13 of the ECH block are on. Similarly, transistors Mp23 and Mn21 of ECL block are on. For example, when Binary Coded Decimal (BCD) is "000" at the input of the block selector, the pulse Vs1 (first output of this block) at output goes to high logic level and the other outputs, Vs2 up to Vs8, goes to low. In this condition, just one PGUs are activated and one monocycle is generated at the output of the pulse generator. However, when the BCD signal is "111" , eight PGUs are activated and eight oscillations per pulse are activated. In this condition, the pulses from Vs1 up to Vs8 goes to high logic level, as shown in Table 1.

Table 1: The selection of ECH and ECL circuits using Binary Code Decimal (BCD).

BCD	Number of the PGUs circuits actived.							
	Vs1	Vs2	Vs3	Vs4	Vs5	Vs6	Vs7	Vs8
000	1	0	0	0	0	0	0	0
001	1	1	0	0	0	0	0	0
010	1	1	1	0	0	0	0	0
011	1	1	1	1	0	0	0	0
100	1	1	1	1	1	0	0	0
101	1	1	1	1	1	1	0	0
110	1	1	1	1	1	1	1	0
111	1	1	1	1	1	1	1	1

4 SIMULATION RESULTS

This section presents simulation results of the PAM pulse generator using a PRF of the 100 MHz and a power supply at 1.2V in the 130nm CMOS process . Besides, was implemented a resistor with 50Ω and a parasitic capacitances (Cp) of nMOS and pMOS transistors. In addition, there is an external 500mV supply voltage (Vr), to polarize the PGU output, as depict Figure 4. Table 2 compares our proposal to related works through implementation technology, voltage supply, design method, area, PRF, power consumption and modulation technique choice. All simulations were carried out using the LTSpice electrical simulator. Figure 6 presents the layout of the pulse generator circuit without PADs, with an area equal to $0.54mm^2$. The proposal in this works stands out in terms of power consumption and adaptivity.

Figure 5(b) depicted that time Tp_{HL} e Tp_{LH} have different times because the gate capacitance of transistors (Mp11 and Mn13) are high, and consequently increase the rise time at node v(b). Under this condition, the channel width of the pMOS transistor must be increased to higher values to decrease the rise time. The resulting circuit has a propagation delay of 249 ps between PGUs (ECH or ECL) to produce one oscillation at the output. Thus, each inverter presents a Tp_{HL} of 131ps, Tp_{LH} of 118ps. The total delay time of the pulse depends on the number of delay blocks selected in the signal path.

The central frequency when Data = '1' is ≈4.3 GHz and when Data = '0' this frequency is ≈3.7 GHz. The difference between the central frequencies is due to non-uniformity of pulses generated at output. This happens because the same circuits produce both pulses, hence zero and one pulses have the same slope, but zero pulses have smaller amplitude, ending each monocycle in less time than one pulses. Consequently, zero pulses carryless energy per pulse and have higher frequency than their corresponding one pulses.

Table 2: Comparative summary of IR-UWB pulse generators (NA: information not available in the reference)

Results	This work	*Ref. [7]	Ref. [9]	Ref.[18]	Ref. [19]	Ref. [20]	*Ref. [21]
CMOS technology (nm)	130	180	130	180	180	40	180
Voltage Supply (V)	1.2	1.8	1.2	~1.8	1.8	0.9	1.2
Method	Edge combiner	LO-based	Filtered Edge Combination	Filtered Edge Combination	LO-based	Edge combiner	Double PLL
Area (core)	0.54mm²	0.2mm²	0.54mm²	0.09mm²	0.55mm²	8200µm²	0.04mm²
PRF (MHz)	100	40.5	100	100-1000	125	100	31.25
Power consumption (mW)	0.047-0.215	1.97	3.84	0.26-0.th76	4	**NA**	**NA**
Modulation	PAM	PAM	OOK	OOK	PPM+BPSK	**NA**	OOK

*UWB transmitter

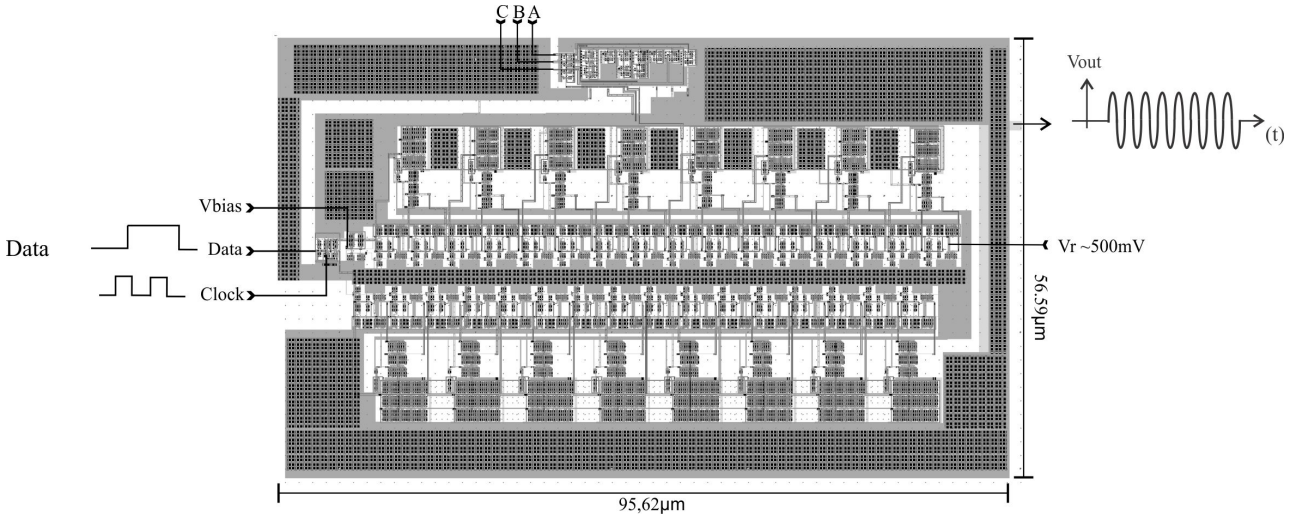

Figure 6: Proposed pulse generator complete layout without PADs.

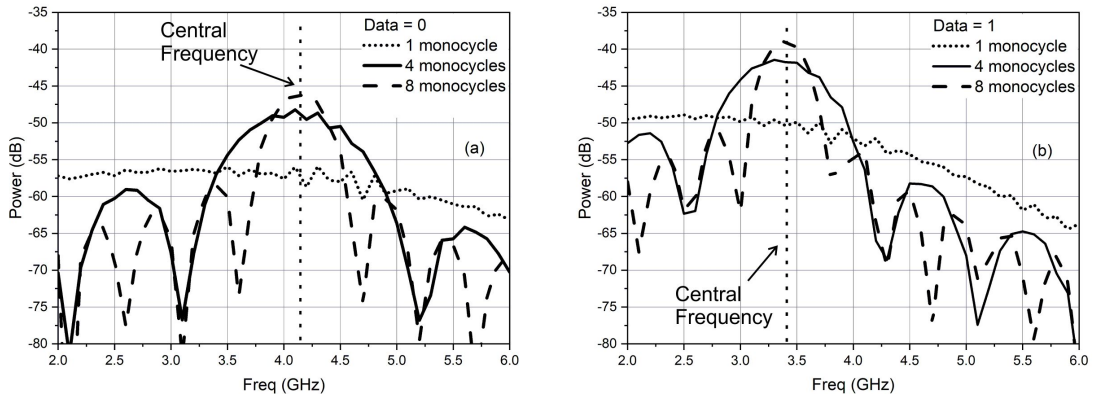

Figure 7: Power Spectrum Density simulation: (a) Data = 0, (b) Data = 1.

Another consequence appears when pulses with more monocycles have more energy than pulses with less monocycles, and because those pulses are longer than the former, their frequencies are smaller than the frequencies of the latter.

The total duration of the pulse with eight monocycles at the output is ≈1.9 ns. The PSD obtained using Discrete Fourier Transformation (DFT) is ≈32dBm for high logic level and ≈42dBm for low level, with a 50Ω load impedance on the output node [17], as shown Figure 7.The pulse generator circuit presents a pulse amplitude of ≈70mVpp for high logic level and ≈35mVpp for low logic level, as shown in Figure 8.

5 CONCLUSION

This work discussed an efficient small pulse generator using PAM modulation designed in a 130nm CMOS technology. Its generated pulse has an output pulse amplitude of ≈70mV for high logic level and an amplitude of ≈35mV for low logic level, both at 100 MHz Pulse Repetition Frequency (PRF), producing a mean pulse duration of ≈270ps, mean central frequency of ≈3.7GHz and low power

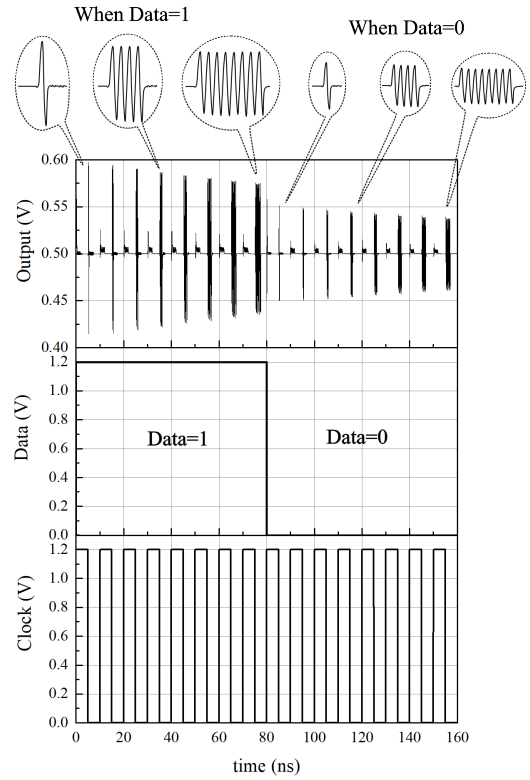

Figure 8: Time-domain waveform of the complete pulse generator circuit: top graph is the output voltage; middle graph shows when Data signal =1 and when Data=0; bottom graph shows the clock signal.

consumption. The full block of the pulse generator occupies an area of $0.54mm^2$. This design presents a small area, low power consumption and low complexity that can be applied in adaptive and reconfigurable transmitters in future designs.

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