

# Microeletrônica

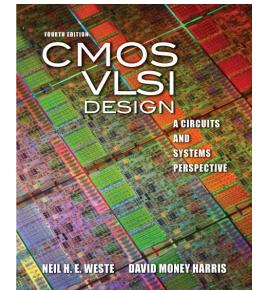
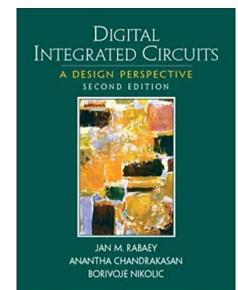
**Aula #1 → Introdução e Dispositivos MOS**

Professor: Fernando Gehm Moraes

Livro texto:

Digital Integrated Circuits a Design Perspective - Rabaey

CMOS VLSI Design - Weste



**Revisão das lâminas: 24/fev/2024**

# Sumário da aulas teóricas

## UNIDADE 1

**#1 → Introdução e Dispositivos MOS**

#2 → Inversor - comportamento estático e dinâmico

#3 → Portas lógicas estáticas

#4 → Dimensionamento de Portas Lógicas

#5 → Portas lógicas dinâmicas

#6 → Processo de fabricação CMOS

## UNIDADE 2

#7 → Circuitos sequenciais estáticos

#8 → Circuitos sequenciais dinâmicos

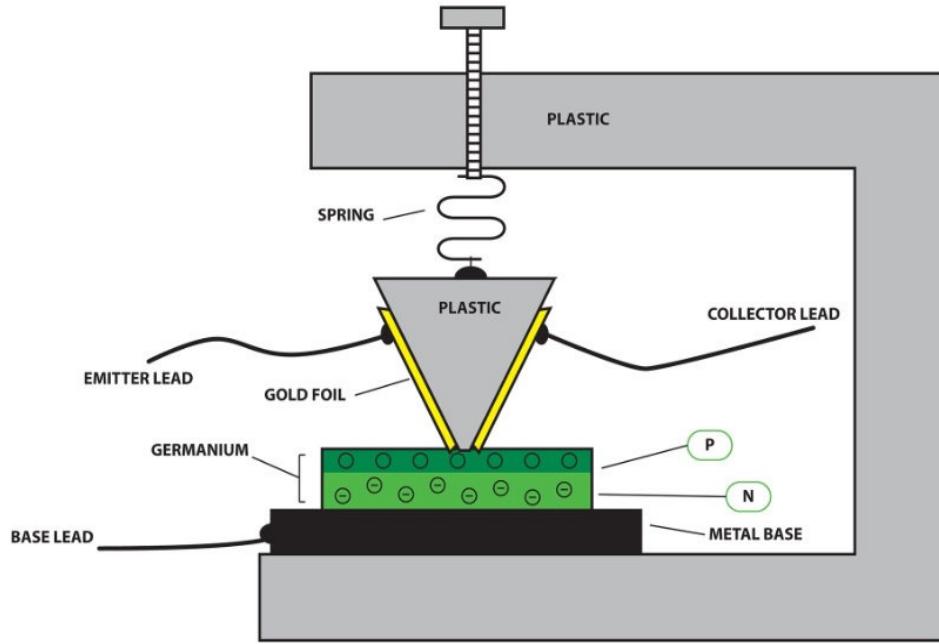
#9 → Circuitos aritméticos

#10 → Multiplicação e Divisão: conceitos básicos

#11 → Metodologias de projeto

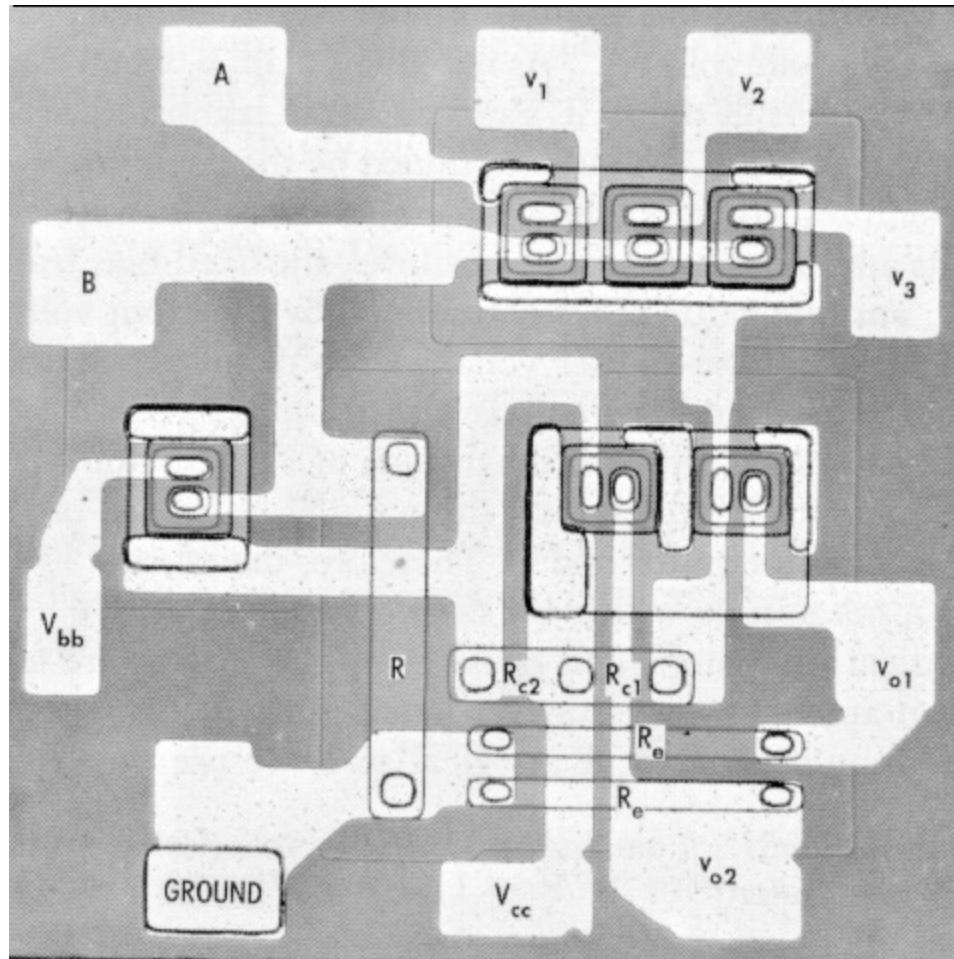
# The First Transistor

<http://www.computerhistory.org/revolution/digital-logic/12/273>



John Bardeen and Walter Brattain at Bell Laboratories constructed the first solid-state transistor. This PNP point-contact germanium transistor operated with a power gain of 18 on Dec. 23, 1947. With their manager, William Shockley, they won the Nobel Prize in 1956.

# The First Integrated Circuits

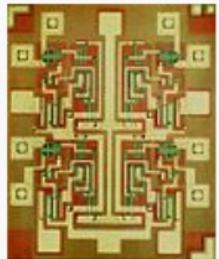


*Bipolar logic  
1960's*

ECL 3-input Gate  
Motorola 1966

The IBM Model 350 disk file with a storage space of 5MB from 1956 and a Micro SD Card

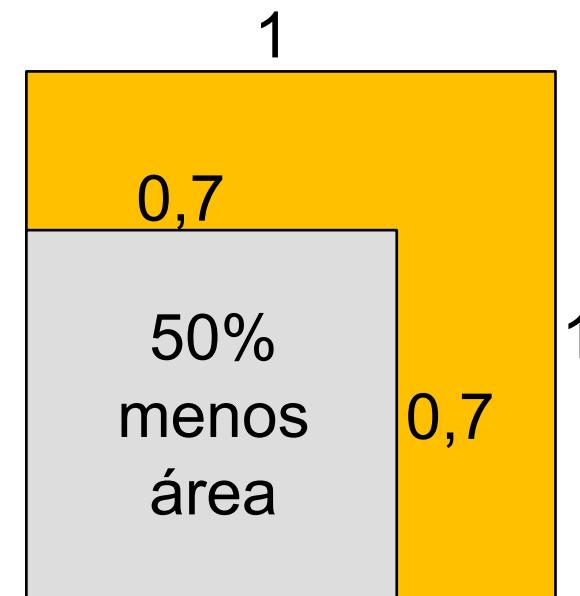
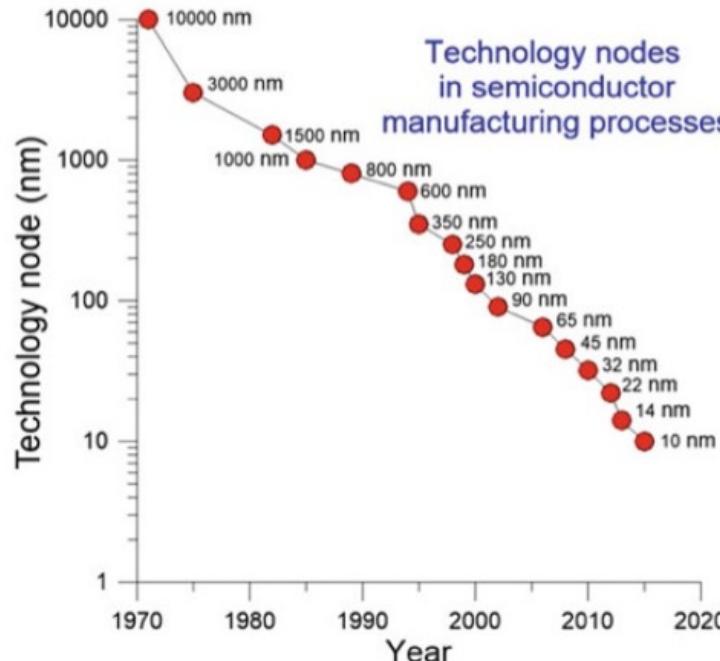




10 µm – 1971  
 6 µm – 1974  
 3 µm – 1977  
 1.5 µm – 1982  
 1 µm – 1985  
 800 nm – 1989  
 600 nm – 1994  
 350 nm – 1995  
 250 nm – 1997  
 180 nm – 1999  
 130 nm – 2001  
 90 nm – 2004  
 65 nm – 2006  
 45 nm – 2008  
 32 nm – 2010  
 22 nm – 2012  
**14 nm** – 2014  
 10 nm – 2017  
 7 nm – ~2018  
 5 nm – ~2020

# Gerações de transistores

- Scaling a technology reduces the lateral and vertical dimensions by 30%
- Die area =  $X * Y = 0.7 * 0.7 = 0,49$



$0,8 \mu\text{m} \rightarrow 0,6 \mu\text{m} \rightarrow \textcolor{red}{0,35 \mu\text{m}} \rightarrow 0,25 \mu\text{m} \rightarrow 0,18 \mu\text{m} \rightarrow 0,13 \mu\text{m} \rightarrow 0,09 \mu\text{m}$  (90 nm)  $\rightarrow 65 \text{ nm} \rightarrow 45 \text{ nm} \rightarrow 32 \text{ nm} \rightarrow 22 \text{ nm} \rightarrow 14 \text{ nm}$

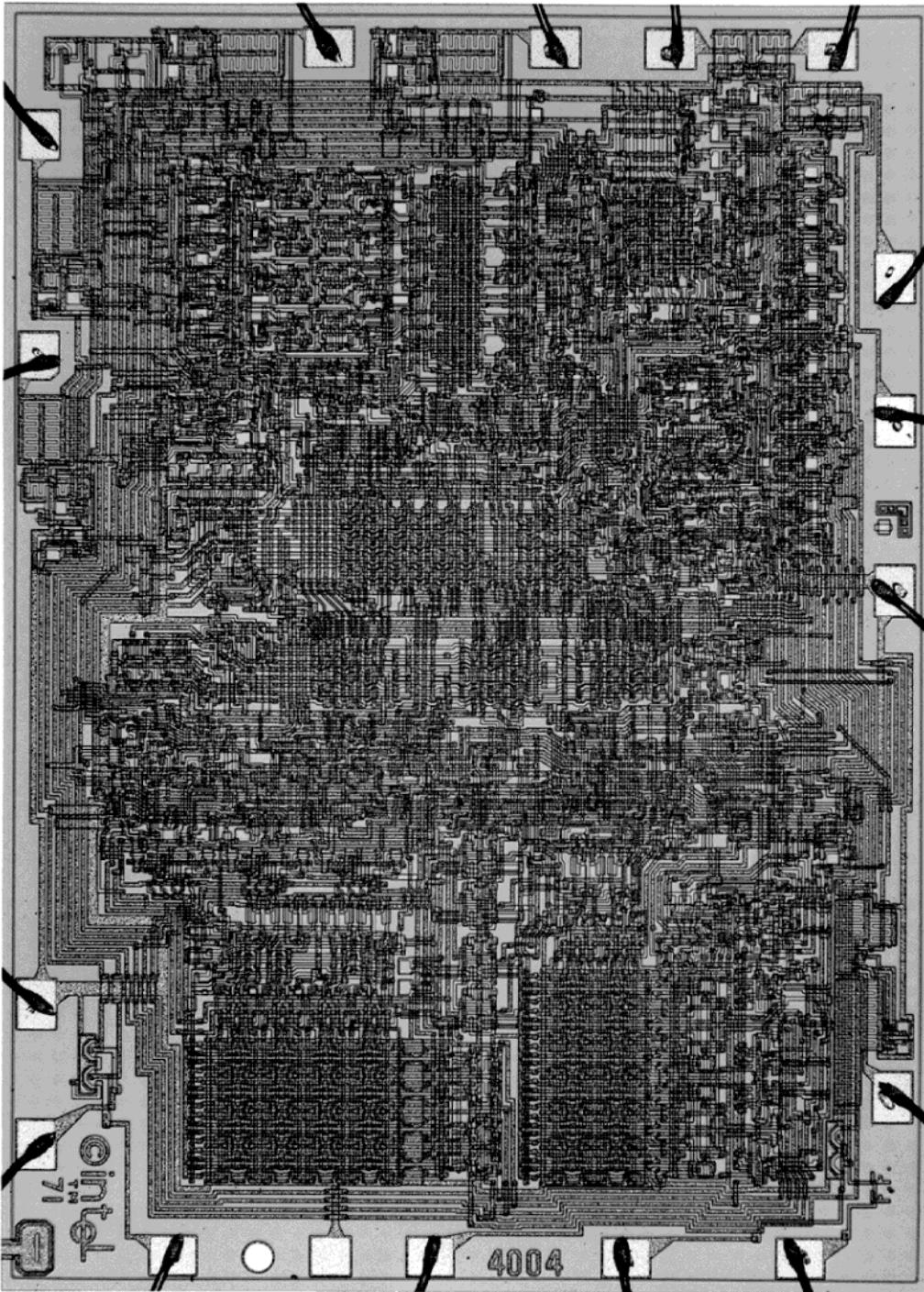
# Mercado de semicondutores

## Logic/Foundry Process Roadmaps (for Volume Production)

	2016	2017	2018	2019	2020	2021	2022
Intel	14nm+	10nm (limited) 14nm++		10nm	10nm+	10nm++	7nm EUV
Samsung	10nm		8nm	7nm EUV 6nm EUV	18nm FDSOI 5nm	4nm	3nm GAA
TSMC	10nm	7nm 12nm		7nm+ EUV	5nm 6nm	5nm+	4nm 3nm
GlobalFoundries		22nm FDSOI	12nm finFET		12nm FDSOI	22nm+ FDSOI	12nm+ finFET
SMIC				14nm finFET	12nm finFET		8-10nm finFET
UMC		14nm finFET			22nm planar		

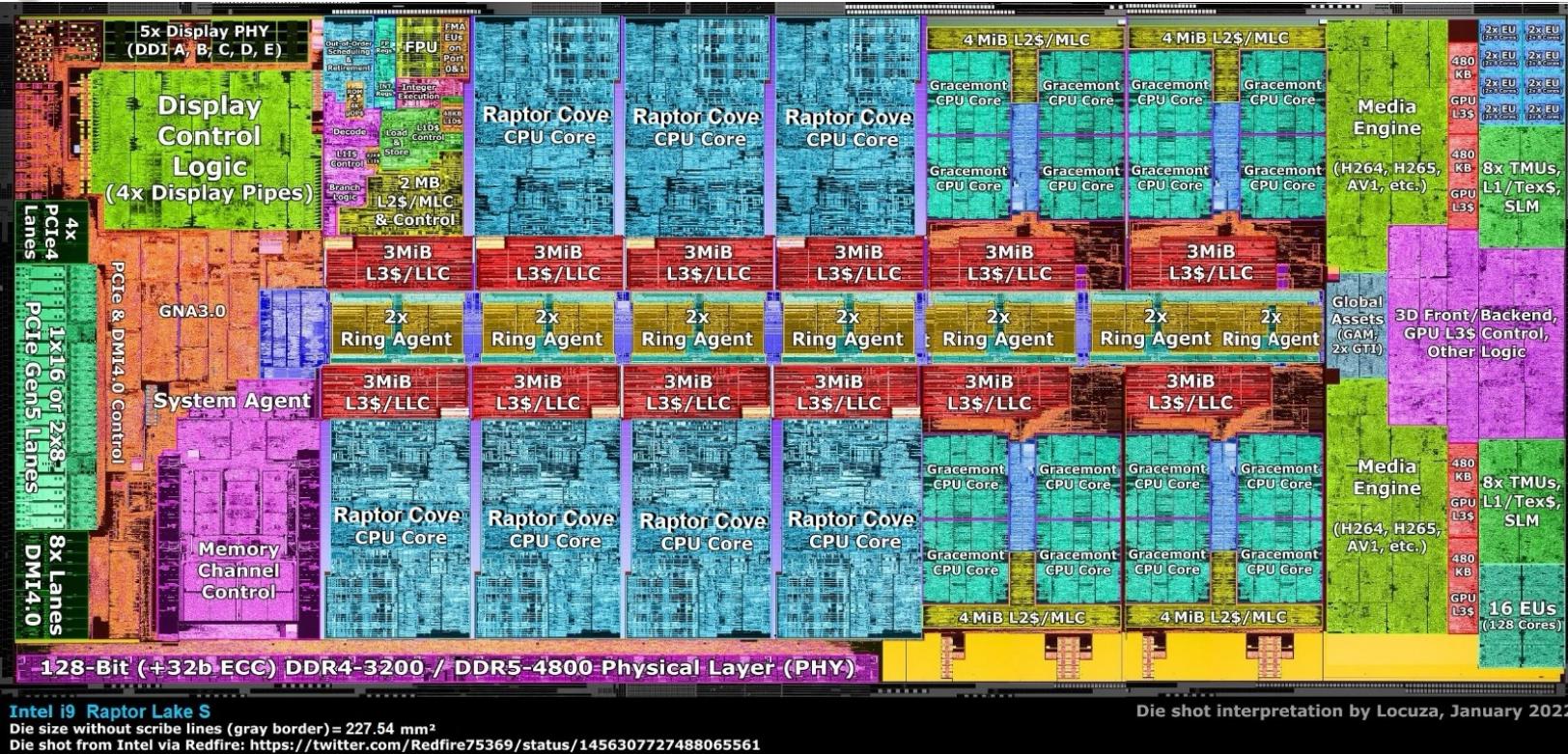
<https://www.icinsights.com/news/bulletins/Revenue-Per-Wafer-Climbs-As-Demand-Surges-For-5nm7nm-IC-Processes/>

<https://www.pcguia.pt/2021/03/tsmc-vai-iniciar-a-producao-de-chips-de-3nm-no-final-deste-ano-em-parceria-com-a-apple/>



# Intel 4004 Microprocessor

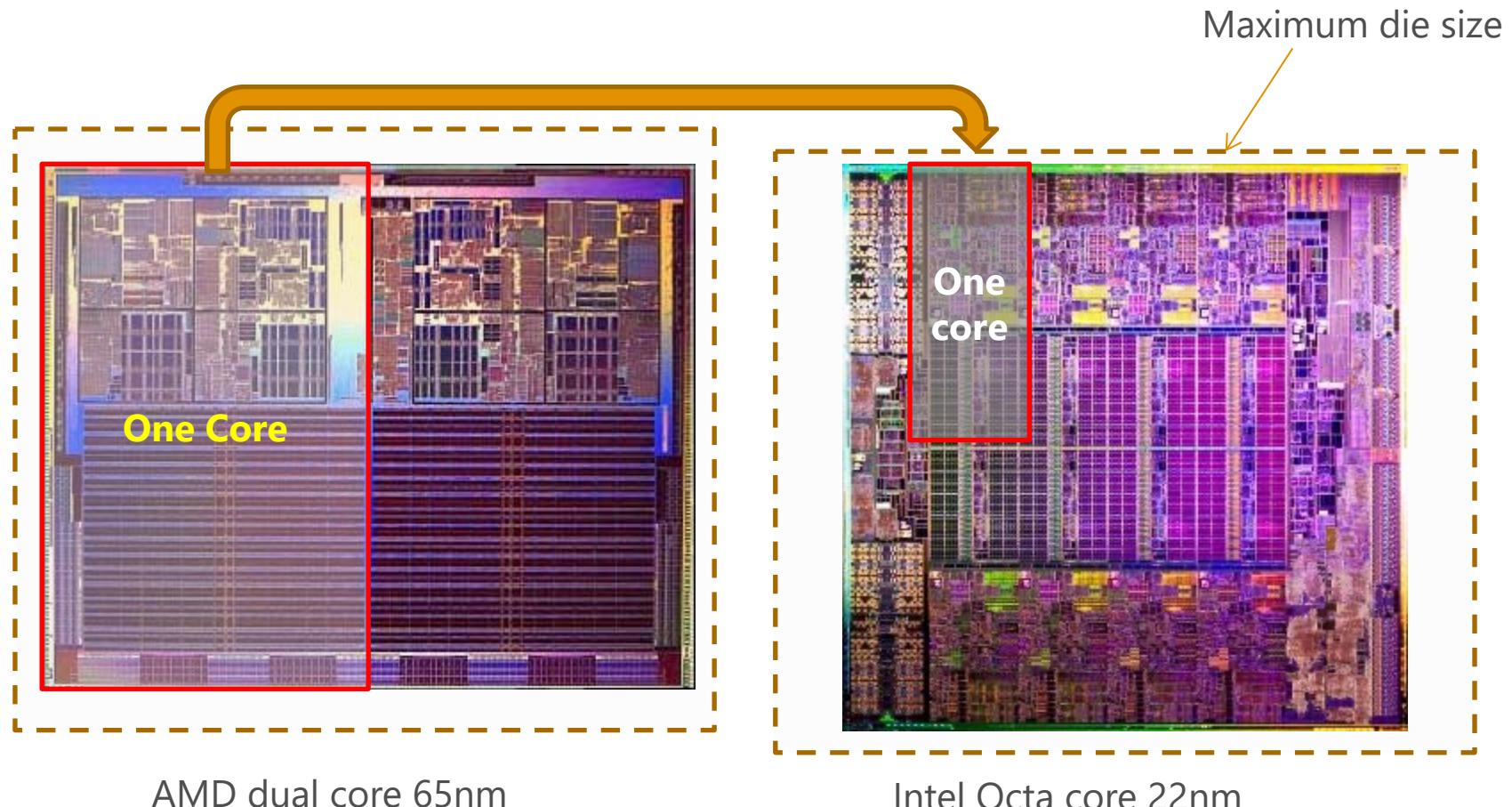
1971  
1000 transistors  
1 MHz operation



# Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months
- Høje: “*more than Moore*”

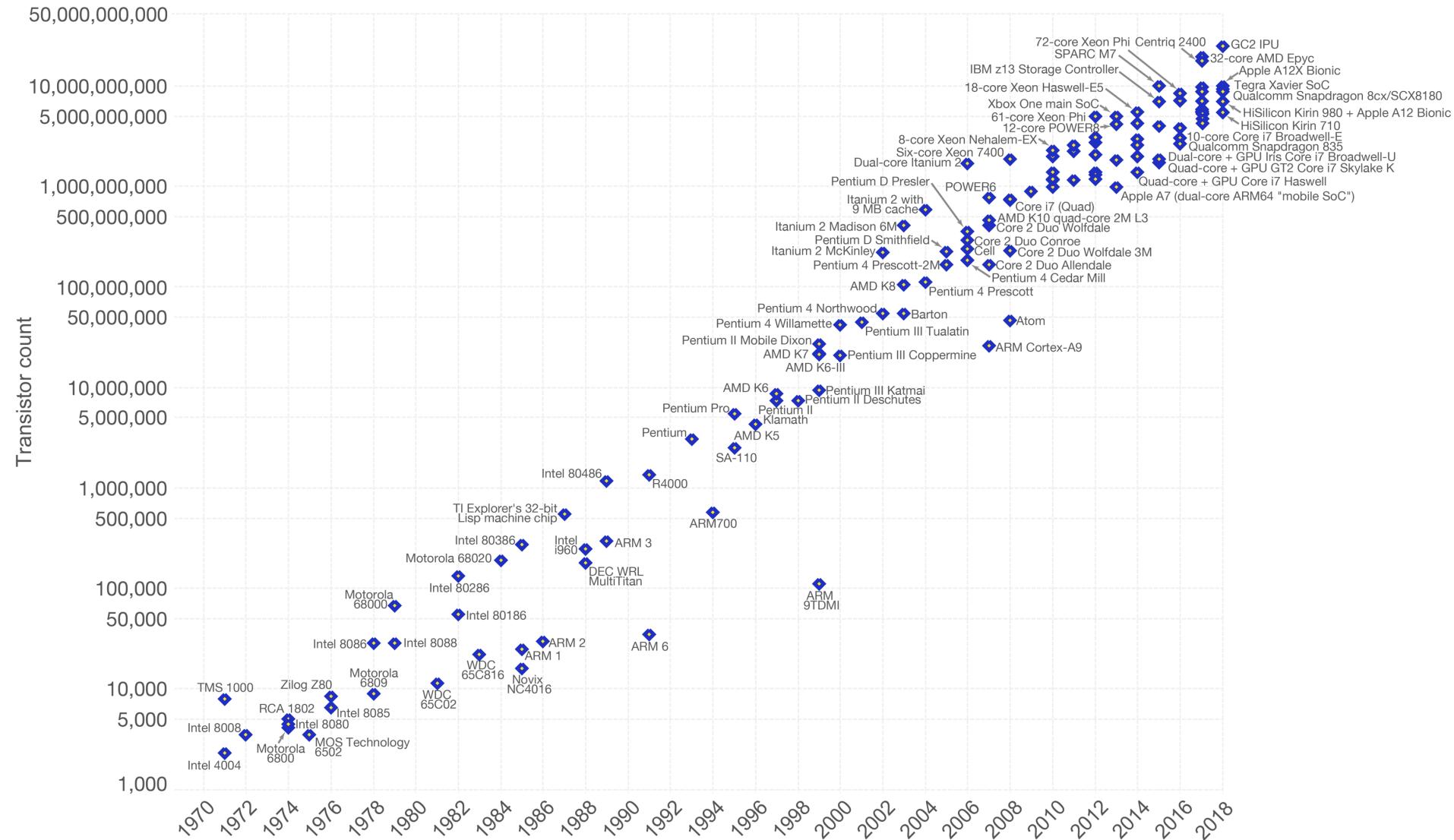
# SCALE DOWN BENEFITS



- 8 cores instead of 2 using the same space
- 3 times faster
- 10 times less power consumption

# Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.



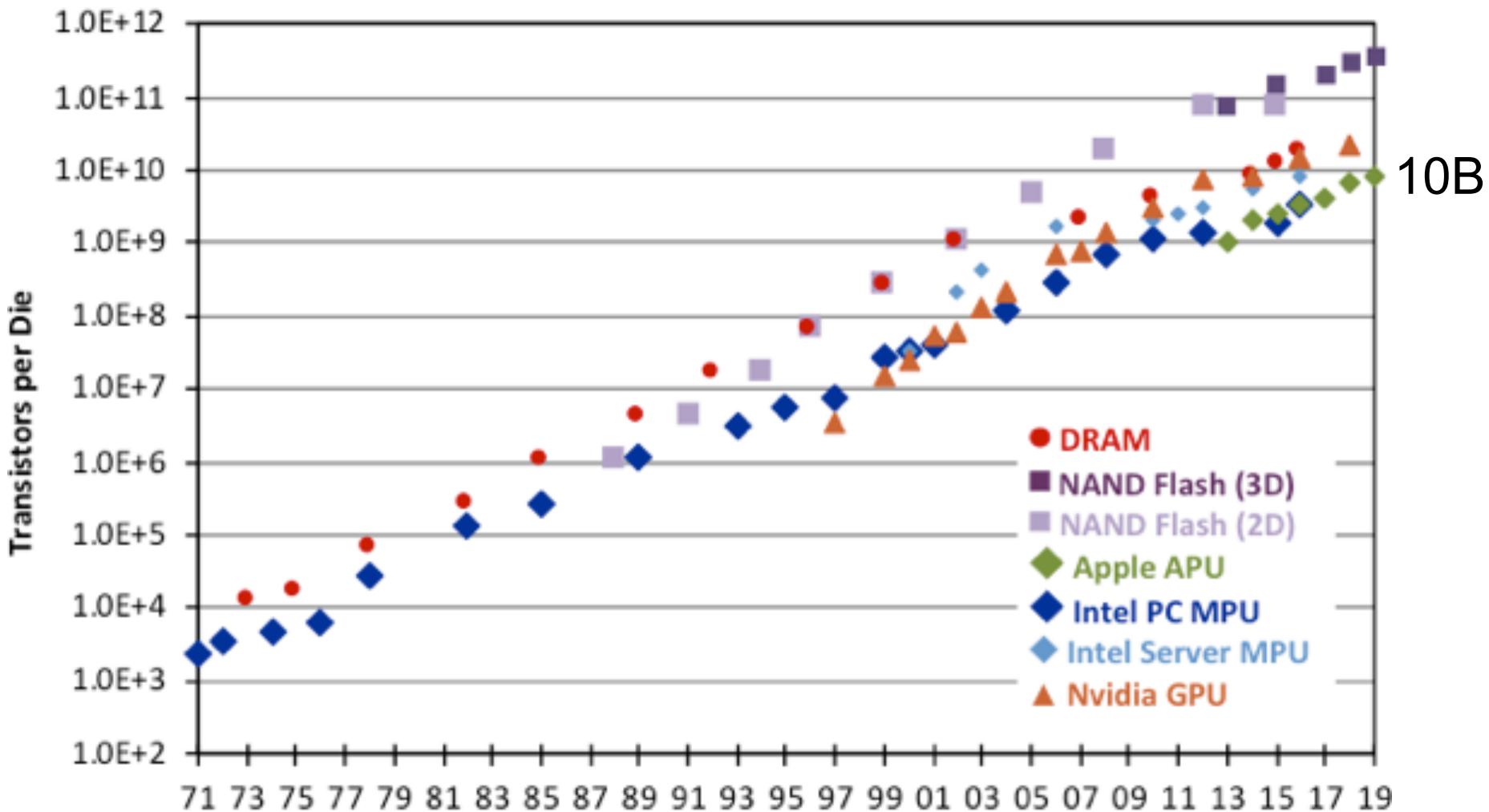
Data source: Wikipedia ([https://en.wikipedia.org/wiki/Transistor\\_count](https://en.wikipedia.org/wiki/Transistor_count))

The data visualization is available at [OurWorldInData.org](http://OurWorldInData.org). There you find more visualizations and research on this topic.

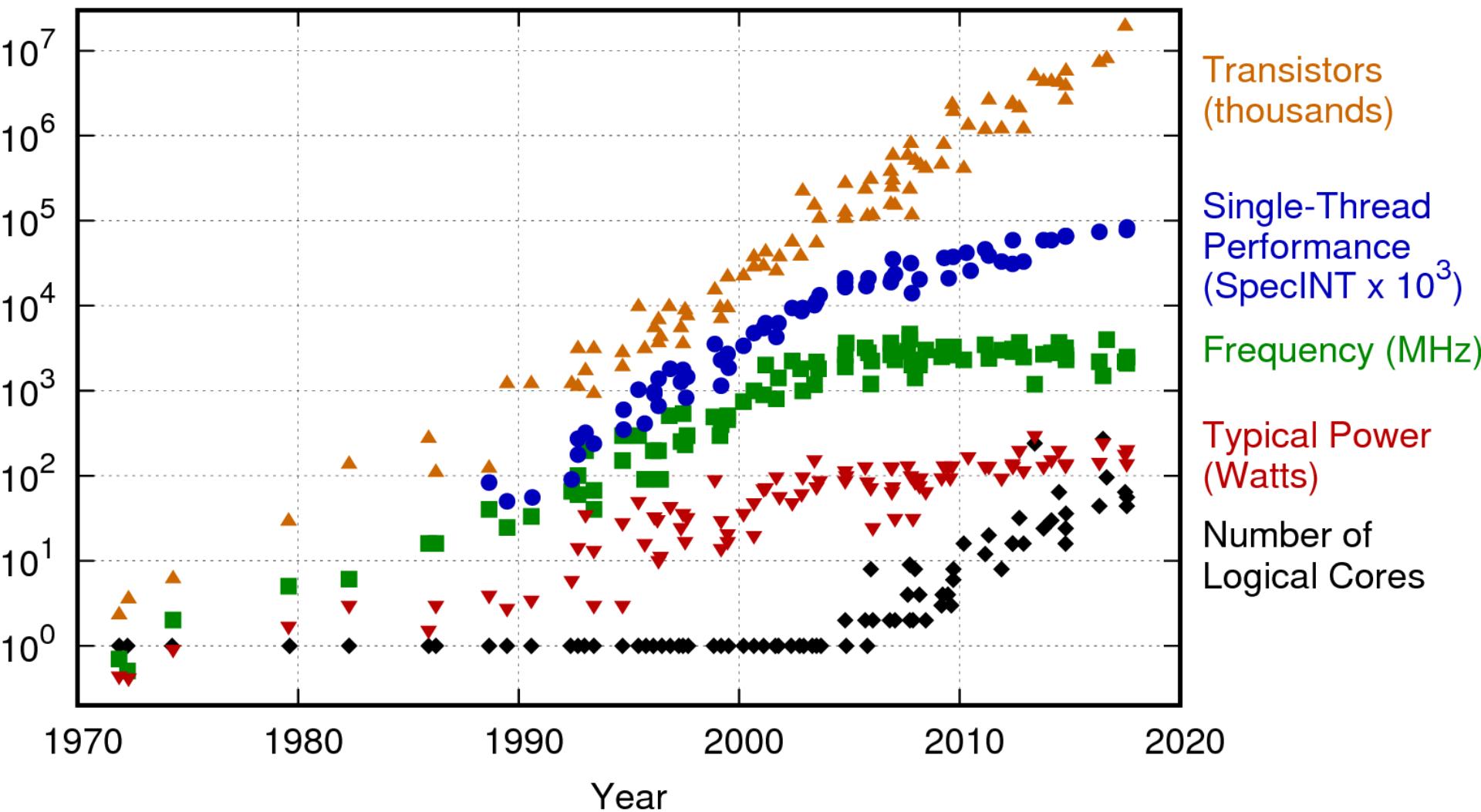
Licensed under CC-BY-SA by the author Max Roser.

# Ainda Lei de Moore (atual - 2020)

## Transistor Count Trends



# 42 Years of Microprocessor Trend Data



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten  
New plot and data collected for 2010-2017 by K. Rupp

<https://www.karlrupp.net/wp-content/uploads/2018/02/42-years-processor-trend.png>

# Dennard Scaling

- Dennard (1974) observou que a tensão e a corrente devem ser proporcionais às dimensões lineares de um transistor
  - Assim, conforme os transistores encolheram, também diminuíram a tensão e a corrente necessárias; **a potência é proporcional à área do transistor.**
- Final da “lei de Dennard”

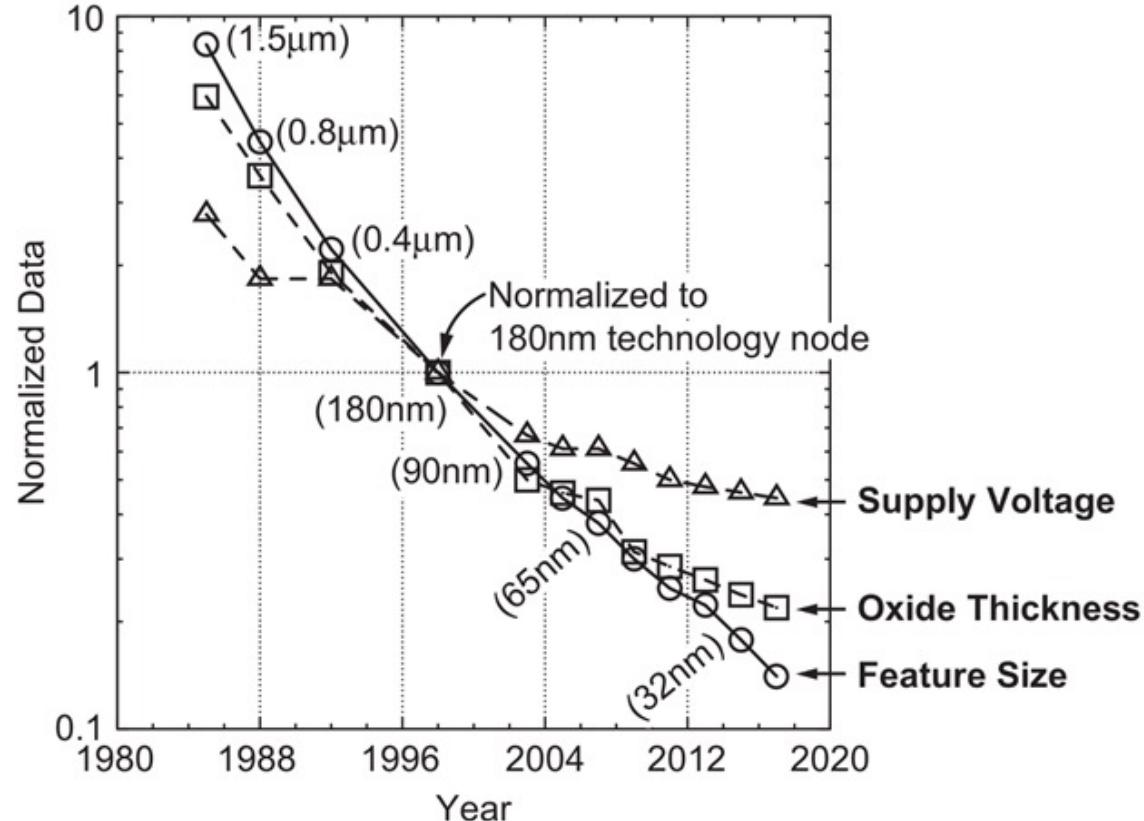
$$P = \alpha \cdot C \cdot F \cdot V^2$$

$\alpha$  - percent time switching

C - capacitance

F – frequency

V - voltage

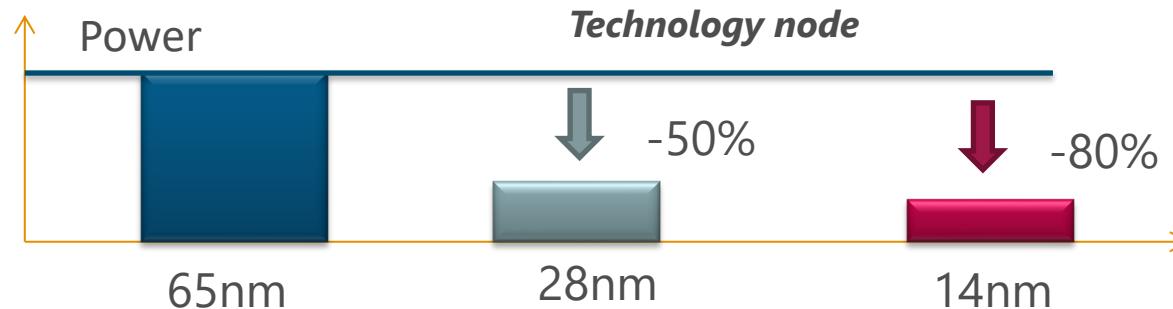
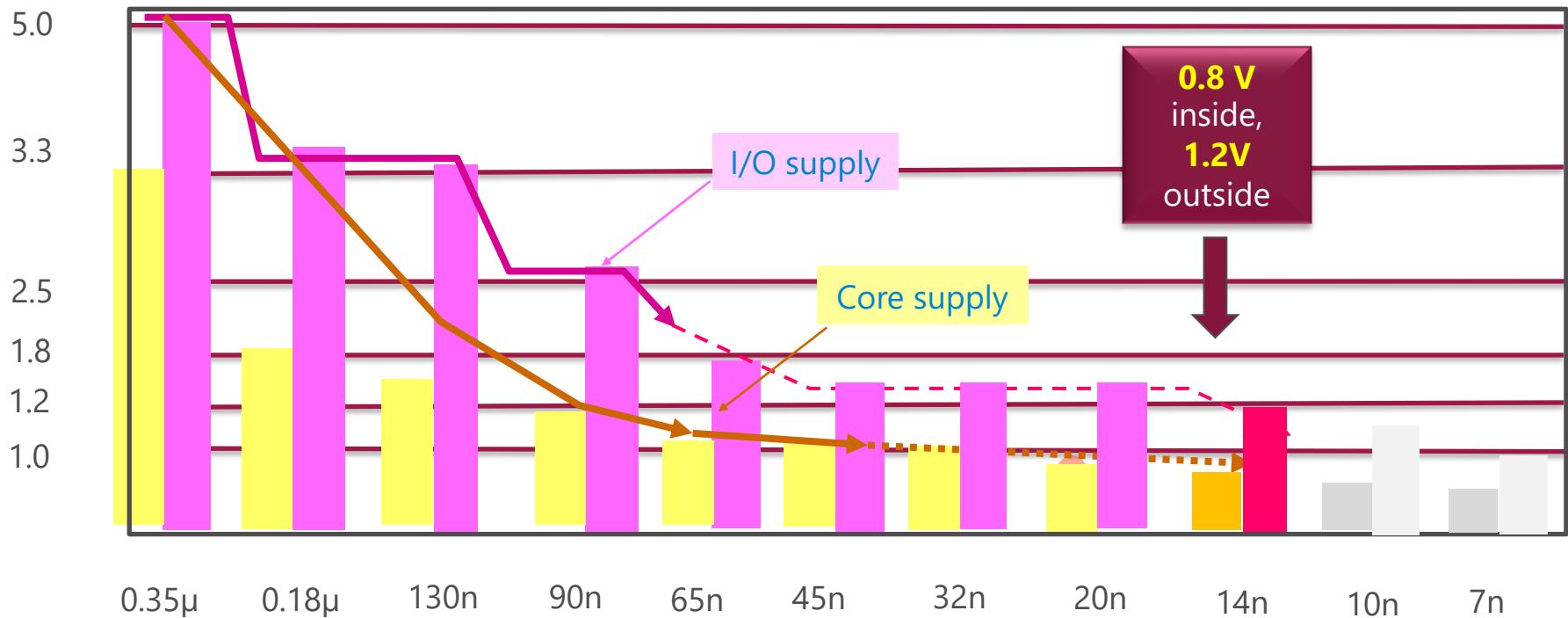


# Tensão de alimentação e potência

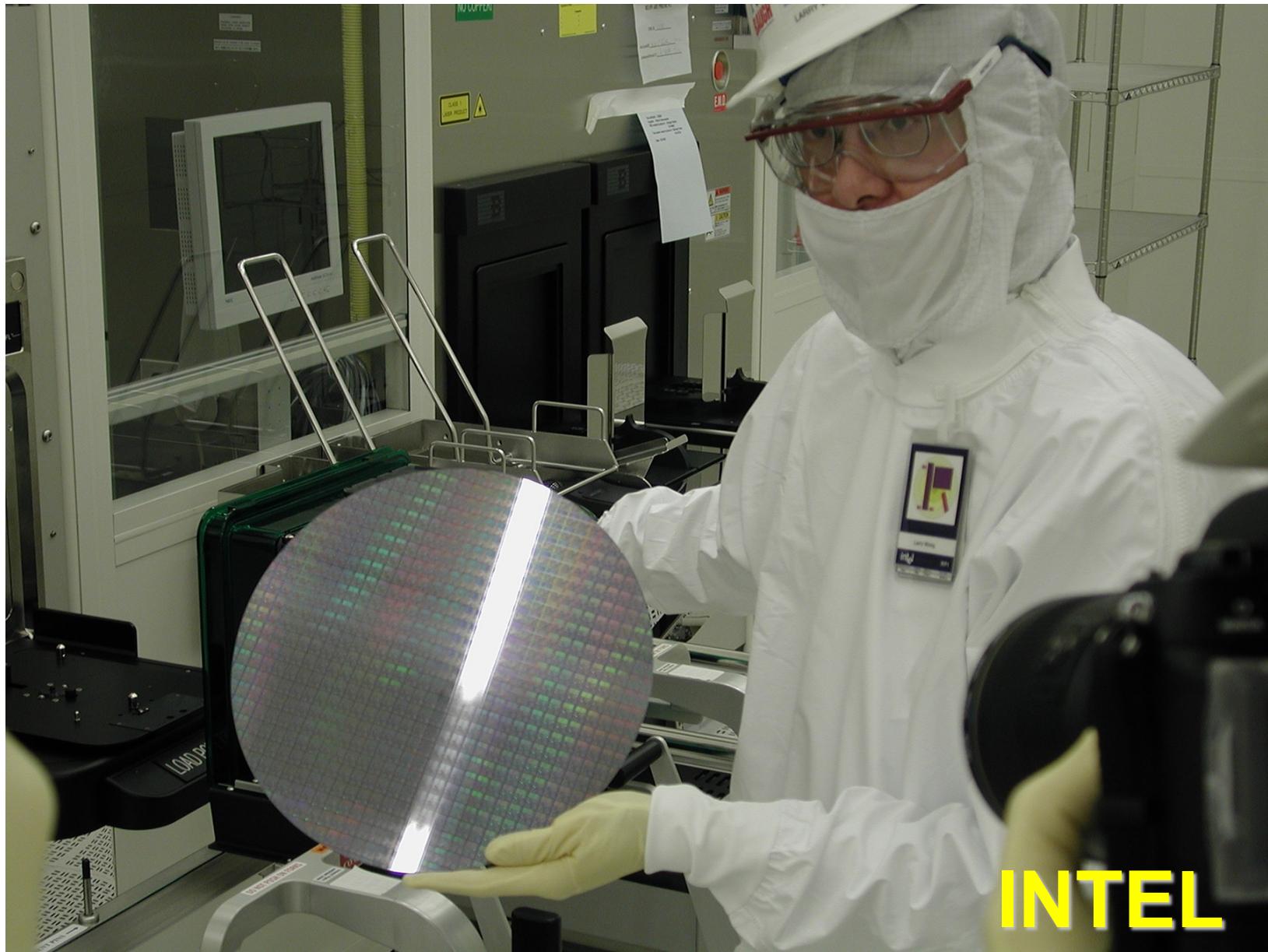
- The supply is lowered below 1V

Supply (V)

14-nm technology

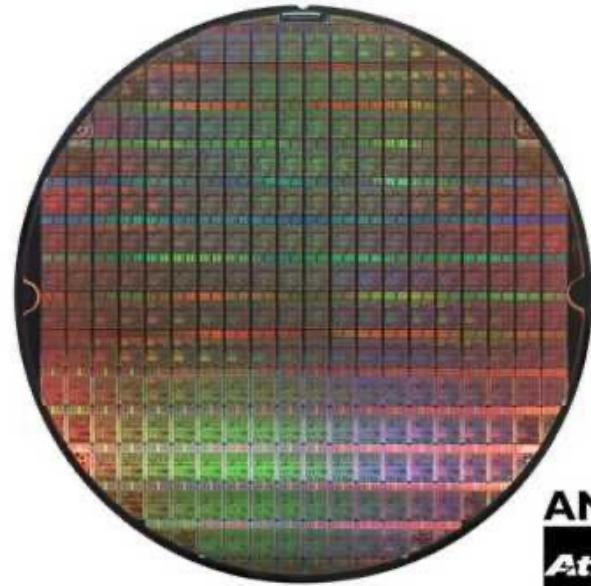
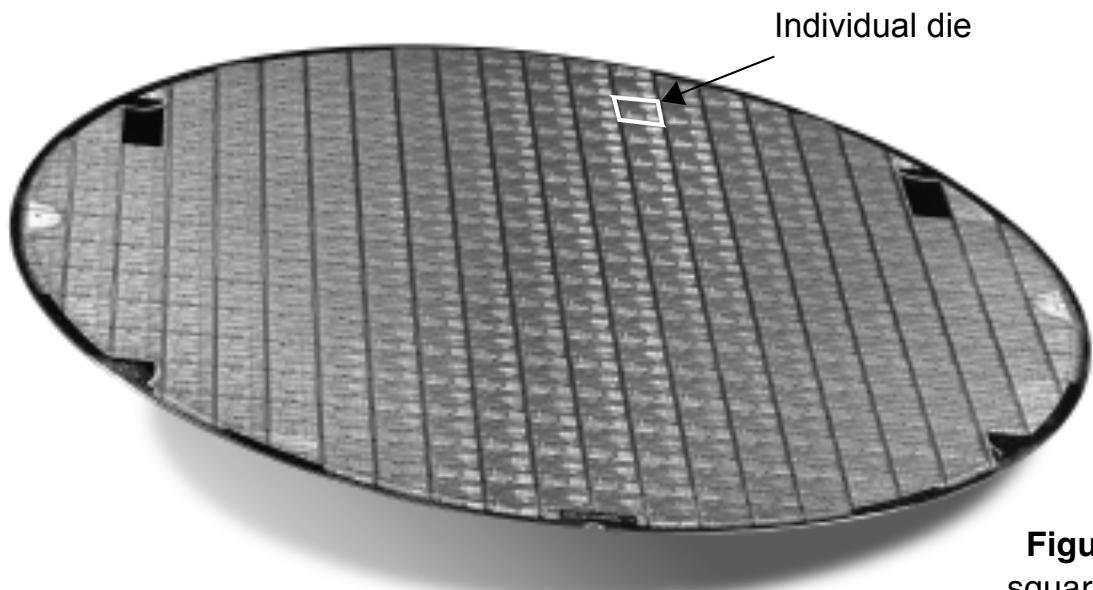


# Silicon Wafer and Dies



**INTEL**

# Silicon Wafer and Dies

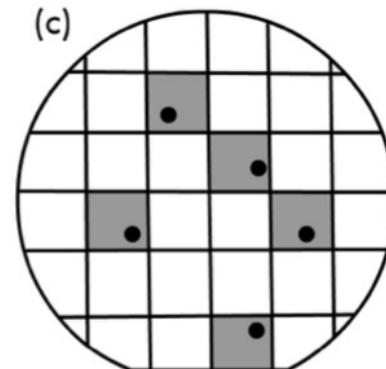
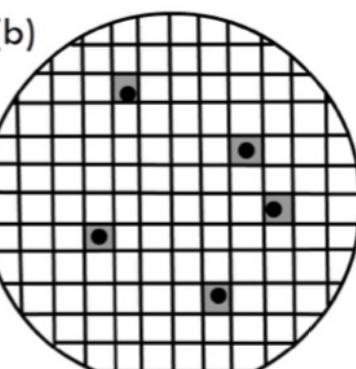
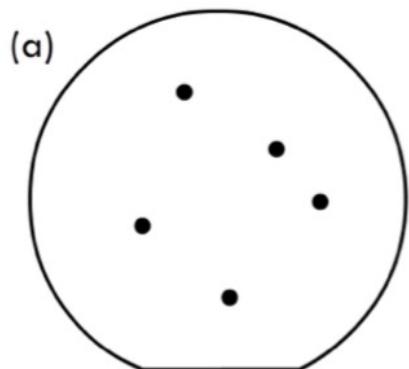


**Figure 1.9** Finished wafer. Each square represents a die - in this case the AMD Duron™ microprocessor (Reprinted with permission from AMD).

# Yield

$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$



# Defects = 5

# Defects = 5

# Defects = 5

$$\text{Yield} = \frac{138 - 5}{138} = 96\%$$

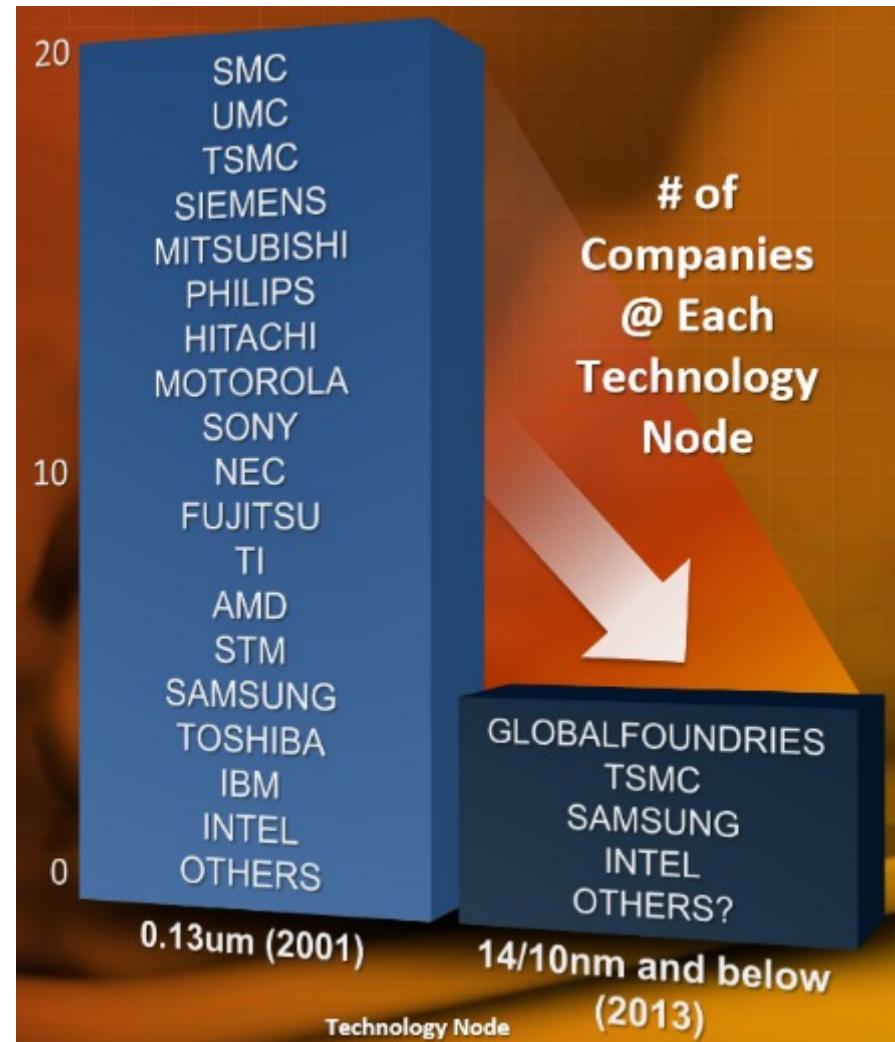
$$\text{Yield} = \frac{16 - 5}{16} = 69\%$$

# Some Examples

Chip	Metal layers	Line width	Wafer cost	Def./ cm <sup>2</sup>	Area mm <sup>2</sup>	Dies/wafer	Yield	Die cost
386DX	2	0.90	\$900	1.0	43	360	71%	\$4
486 DX2	3	0.80	\$1200	1.0	81	181	54%	\$12
Power PC 601	4	0.80	\$1700	1.3	121	115	28%	\$53
HP PA 7100	3	0.80	\$1300	1.0	196	66	27%	\$73
DEC Alpha	3	0.70	\$1500	1.2	234	53	19%	\$149
Super Sparc	3	0.70	\$1700	1.6	256	48	13%	\$272
Pentium	3	0.80	\$1500	1.5	296	40	9%	\$417

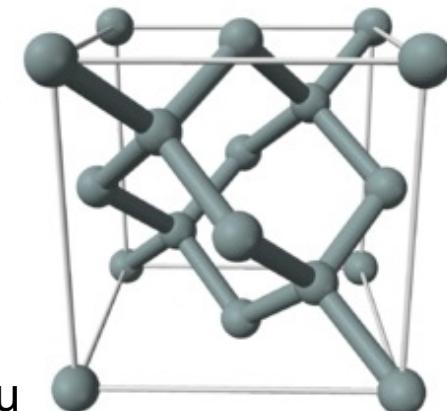
# TECHNOLOGY INNOVATION & COST

- Less and less companies in the 14-nm market
- 3 companies in 10-nm market
- 3 companies in 7-nm?
- 2 companies in 5-nm?



# Materiais Semicondutores

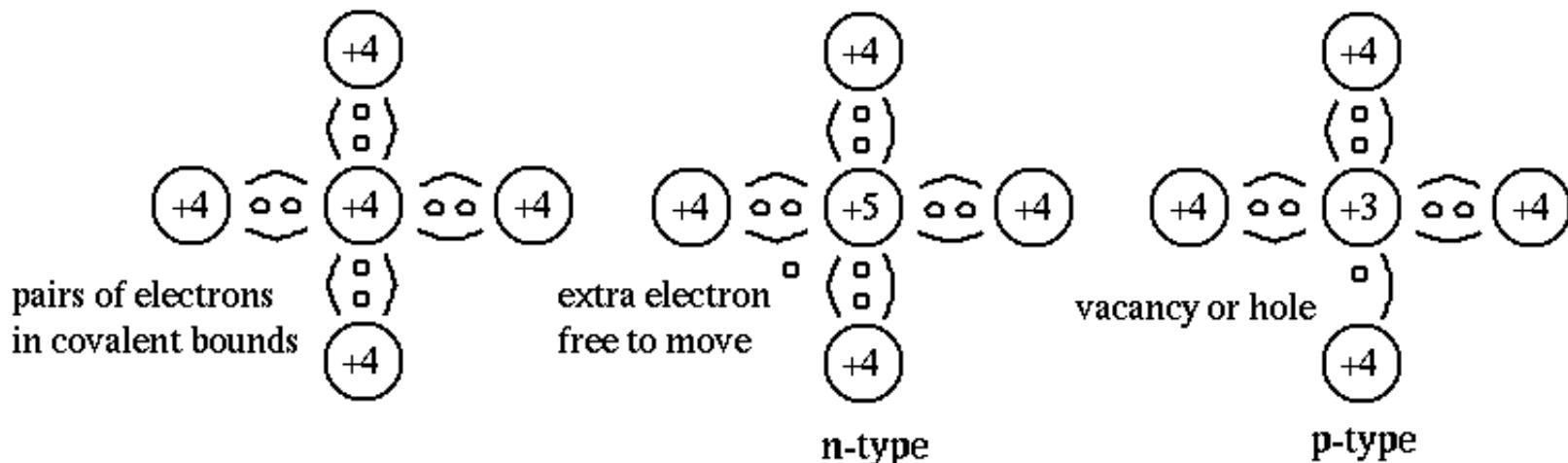
- 4 elétrons na última camada – **valência 4**
- condutividade desses elementos com valência 4 não é tão boa quanto os condutores mas ainda melhor do que os isolantes
- os dois semicondutores de grande importância são o **silício** e e **germânio**
- cristal estrutura cristalina tem um padrão tetraédrico com cada átomo → **silício monocristalino**
- um elétron ganha energia térmica suficiente (1,1 eV para Si ou 0,7 eV para Ge), ele pode quebrar a ligação covalente e torna-se **um elétron livre da carga negativa, deixando uma vaga ou um buraco de carga positiva**
- Sob um campo elétrico, um elétron livre pode mover-se para um novo local para preencher um buraco ali, ou seja, tanto esses elétrons e buracos contribuem para condução elétrica
- à **temperatura ambiente**, relativamente poucos elétrons ganham energia suficiente para tornar-se elétrons livres, logo a condutividade de tais materiais é baixo, desse modo estes materiais recebem o nome de **semicondutores**



# Mat. Semicond. Dopados

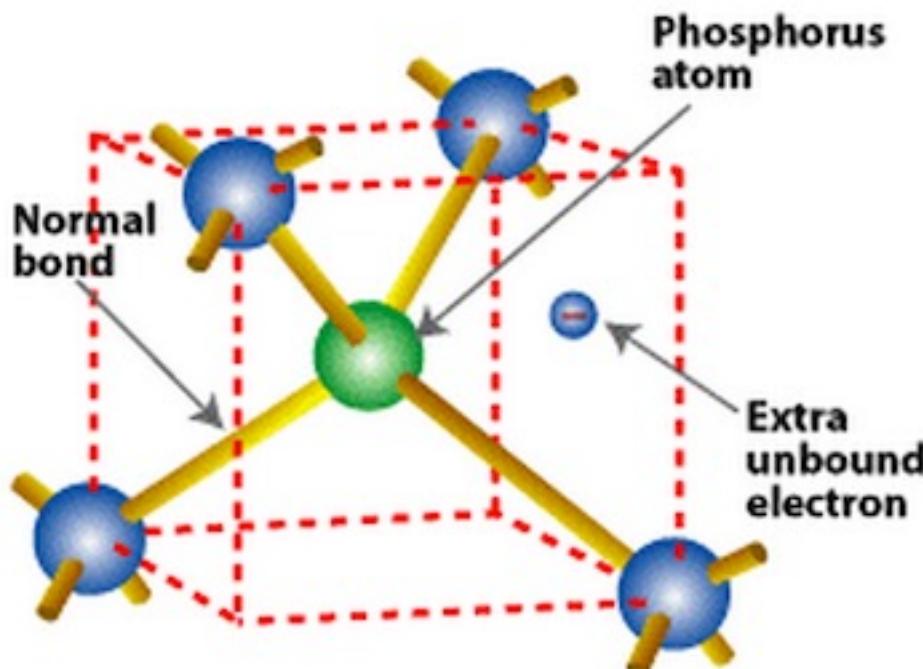
- a condutividade dos materiais semicondutores pode ser melhorada através de dopagem, ou seja, adicionando um elemento de impureza com valência três ou cinco
- silício puro: semicondutor **intrínseco**
- silício dopado: semicondutor **extrínseco**

5 BORON	6 CARBON	7 NITROGEN
13 ALUMINUM	14 SILICON	15 PHOSPHORUS
31 GALLIUM	32 GERMANIUM	33 ARSENIC
49 INDIUM	50 TIN	51 ANTIMONY



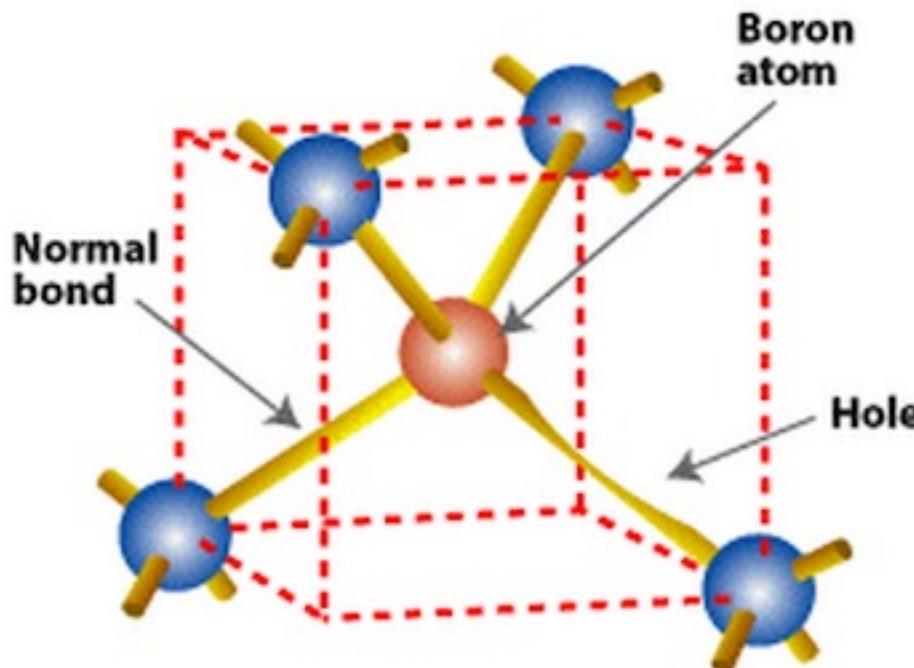
# Semicondutores Tipo N

- quando uma pequena quantidade de átomos com **valência 5** (por exemplo, o fósforo (P) ou o arsénico (As)) são adicionados, um átomo de silício na estrutura cristalina é substituído por um átomo **doador** com quatro de seus elétrons de valência formando os limites de ligações e um elétron extra livre
- Esta dopagem caracteriza um **semicondutor do tipo N**, com condutividade muito melhor em comparação com os semicondutores intrínsecos



# Semicondutores Tipo P

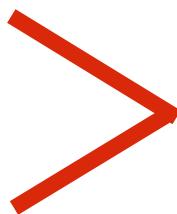
- quando uma pequena quantidade de átomos com valência 3 (por exemplo, o boro (B) ou o alumínio(Al)) são adicionados, um átomo de silício na estrutura cristalina é substituído por um átomo **receptor** com três de seus elétrons de valência formando os limites, ocorrendo a formação de um “**buraco**”
- Esta dopagem caracteriza um **semicondutor do tipo P**, com condutividade muito melhor em comparação com os semicondutores intrínsecos



# Materiais Semicondutores

Mobilidade dos elétrons

$$\mu_n$$



Mobilidade dos buracos

$$\mu_p$$

OBS: Cerca de 3 vezes para o silício e 30 vezes para o AsGa

**Resistividade:** capacidade de um material veicular corrente

**depende:** - concentração de portadores (temperatura, dopagem)  
- mobilidade dos portadores no material

**Dopantes:** átomos com excesso de elétrons ou de buracos

dopantes do **tipo P**: falta de elétrons

dopantes do **tipo N**: excesso de elétrons

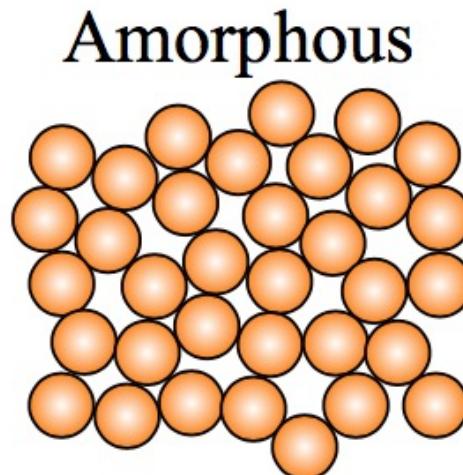
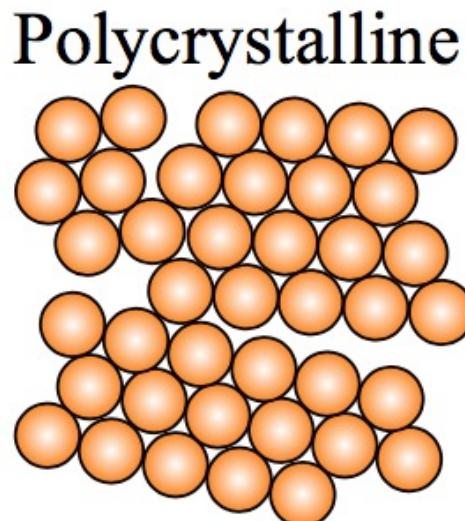
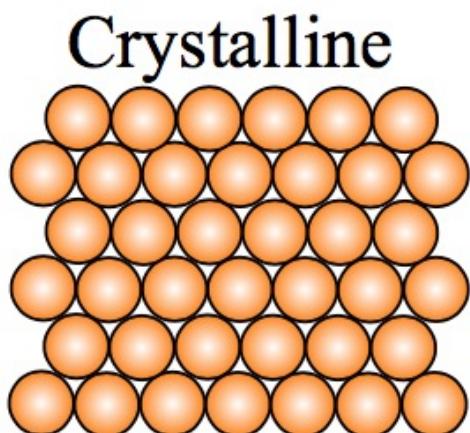
exemplo: **boro**

exemplo: **fósforo**

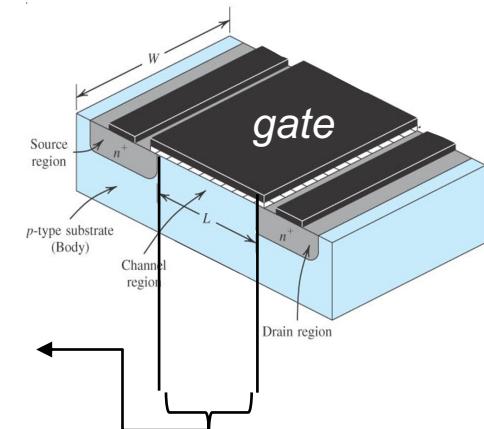
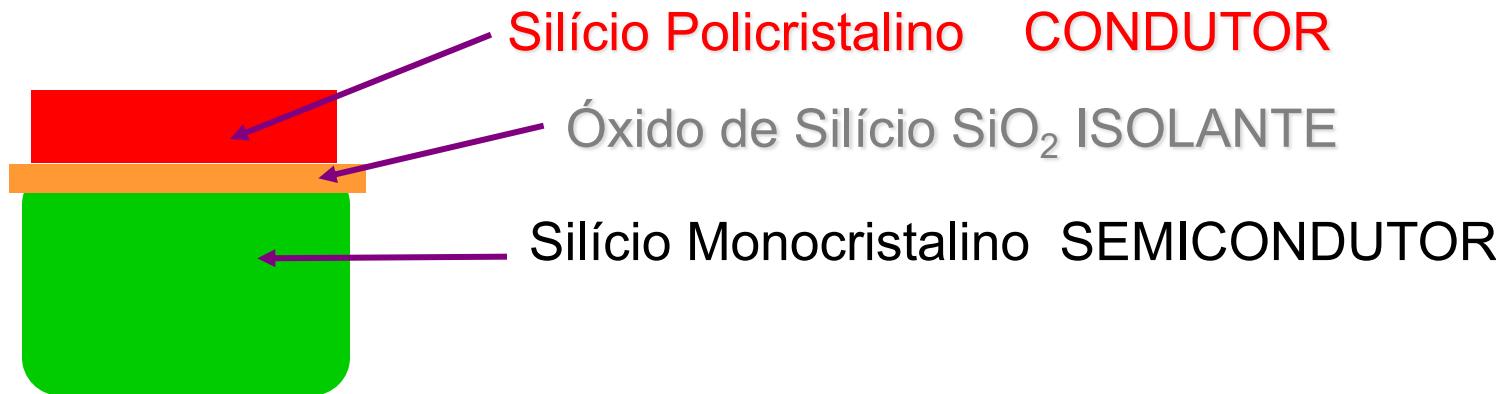
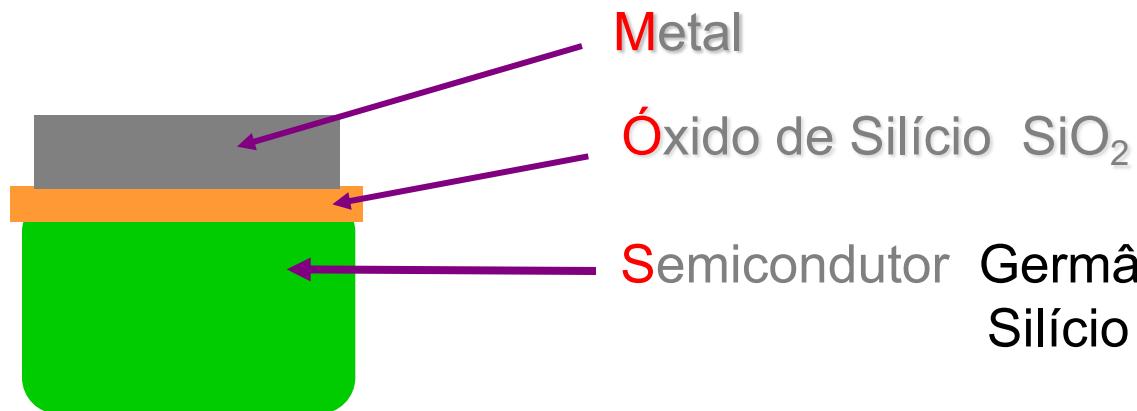
# Arranjos atômicos

- **Microscopicamente**

- um único cristal tem átomos em um arranjo periódico quase perfeita
- um "polycrystal" é composto por muitos cristais microscópicos
- um sólido amorfó (tais como o vidro) não tem nenhum arranjo periódico mesmo microscopicamente

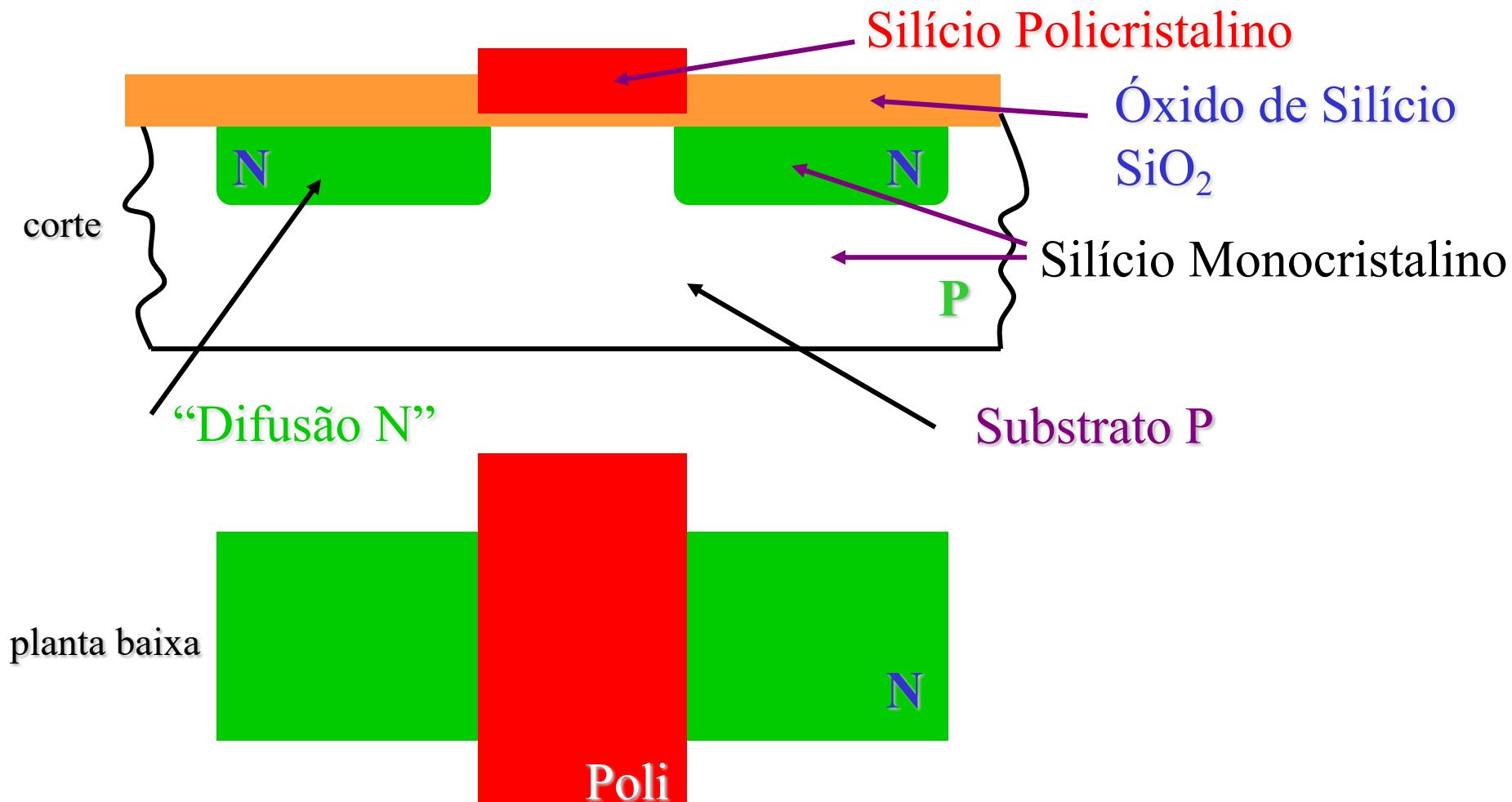
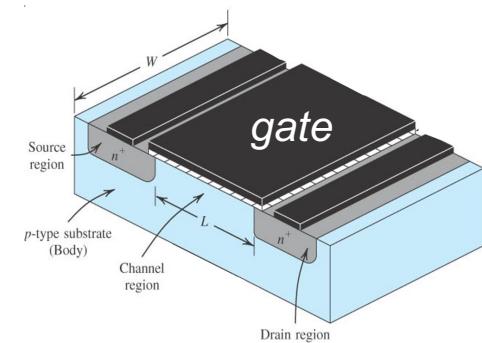


# Transistor MOS

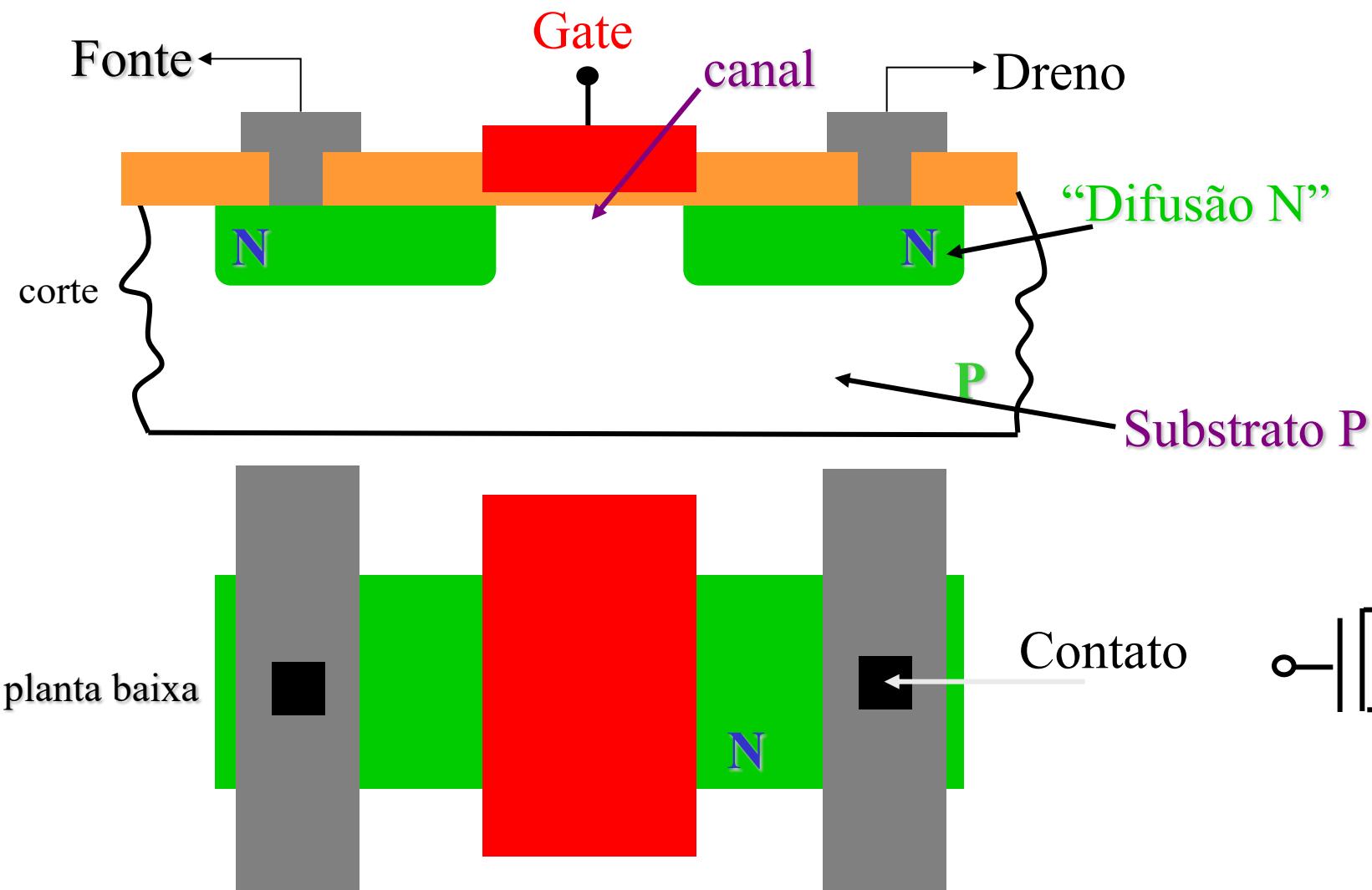


- condutividade elétrica do polisilício (ou **poli**) pode ser aumentada mediante depósito de metal (como tungstênio) ou um siliceto de metal (tais como siliceto de tungstênio). **Poli** pode também ser empregado como um resistor ou um capacitor.

# Transistor MOS

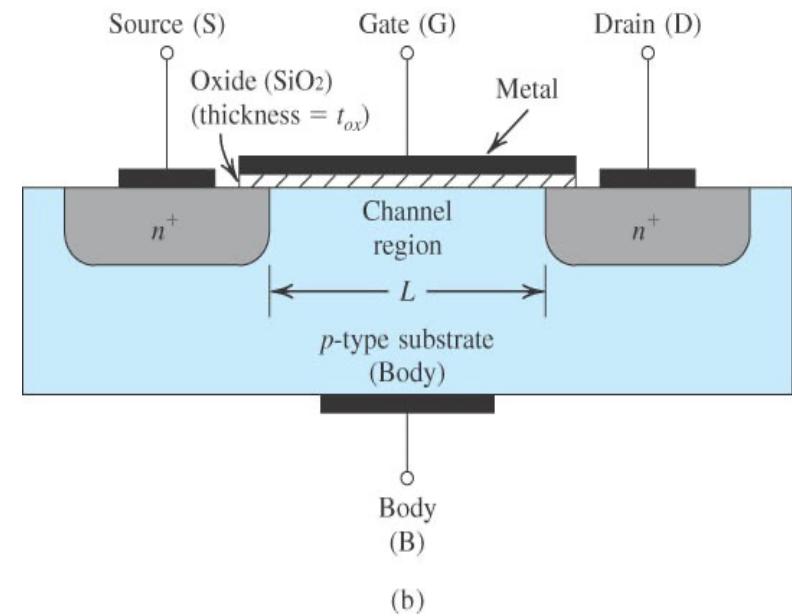
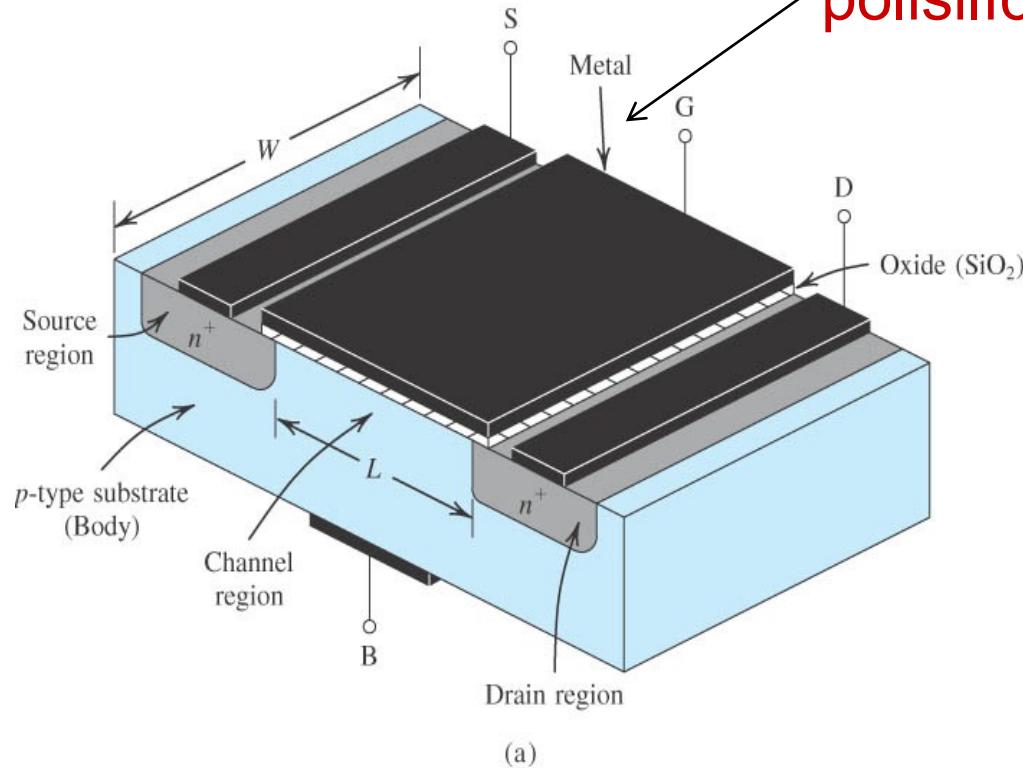


# Transistor MOS



# Transistor MOS

Hoje: gate é implementado com polisilício, mas voltando para metal



**Se:**

$$L = 0,065 \mu\text{m}$$

$$W = 0,8 \mu\text{m}$$

$$C_{\text{ox}} = 18,367 \text{ fF}/\mu\text{m}^2$$

**Notar:**

**Dispositivo com  
4 terminais**

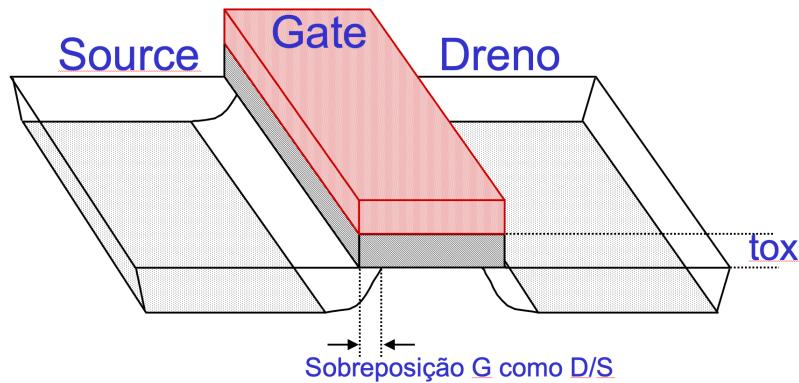
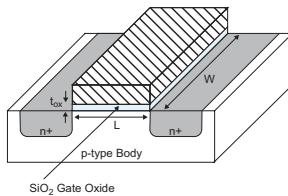
$$C_g = 0,96 \text{ fF}$$

# Transistor MOS

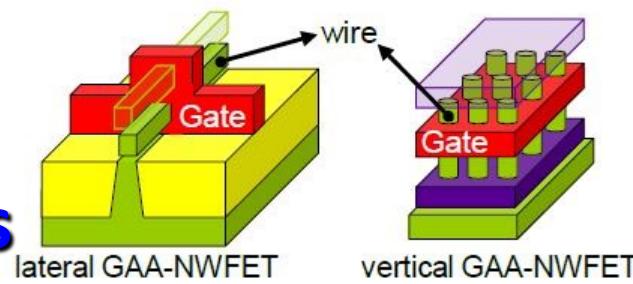
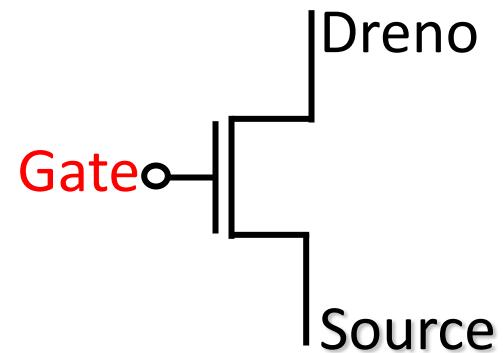
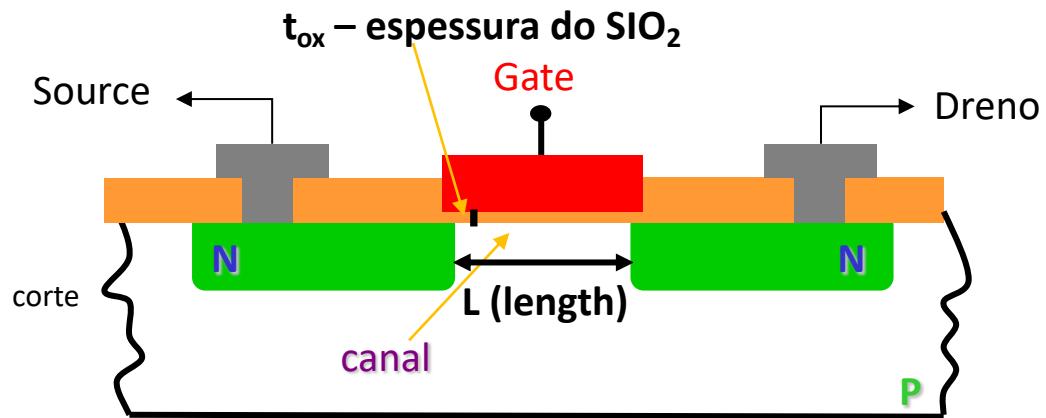
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

is oxide capacitance per unit area

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} \text{ F/m}$$



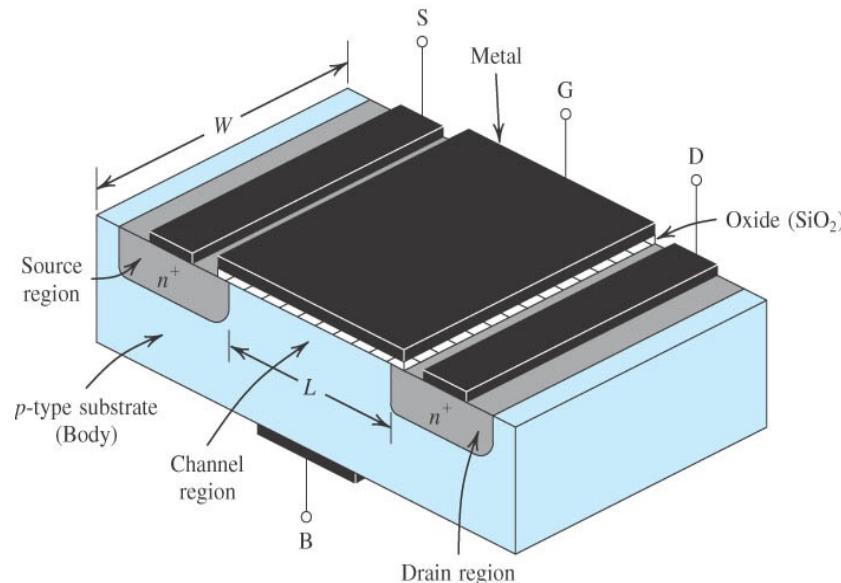
$$\beta \approx \frac{\mu}{t_{ox}} \cdot \frac{W}{L} \quad \text{ou} \quad \beta \approx \mu \cdot C_{ox} \cdot \frac{W}{L}$$



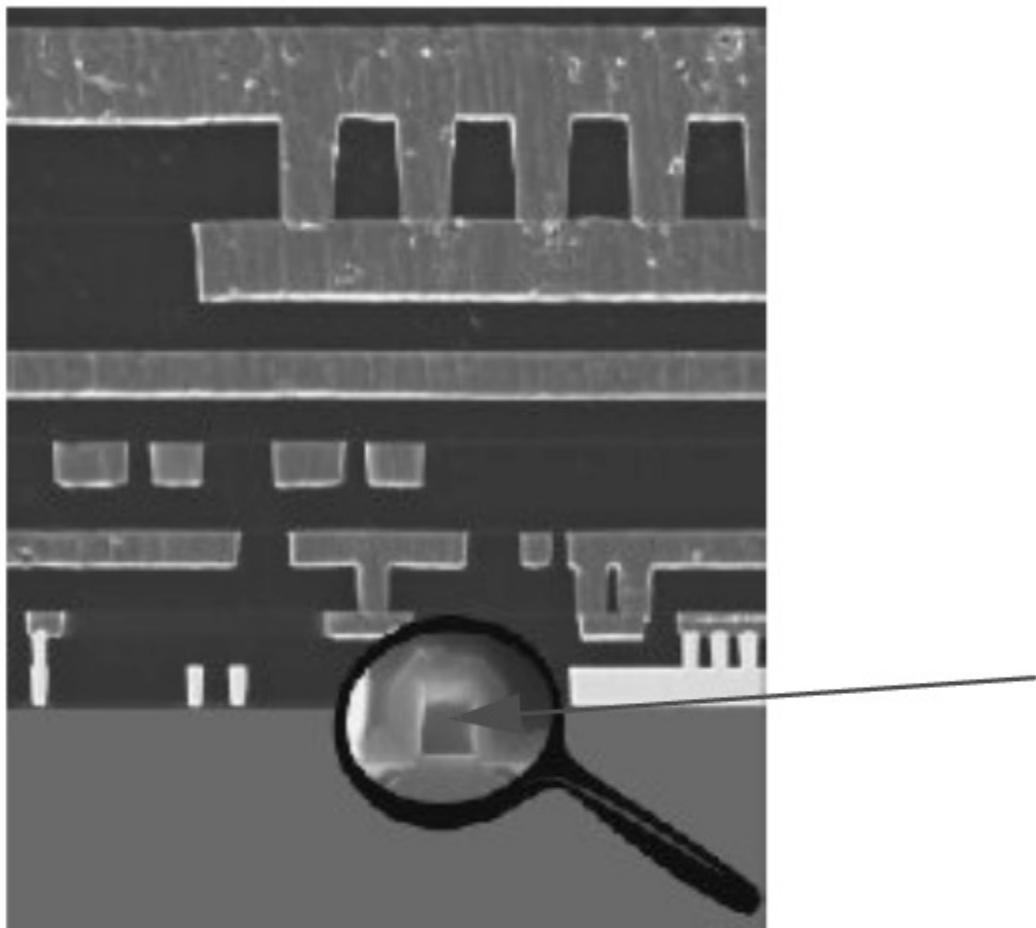
## Evolução dos dispositivos

# Explique na tabela abaixo a influência dos principais parâmetros do transistor MOS na corrente $I_{ds}$ (corrente dreno-source).

Parâmetro	Ação para <u>AUMENTAR</u> o $I_{ds}$ (duas respostas possíveis: aumentar ou diminuir)	Explicar a razão
W	<b>AUMENTAR</b>	<b>Maior</b> quantidade de portadores entre o dreno e source
L	<b>DIMINUIR</b>	<b>Menor</b> distância para os portadores percorrem
Mobilidade	<b>AUMENTAR</b>	Maior número de portadores livres
Espessura óxido	<b>DIMINUIR</b>	Aumenta a capacidade Cox



# Transistor MOS – Seção transversal

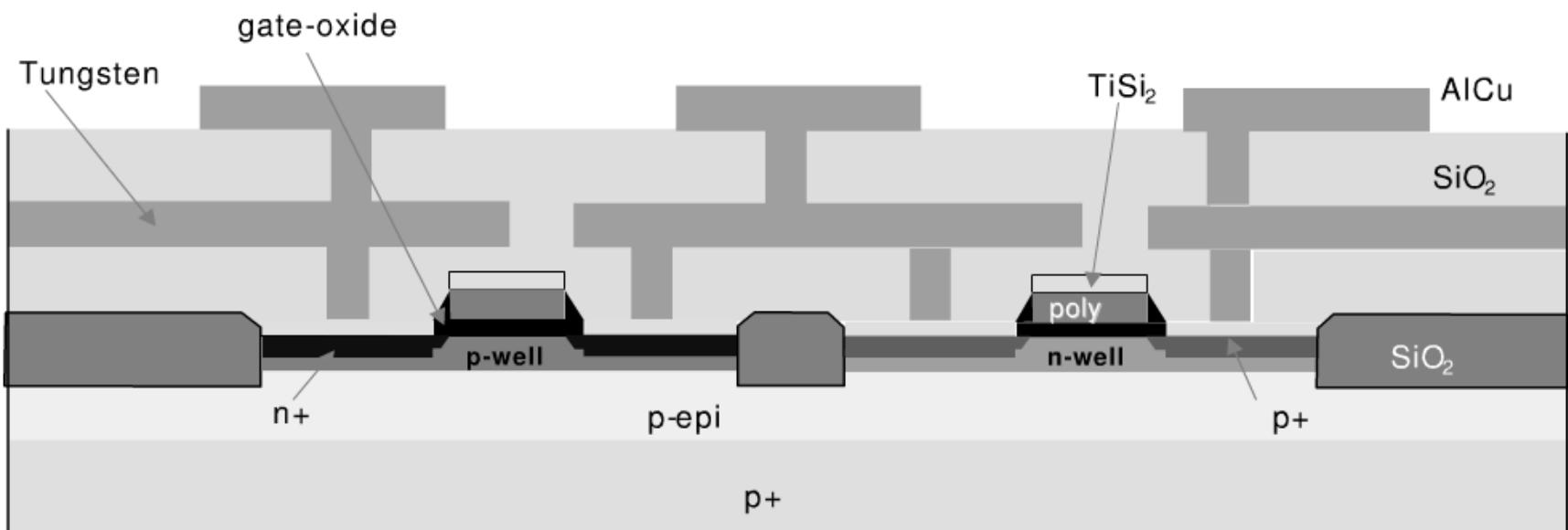


transistor

**Figure 2.8** Cross-section of state-of-the-art CMOS process.

Do livro texto, Rabaey, página 46

# Transistor MOS – Seção transversal



**Figure 3.11** Cross-section of contemporary dual-well CMOS process.

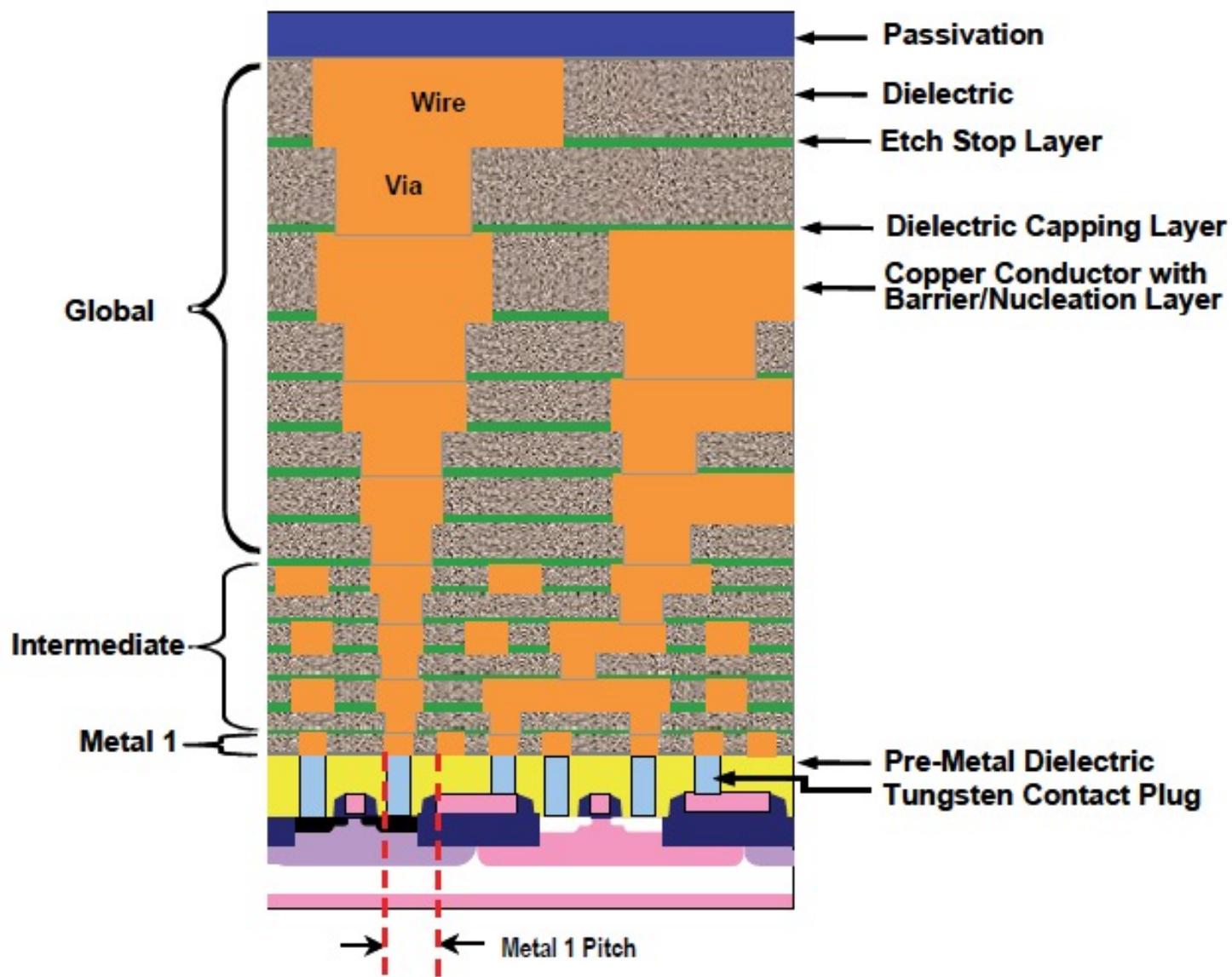
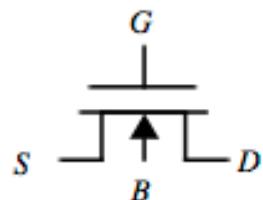


Figure INTC2 Cross-section of Hierarchical Scaling—MPU Device

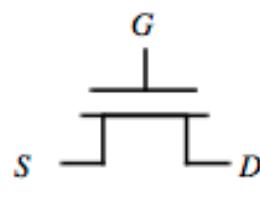
# MOS Transistors

- Dispositivo com 4 terminais

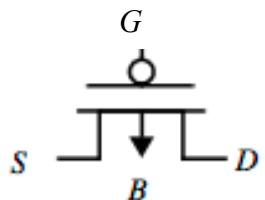
- Dreno, gate, source
- Bulk (poço) – polariza o substrato (normalmente omitido)



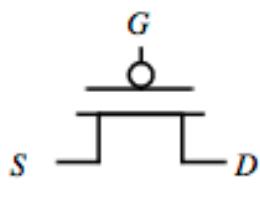
(a) NMOS transistor  
as 4-terminal device



(b) NMOS transistor  
as 3-terminal device



(a) PMOS transistor  
as 4-terminal device

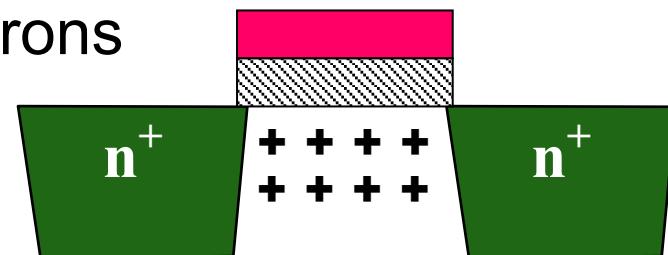


(d) PMOS transistor  
as 3-terminal device

Figure 3.12 Circuit symbols for MOS transistors.

# Transistor MOS - Princípio de Funcionamento

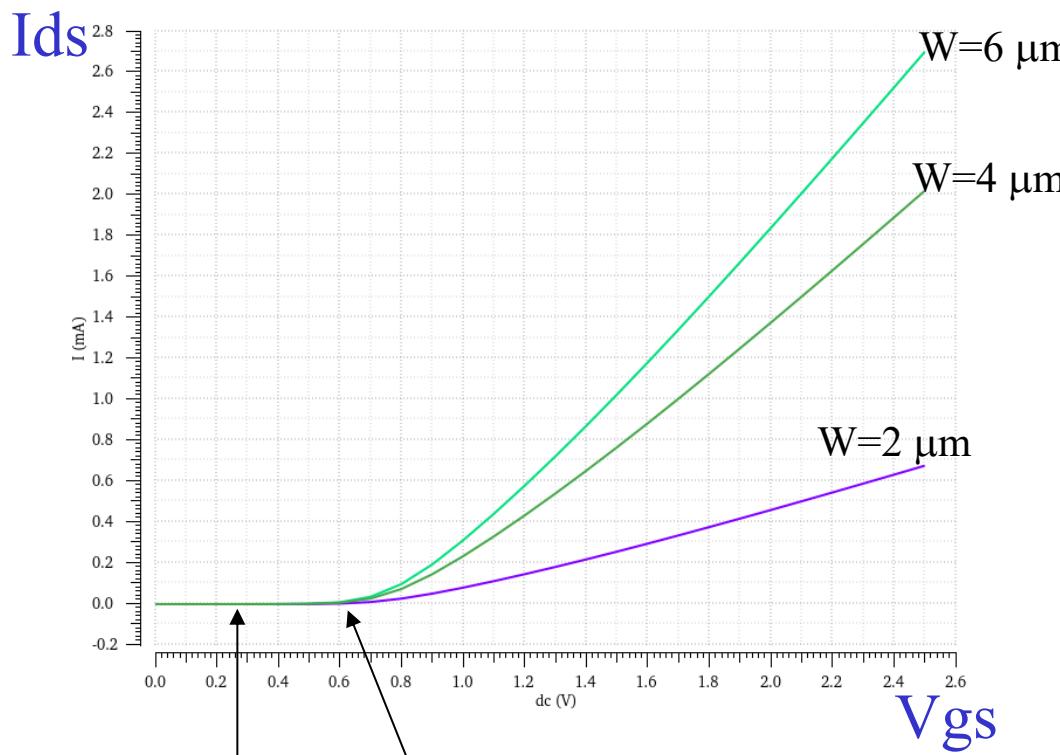
- Substrato P - alta concentração de “buracos” (cargas positivas)
- Regiões N - alta concentração de elétrons



- Chave controlada por tensão
- Devido ao isolamento entre gate e source/dreno praticamente não há corrente no gate
- **Tensão de threshold**
  - tensão a partir da qual o transistor começa a conduzir

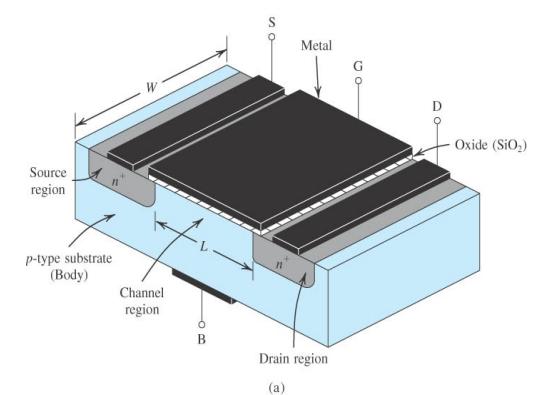
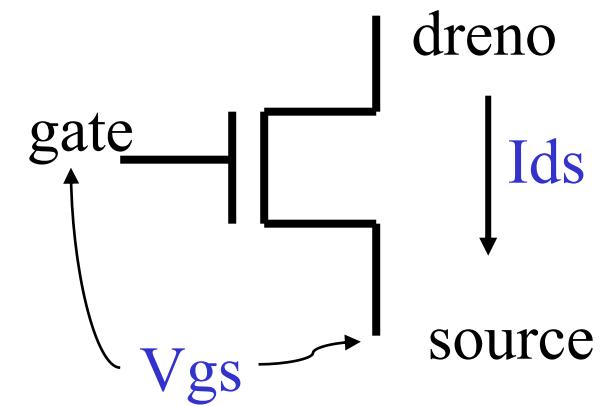
# Transistor MOS - Princípio de Funcionamento

Voltagem aplicada no gate, em relação ao source, aumenta o número de elétrons no canal, aumentando sua condutividade



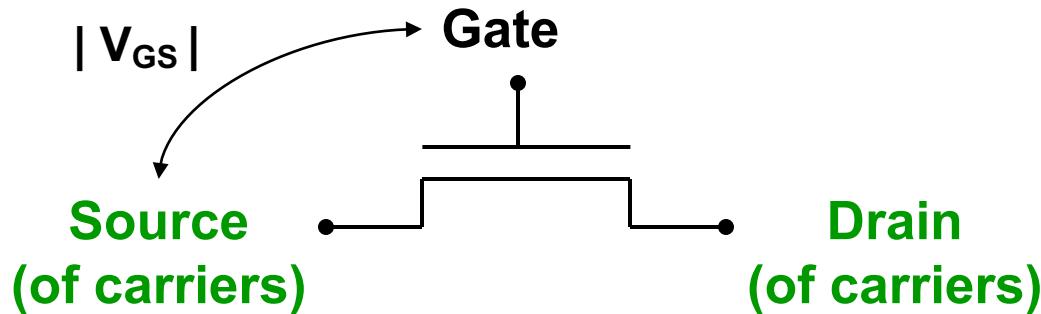
Corrente  $I_{ds} \sim n\text{A}$

$V_t$  (threshold): parâmetro da tecnologia

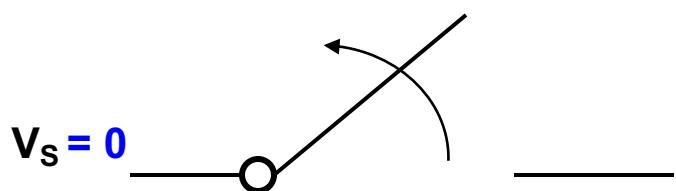


(a)

# Switch Model of NMOS Transistor



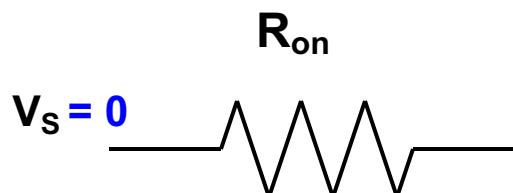
Open (off) (Gate = '0')



$$|V_{GS}| < |V_T|$$

$$|0| < |0,5| \\ 0 < 0,5 \rightarrow \text{cortado}$$

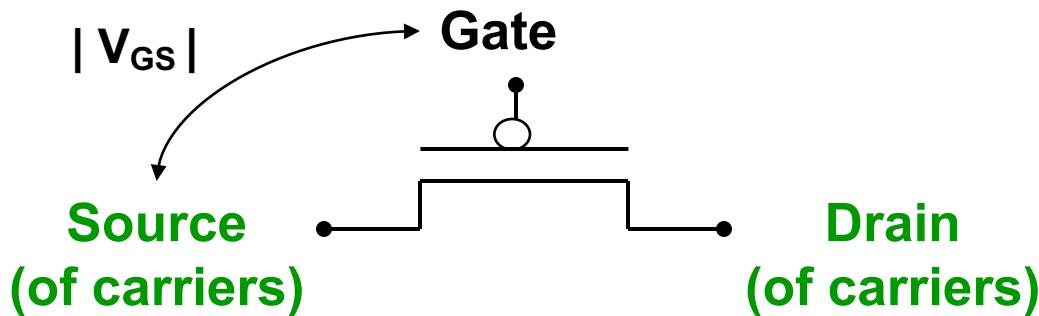
Closed (on) (Gate = '1')



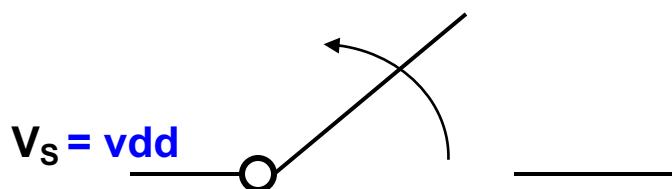
$$|V_{GS}| > |V_T|$$

$$|1,2| > |0,5| \\ 1,2 > 0,5 \rightarrow \text{fechado}$$

# Switch Model of PMOS Transistor



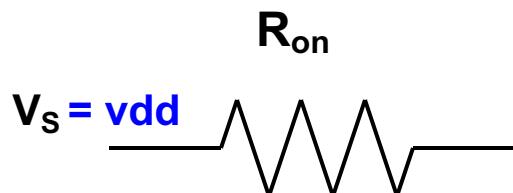
**Open (off) (Gate = '1')**



$$| V_{GS} | < | V_T |$$

$$\begin{aligned}V_{dd} &= 1,2 \\| 0 | &< | -0,5 | \\0 < 0,5 &\rightarrow \text{cortado}\end{aligned}$$

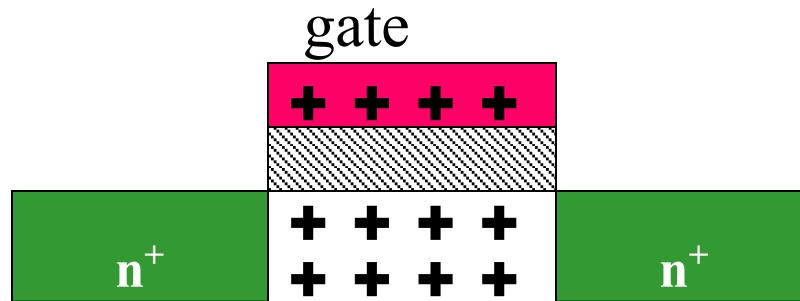
**Closed (on) (Gate = '0')**



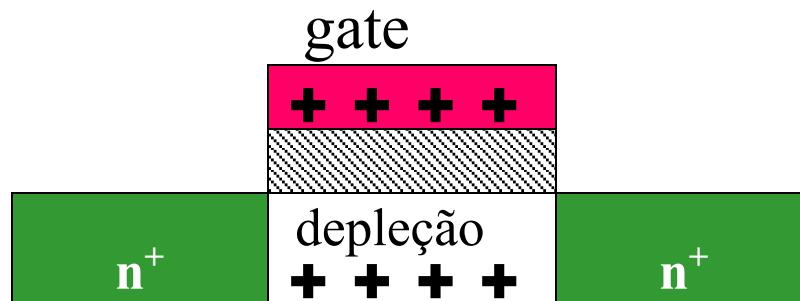
$$| V_{GS} | > | V_T |$$

$$\begin{aligned}V_{dd} &= 1,2 \\| -1,2 | &> | -0,5 | \\1,2 > 0,5 &\rightarrow \text{fechado}\end{aligned}$$

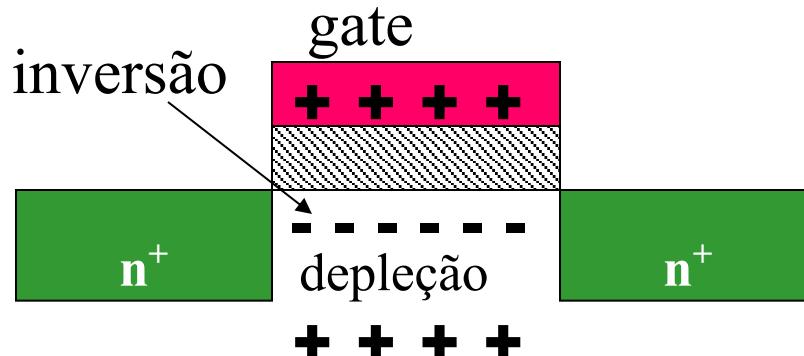
# Transistor MOS - Princípio de Funcionamento



- $V_{gs} \ll V_t$ 
  - cortado

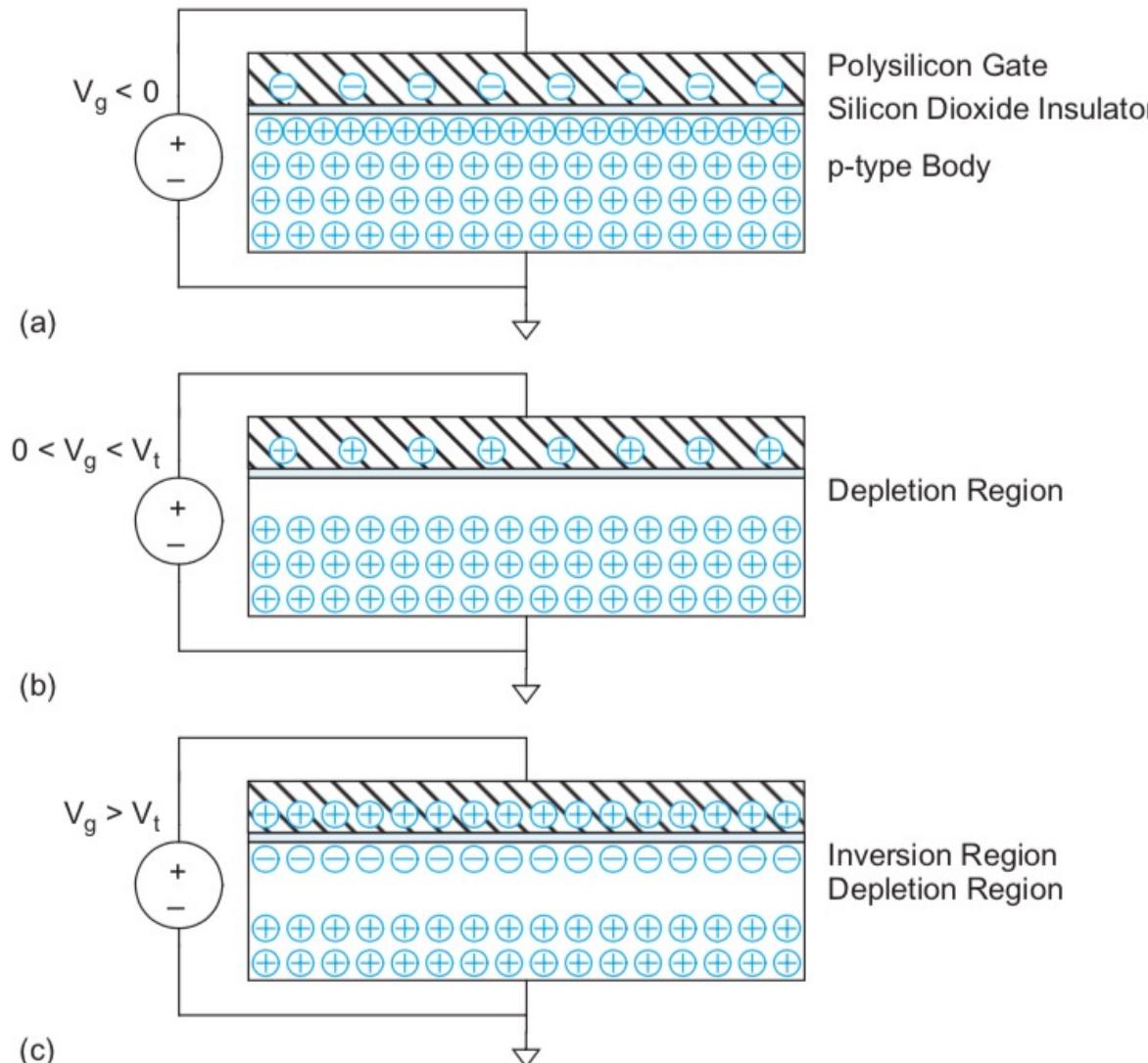


- $V_{gs} \approx V_t$ 
  - início da condução
  - zona depleção



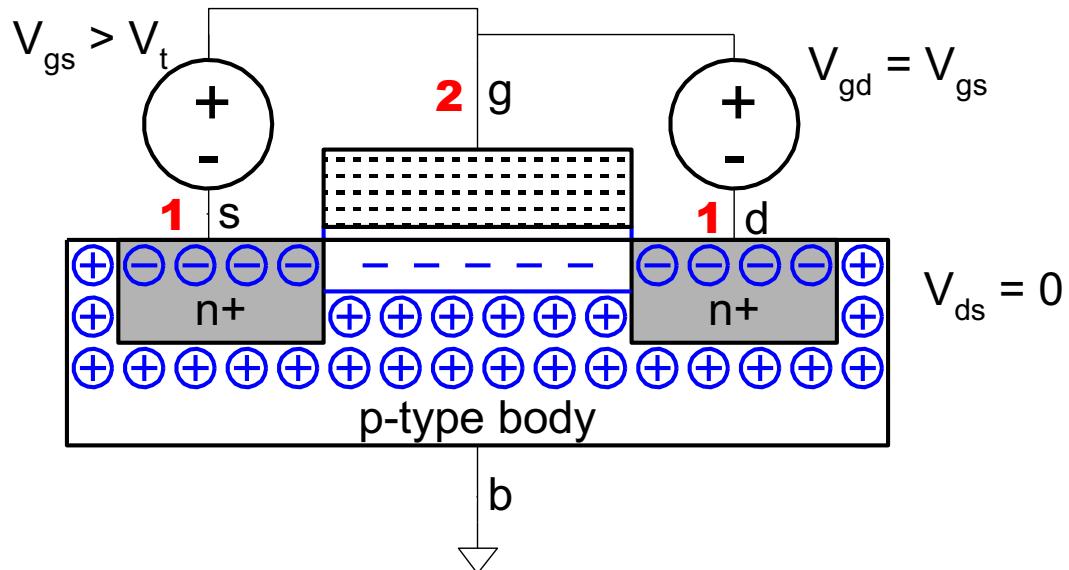
- $V_{gs} > V_t$ 
  - conduzindo
  - zonas lineares e saturado

# Transistor MOS - Princípio de Funcionamento



**FIGURE 2.2** MOS structure demonstrating (a) accumulation, (b) depletion, and (c) inversion

# NMOS linear (linear, resistivo, triodo)



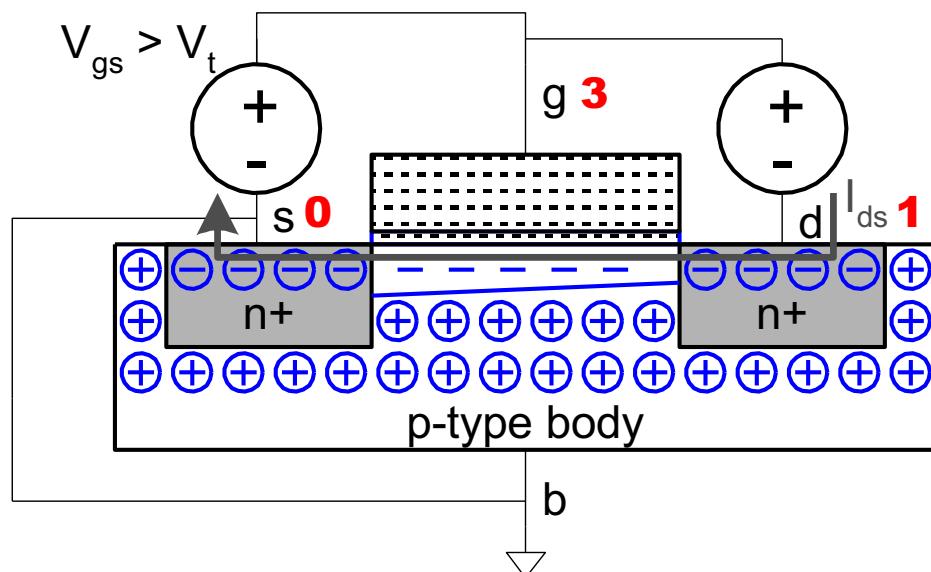
Formação do canal,  
mas sem corrente

Assumir  $V_{cc}=3$ ,  $V_t=0,5$ ,

$V_s=1$ ,  $V_g=2$ ,  $V_d=1$

Logo:

$V_{gd} = V_{gs}$ , sem corrente, mas  
com canal



Potencial no  
dreno maior que  
 $V_t$  implica em em  
 $I_{ds}$

$$1 \quad 2,5$$
$$0 < V_{ds} < V_{gs} - V_t$$

Assumir  $V_{cc}=3$ ,  $V_t=0,5$ ,

$V_s=gnd$ ,  $V_g=3$ ,  $V_d=1$

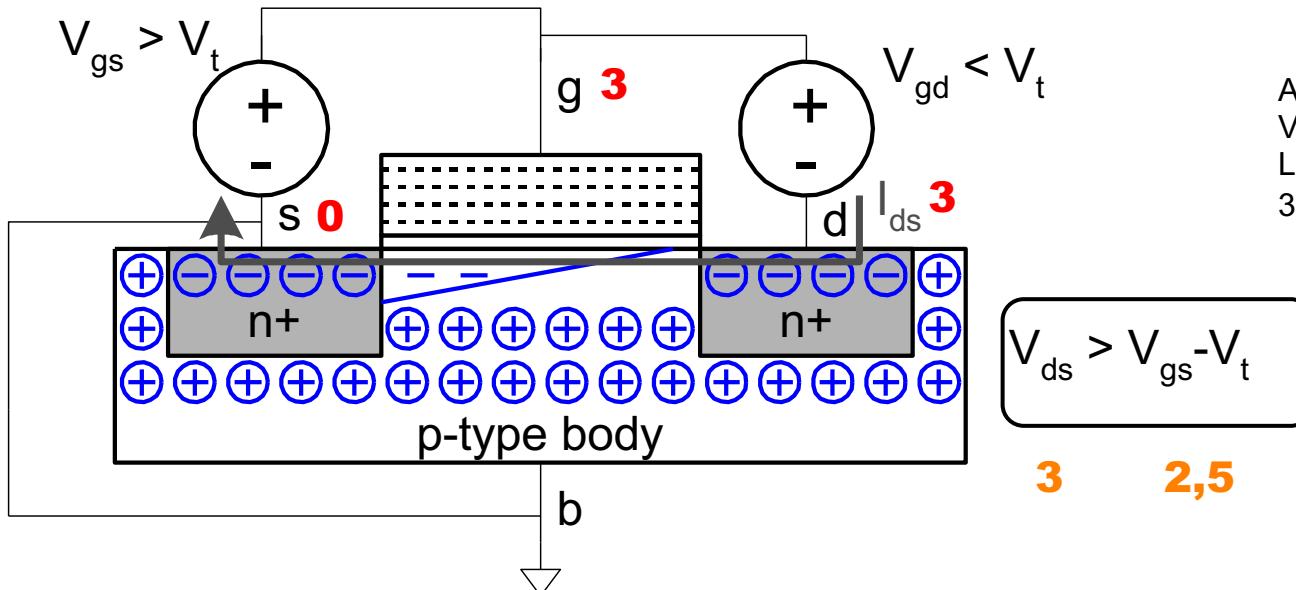
Logo:

$0 < 1 < 2,5$

# NMOS saturado

- Channel pinches off (estrangulamento)
- $I_{ds}$  independent of  $V_{ds}$
- We say current saturates
- Similar to **current source**

Saturação:  $V_{ds}$  não influi mais em  $I_{ds}$



Assumir  $V_{cc}=3$ ,  $V_t=0,5$ ,  
 $V_s=gnd$ ,  $V_g=3$ ,  $V_d=3$   
Logo:  
 $3 > 2,5$

- Os elétrons do canal são “injetados” na região de depleção do dreno e **acelerados** em direção ao source

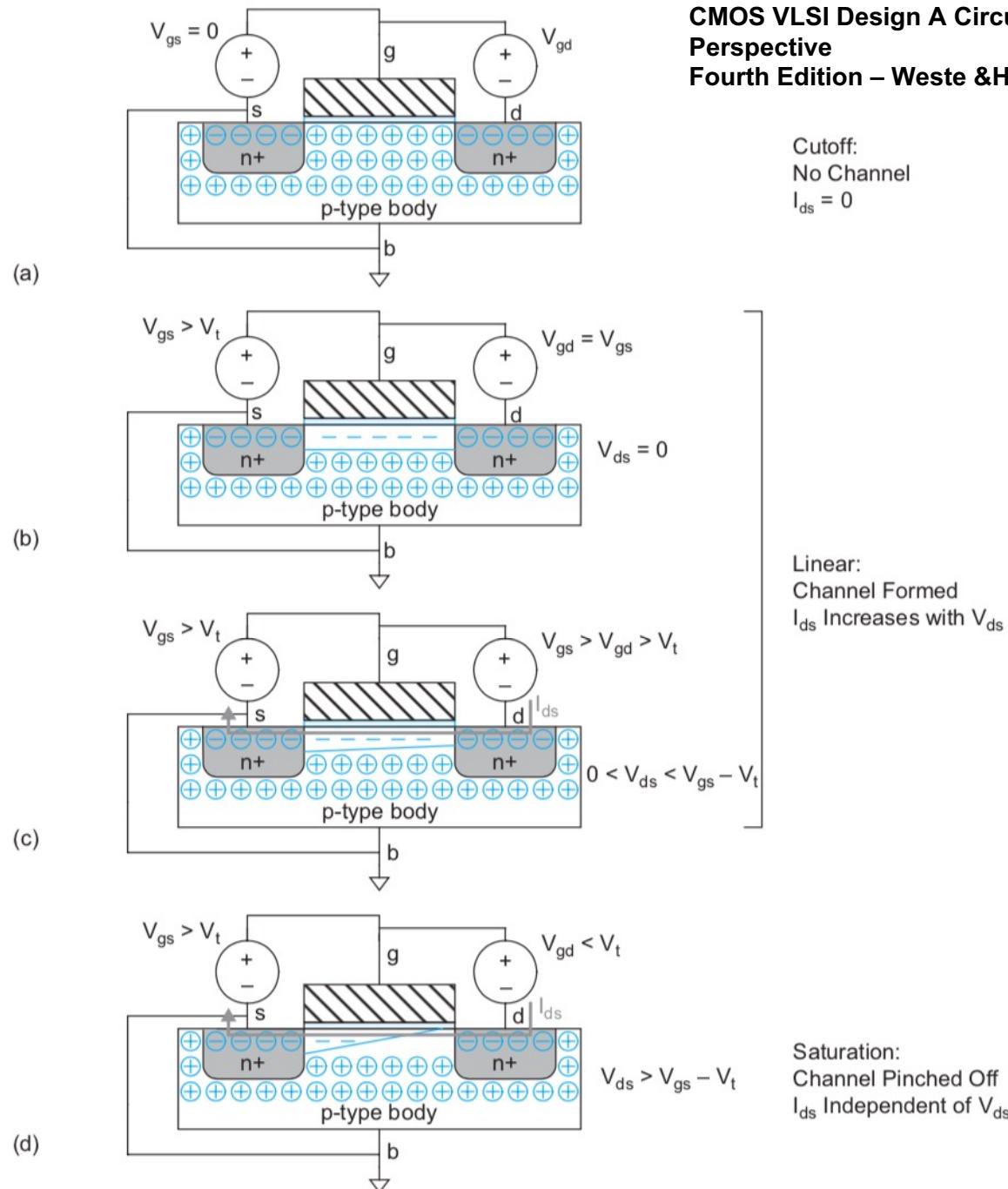


FIGURE 2.3 nMOS transistor demonstrating cutoff, linear, and saturation regions of operation

# Porque satura?

## Velocidade de saturação

- $10^5$  m/s
- Razão: colisão entre os elétrons

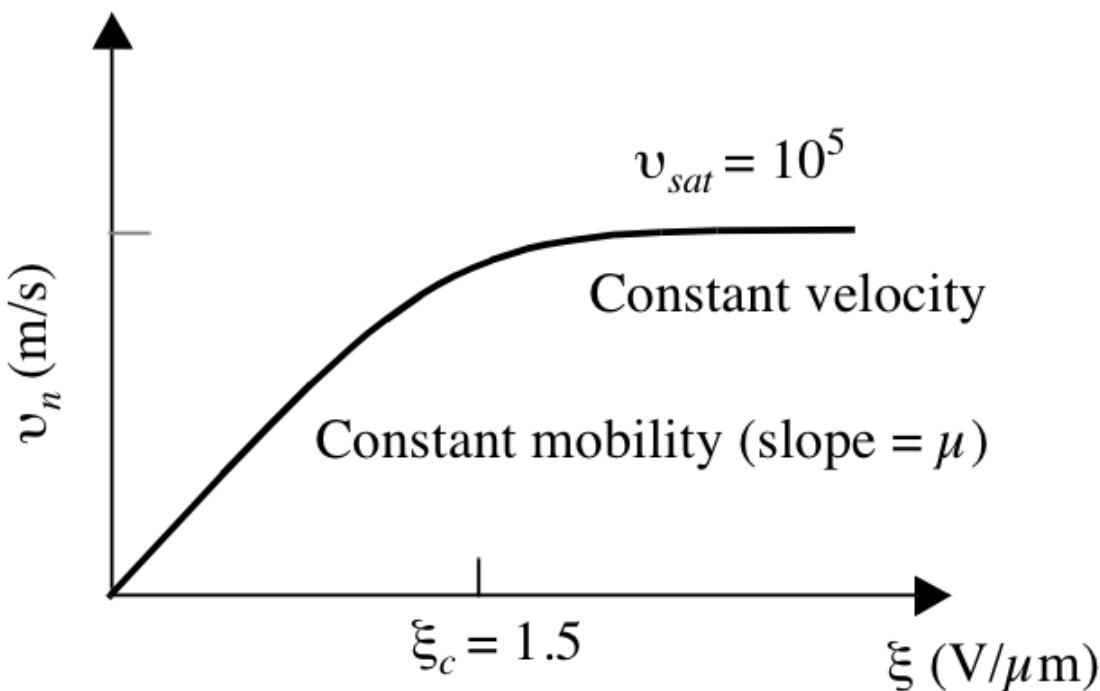


Figure 3.17

# Corrente Ids

Modelo de 1<sup>a</sup> ordem

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L} \quad \textcolor{red}{\text{Ganho do transistor}}$$

$$V_{DS} = V_{GS} - V_T$$

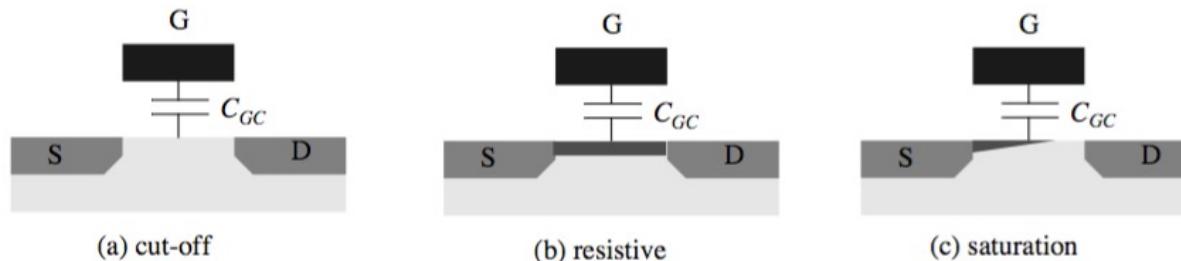
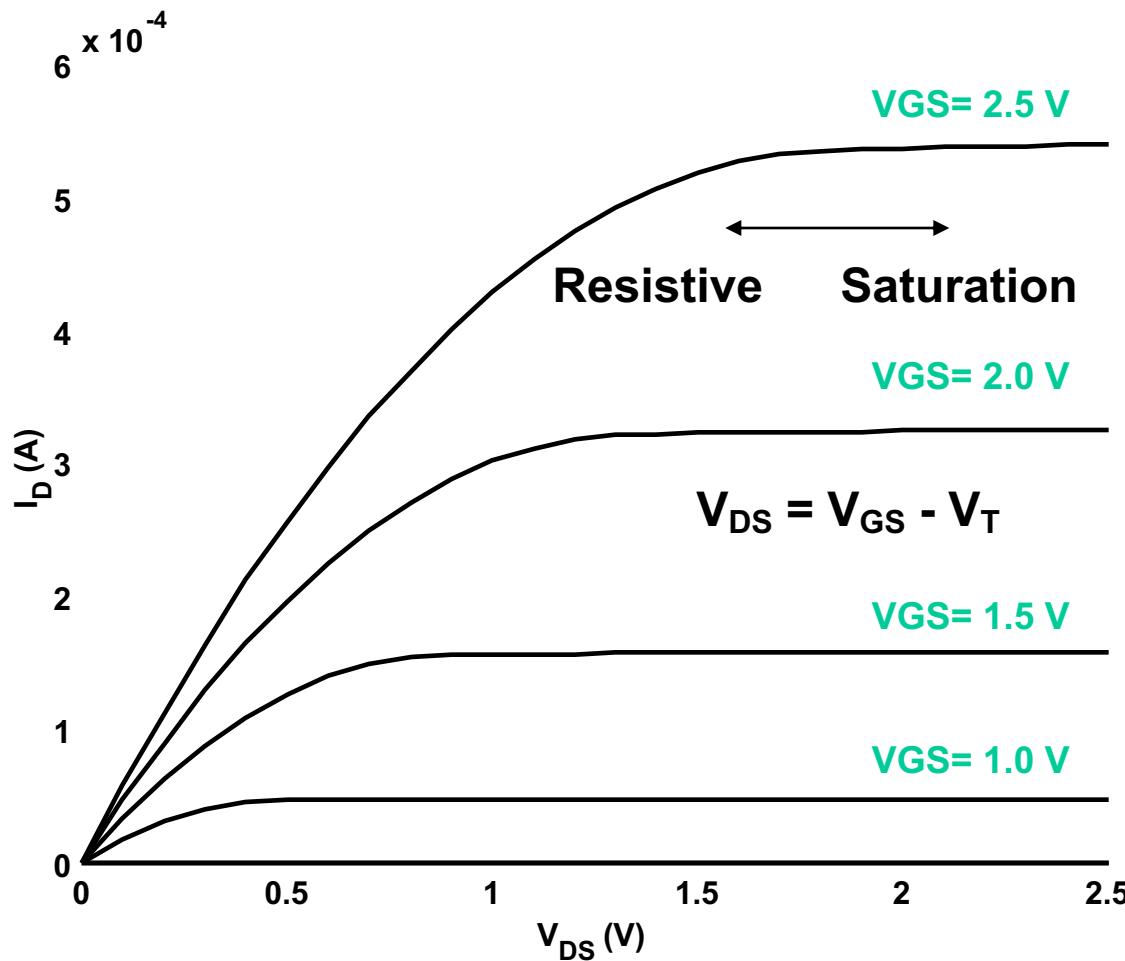


Figure 3.29 The gate-to-channel capacitance and how the operation region influences its distribution over the three other device terminals.

# Curva I-V



**Região linear (resistiva):**

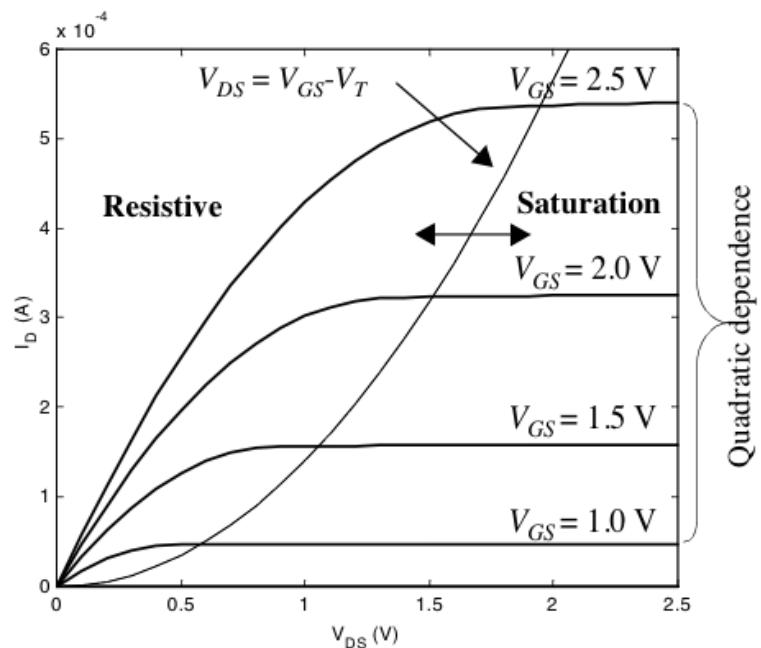
- o transistor funciona como um resistor controlado por tensão

**Região de saturação:**

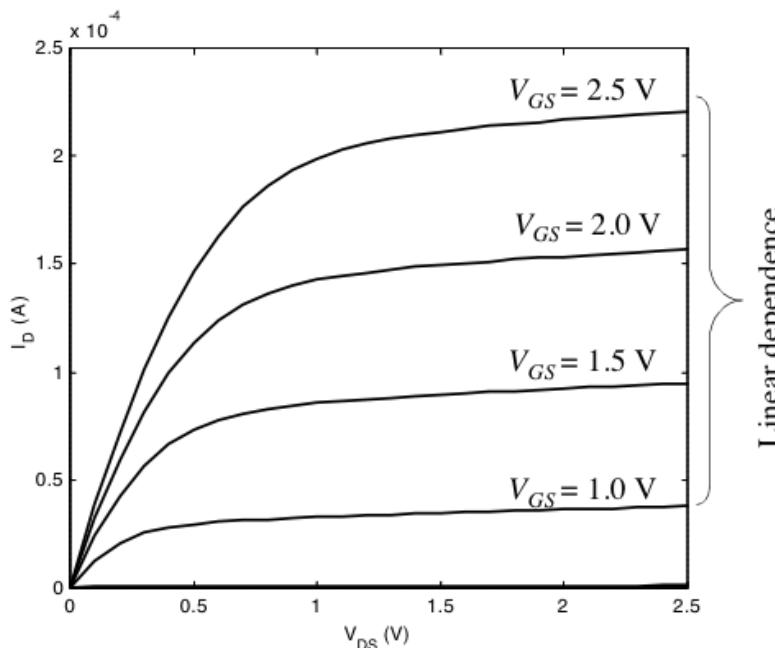
- o transistor funciona como uma fonte de corrente controlada por tensão

# Curva I-V

- Com canal menor ( $L$  menor) velocidade de saturação é atingida mais cedo

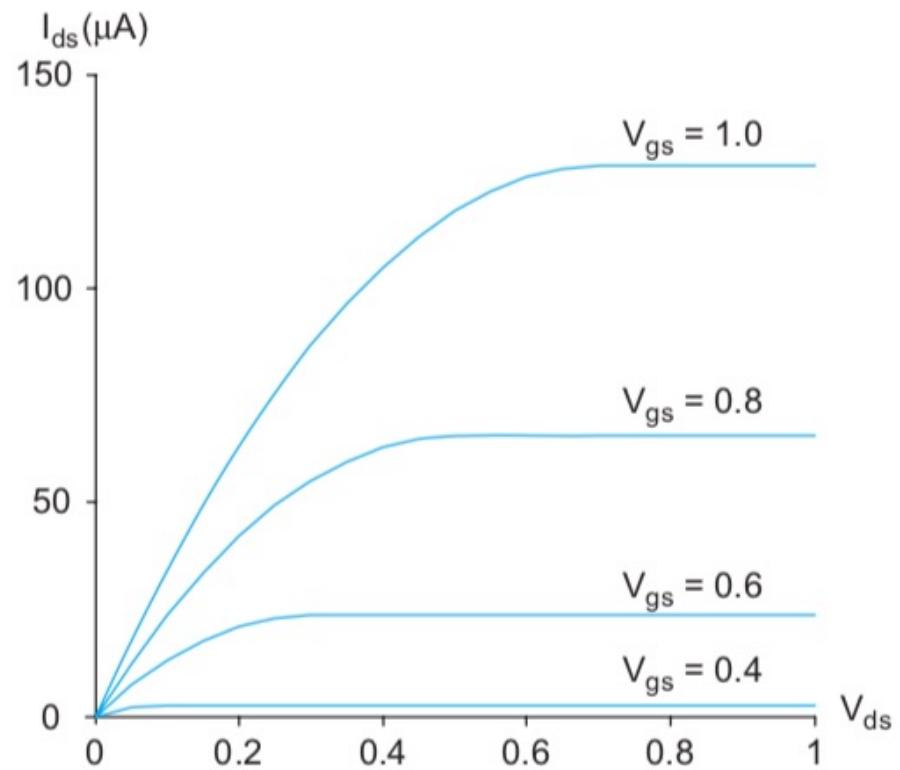


(a) Long-channel transistor ( $L_d = 10 \mu\text{m}$ )

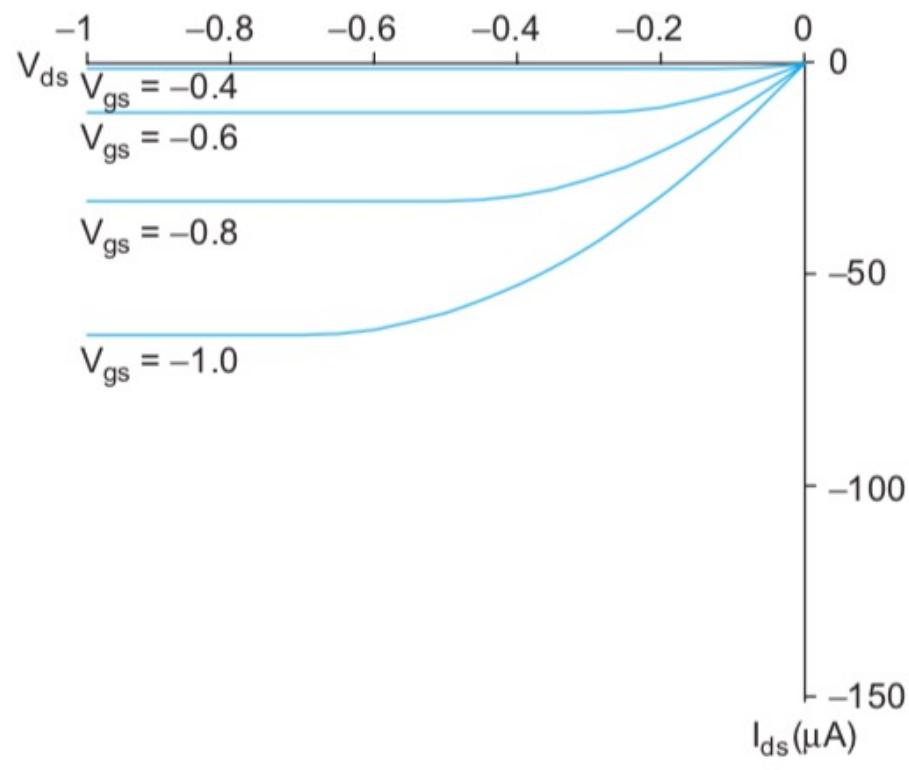


(b) Short-channel transistor ( $L_d = 0.25 \mu\text{m}$ )

**Figure 3.19**  $I_V$  characteristics of long- and a short-channel NMOS transistors in a  $0.25 \mu\text{m}$  CMOS technology. The  $(W/L)$  ratio of both transistors is identical and equals 1.5



(a)



(b)

**FIGURE 2.7** I-V characteristics of ideal  $4/2 \lambda$  (a) nMOS and (b) pMOS transistors

## Fatores que influenciam $I_{ds}$

- distância entre o source e o dreno (L)
- largura do dreno/source (W)
- tensão de threshold
- espessura do isolante do gate
- a constante dielétrica do isolante
- a mobilidade dos portadores (elétrons ou buracos)
- temperatura

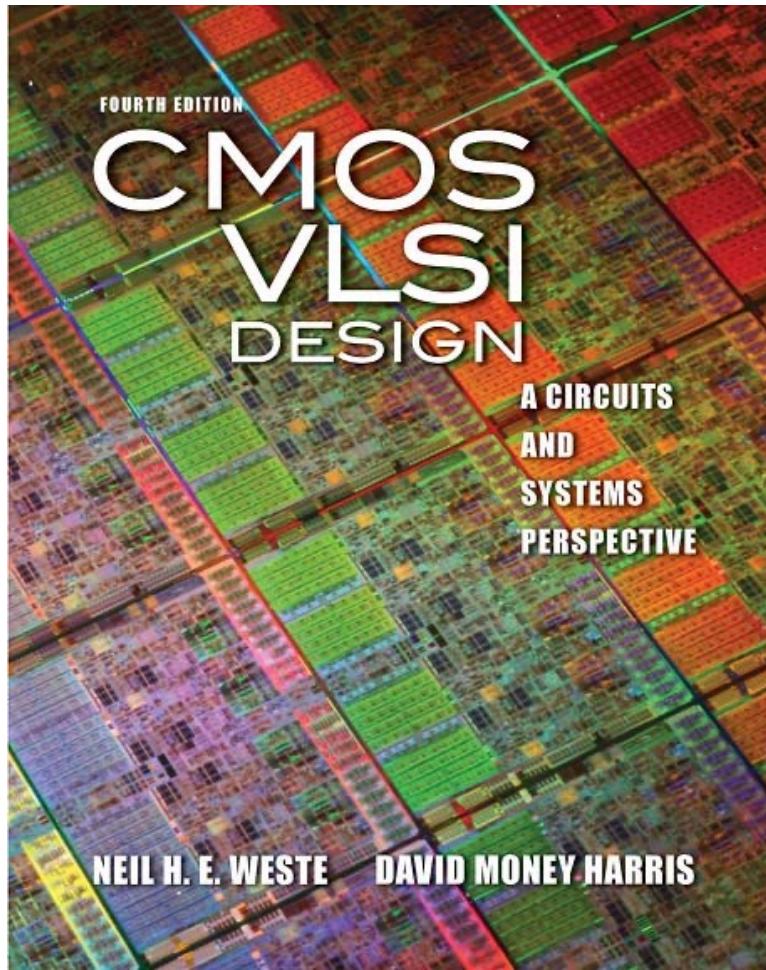
# Resumindo....

- Consideraremos inicialmente  $VDS=0$ . Quando uma tensão positiva  $VGS$  é aplicada, um campo é induzido na região do semicondutor entre o gate e dreno, fazendo com que as lacunas na região do substrato abaixo do gate sejam repelidas (depleção).
- Se esta tensão  $VGS$  for superior à tensão de limiar do transistor, elétrons são atraídos, para dentro da região abaixo do gate. Teremos então a formação de um caminho condutivo com cargas negativas entre o dreno e o gate. Esse caminho é chamado de canal N e sua resistência dependerá da tensão  $VGS$ . Adicionalmente se aplicarmos uma pequena tensão entre dreno e gate, teremos a passagem de corrente pelo canal N proporcional a tensão  $VDS$  aplicada.
- Elevando a tensão  $VDS$ , poderemos atingir uma situação onde a corrente permanecerá essencialmente constante, independente de posteriores aumentos de  $VDS$ . Esta condição de saturação da corrente se deve ao estrangulamento (*pinch-off*) do canal.

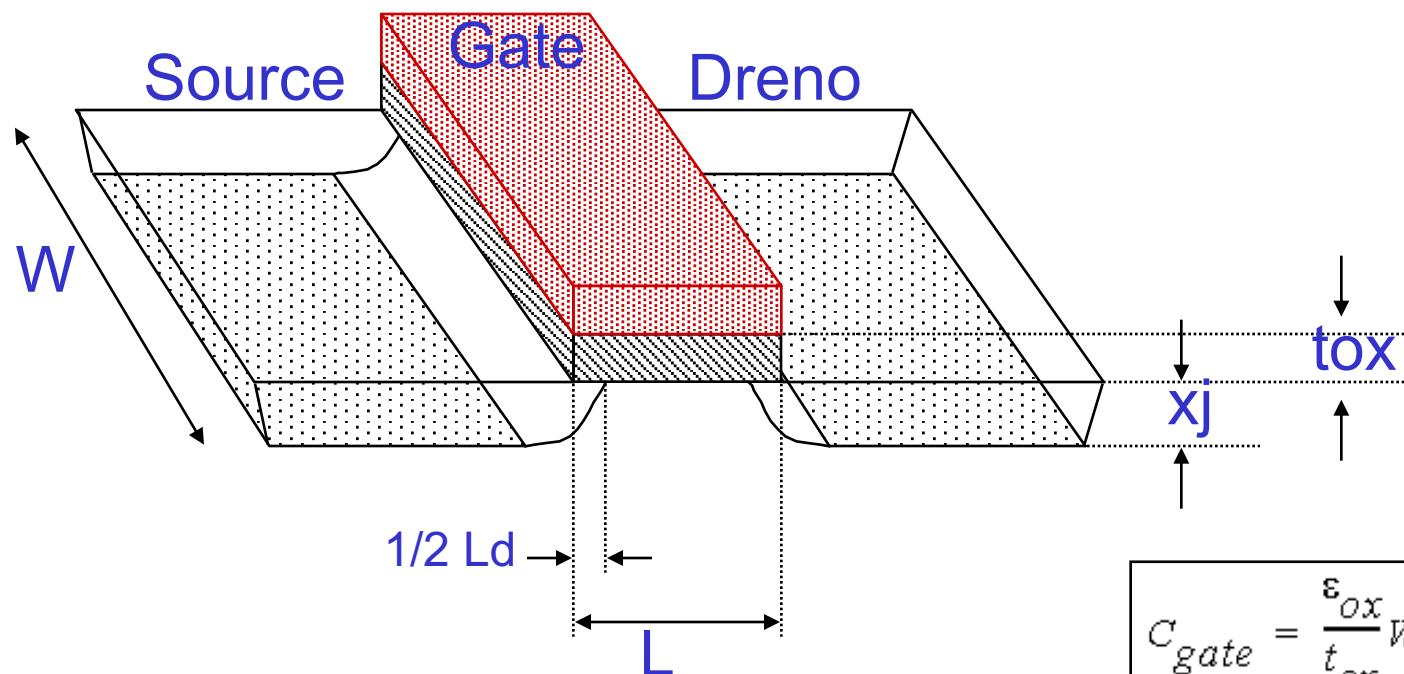
# Leitura recomendada:

Quarta edição do CMOS VLSI DESIGN

- 4<sup>a</sup> edição, de 2010
- Caps 1 (1.1 a 1.5) e 2



- Parâmetros geométricos do dreno/source



$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} WL$$

# Exemplo de netlist Spice - 1

\*\* modelo elétrico para uma tecnologia 0.35 um

.include tsmc035.mod

M1 DN gate 0 0 nmos I=0.35e-6 W=3.0U

\*\*\* fonte de tensão apenas para medida de corrente

vni n3 DN

\*\*\* fonte de tensão entre o dreno e o source, 0 a 2.5 volts

vds\_n n3 0

.dc vds\_n 0 2.5 .1

\*\*\*\* seis valores de tensão aplicados ao gate

vgs gate 0 dc 0

.alter

vgs gate 0 dc 0.5

.alter

vgs gate 0 dc 1.0

.alter

vgs gate 0 dc 1.5

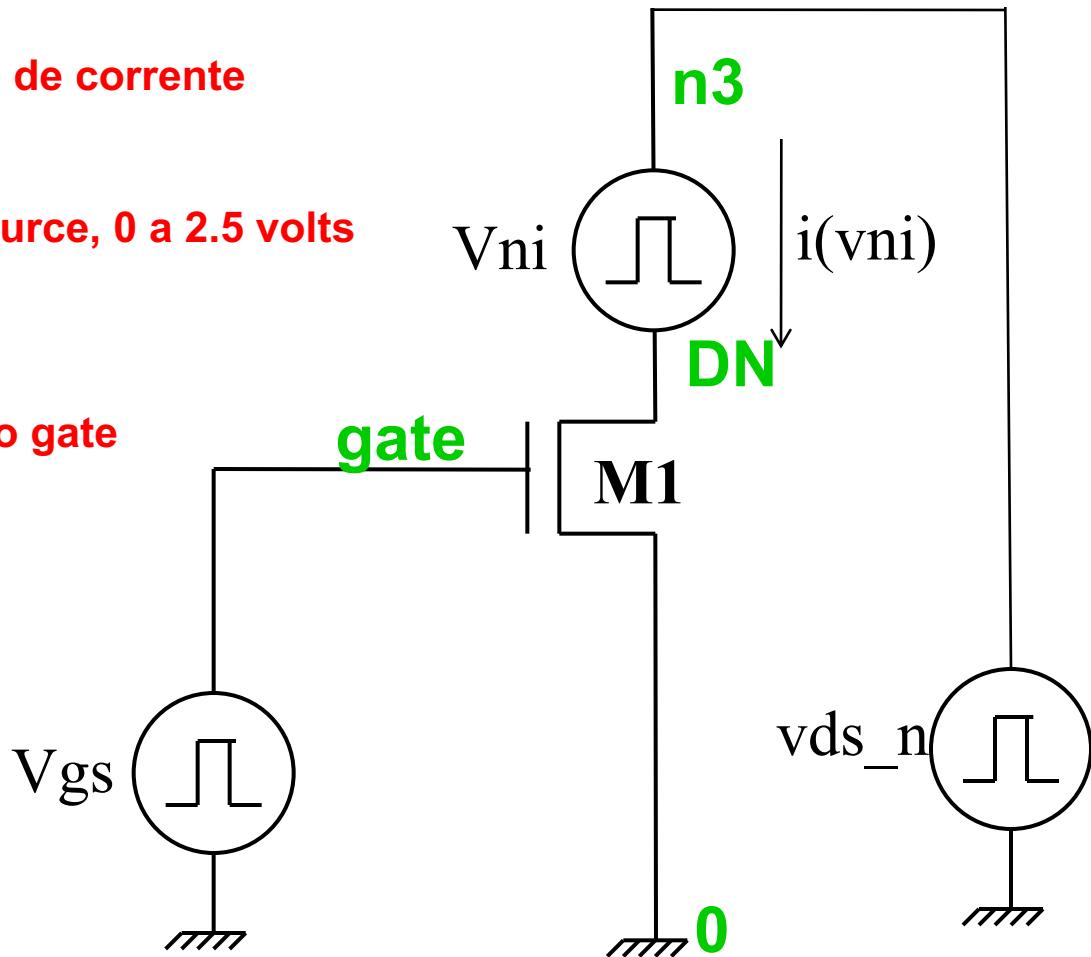
.alter

vgs gate 0 dc 2.0

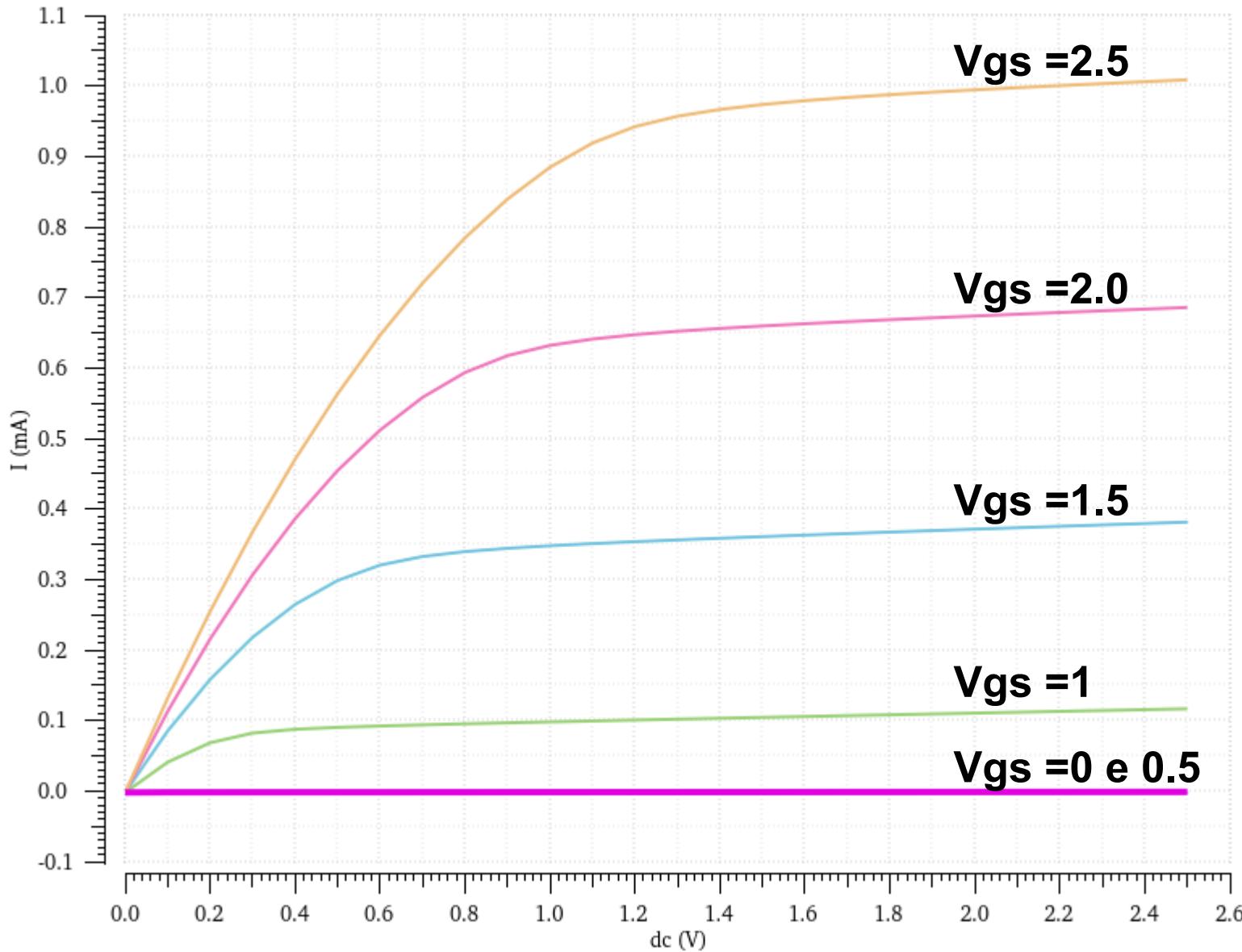
.alter

vgs gate 0 dc 2.5

.END

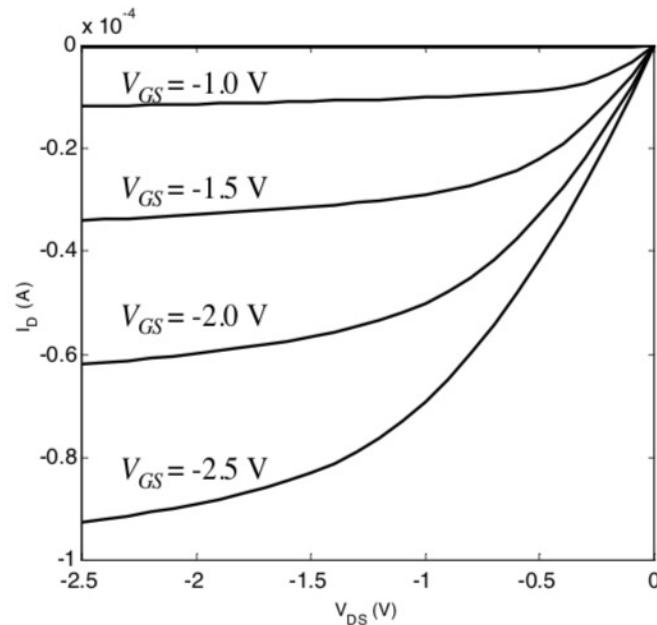


# Resultado da simulação - $i(v_3)$



# Curva para o transistor P

All the derived equations hold for the PMOS transistor as well. The only difference is that **for PMOS devices, the polarities of all voltages and currents are reversed**. This is illustrated in Figure 3.21, which plots the  $I_D$ - $V_{DS}$  characteristics of a minimum-size PMOS transistor in our generic 0.25  $\mu\text{m}$  CMOS process. The curves are in the third quadrant as  $I_D$ ,  $V_{DS}$ , and  $V_{GS}$  are all negative. Interesting to observe is also that the effects of velocity saturation are less pronounced than in the CMOS devices. This can be attributed to the higher value of the critical electrical field, resulting from the smaller mobility of holes versus electrons.



**Figure 3.21**  $I$ - $V$  characteristics of ( $W_d=0.375 \mu\text{m}$ ,  $L_d=0.25 \mu\text{m}$ ) PMOS transistor in 0.25  $\mu\text{m}$  CMOS process. Due to the smaller mobility, the maximum current is only 42% of what is achieved by a similar NMOS transistor.

# MOSFET Elements

---

M element for MOSFET

Mname drain gate source body type

- + W=<width> L=<length>
- + AS=<area source> AD = <area drain>
- + PS=<perimeter source> PD=<perimeter drain>

## Netlist Spice – exemplo: tsmc035.mod

```
.MODEL NMOS NMOS ( LEVEL = 53
+VERSION = 3.1      TNOM  = 27      TOX   = 7.7E-9
+KJ     = 1E-7      NCH   = 2.35    VTH0  = 0.50
...
+U0  = 415.8570638 UA    = 5.057324E-11 UB    = 1.496793E-18
...
+LKETA = -0.018518 )
```

```
.MODEL PMOS PMOS ( LEVEL = 53
+VERSION = 3.1      TNOM  = 27      TOX   = 7.7E-9
+XJ     = 1E-7      NCH   = 8.52E16   VTH0  = -0.6897992
...
+U0  = 150.6275733 UA    = 2.016943E-10 UB    = 1.714919E-18
...
+LKETA = 7.702974E-3 )
```

# Sources

## DC Source

vdd vdd gnd 2.5

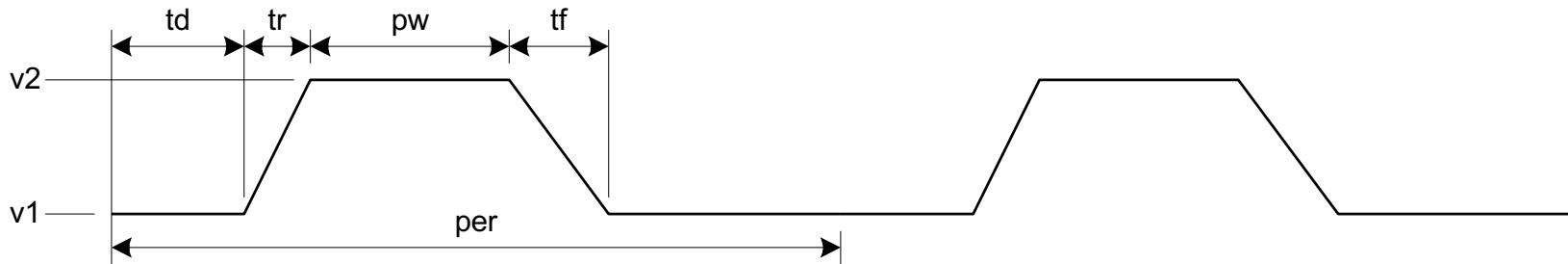
## Piecewise Linear Source

vin in gnd pwl 0ps 0 100ps 0 150ps 1.8 800ps 1.8

## Pulsed Source

vck clk gnd PULSE 0 1.8 0ps 100ps 100ps 300ps 800ps

PULSE v1 v2 td tr pw per



# SPICE Elements

Letter	Element
R	Resistor
C	Capacitor
L	Inductor
K	Mutual Inductor
V	Independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
W	Lossy transmission line
X	Subcircuit
E	Voltage-controlled voltage source
G	Voltage-controlled current source
H	Current-controlled voltage source
F	Current-controlled current source

# Units

Letter	Unit	Magnitude
a	atto	$10^{-18}$
f	femto	$10^{-15}$
p	pico	$10^{-12}$
n	nano	$10^{-9}$
u	micro	$10^{-6}$
m	milli	$10^{-3}$
k	kilo	$10^3$
x	mega	$10^6$
g	giga	$10^9$

## Exemplo de netlist Spice - 2

\*\* MODELO ELÉTRICO DOS TRANSISTORES

. include tsmc035.mod

M1 o1 i vdd vdd pmos l=1e-06 w=2e-06

M2 o1 i 0 0 nmos l=1e-06 w=2e-06

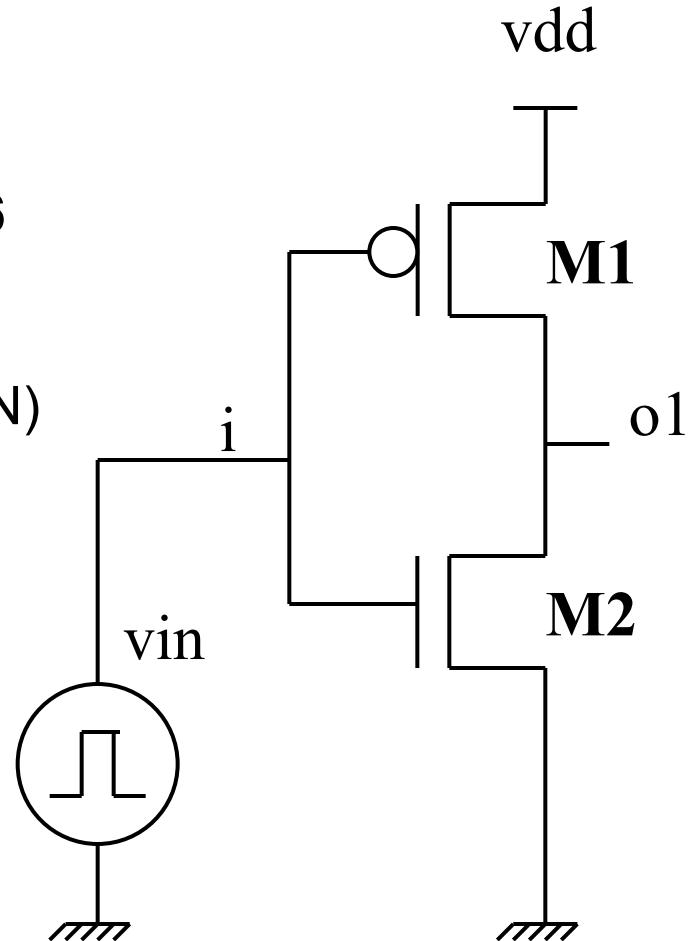
vcc vdd 0 dc 5

vin1 i 0 pulse (5 0 0 0.1N 0.1N 10N 20N)

.tran 0.5N 80N

C1 o1 0 100fF

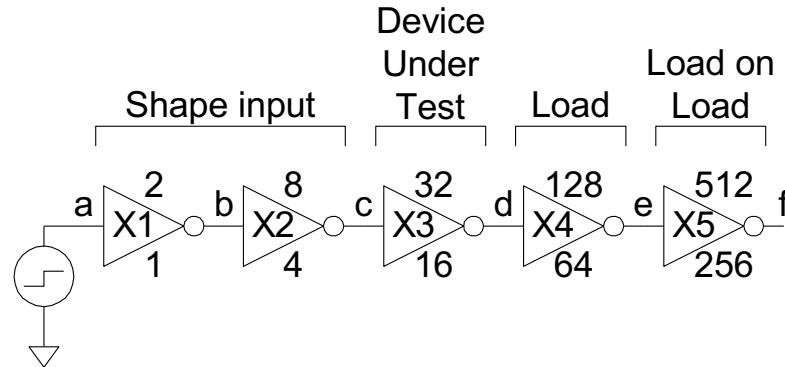
.END



# Subcircuits

- Declare common elements as subcircuits

```
.subckt inv out in vcc
M1 out in vcc vcc pmos l=0.35e-6 w=9U
M2 out in 0 0 nmos l=0.35e-6 w=3U
.ends inv
```



# Subcircuits

```
.....  
  
.include tsmc035.mod  
  
Vdd      vdd      0      3.3  
Vin      ent      0      PULSE    0 vdd 0ps 100ps 100ps 500ps 1000ps  
  
**  out  in  
X1  a    ent    vcc inv  
X2  b    a     vcc inv  
X3  c    b     vcc inv  
X4  d    c     vcc inv  
X5  e    d     vcc inv  
  
C1  e  0  5ff  
  
.end
```