Power Estimation at Logic-Level Considering Interconnection Capacitances

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Abstract

Accurate and fast power estimation of CMOS circuits during the design phase is required to guide power optimization techniques employed to meet stringent power specifications. Logic-level power estimation tools, such as those available in the SIS frameworks (POSE and Power Estimate) are able to accurately calculate the switching activity under a given delay model. However, capacitance modeling is crude. The goal of the work described in this paper is to estimate the average power of a circuit with interconnection capacitances and transistors extracted from the layout. To validate the method we user the Diva extractor (Cadence Design Systems) and LASCA [8] extractor. We propose new models for the input and output capacitances of logic gates, taking into account the internal capacitances of the gates. The results we present show a comparison of logic-level power estimation with capacitances extracted of DIVA and LASCA, with less that 10% error.

1. Introduction

Power consumption is becoming one of the most important VLSI design. Optimization techniques for low power are being employed at all design levels of abstraction. In order to guide designers and optimization tools, there is a pressing need for accurate and fast power estimation tools.

During normal operation, the power dissipation of a CMOS circuit is directly related to the switching activity. For a well designed circuit, the total average power can be approximated by the switched-capacitance power [1]. This is an underlying assumption of almost all available power estimation tools at the logic and higher levels of abstraction. The average dynamic power consumption of a CMOS circuit is then given by:

$$Power = \frac{1}{2}.f.V_{dd}^2.\sum_{i=1}^{n} C_i.\alpha_i \qquad (1)$$

Where f is the clock frequency, Vdd is the supply voltage, Ci and αi are capacitance load and average switching of the logic gate i, respectively.

Significant amount of work has been carried out in developing efficient techniques to estimate the switching activity of a CMOS circuit [2]. These techniques can be divided into two classes: statistical techniques (also known as dynamic techniques), e.g. [3]; probabilistic (or static) techniques, e.g. [4].

Probabilistic techniques propagate input statistics through the circuit to obtain the switching probability for each gate in the circuit. Probabilistic techniques are employed in the power estimation tools of SIS [5] and POSE [6].

In this paper, we focus on the problem of capacitance modeling. This is typically done very simplistically at the logic level. We propose to build a more accurate model. At the logic-level, only the input and output nodes of the gates are available. We present an equivalent load capacitance model for each external node, computed from the internal transistor capacitances and the interconnection capacitance.

The interconnection capacitance is currently being extracted from layout information. We have performed several experiments on (necessarily) simple circuits where power estimates were obtained both using SPICE and SIS using the capacitance values obtained through our model. The results are very promising, with power estimation differences of less than 10%.

This paper is organized as follows. In Section 2, we briefly present the capacitance gate model used for a transistor MOSFET. In Section 3, we describe the methodology to extract the coupling and ground capacitances of interconnections. In the section 4 is presented the modeling of gate capacitance at logic level. In Section 5, we describe the experimental setup for to validate the propose method. Experimental results are presented in Section 6. In Section 7, we give some conclusions and discuss future research.

2. Capacitance Gate Model

The MOSFET transistors exhibit a number of parasitic capacitance [7] (Figure 1), which must be accounted in circuit design: gate-to-source capacitance (CGS), gate-to-drain capacitance (CGD), gate-to-bulk capacitance (CGB), source-to-bulk capacitance (CSB) and drain to bulk capacitance (CDB). In this work, our interest is the switching region of the transistors and all the capacitances will be considered, with the exception of CGB.

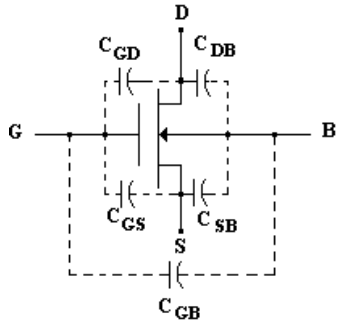

Figure 1- Parasitic Capacitances of the MOSFET

Although these capacitances are a nonlinear function of the voltage, the general approach is to assume them as a linear, time-invariant element. Given some technology parameters and the size the transistor (W/L), a value for each of these parasitic capacitances can be computed [7].

3. Interconnection Capacitances

The interconnection capacitances are extracted directly from a flat layout of a circuit. We developed a fast capacitance extraction tool (LASCA wire extractor [8]) using a Bin-Based algorithm [9] to extract the connectivities, empirical formulation [10] to compute the capacitances, and a simple 2½D methodology described in [11]. The input of the extractor is a flat layout description and a technology file. The layout description is scanned and during this process a net list describing all parasitic capacitances is generated.

The 2½D methodology described in [11] was based on experiments with a 3D field solver over 0.50μm, 0.35μm and 0.18μm process. Briefly, for each connection in the layer i, we should analyze the immediate neighbor in the same layer, all crossunders in the layer i-1 and all crossovers in the layer i+1, treating the layers i±2 like ground planes.

In Figure 2 is presented the model to calculate the interconnect capacitance in each node of the circuit. It consists of two conduction layers over the substrate, considered as a reference plane (ground plane). There are three capacitance components at any node [12]:

Overlap capacitance (C_{over}) - due the overlap between two conductors in different planes. They are C_{21a} and C_{23a} in the Figure 2.

Lateral capacitance (C_{lat}) - is the capacitance between two conductors in the same plane. In the Figure 2 is C_{22lat}.

Fringing capacitance (C_{fr}) - due the coupling between two conductors of different planes. They are C_{21fr} and C_{23fr} in the Figure 2.

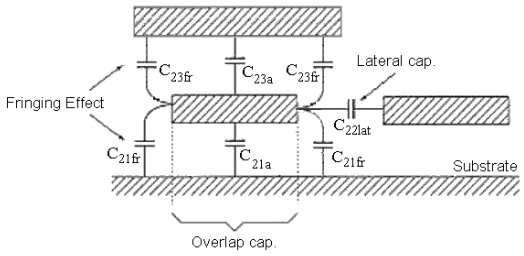

Figure 2 – Capacitance Model

The capacitances C_{ij} (i,j=1...*n*, where *n* is the number of conductors) are calculate by an empiric formulation.

3.1 Intrinsic Capacitance

The intrinsic capacitance is the capacitance between one conductor layer and the ground plane. It has two components: overlap and fringing capacitances.

Two parallel plates model the overlap capacitance. The fringing capacitance is due to the edge of one conductor and the surface of the other one (in this case, the ground plane). They are calculated using the traditional formulation based in the overlap area and perimeter. Thus, the intrinsic capacitance is the sum of these two components:

$$C_{int}=(C_{area}.W+2.C_{length}).L \qquad (2)$$

Where C_{area} is capacitance per unit area (fF/μm2), C_{length} is the capacitance per unit length (fF/μm), W is the wire width and L is the wire length.

3.2 Coupling Capacitance

The coupling capacitances are extracted, because, in deep-submicron processes, the increase in the ratio between wire thickness and space between wires has substantially increased the lateral capacitance.

The lateral coupling capacitance is a function, basically, of two factors: wire thickness and the space between wires. The wire thickness is a function of the technology and the layer considered. However, the space between wires is the main factor, depending of structure analyzed. As the space between two wires can have a large variation, we can not use the capacitance informed by technology rules, because it is restrict to the minimum distance of separation.

In deep-submicron process, the foundries set the minimum area usage for each metal layer. This value is normally fixed to 30%, for uniformity of etches rate or CMP planarization. The maximum area usage is around 50%, when the distance between two wires is equal to the minimum distance of the process. Thus, the distance between two wires has a large variation. If we use the capacitance from the technology rules, we have a large error.

To calculate the coupling capacitance it was used the empirical formulation described in [10], and two cases can happen: just one ground plane or two ground planes, where the second plane is the i+2 plane. These formulations need some parameters from layout, like the space between two wires and some others from the technology like thickness of metal line, width of metal line and thickness of dielectric layer between metal layer and ground plane.

3.3 Crossover Capacitance

The crossover capacitance is only calculated if there is a common area between two wires in two different planes. This common area is extracted by the AND logic operator, between the two wires. As the intrinsic capacitance, the crossover capacitance (Ccross) is modeled considering two parallel plates. It is calculated using the follow equation:

$$C_{cross}=C_{area}.W_1.W_2+2.C_{length}.(W_1+W_2) \quad (3)$$

4. Modeling Gate Capacitances in the Logic Level

For circuits described at the logic level there is only access to the logic gates input and output nodes. Therefore, all internal gate capacitances have to be taken into account in concentrated capacitance model to external nodes. In this section we describe how we compute the equivalent capacitance load for any logic gate from its transistor level description.

A. Inverter

The CMOS inverter (Figure 3) presents two externals nodes. In this case, equivalent capacitances at the input x. Cin x, and output y, Cout y, nodes can be simply computed using:

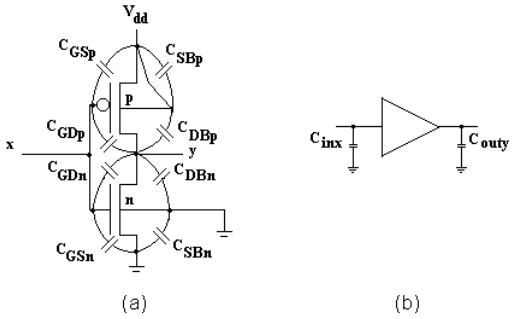

Figure 3 – Parasitic capacitances of CMOS inverter

(a) Transistor-level representation

(b) Logic-level representation

$$C_{inx} = C_{GSp} + C_{GDp} + C_{GSn} + C_{GDn} \quad (4)$$

$$C_{outy} = C_{DBp} + C_{GDp} + C_{GDn} + C_{DBn} \quad (5)$$

A. NAND2

In the case of a CMOS 2-input NAND gate (Figure 4), there are two input nodes with a concentrate capacitance and one output node. The additional difficulty is that now it is necessary to model the internal capacitance. We analyze the equivalent capacitance by a superposition of signals. For example, when we calculate the equivalent capacitance of an input node, the inputs and output will be in the ground level.

The capacitance of internal nodes depends on the logic value of the others inputs. To model this effect we are assuming a probability of 0.5 that all inputs are set to 1. That is, the NMOS transistors will be ON at half the time.

In the case NAND2, the input combination possible is 00, 01, 10 and 11.

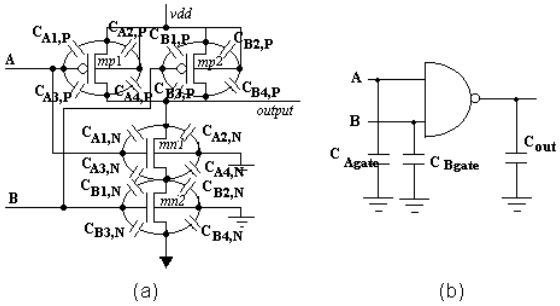

Figure 4 – Parasitic Capacitances of 2-input NAND

(a) Transistor-level representation

(b) Logic-level representation

Input "a":

For input combinations 00 and 10, the "mn2" transistor is OFF and equivalent capacitance node (Ca1) is equal:

$$C_{a1} = 0.5(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}) \quad (6)$$

$$C_{T,N} = C_{A4,N} + C_{B1,N} + C_{B2,N} \quad (7)$$

For input combinations 01 and 11, the mn2 transistor is ON and equivalent capacitance (Ca2) is equal:

$$C_{a2} = 0.5(C_{A1,N} + C_{A3,N}) \quad (8)$$

Then

$$C_{A,N} = C_{a1} + C_{a2}$$

$$C_{A,N} = 0.5(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}) + 0.5(C_{A1,N} + C_{A3,N}) \quad (9)$$

In terms probabilistics:

$$C_{A,N} = p_0(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}) + p_1(C_{A1,N} + C_{A3,N}) \quad (10)$$

And C_{Agate} is:

$$C_{Agate} = p_0(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}) + p_1(C_{A1,N} + C_{A3,N}) + C_{A1,P} + C_{A3,P} \quad (11)$$

Where p0 is probability that the second input is equal the ZERO and p1 is the probability that the second input is equal the ONE (p0 + p1 = 1).

Input "b"

In the same way, can analyze the second input.

For input combinations 00 and 01, the mn1 transistor is OFF and Cb1 is equal:

$$C_{b1,N} = 0.5(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}}) \quad (12)$$

For input combinations 10 and 11, the mn1 transistor is ON and CB2 is equal:

$$C_{b2,N} = 0.5(C_{B1,N} + C_{B3,N}) \quad (13)$$

Then

$$C_{B,N} = C_{b1,N} + C_{b2,N} \quad (14)$$

$$C_{B,N} = 0.5(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}}) + 0.5(C_{B1,N} + C_{B3,N}) \quad (15)$$

$$C_{T1,N} = C_{A4,N} + C_{A3,N} + C_{B2,N} \quad (16)$$

In terms probabilistics :

$$C_{B,N} = p_0(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B3,N} + C_{T1,N}}) + p_1(C_{B1,N} + C_{B3,N}) \quad (17)$$

and C_{Bgate} is:

$$C_{Bgate} = p_0(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}}) + p_1(C_{B1,N} + C_{B3,N}) + C_{B1,P} + C_{B3.P} \quad (18)$$

Where C_{Agate} and C_{Bgate} are equivalent capacitances for input A and input B, respectively.

And output is:

$$C_{out} = C_{A1,N} + C_{A2,N} + C_{A3,P} + C_{A4,P} + C_{B3,P} + C_{B4,P} \quad (19)$$

B. CMOS NOR's

The NOR logic gates are dual NAND logic gate. In this case the internal capacitance will be present in the transistor pmos network.

5. Experimental Setup

The block diagram in Figure 5 gives an overview of the proposed method for validation of the proposed model. The method consists in extraction of capacitances and transistors from the layout of the circuit. We use the following tools in the validation process:

TROPIC3 [13] – This tool automatically generates the layout of a circuit with a "linear-matrix multi-row" layout style. It makes the partitioning, placement and routing of a circuit, generating the layout output file. The input file uses the SPICE format.

LASCA [8] – This tool is responsible by the capacitance extraction of the circuit since generate layout. The layout is generated by TROPIC3 tool.

Diva – The Cadence system was used for capacitance extraction.

Power Estimate – This program is embedded into SIS. It calculates the switching activity circuit using various delays model: zero delay, unit delay and general delay.

The validation flow used is the following:

Read circuit in the format *.cif* file (layout);

The *.cif* file is read by LASCA, that extracts the capacitances and transistors;

The gate capacitances are estimated using the extracted transistors file;

The interconnection capacitances and the gate capacitance are concentrated in the nodes (logic level);

The average power is estimated by Power Estimate tool using as input the extracted capacitance file, as well the switching activity and logic description of the circuit;

In proposed method of power estimation, the capacitances are concentrated in the external nodes of the logic gates;

The validation of the values of interconnection capacitances and proposed method of power estimate is made by the comparison with the DIVA extractor tool and LASCA extractor.

The results were analyzed and compared.

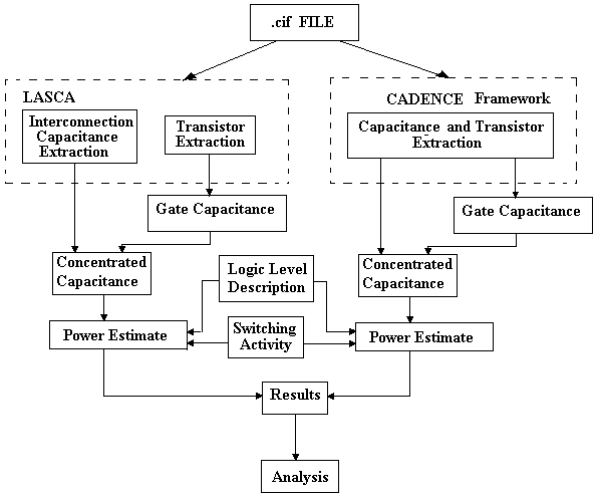

Figure 5 - Fluxogram of the Experimental Setup

6. Experimental Results

In this section, we present some power estimation results using the methods described in the previous sections. In Table 1 and 2, we present any benchmarks circuits: C17m, cm42a, decod and majority and power estimation results, respectively. The layout files were generated with TROPIC [13]. The interconnection capacitances and transistors were extracted using the LASCA tool [8].

In order to confirm the accuracy of the approximations made, we compare the results obtained at logic level

with the ones obtained with since capacitances extracted DIVA. We evaluated the average power using Power Estimate. It was done the comparison between interconnection capacitances using LASCA and DIVA The simulations were made with transistors using a 0.25μm technology. The average power values are in microWatts, assuming a 2.5V-supply voltage and 20MHz-clock frequency. The general results of these comparisons are presented in Table 1 and 2.
The small errors of the evaluations presented in the last column encourage us to continue the investigation for larger circuits.

Name	#gates	# Transistor	#nodes
C17m	6	24	19
Cm138a	13	96	56
Cm42a	16	100	56
Decod	22	146	80
Majority	7	46	30

Table 1 – Characteristics of the Circuits Benchmarks Analyzed

	Average	Power(μW)	
Name	LASCA	DIVA	%
C17m	9.60	8.69	9,47
Cm42a	8.49	7.88	7,1
decod	16.22	15.56	4,06
majority	8.10	8.66	5,43
Cm138a	10.47	9.68	9,47

Table 2 – Evaluations of Power Consumption for the MCNC'91 Benchmarks Circuits

7. Conclusion and Future Work

We presented an method for capacitance modeling by computing equivalent concentrated capacitances at the external nodes of the logic and interconnection capacitances. The model is able to take into account the capacitance of internal nodes and the interconnect capacitance extracted from layout. The interconnection capacitances was extracted for LASCA [8] extractor and DIVA extractor. The results of experimental application to standard logic gates validated the proposed procedure. With MCNC'91 benchmark circuits, it was done a comparison between circuits with less than three logic levels. For logic with more than three levels, delay must be considered in power a consumption evaluation.The next step of this research will consist in taking account of each logic gate delay and of switching activity with variable probability.

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