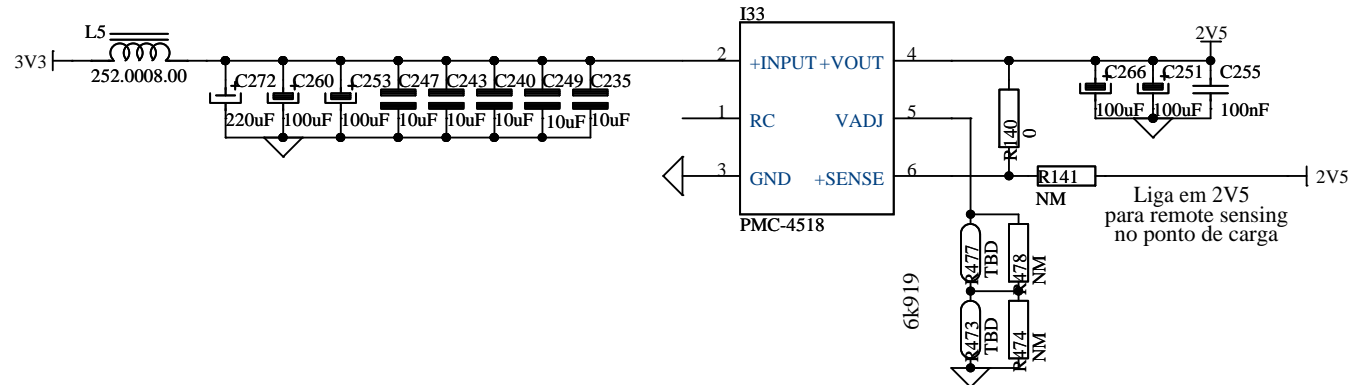
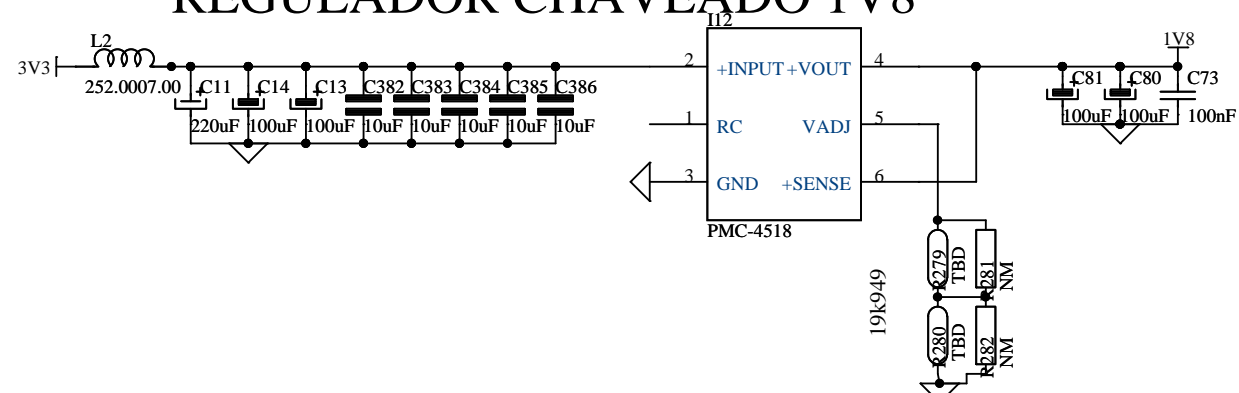


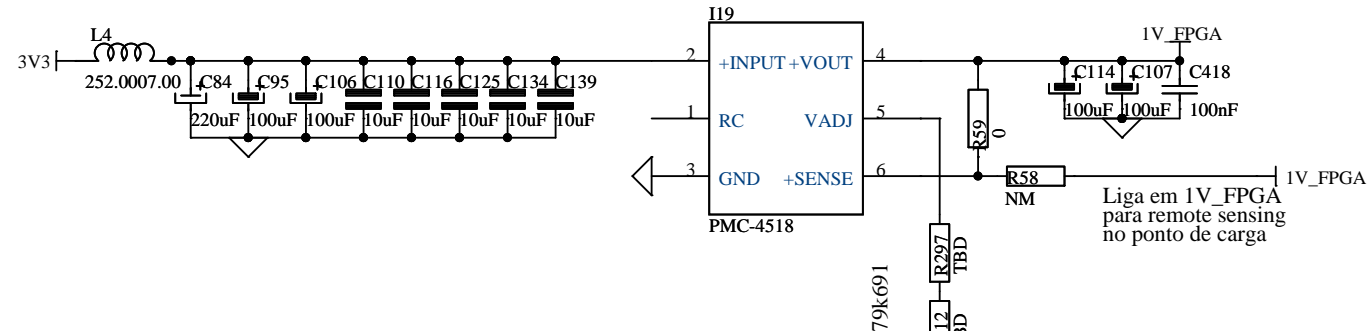
REGULADOR CHAVEADO 2V5



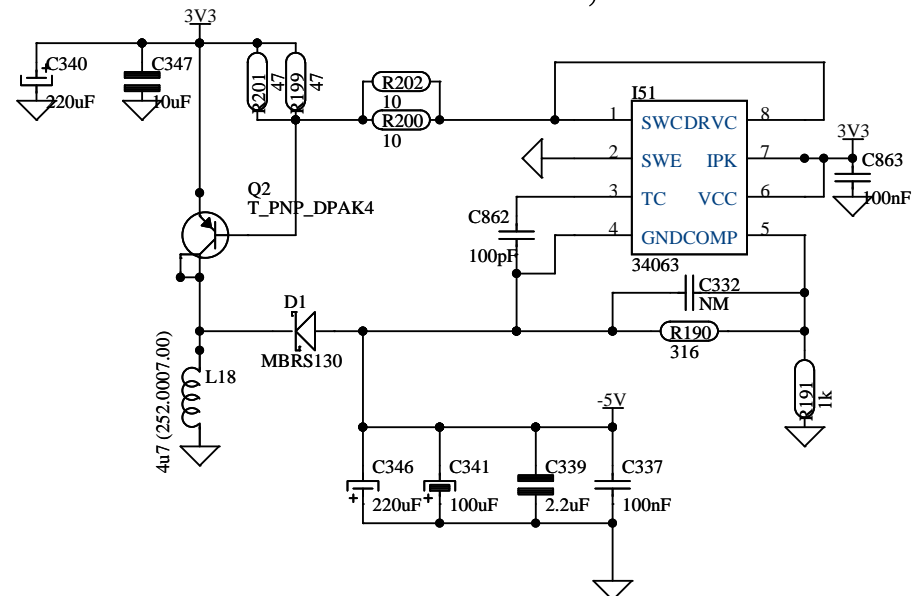
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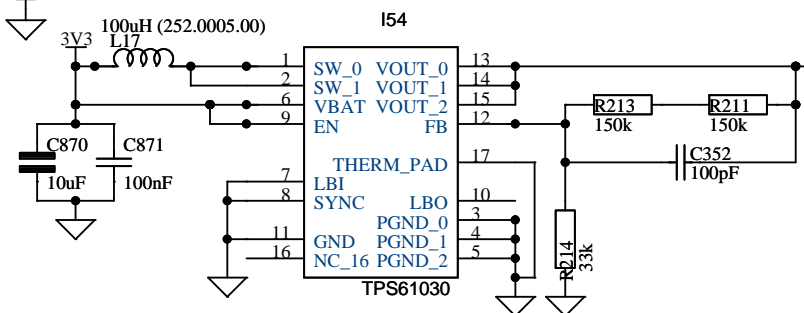
REGULADOR CHAVEADO 1V0



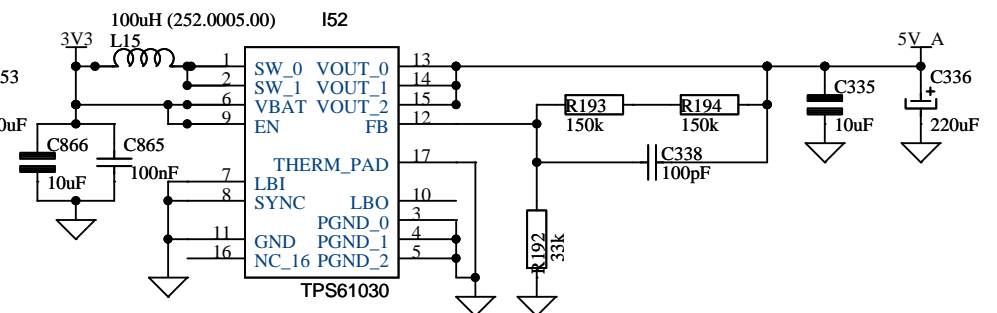
INVERTER -5V2, -1000mA



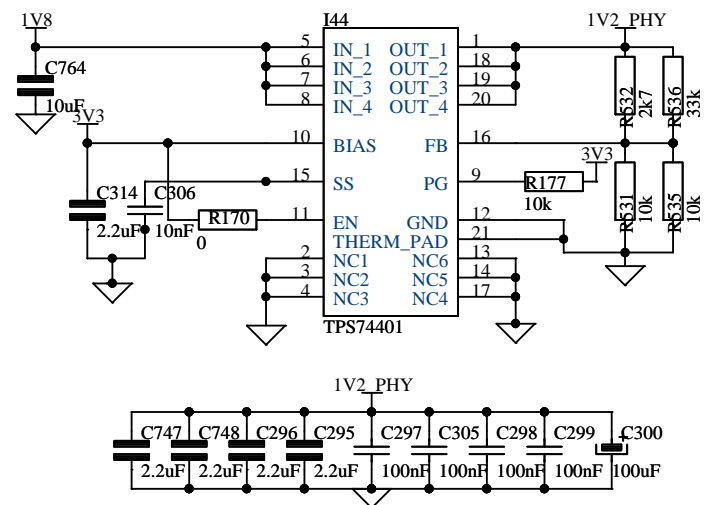
BOOSTER 5V, 600mA



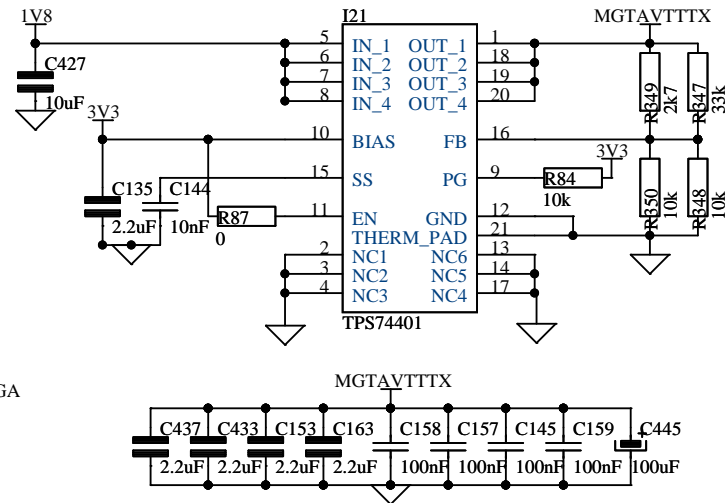
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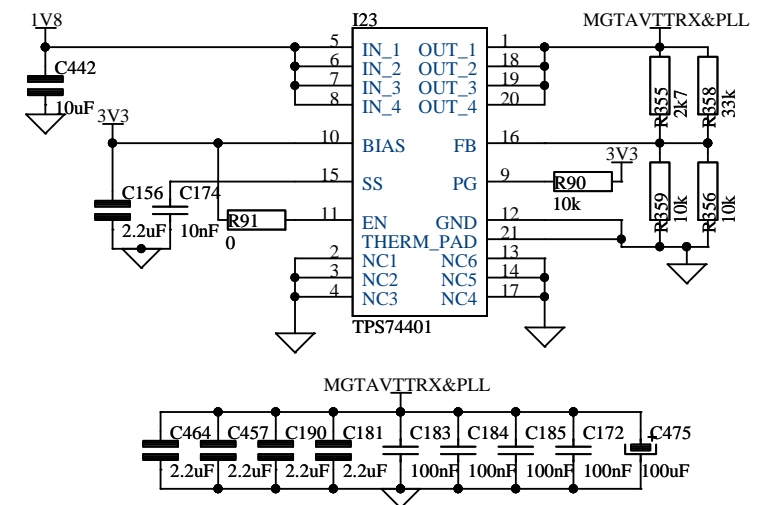
REGULADOR 1V2_PHY



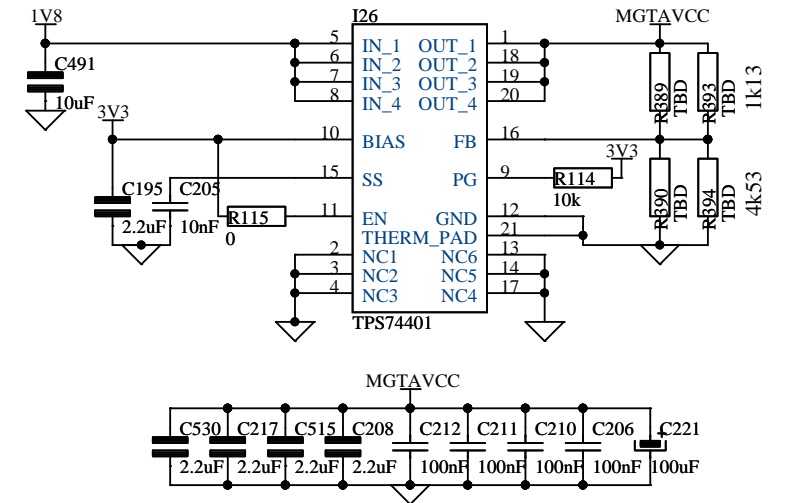
MGTAVTTTX (1V2)





MGTAVTTRX&PLL (1V2)



MGTA VCC (1V)



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	Title X10Giga Project		PCB P.N. 400.0263.00		
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	Observation		Scale	Size A3	Rev A
Monday, June 09, 2008	Engineer <Engineer>	Designer <Designer>	Sheet 1 of 30		

A

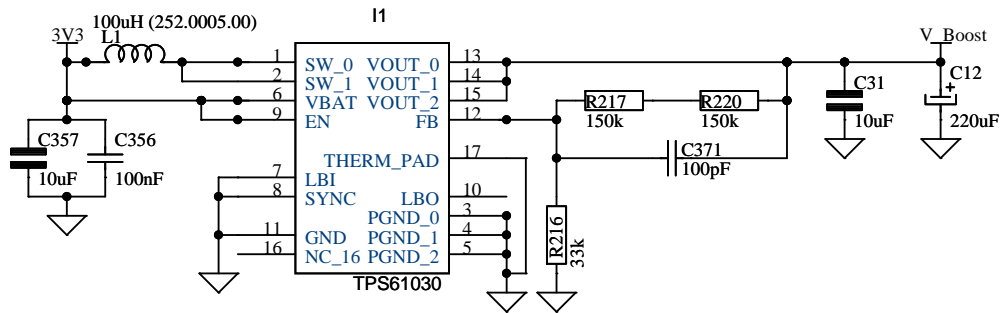
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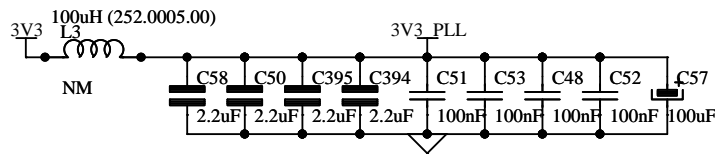
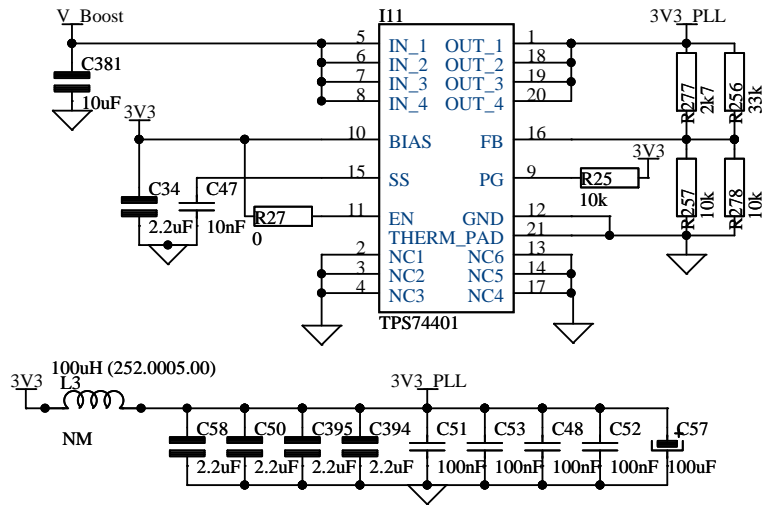
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BOOSTER 5V, 600mA

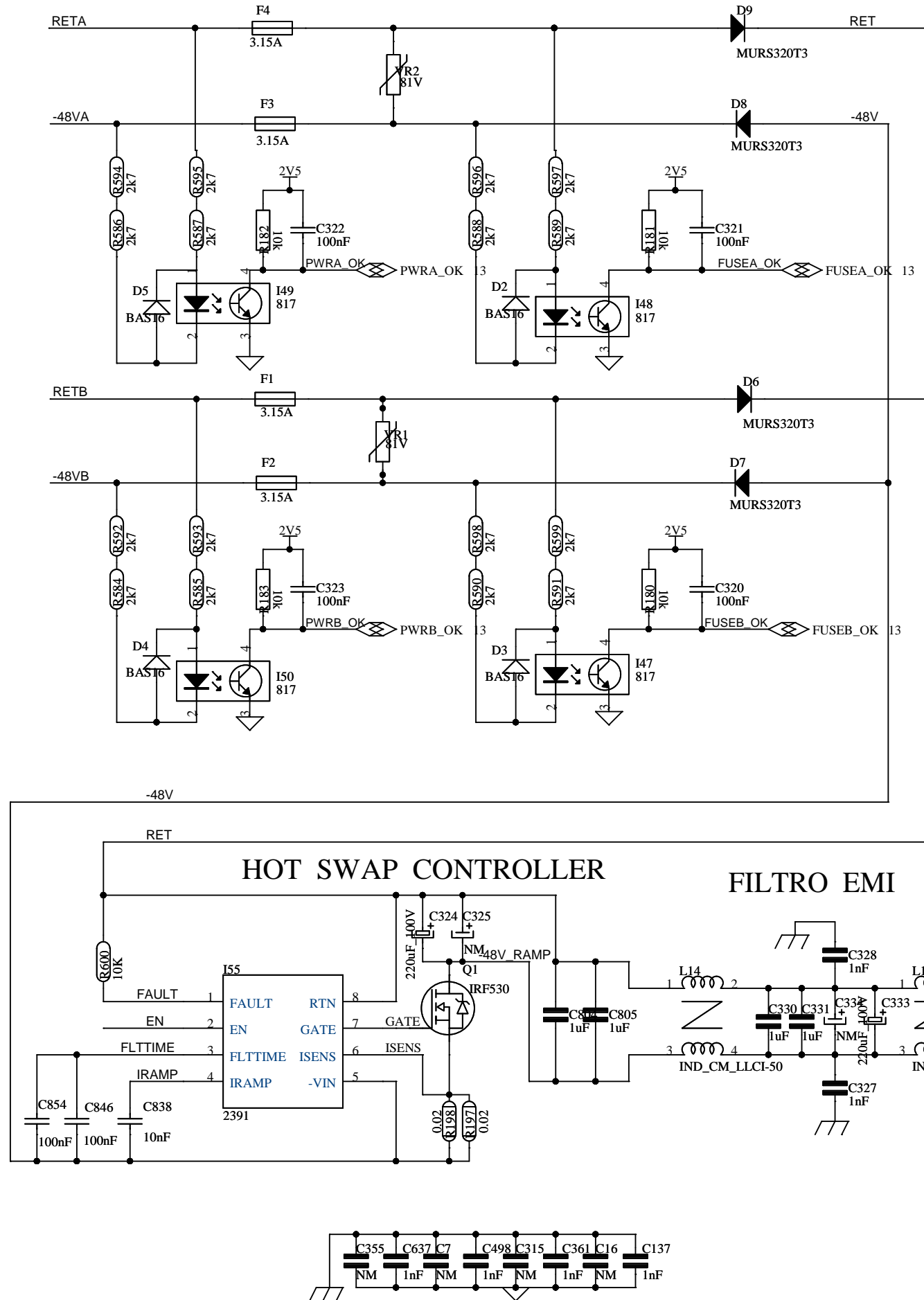


3V3 PLL

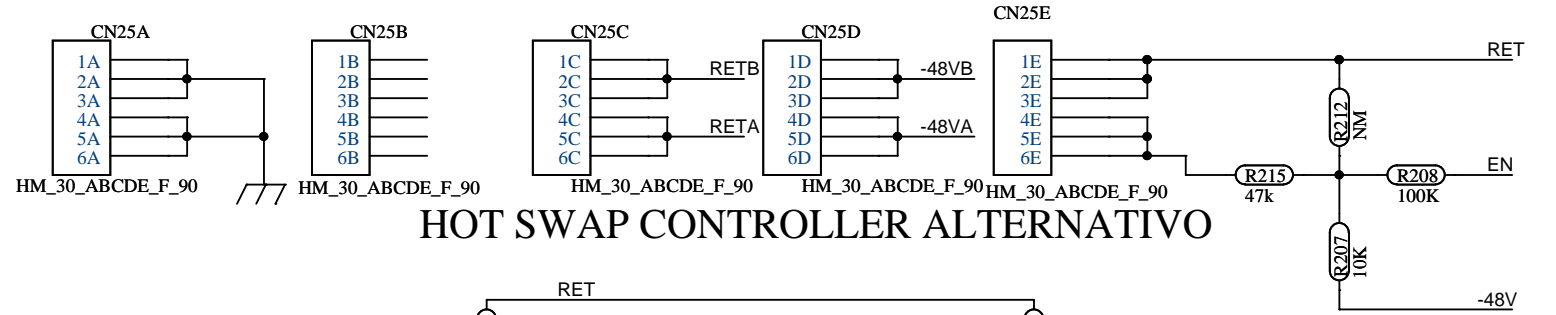


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Monday, June 09, 2008		Engineer <Engineer>	Rev A
		Designer <Designer>	Sheet 2 of 30

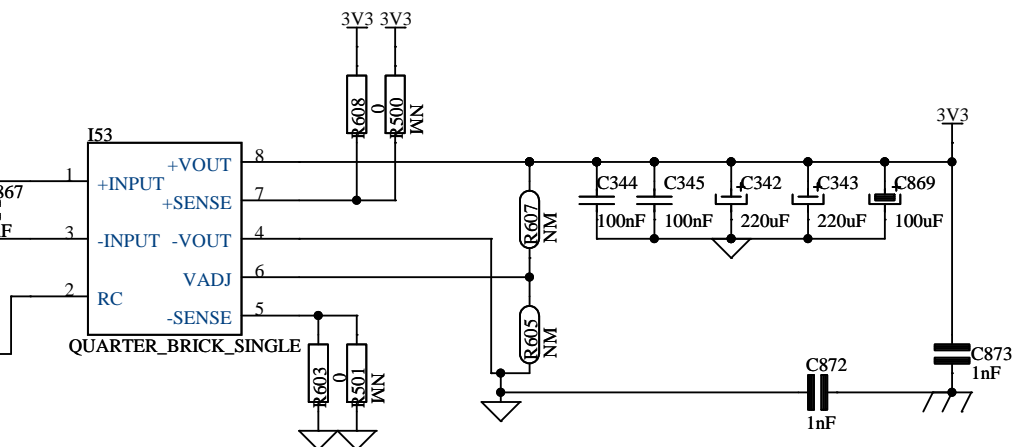
ENTRADA DE ALIMENTAÇÃO



CONECTOR HM POWER

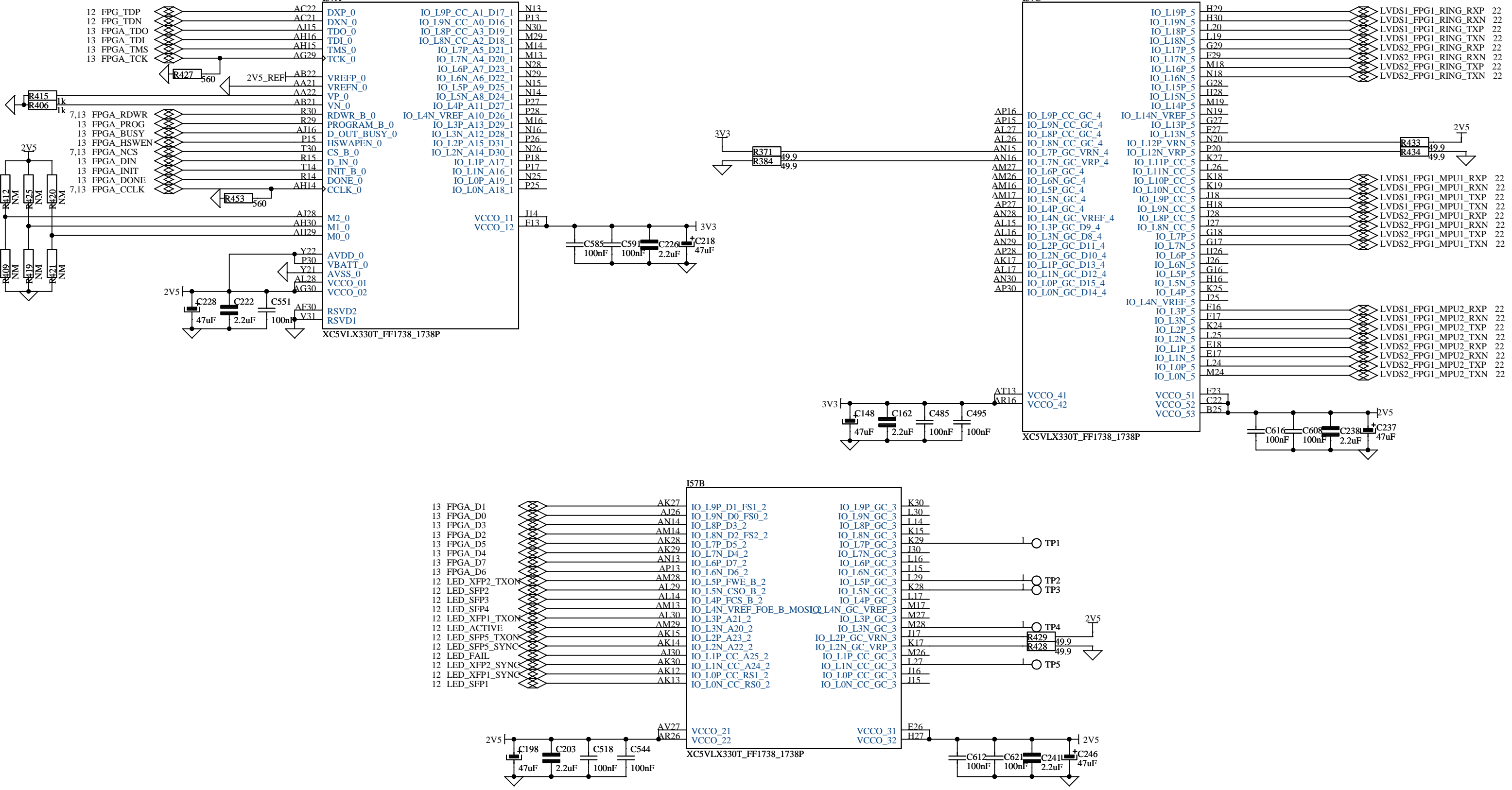




CONVERSOR DC / DC



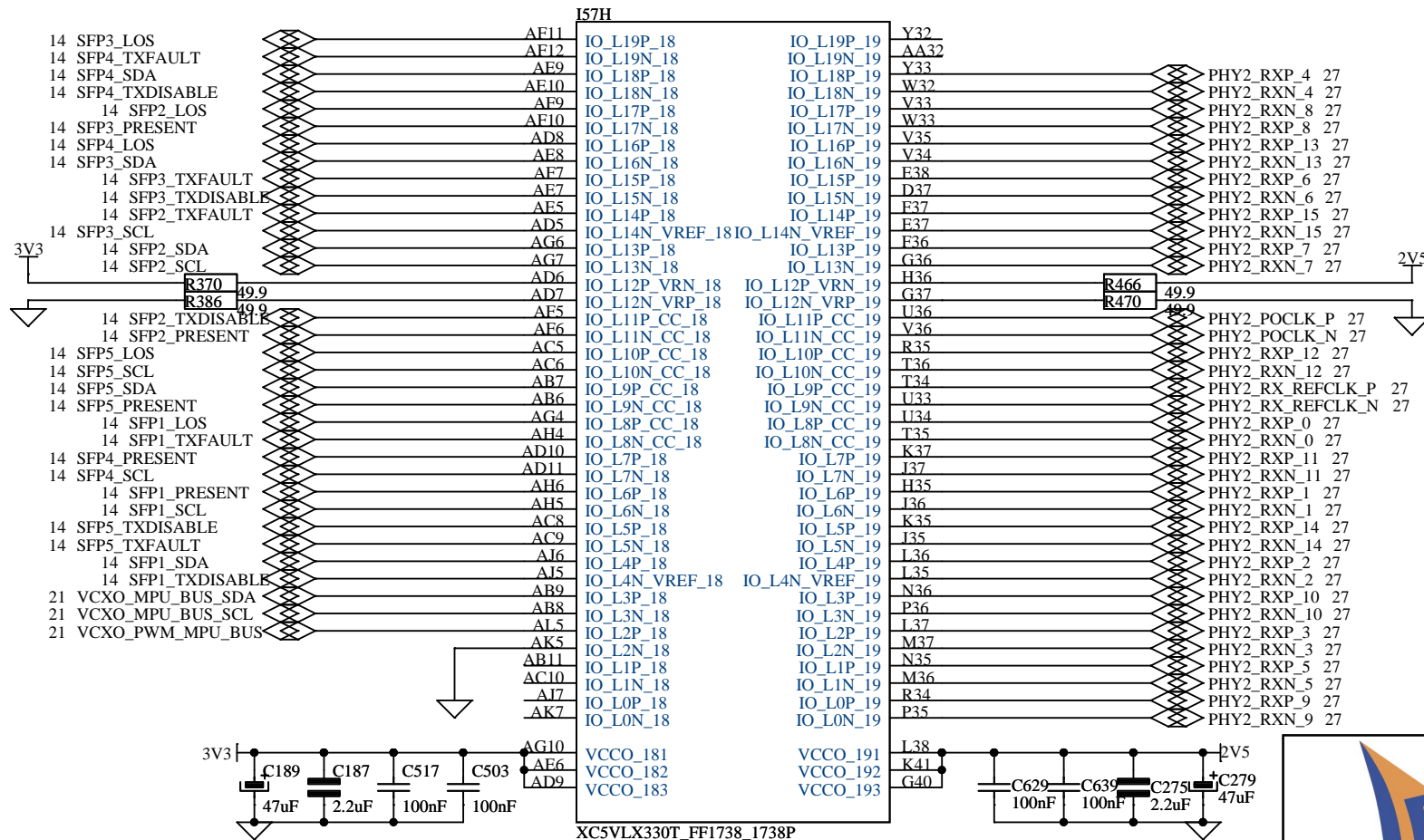
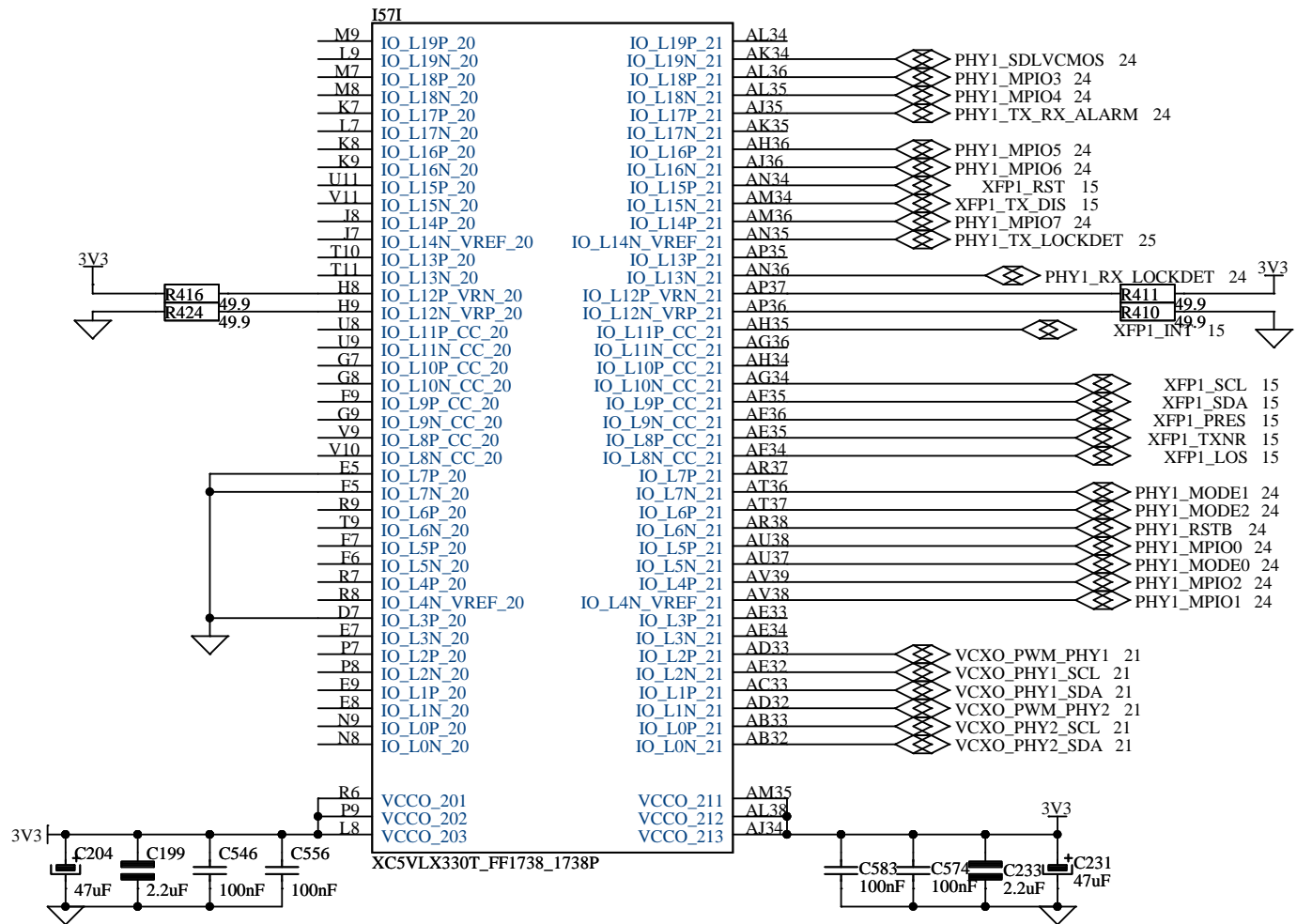
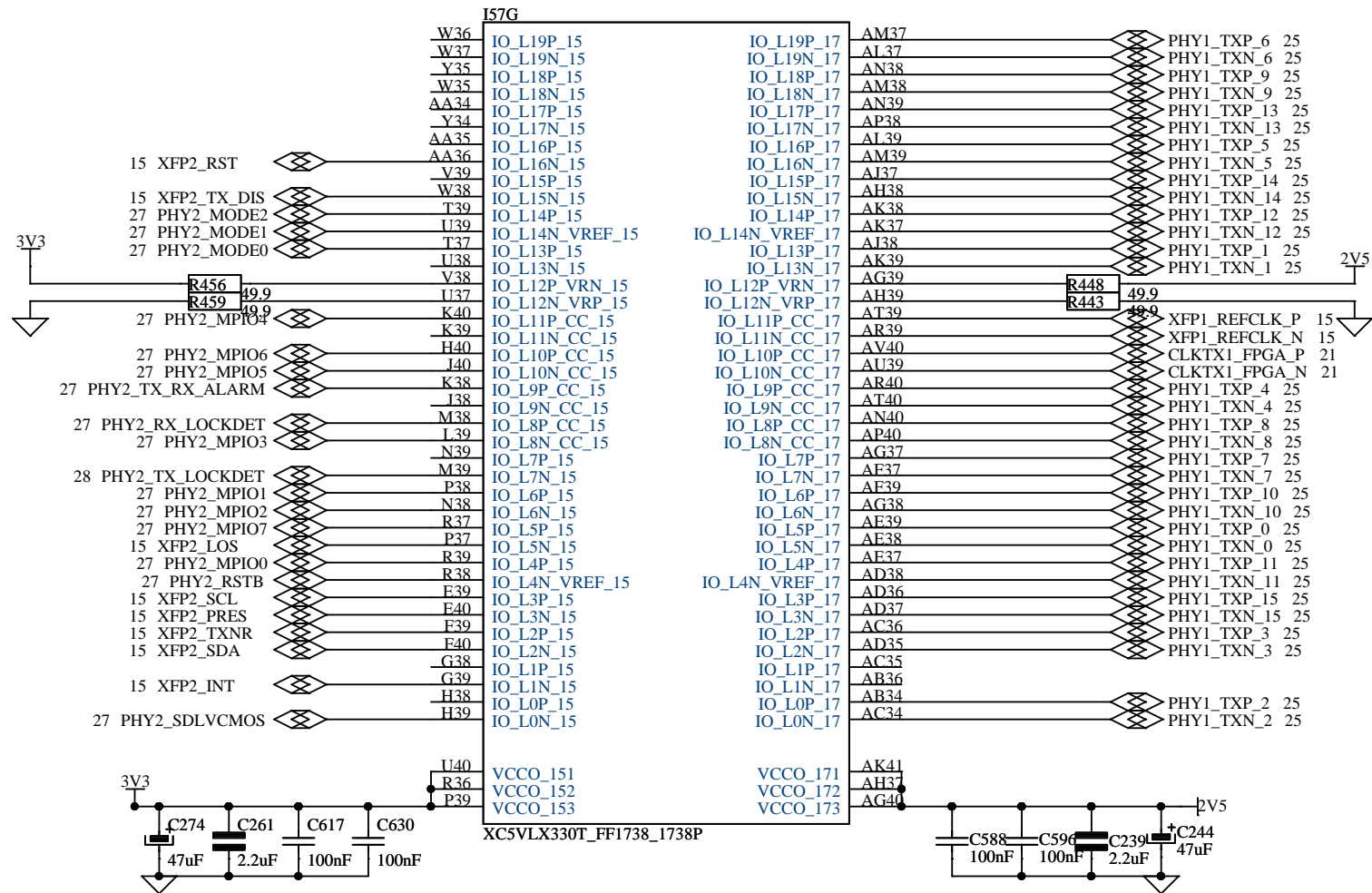
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FPGA_1





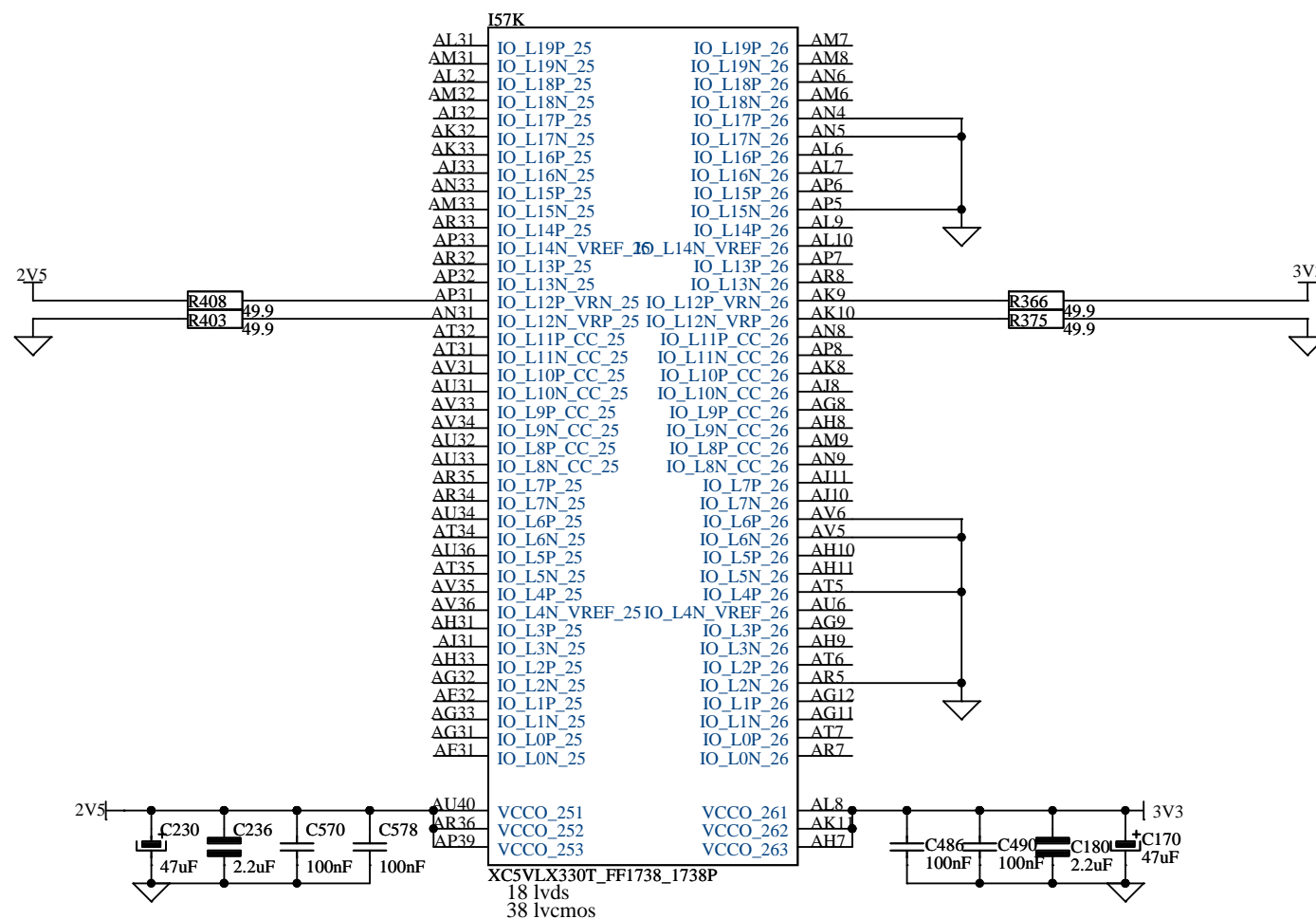
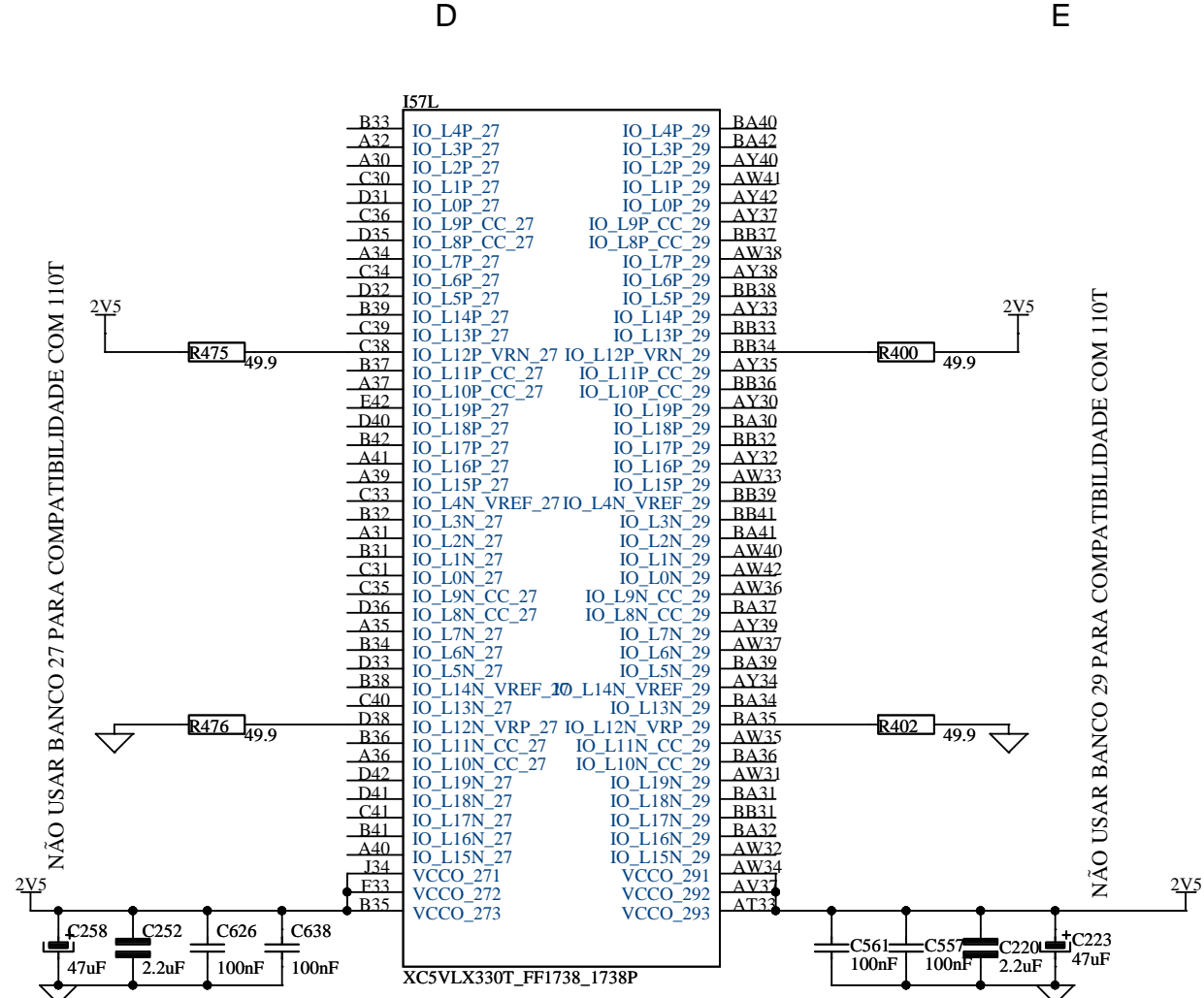
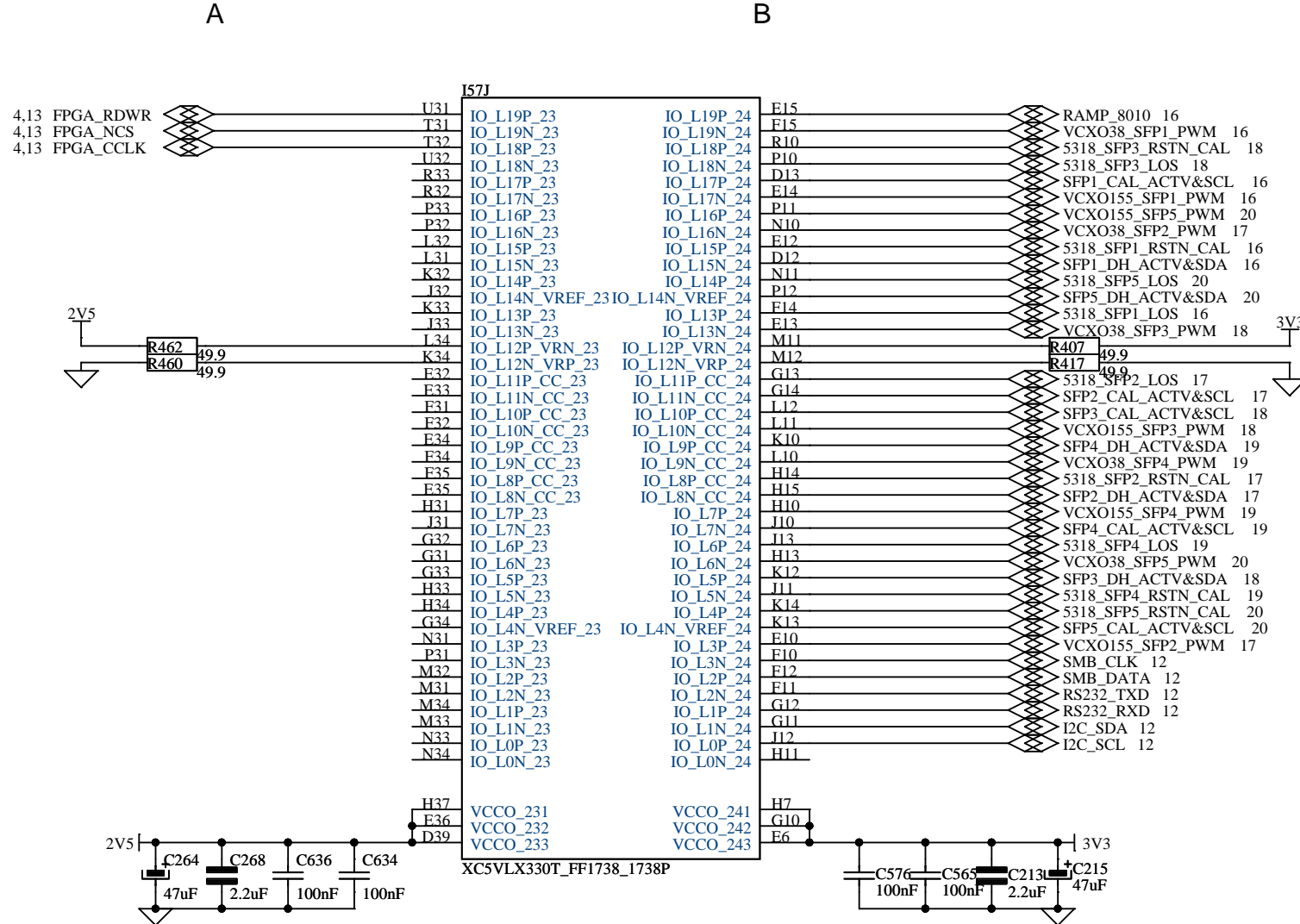
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	Title X10Giga Project		Status		
	Contents FPGA1_1				
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FPGA_3





All RxN/P and TxN/P can be swapped in the same bank, being neighbors

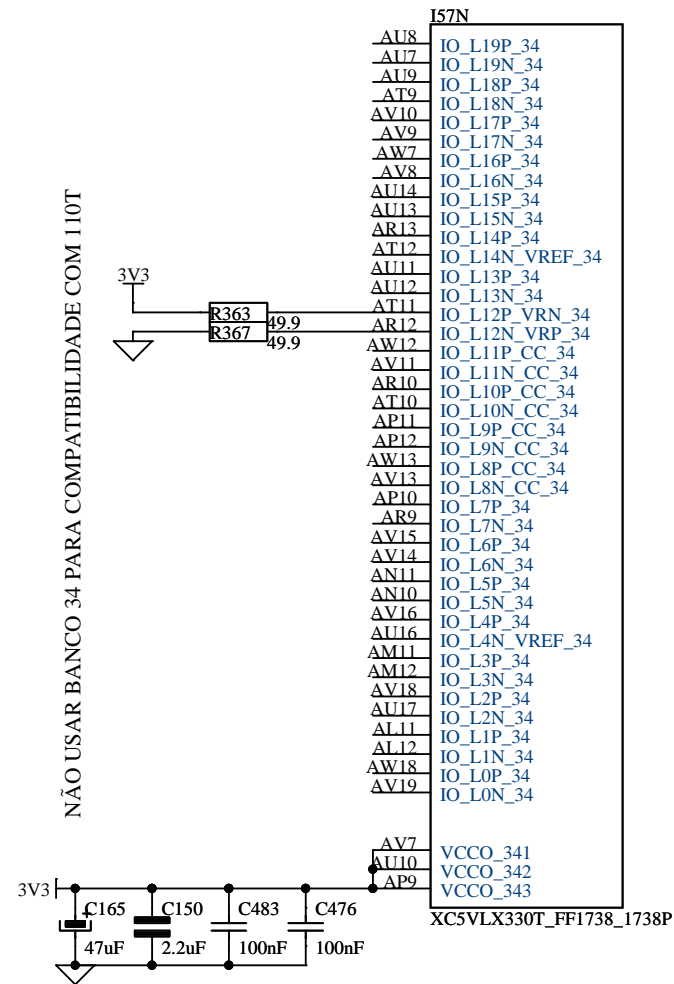
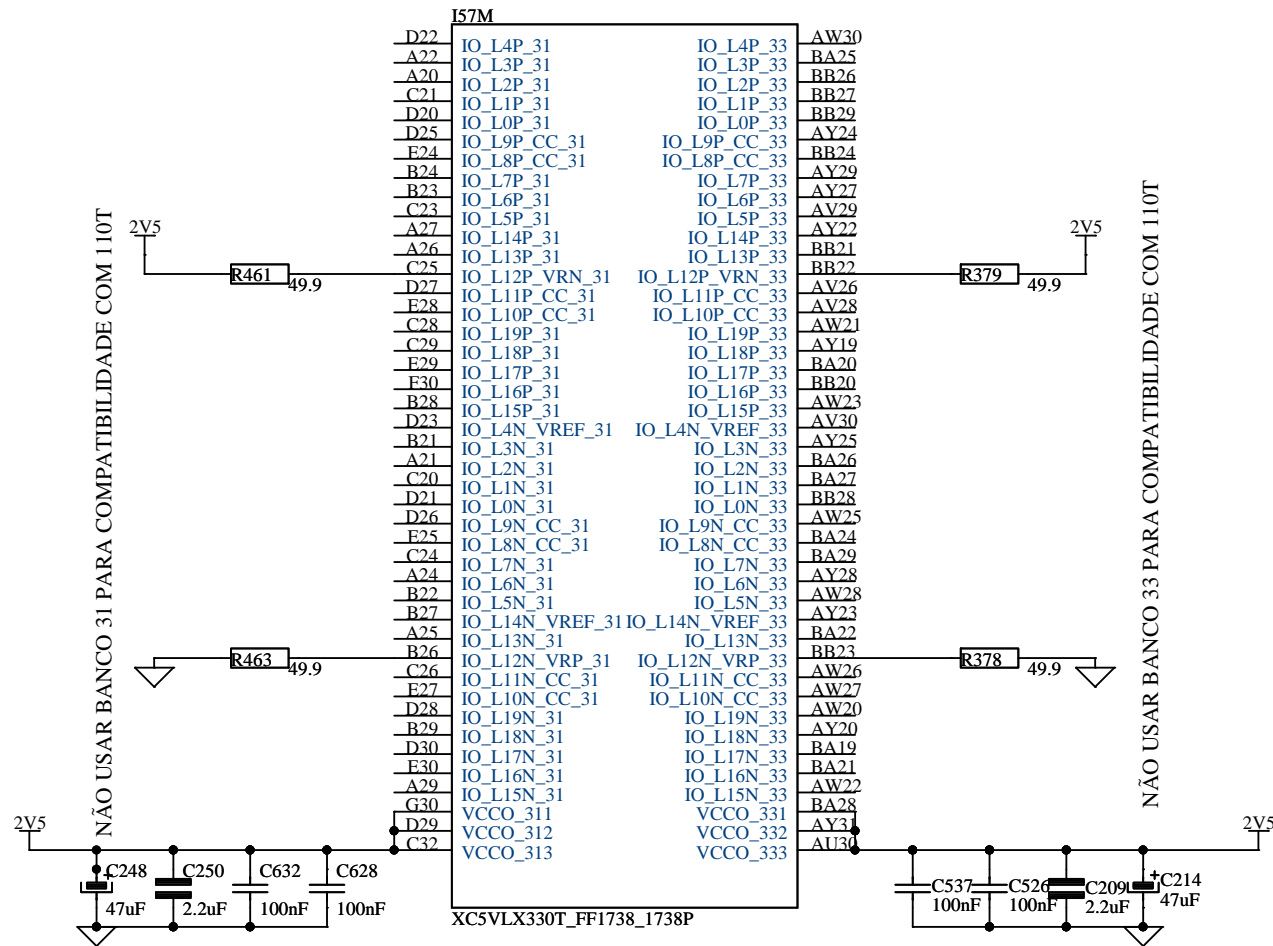
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Observation			Scale	Size A3	Rev A
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FPGA_4

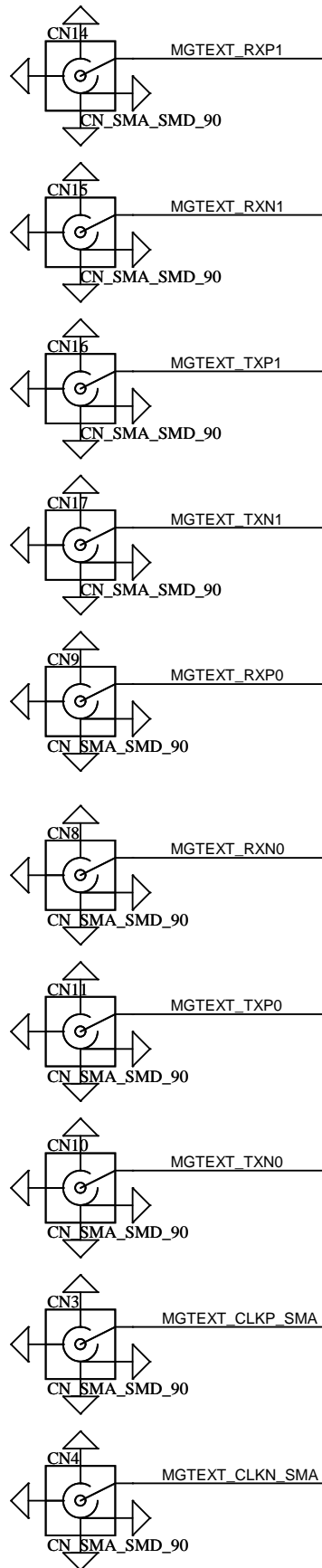
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FPGA_5



 	LESC - Computer Systems Engineer Laboratory Campus do Pici S/N Block 723 Fortaleza, Ceará www.lesc.ufc.br		Project P.N. PD1461	
	Title X10Giga Project		PCB P.N. 400.0263.00	
	Contents FPGA1_5		Status	
	Observation		Scale	Size A3
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CONECTORES EM BOTTOM



MGTEXT_CLKP_SMA|C93 MGTEXT_CLKP
TBD

MGTEXT_CLKN_SMA|C94 MGTEXT_CLKN
TBD

FPGA_6 (GTP_PORTS)

MGTEXT_RXP1	AV1	MGTRXP1_122	MGTRXP1_134
MGTEXT_RXN1	AI1	MGTRXN1_122	MGTRXN1_134
MGTEXT_TXP1	AW2	MGTXP1_122	MGTXP1_134
MGTEXT_TXN1	AV2	MGTXN1_122	MGTXN1_134
MGTEXT_RXP0	AR1	MGTRXP0_122	MGTRXP0_134
MGTEXT_RXN0	AT1	MGTRXN0_122	MGTRXN0_134
MGTEXT_TXP0	AP2	MGTXP0_122	MGTXP0_134
MGTEXT_TXN0	AR2	MGTXN0_122	MGTXN0_134
MGTEXT_CLKP	AT4	MGTRFCLKP_122	MGTRFCLKP_134
MGTEXT_CLKN	AT3	MGTRFCLKN_122	MGTRFCLKN_134
22 RIO_MPU1_2_RXP	H1	MGTRXP1_120	MGTRXP1_132
22 RIO_MPU1_2_RXN	G1	MGTRXN1_120	MGTRXN1_132
22 RIO_MPU1_2_TXP	J2	MGTXP1_120	MGTXP1_132
22 RIO_MPU1_2_TXN	H2	MGTXN1_120	MGTXN1_132
22 RIO_MPU1_1_RXP	E1	MGTRXP0_120	MGTRXP0_132
22 RIO_MPU1_1_RXN	F1	MGTRXN0_120	MGTRXN0_132
22 RIO_MPU1_1_TXP	D2	MGTXP0_120	MGTXP0_132
22 RIO_MPU1_1_TXN	E2	MGTXN0_120	MGTXN0_132
21 VCXO_MPU_BUS_P	F4	MGTRFCLKP_120	MGTRFCLKP_132
21 VCXO_MPU_BUS_N	E3	MGTRFCLKN_120	MGTRFCLKN_132
22 RIO_MATE_4_RXP	AM1	MGTRXP1_118	MGTRXP1_130
22 RIO_MATE_4_RXN	AI1	MGTRXN1_118	MGTRXN1_130
22 RIO_MATE_4_TXP	AN2	MGTXP1_118	MGTXP1_130
22 RIO_MATE_4_TXN	AM2	MGTXN1_118	MGTXN1_130
14 SFP4_MGT_RX_P	AI1	MGTRXP0_118	MGTRXP0_130
14 SFP4_MGT_RX_N	AK1	MGTRXN0_118	MGTRXN0_130
14 SFP4_MGT_TX_N	AH2	MGTXP0_118	MGTXP0_130
14 SFP4_MGT_TX_P	AI2	MGTXN0_118	MGTXN0_130
19 CLK155M_SFP4_P	AK4	MGTRFCLKP_118	MGTRFCLKP_130
19 CLK155M_SFP4_N	AK3	MGTRFCLKN_118	MGTRFCLKN_130
22 RIO_MATE_1_RXP	P1	MGTRXP1_116	MGTRXP1_128
22 RIO_MATE_1_RXN	N1	MGTRXN1_116	MGTRXN1_128
22 RIO_MATE_1_TXP	R2	MGTXP1_116	MGTXP1_128
22 RIO_MATE_1_TXN	P2	MGTXN1_116	MGTXN1_128
14 SFP1_MGT_RX_P	L1	MGTRXP0_116	MGTRXP0_128
14 SFP1_MGT_RX_N	M1	MGTRXN0_116	MGTRXN0_128
14 SFP1_MGT_TX_N	K2	MGTXP0_116	MGTXP0_128
14 SFP1_MGT_TX_P	L2	MGTXN0_116	MGTXN0_128
16 CLK155M_SFP1_P	M4	MGTRFCLKP_116	MGTRFCLKP_128
16 CLK155M_SFP1_N	M3	MGTRFCLKN_116	MGTRFCLKN_128
22 RIO_MATE_3_RXP	AE1	MGTRXP1_114	MGTRXP1_126
22 RIO_MATE_3_RXN	AE1	MGTRXN1_114	MGTRXN1_126
22 RIO_MATE_3_TXP	AG2	MGTXP1_114	MGTXP1_126
22 RIO_MATE_3_TXN	AE2	MGTXN1_114	MGTXN1_126
14 SFP3_MGT_RX_P	AC1	MGTRXP0_114	MGTRXP0_126
14 SFP3_MGT_RX_N	AD1	MGTRXN0_114	MGTRXN0_126
14 SFP3_MGT_TX_N	AB2	MGTXP0_114	MGTXP0_126
14 SFP3_MGT_TX_P	AC2	MGTXN0_114	MGTXN0_126
18 CLK155M_SFP3_P	AD4	MGTRFCLKP_114	MGTRFCLKP_126
18 CLK155M_SFP3_N	AD3	MGTRFCLKN_114	MGTRFCLKN_126
22 RIO_MATE_2_RXP	Y1	MGTRXP1_112	MGTRXP1_124
22 RIO_MATE_2_RXN	W1	MGTRXN1_112	MGTRXN1_124
22 RIO_MATE_2_TXP	AA2	MGTXP1_112	MGTXP1_124
22 RIO_MATE_2_TXN	Y2	MGTXN1_112	MGTXN1_124
14 SFP2_MGT_RX_P	U1	MGTRXP0_112	MGTRXP0_124
14 SFP2_MGT_RX_N	V1	MGTRXN0_112	MGTRXN0_124
14 SFP2_MGT_TX_N	T2	MGTXP0_112	MGTXP0_124
14 SFP2_MGT_TX_P	U2	MGTXN0_112	MGTXN0_124
17 CLK155M_SFP2_P	V4	MGTRFCLKP_112	MGTRFCLKP_124
17 CLK155M_SFP2_N	V3	MGTRFCLKN_112	MGTRFCLKN_124
MGTAVTTRX&PLL	AB4	MGTRREF_112	MGTRREF_112

1570



XC5VLX330T_FF1738_1738P

NÃO USAR BANCO 134
PARA OS SFPs

NÃO USAR BANCO 130
PARA OS SFPs

NÃO USAR BANCO 132
PARA OS SFPs

NÃO USAR BANCO 128
PARA OS SFPs

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			PCB P.N. 400.0263.00		
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Monday, June 09, 2008	Engineer <Engineer>	Designer <Designer>	Sheet 9 of 30		

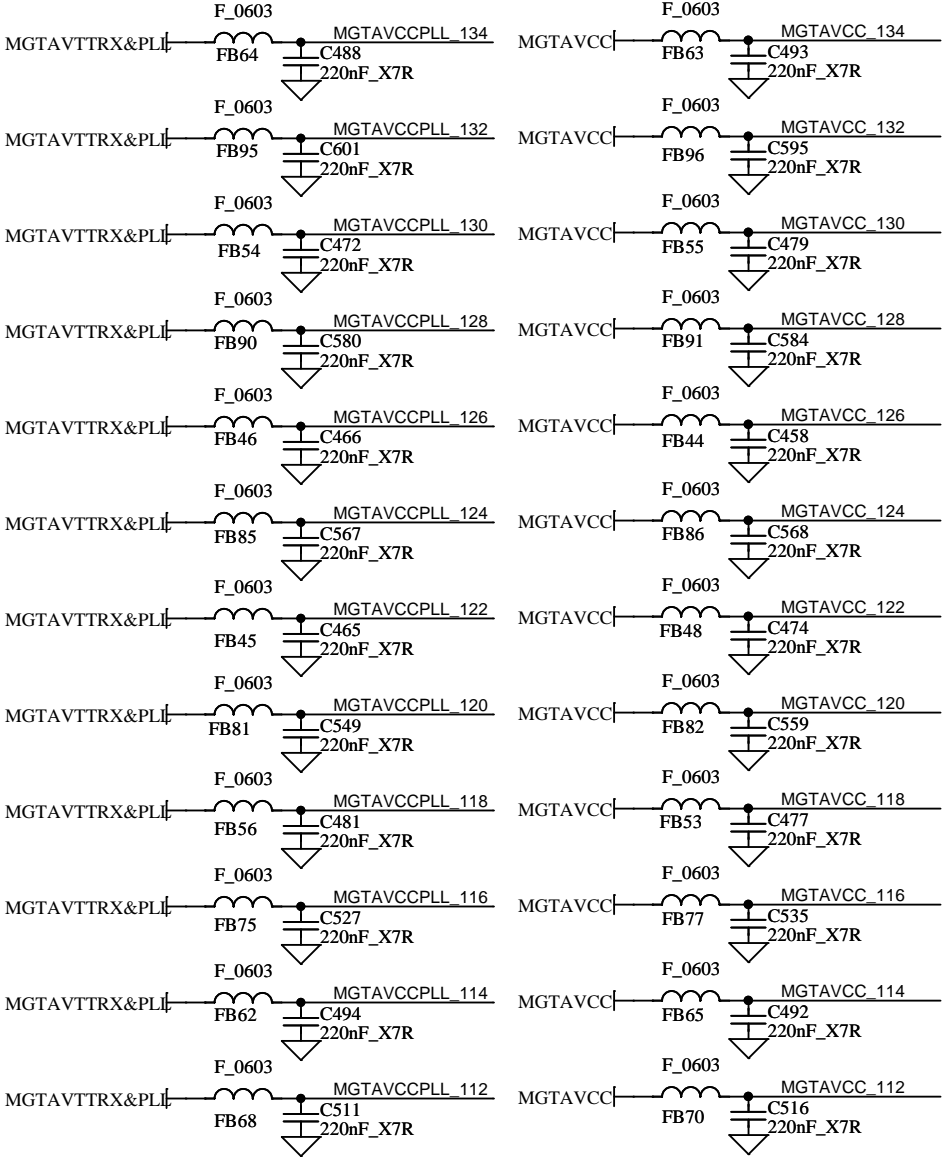
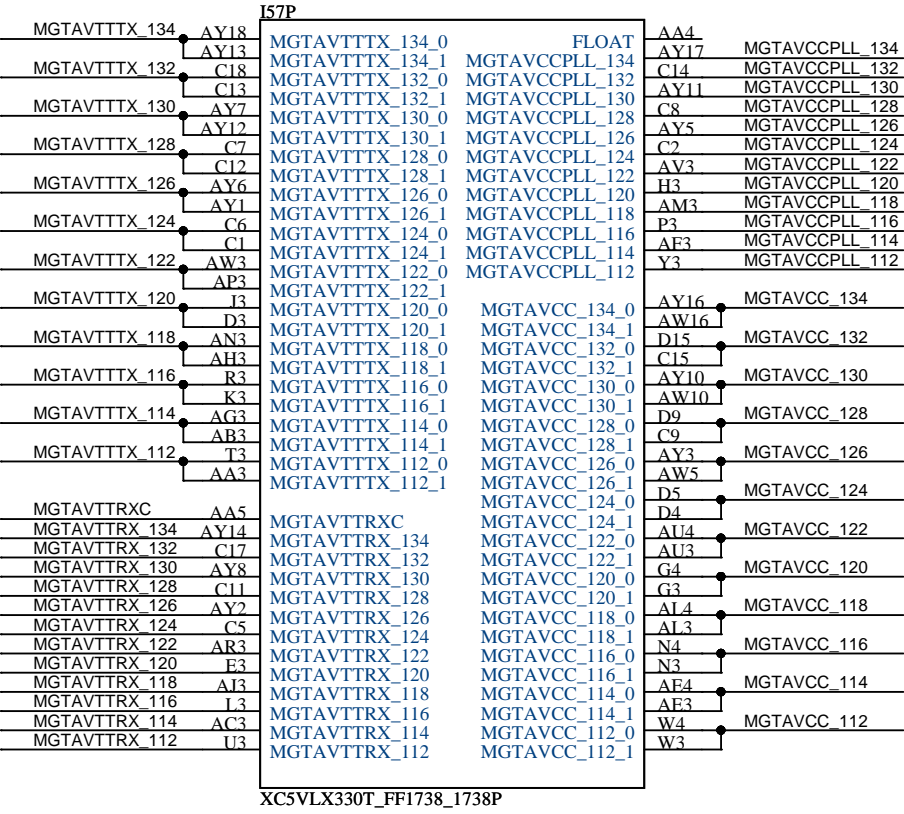
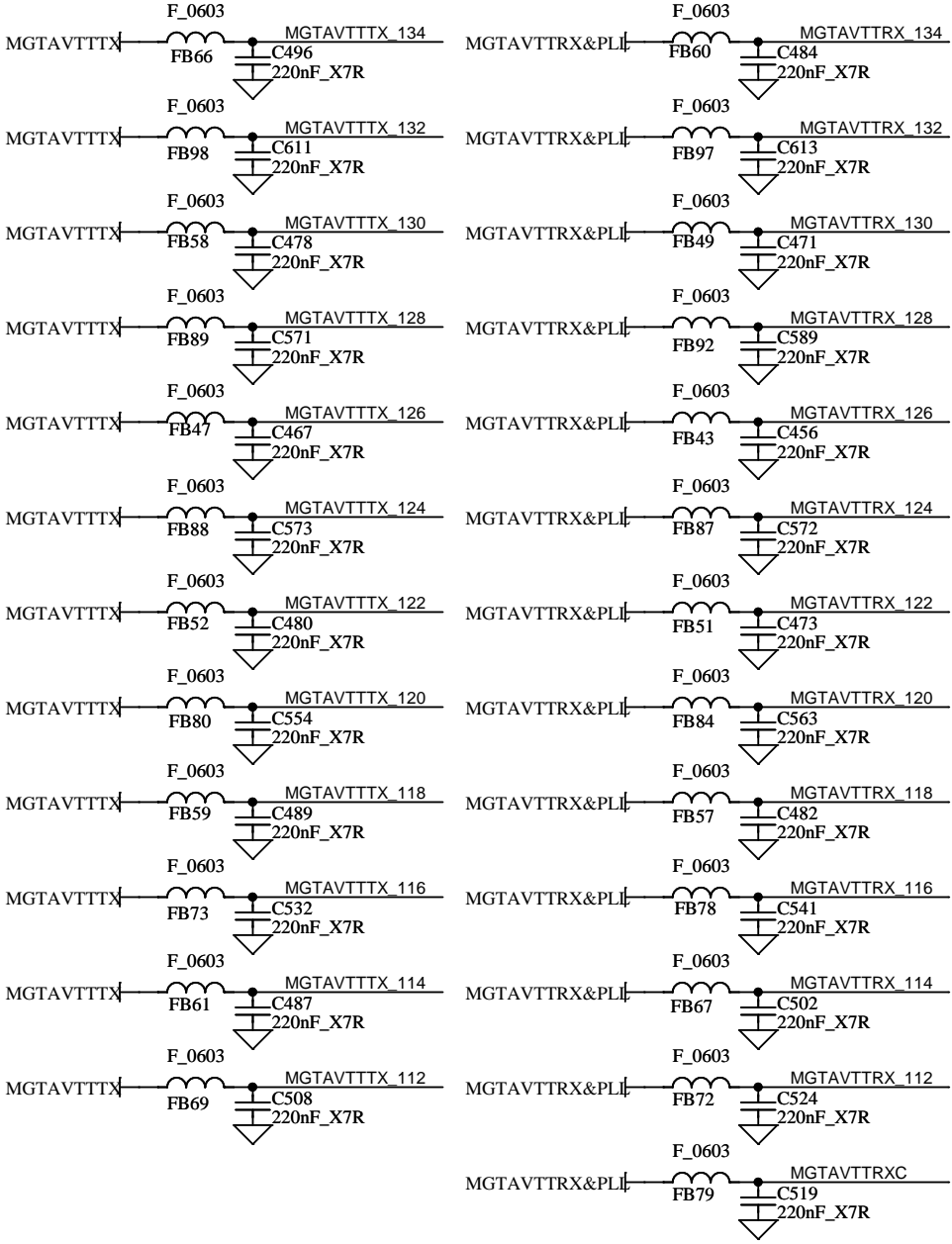
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FPGA_8 (GTP_POWER)



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Monday, June 09, 2008	Engineer <Engineer>	Designer <Designer>	Sheet 11	Rev A

4

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A

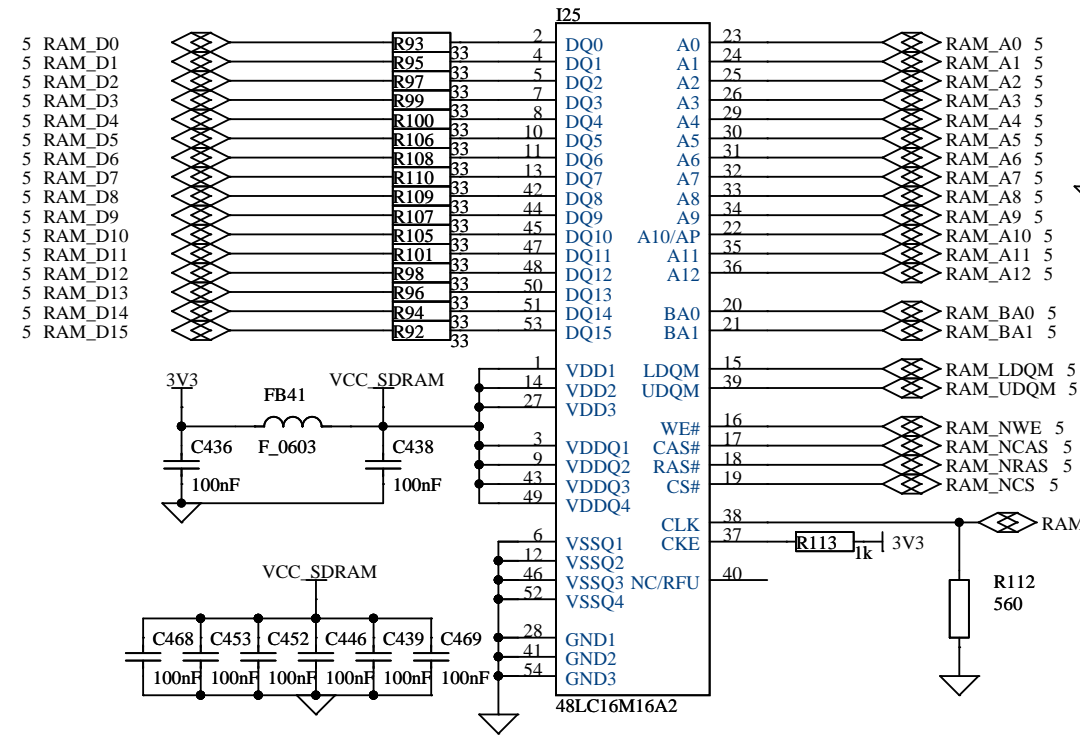
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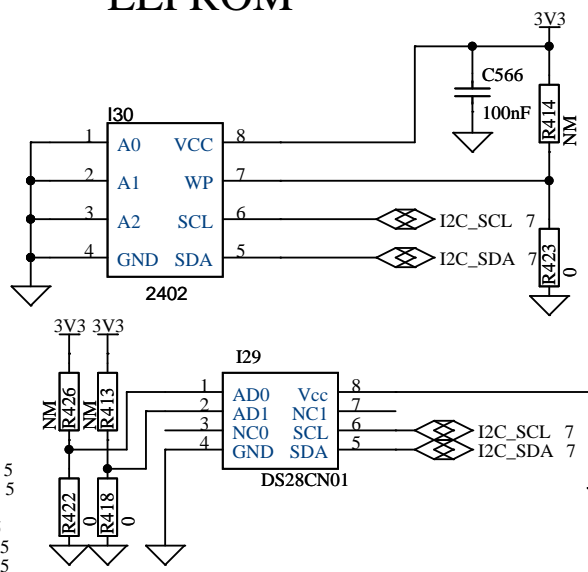
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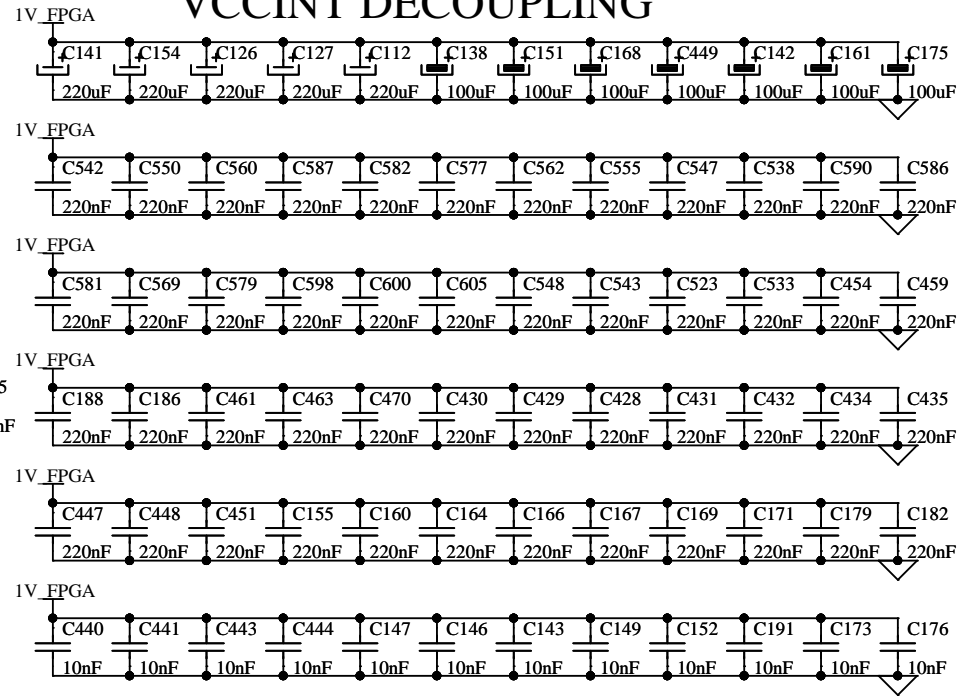
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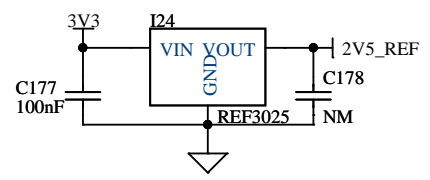
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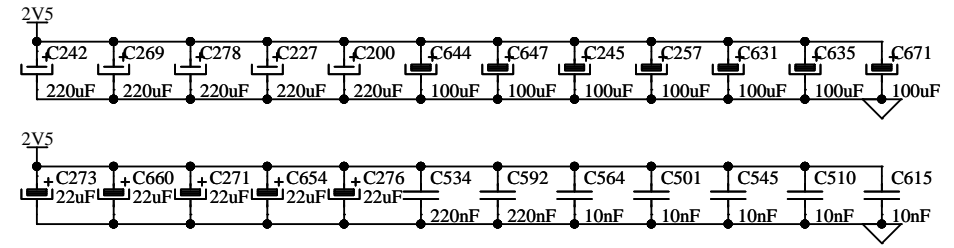
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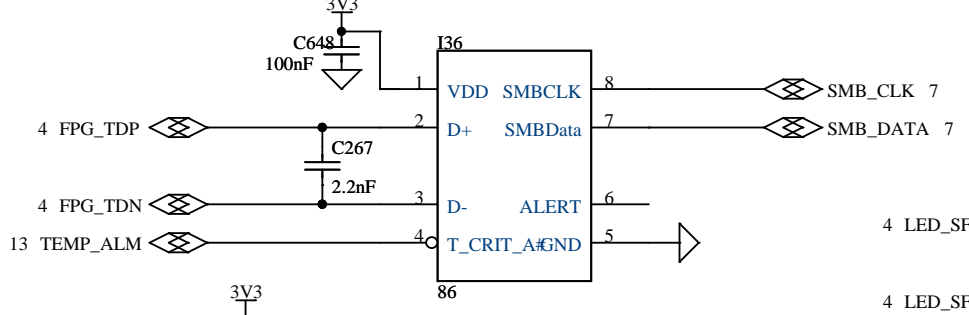
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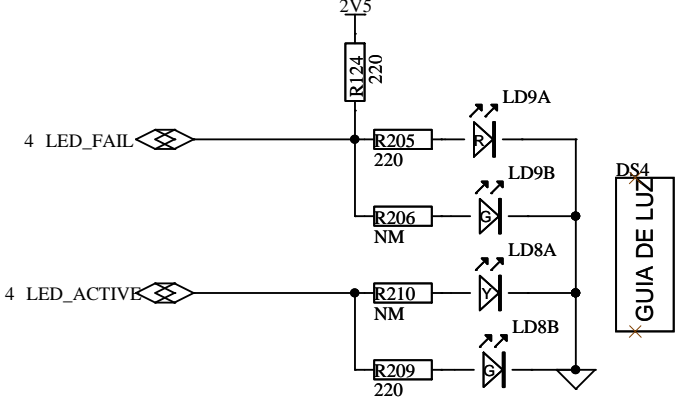
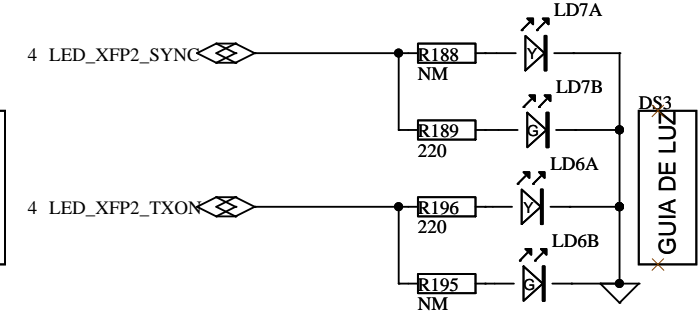
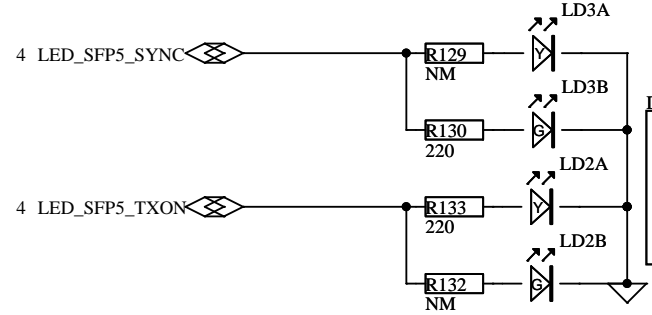
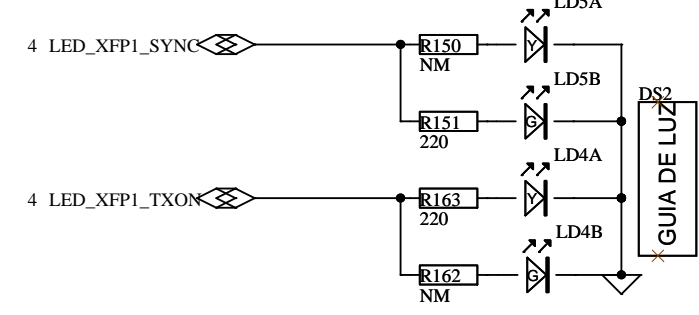
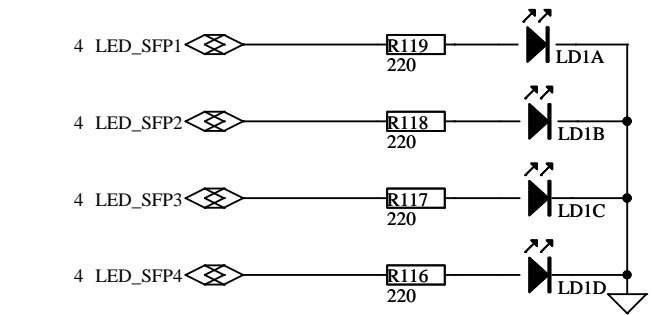
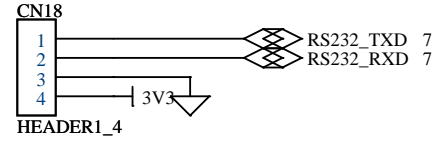
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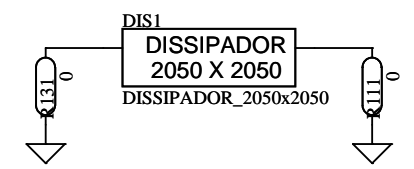
SUPERVISORES DE TEMPERATURA





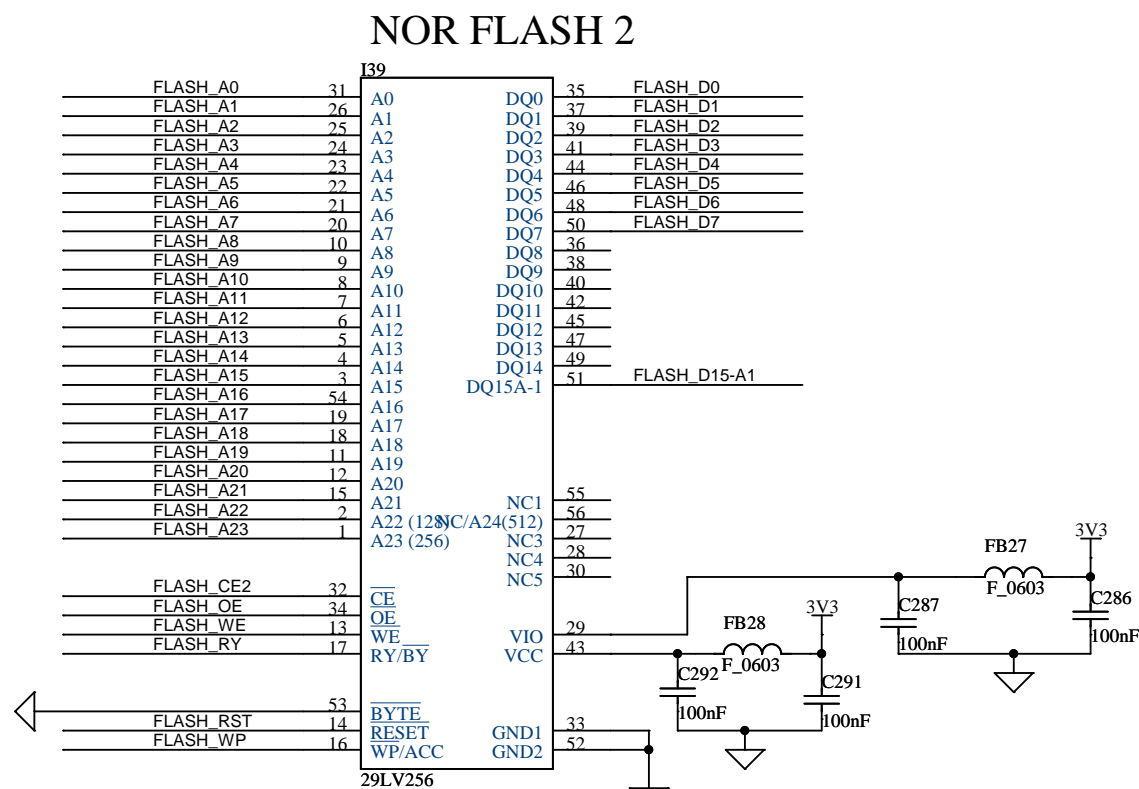
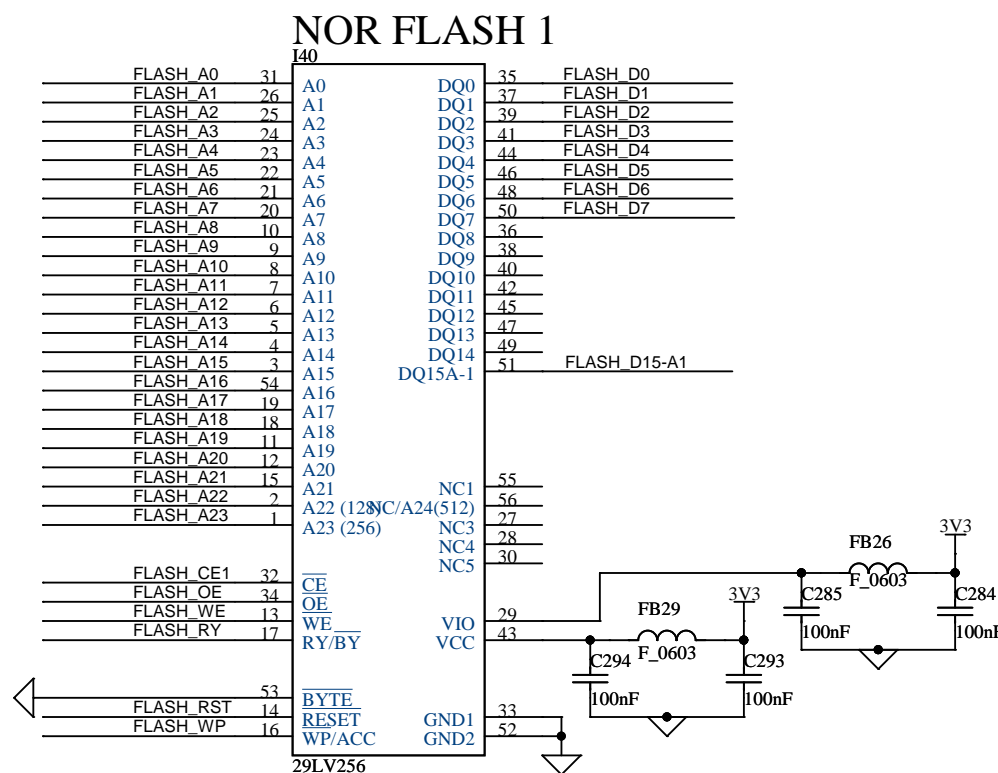
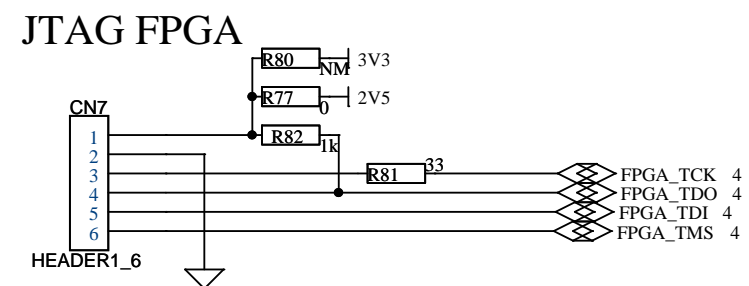
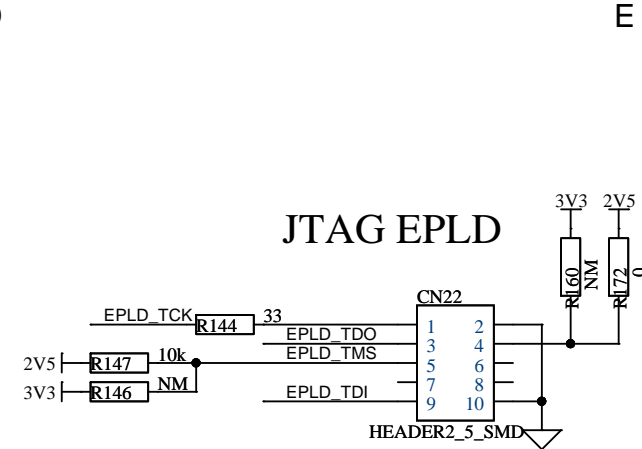
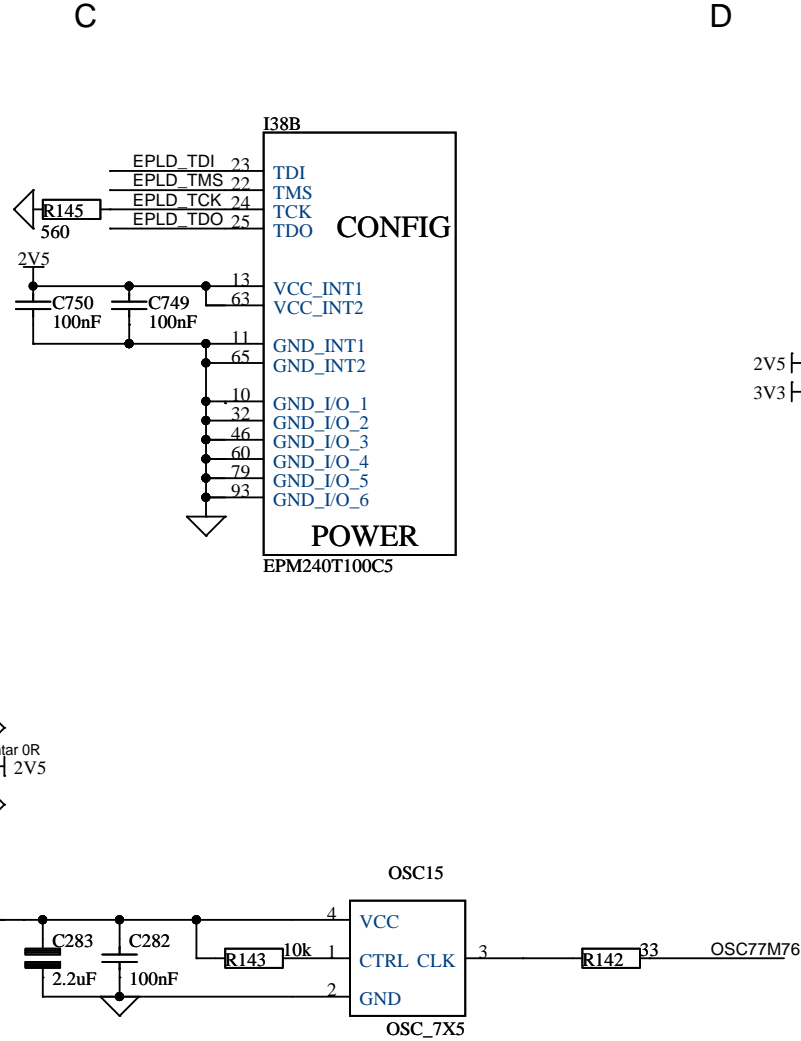
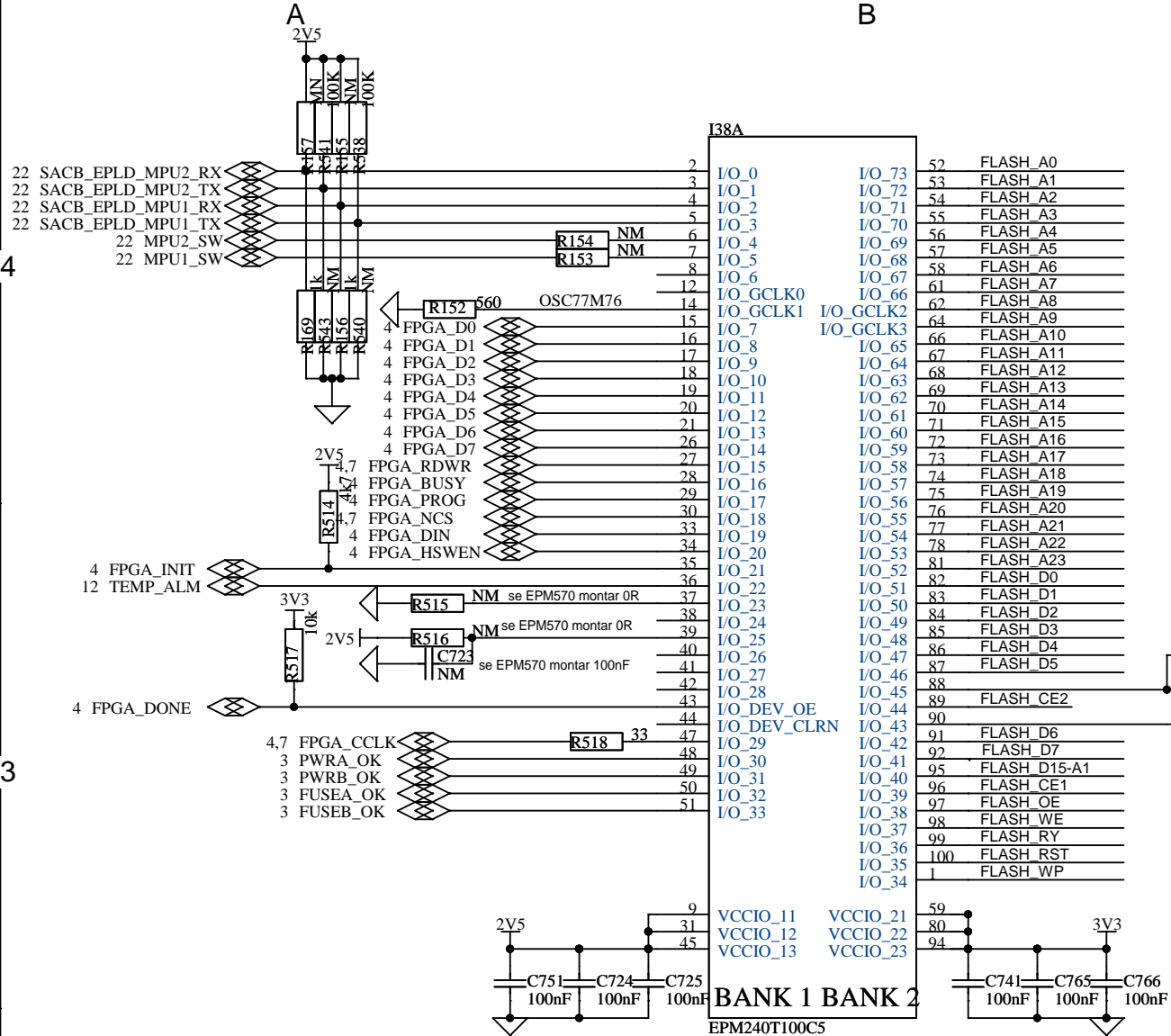
SERIAL DEBUG





FPGA_9 (DIVERSOS)



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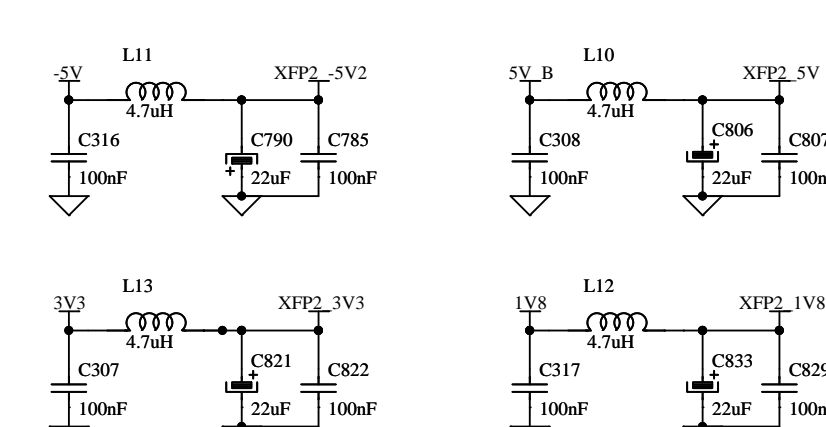
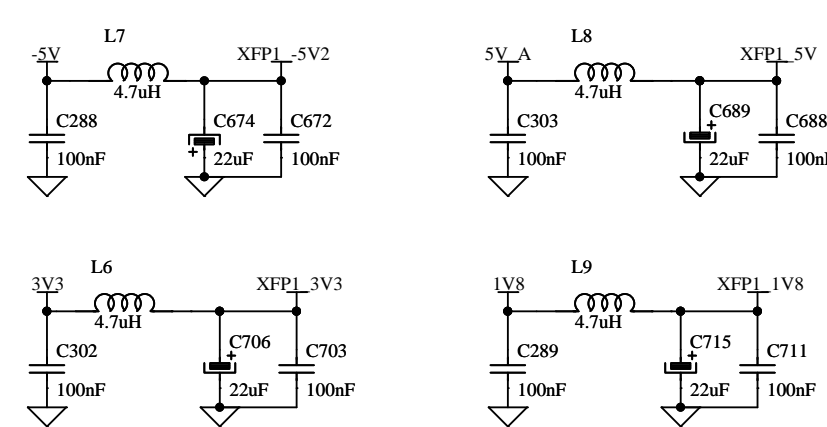
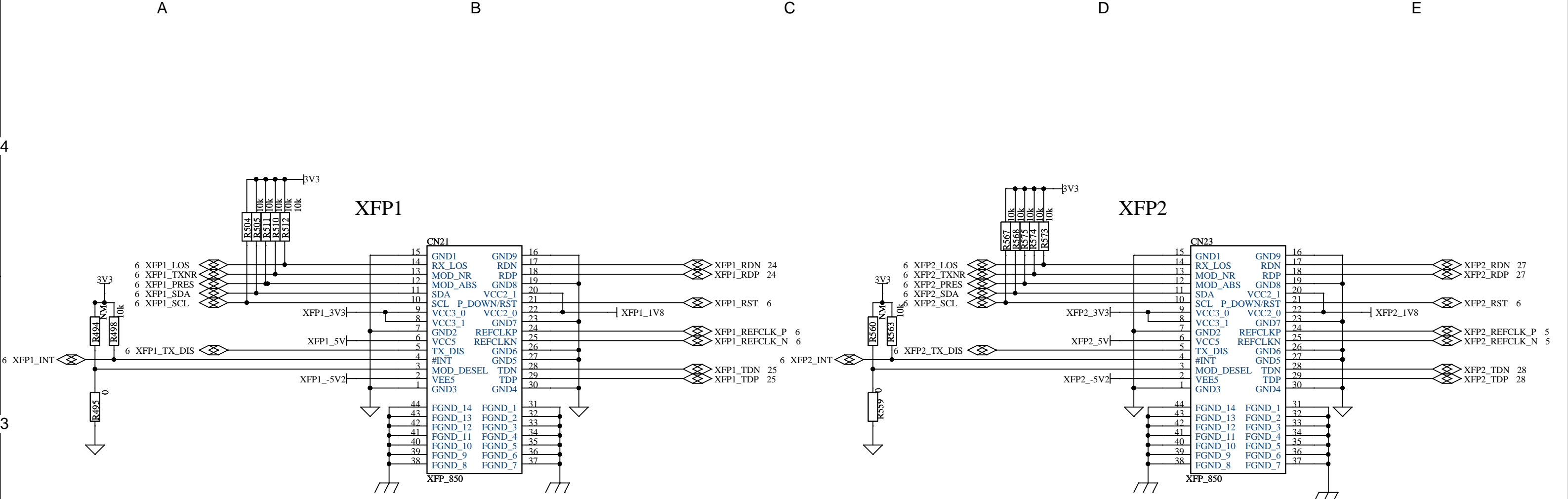
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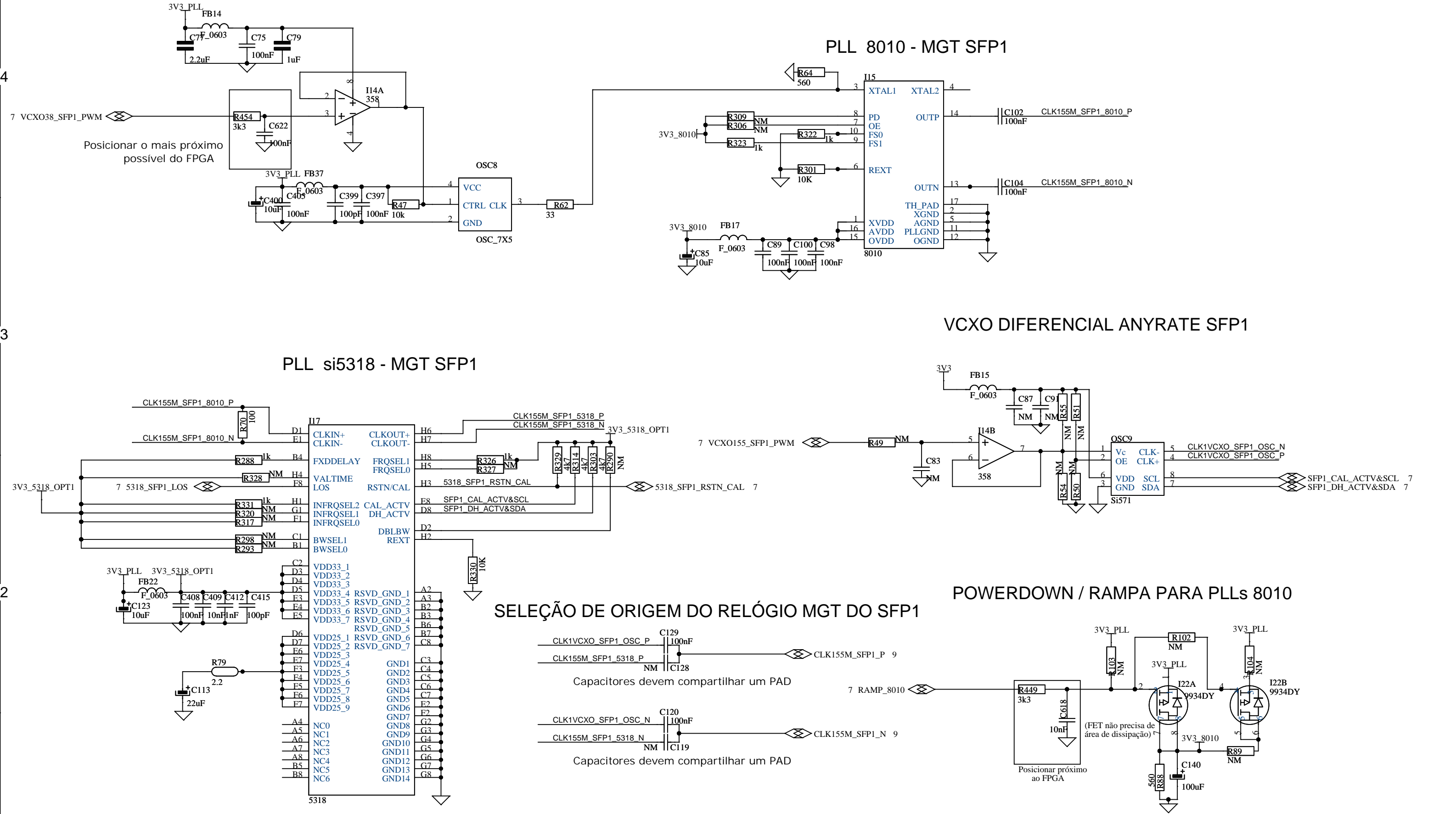
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GERAÇÃO DE RELÓGIO PARA MGT DO SFP1

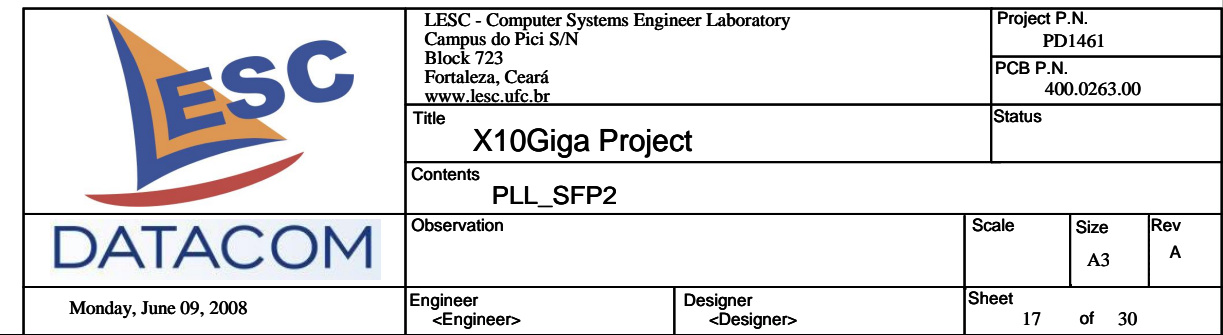


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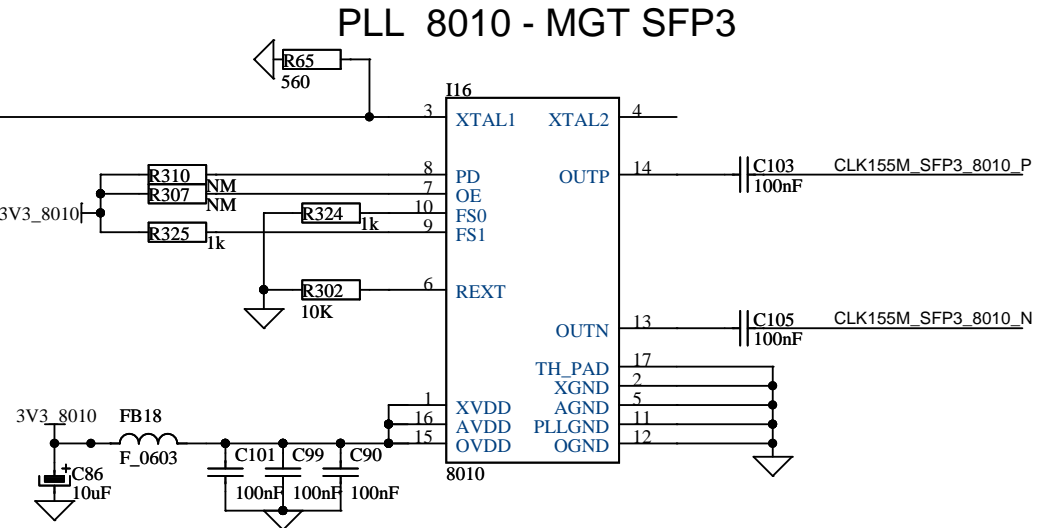
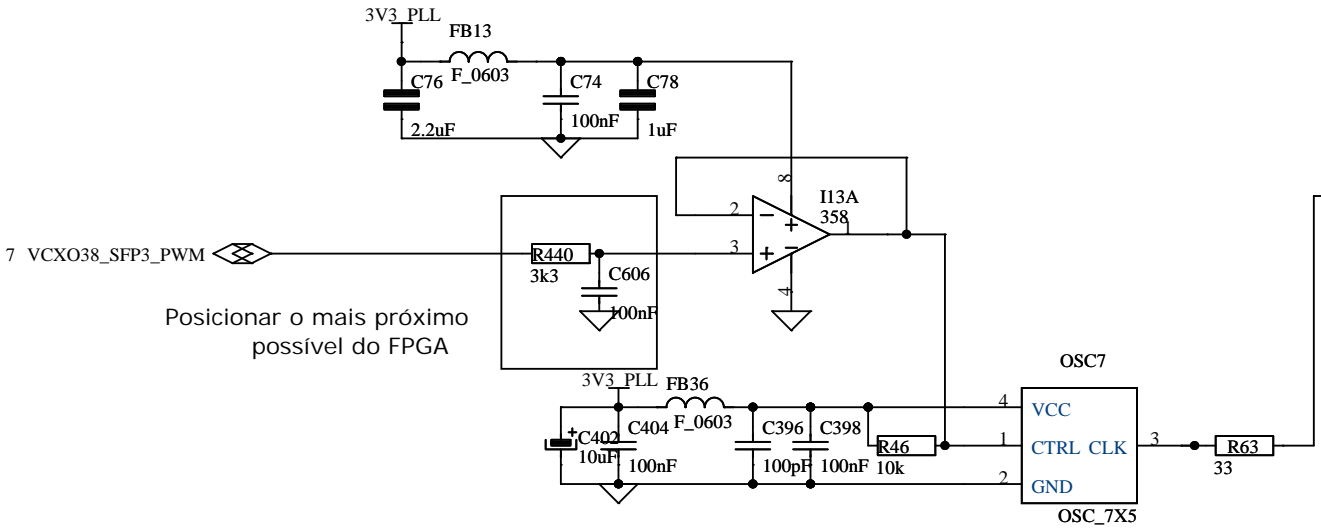
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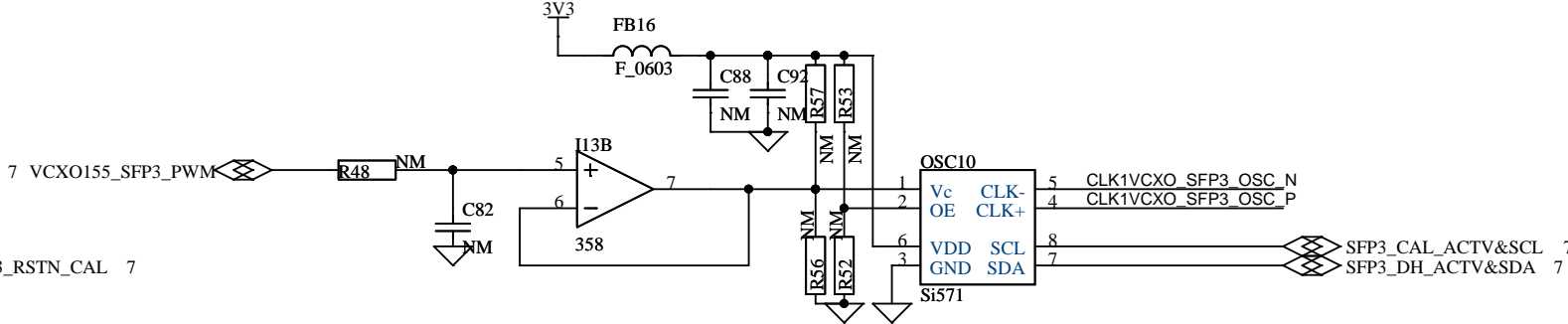
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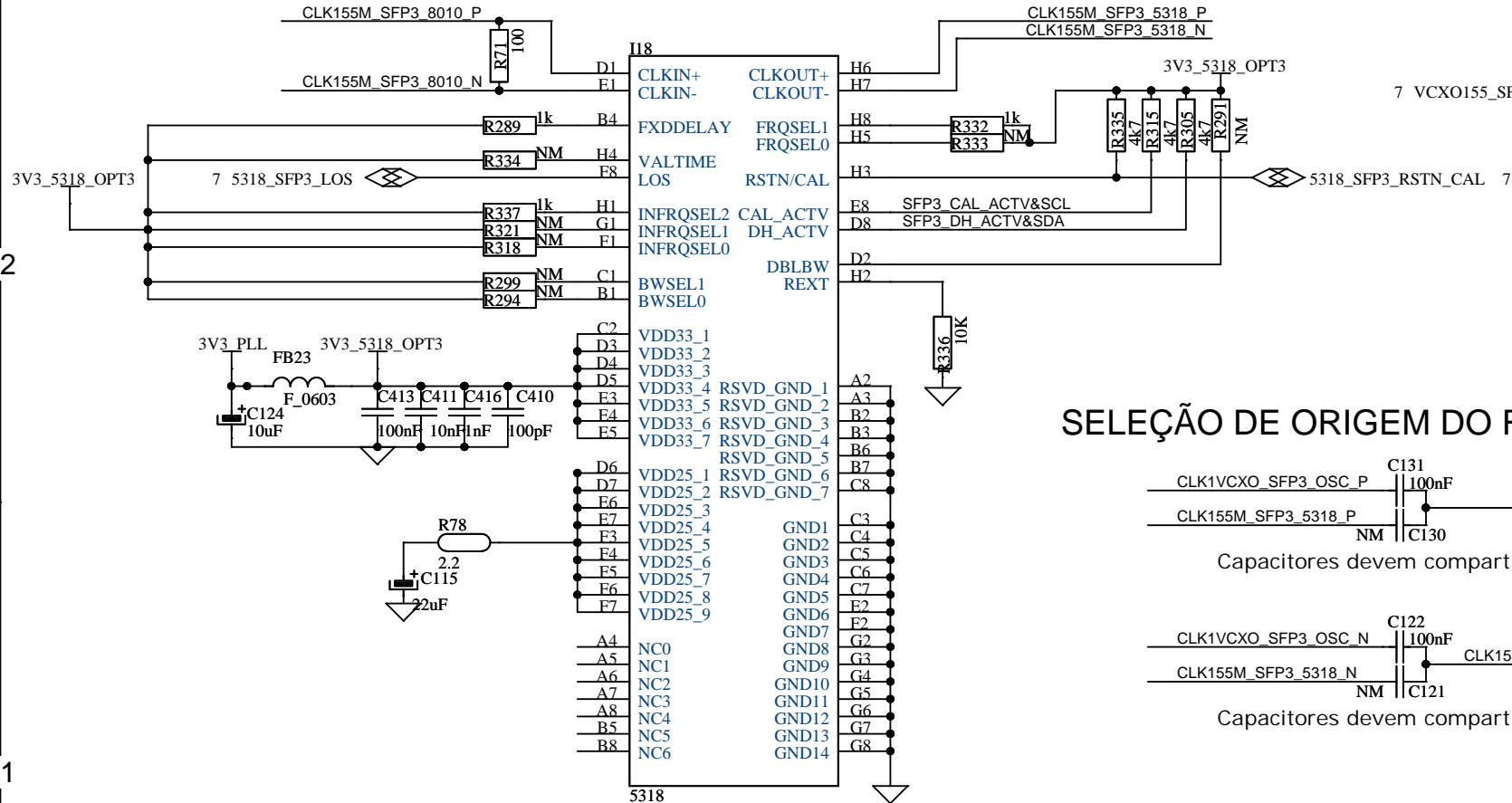
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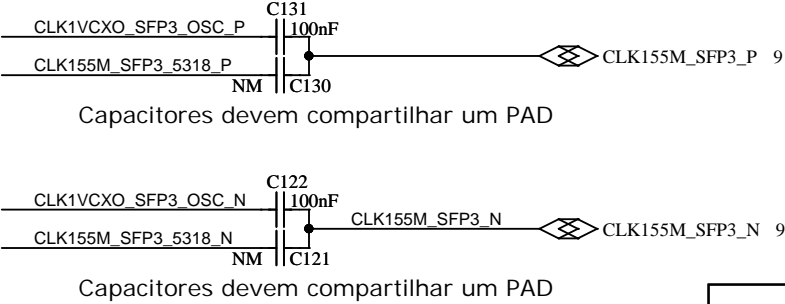
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PLL si5318 - MGT SFP3

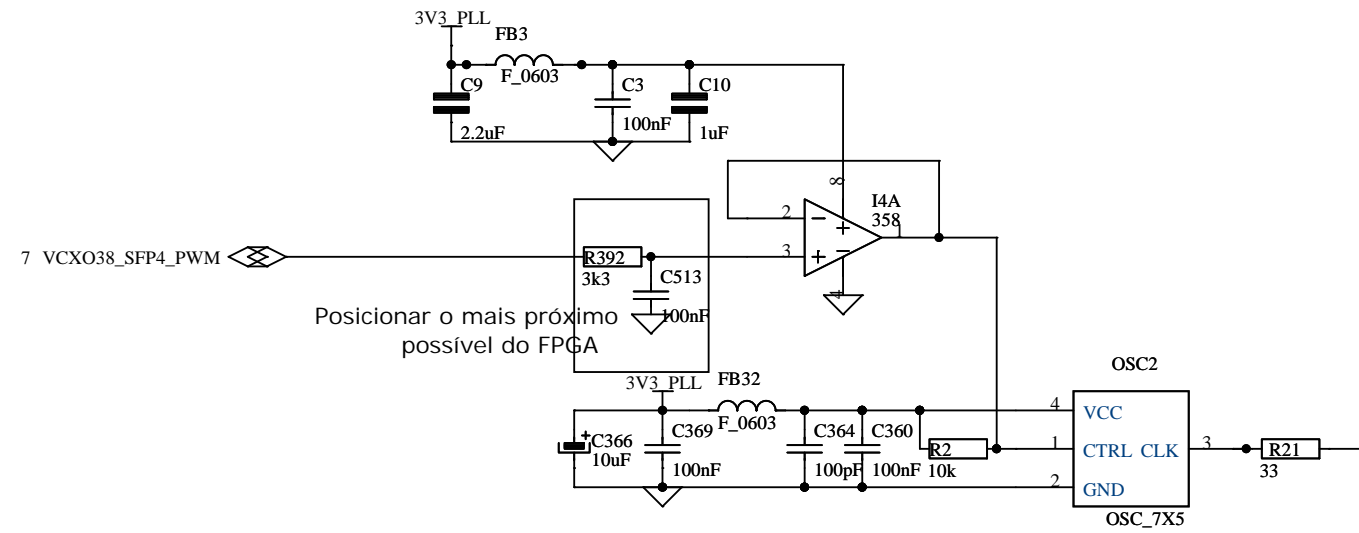


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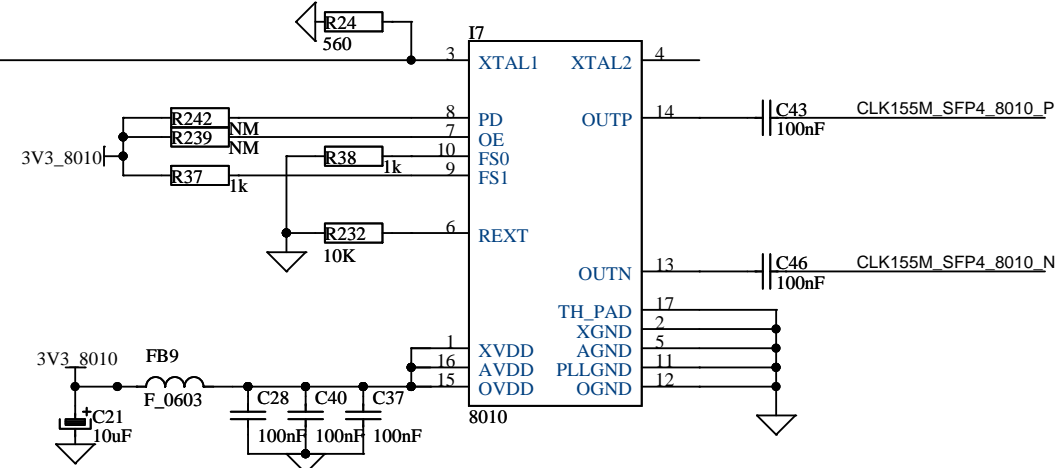


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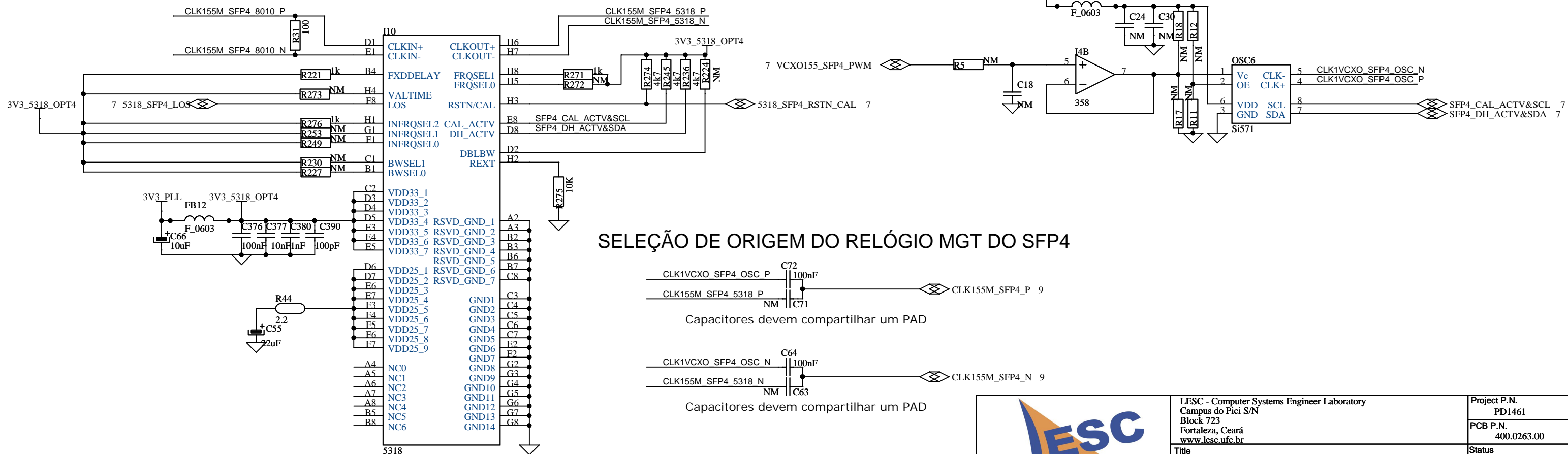


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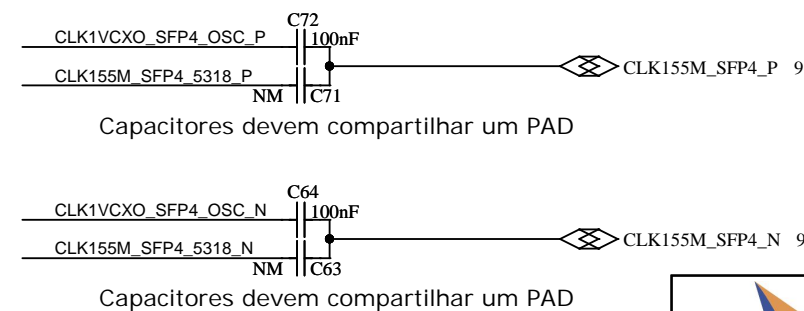




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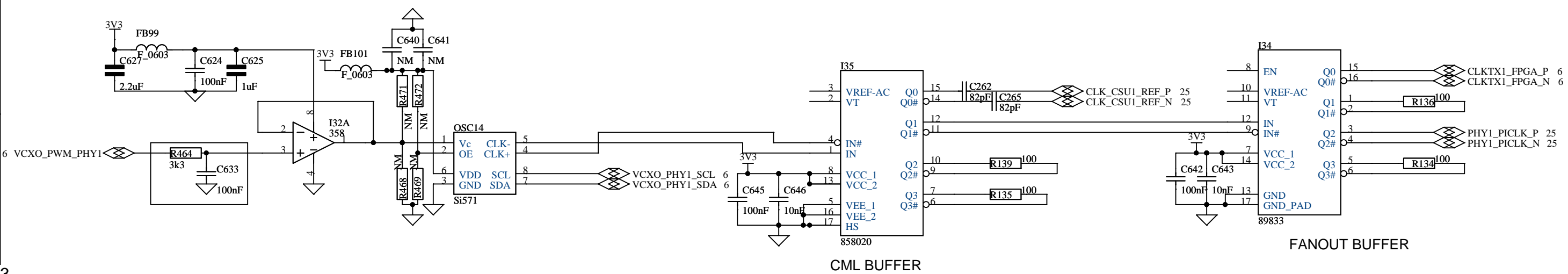
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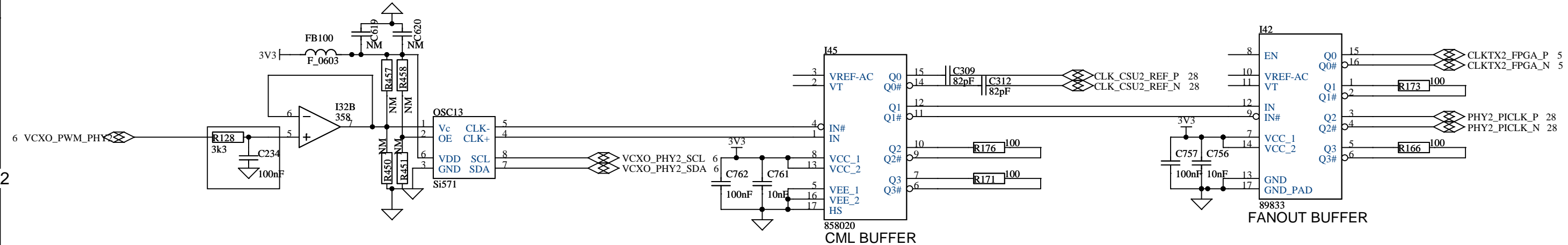
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GERAÇÃO DE RELÓGIO PARA OS PHYs, FPGA E BUS_MPU

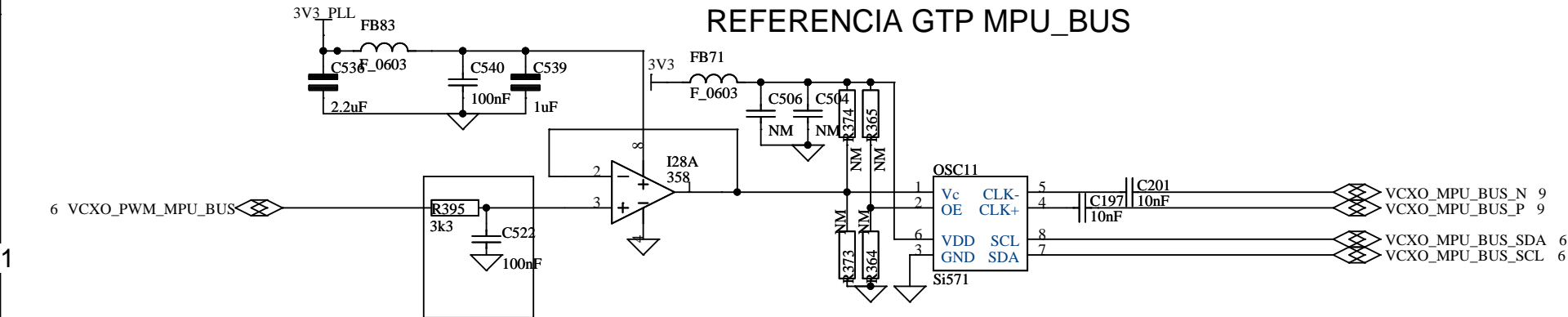
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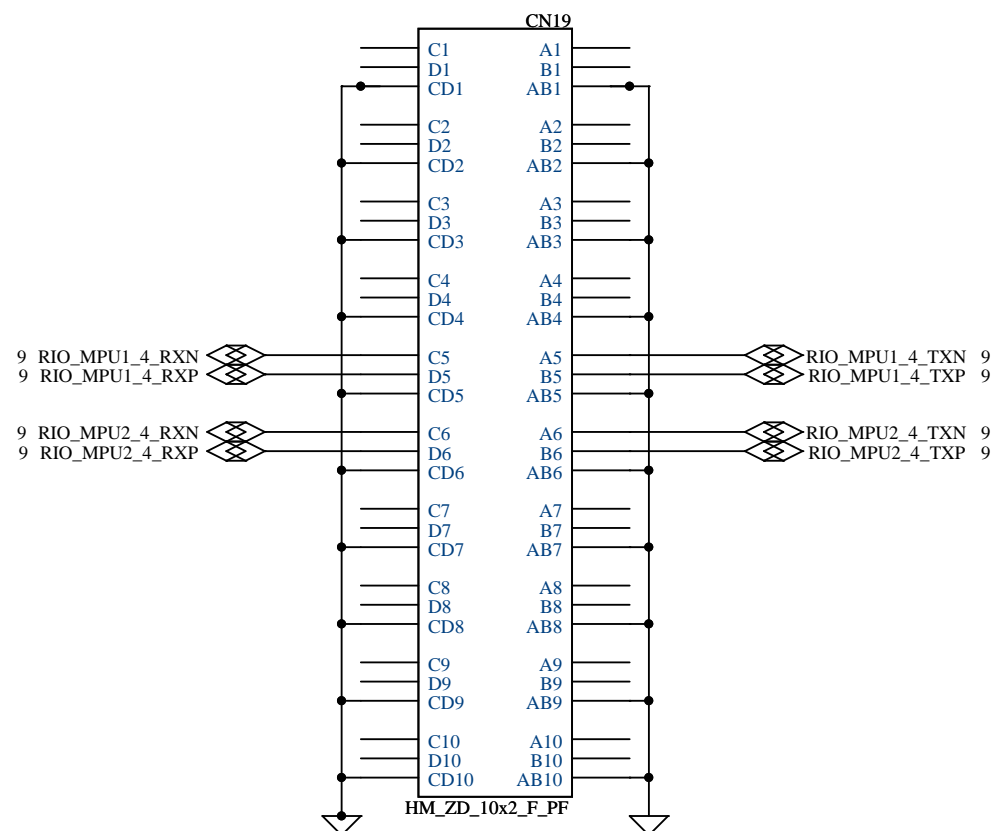
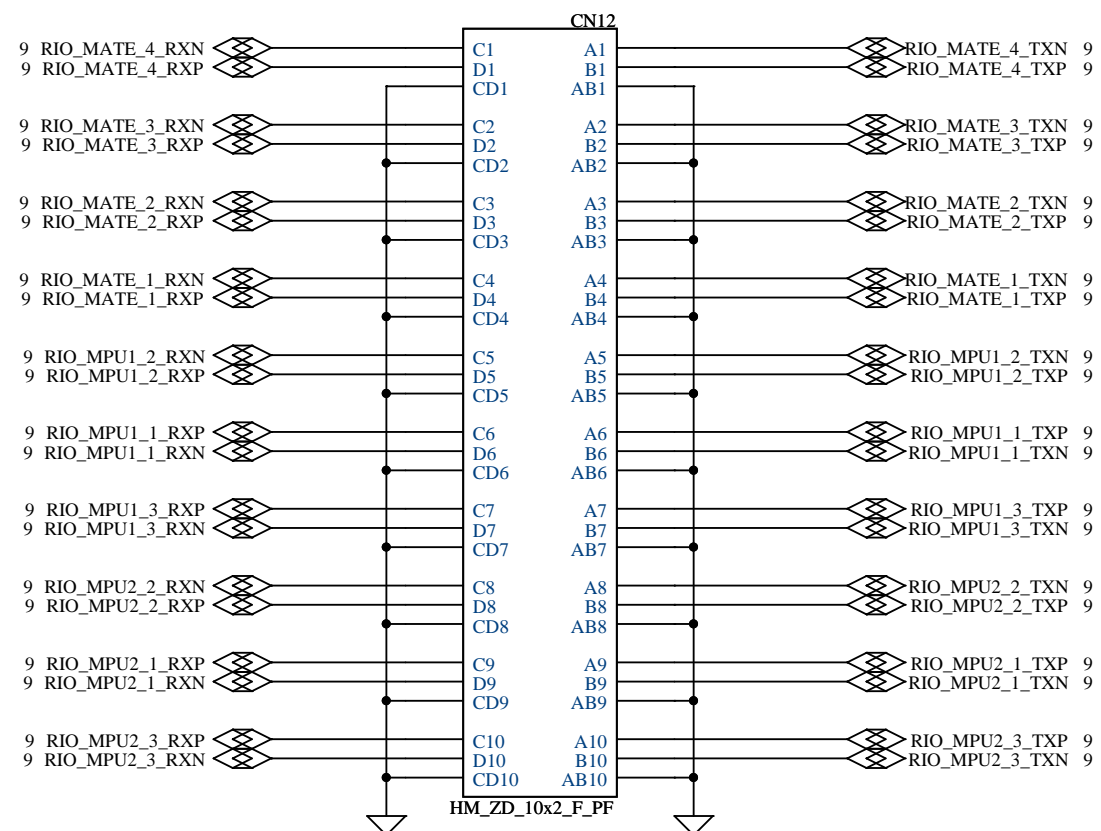
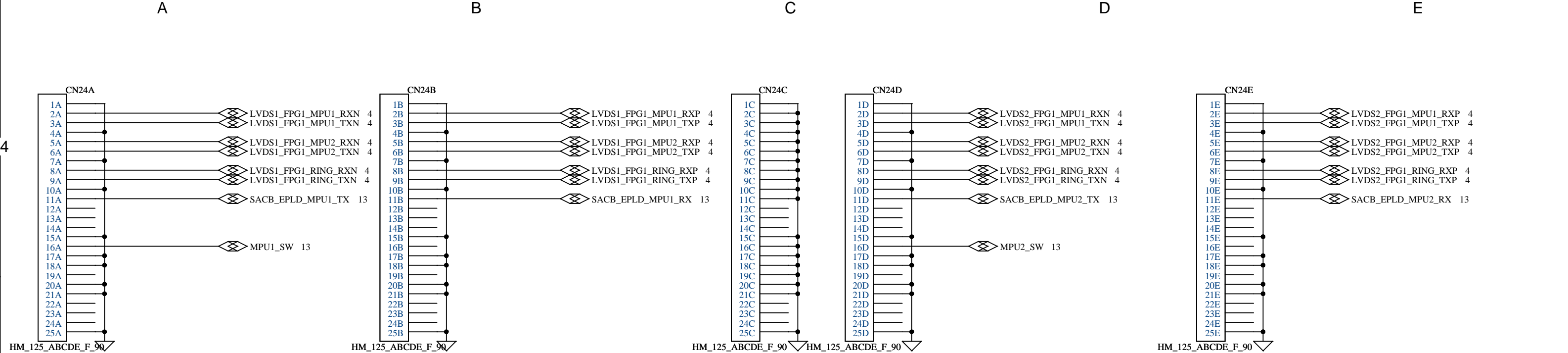
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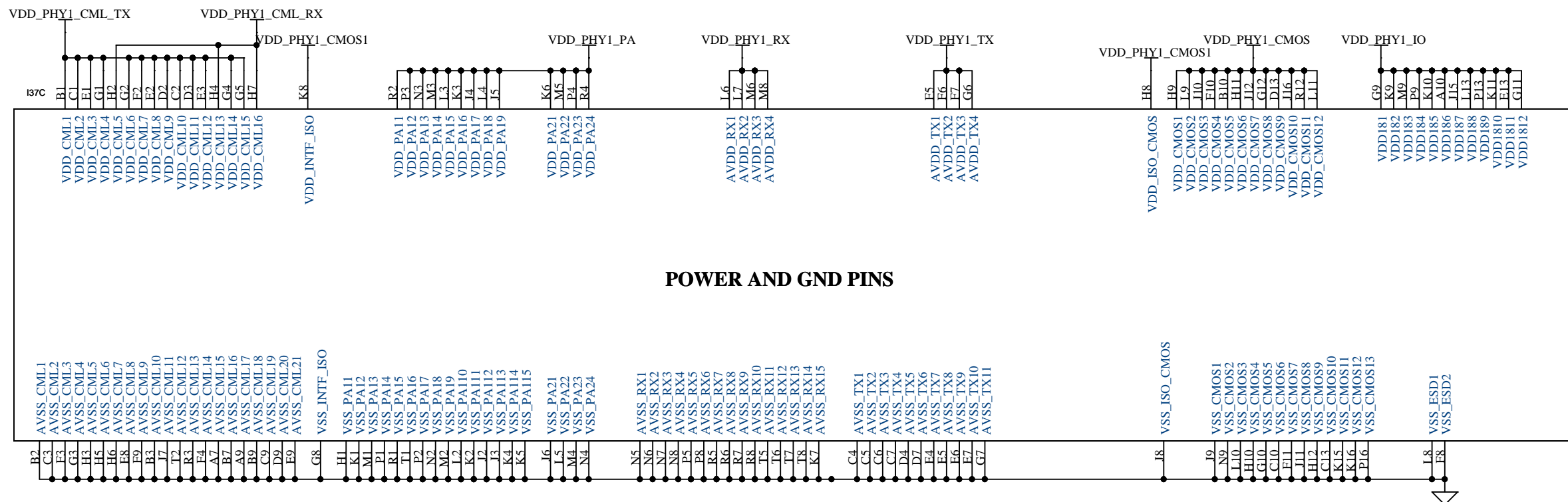
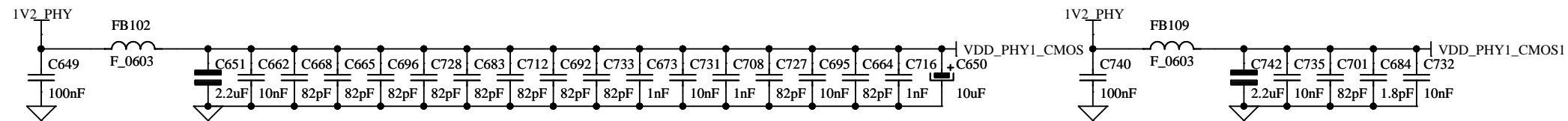
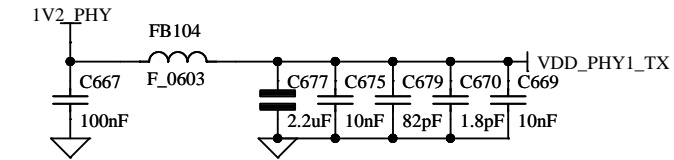
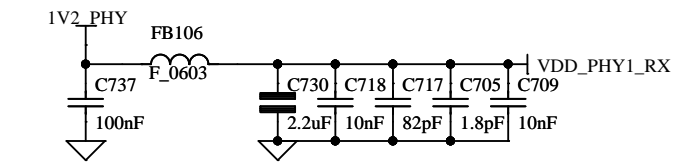
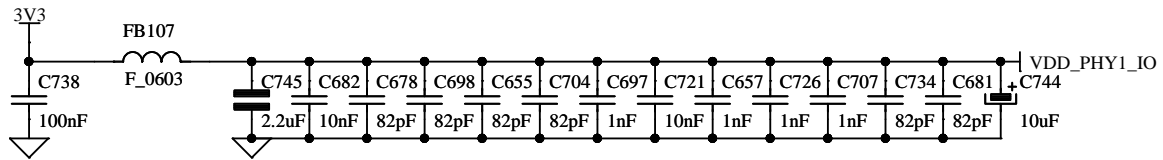
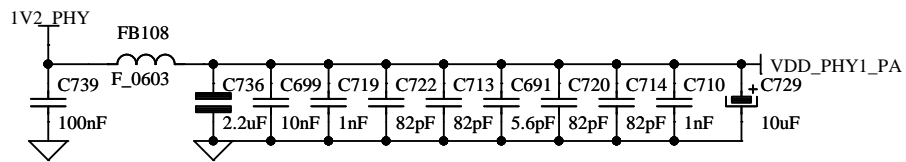
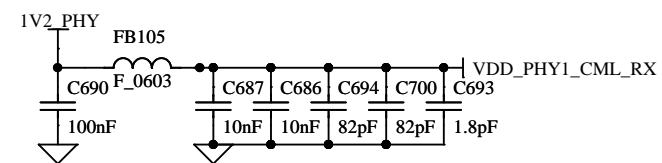
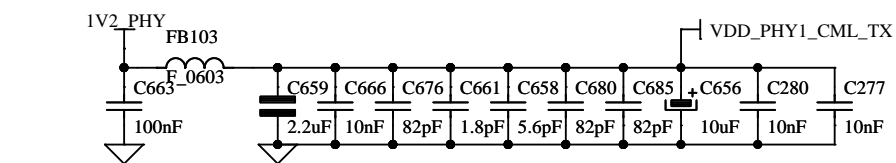


REFERENCIA GTP MPU_BUS



	LESC - Computer Systems Engineer Laboratory Campus do Pici S/N Block 723 Fortaleza, Ceará www.lesc.ufc.br		Project P.N. PD1461	
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DATACOM

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www.lesc.ufc.br

Title X10Giga Project

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Project P.N.
PD1461

PCB P.N.	400.0263.00
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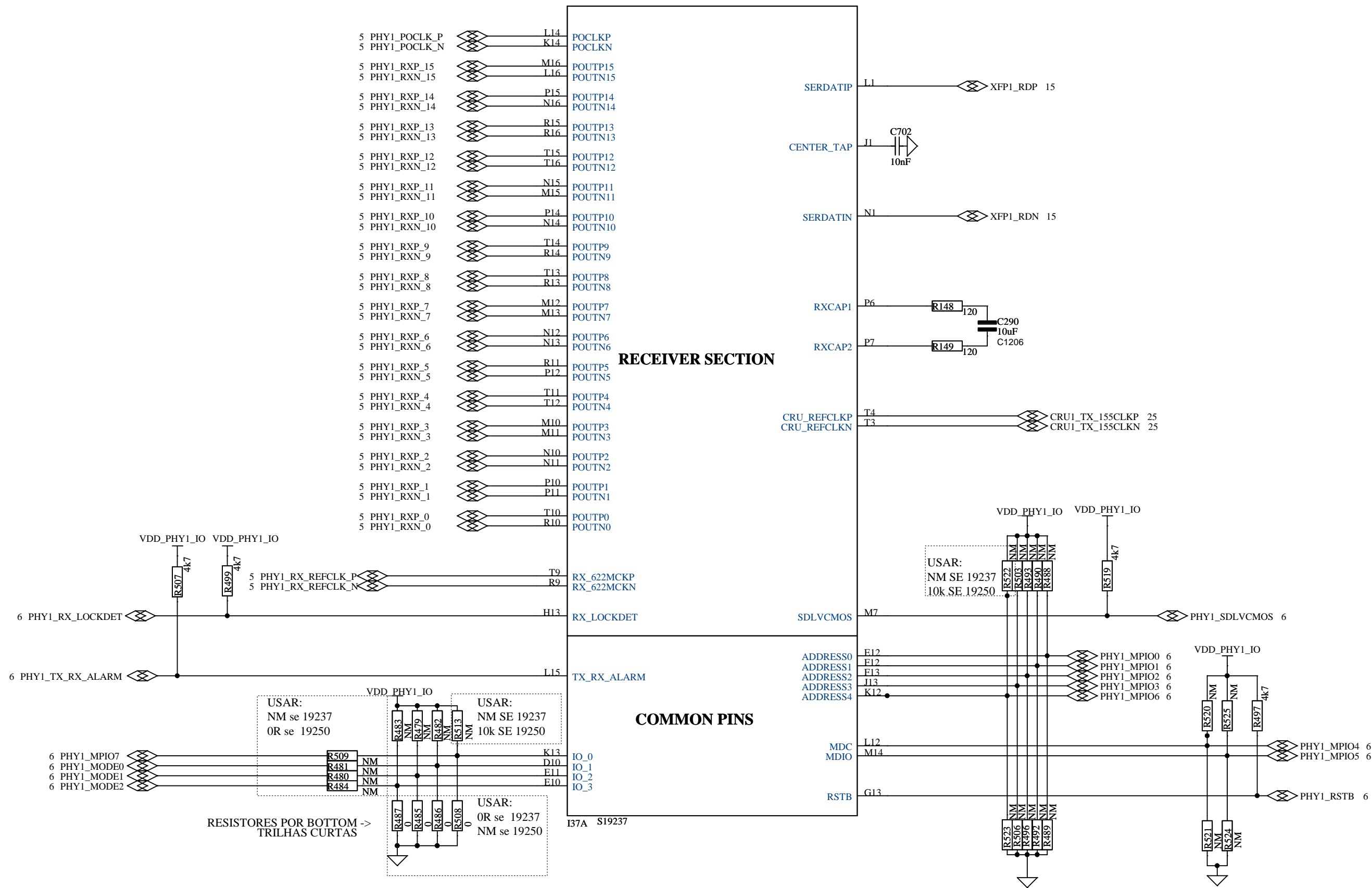
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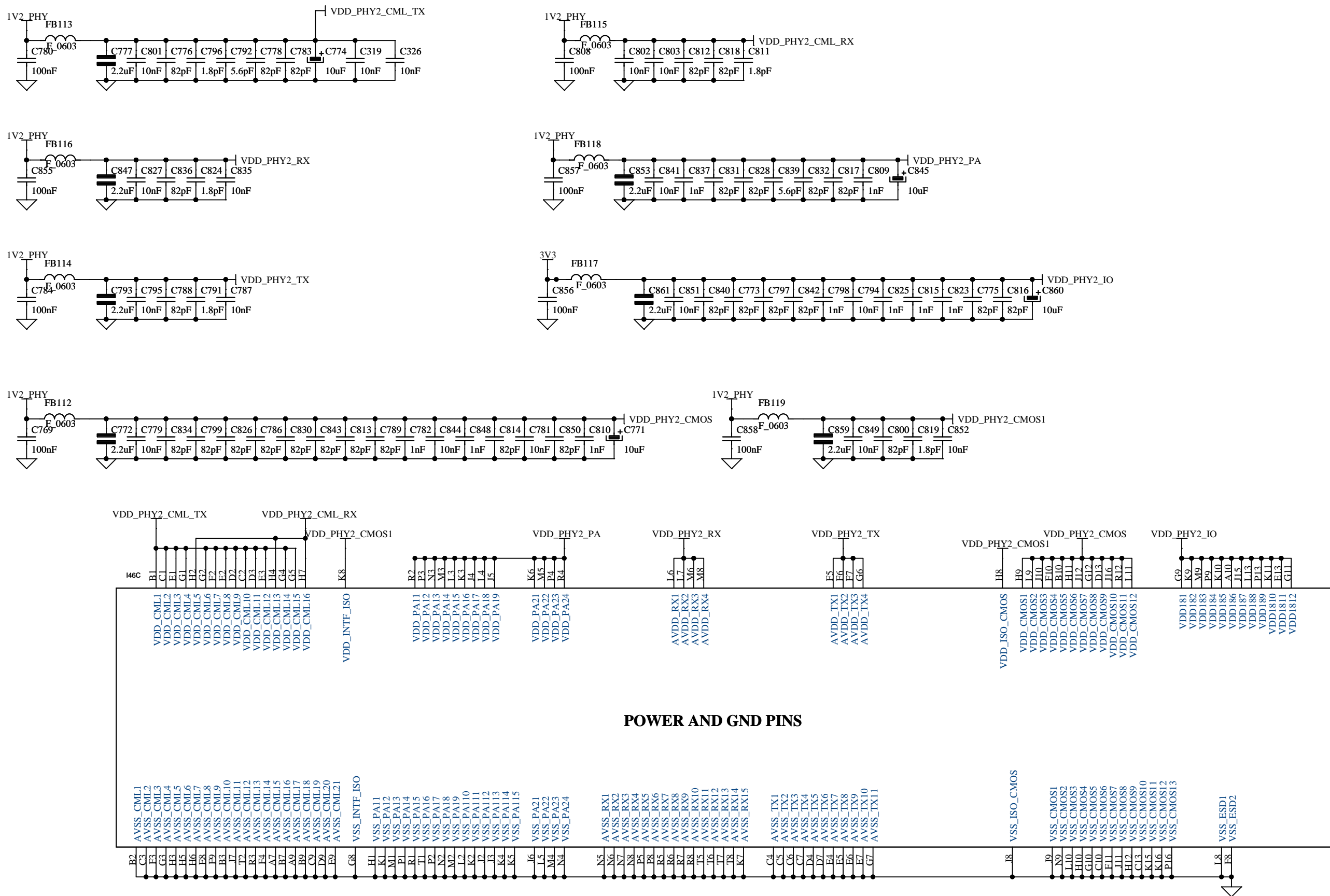
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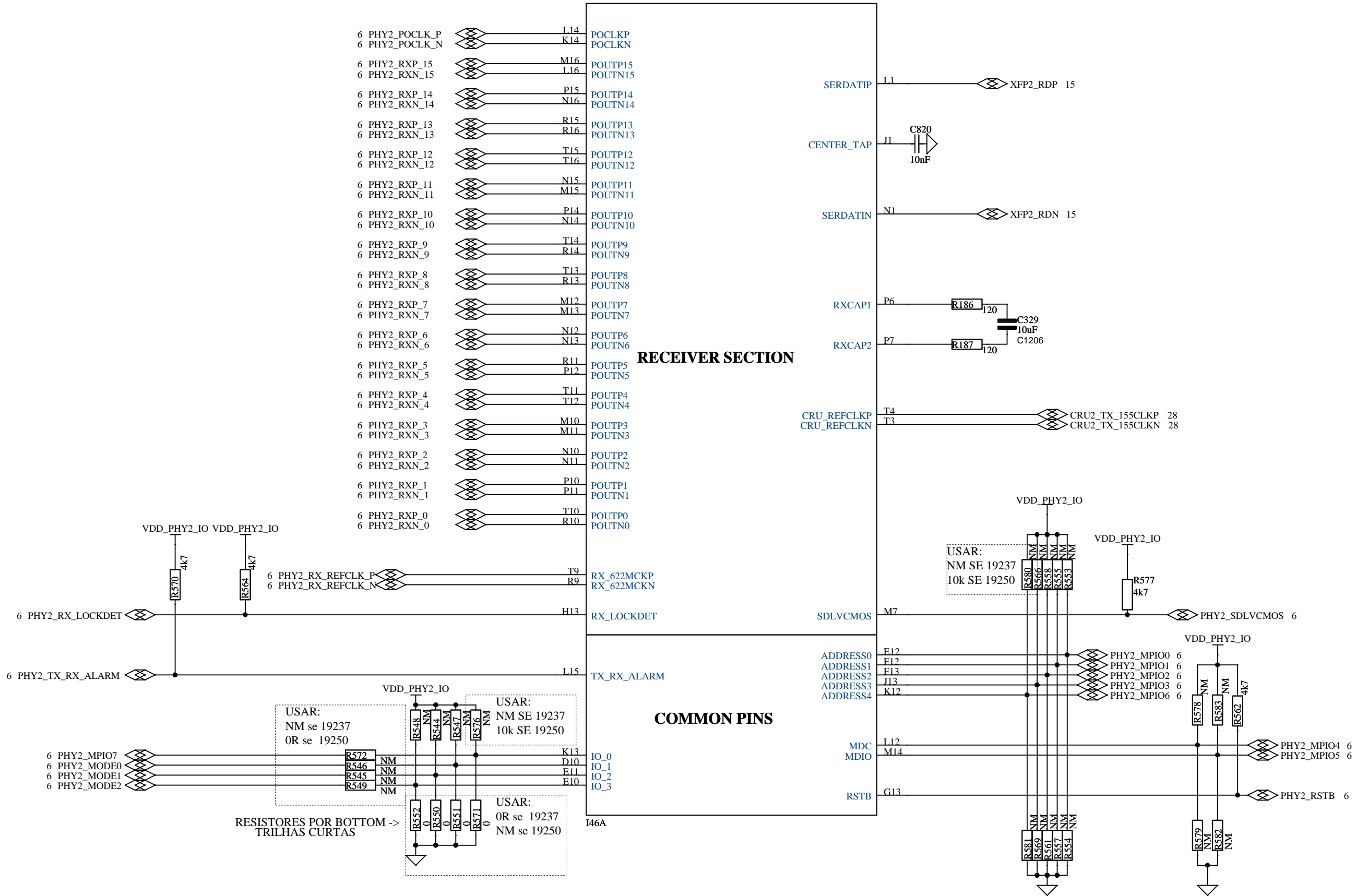
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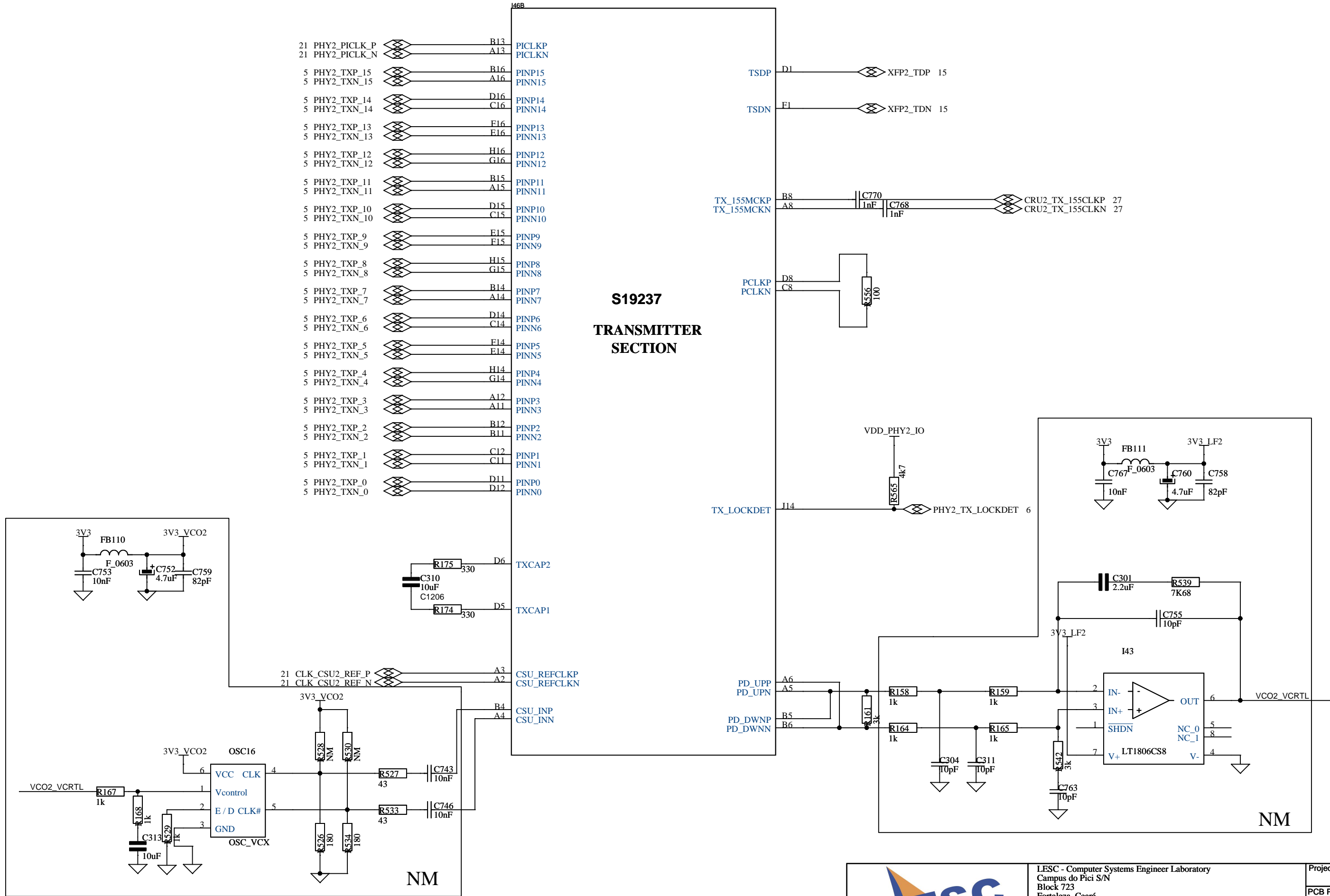
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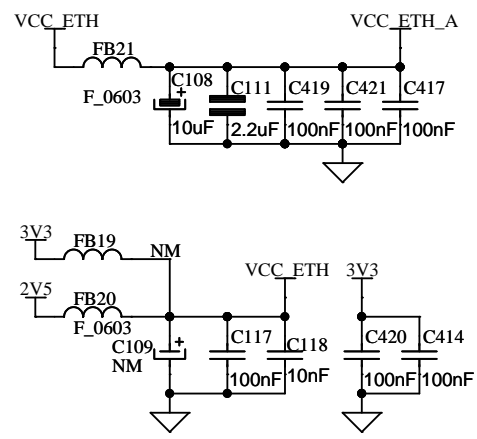
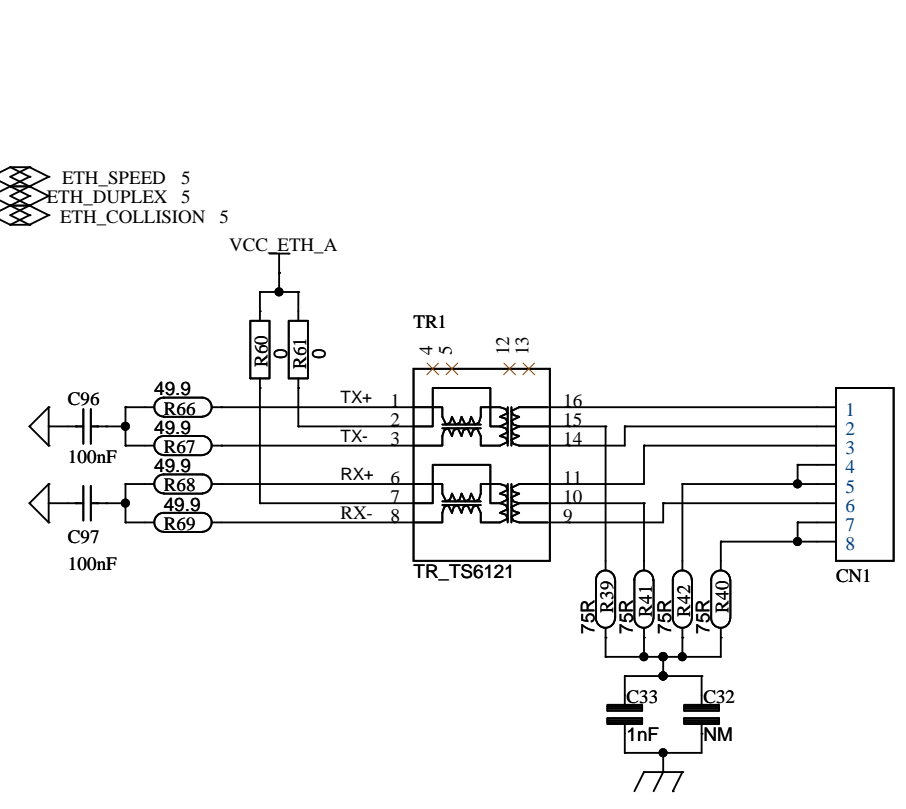
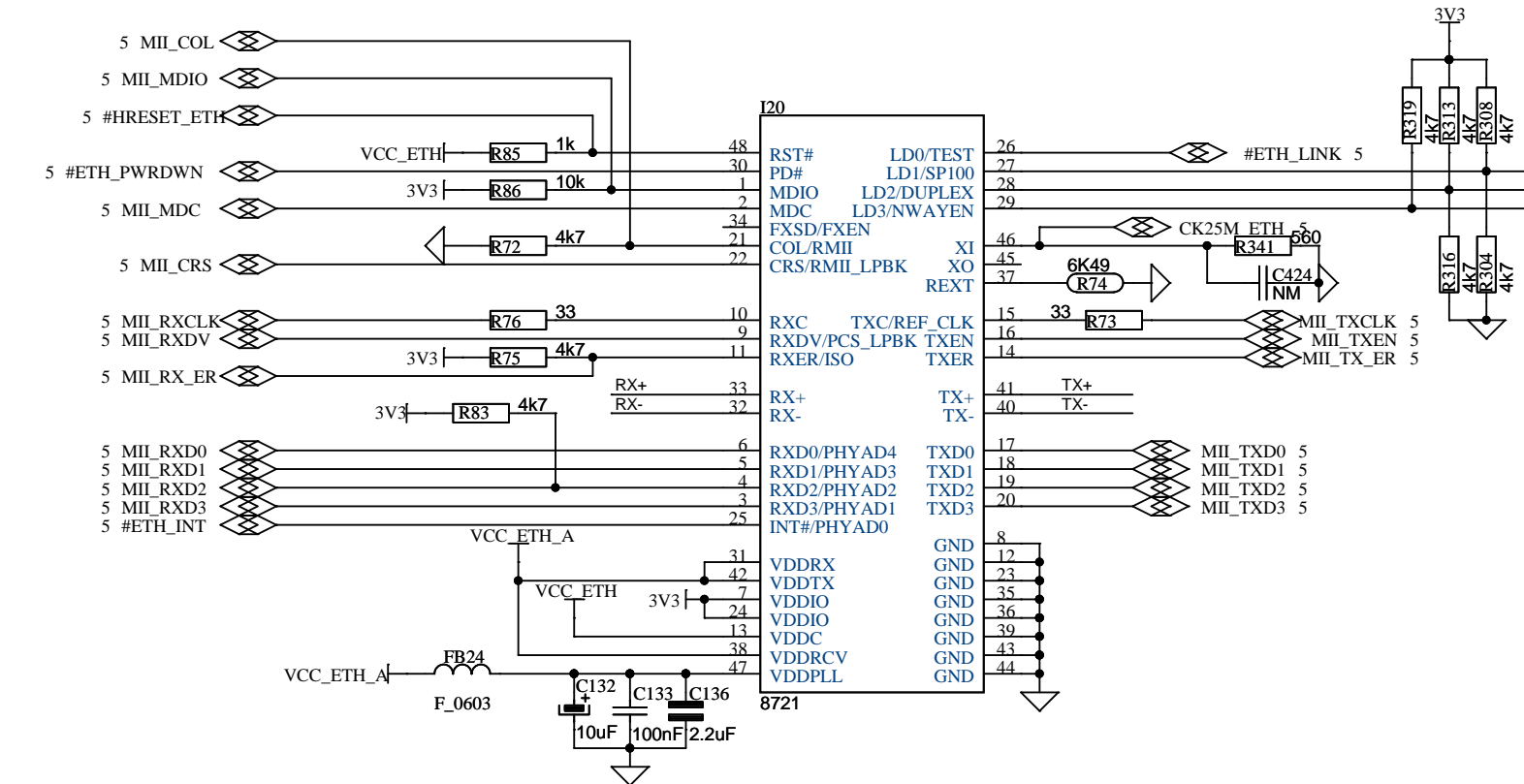
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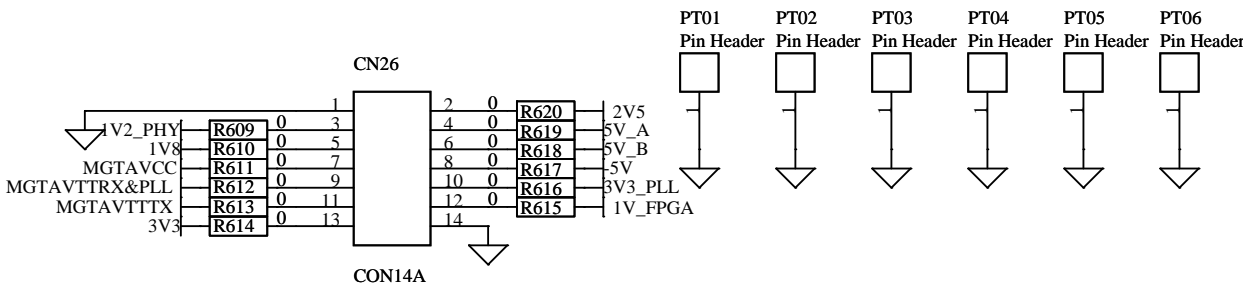
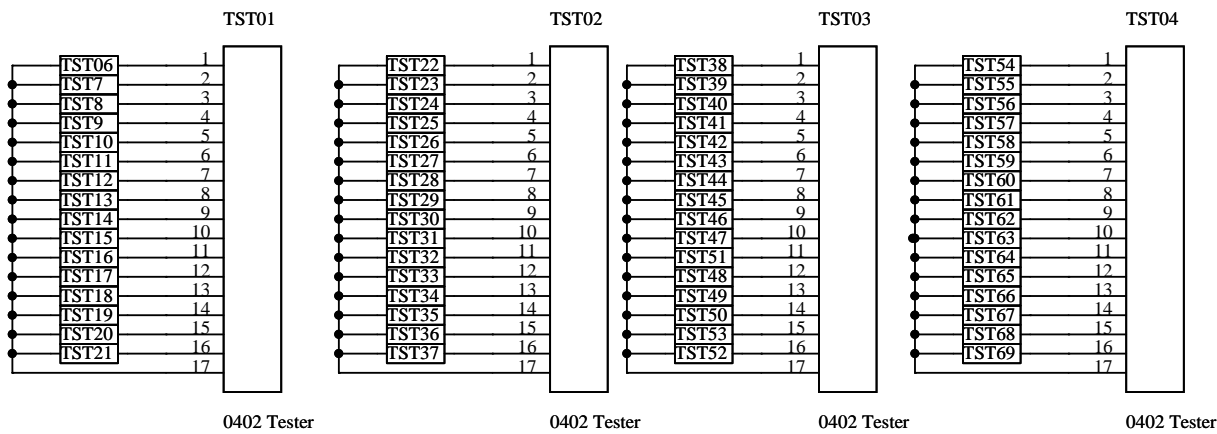
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Testadores 0402



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