Design of a Fingerprint System Using a Hardware/Software Environment

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Processing system of fingerprint are CPU time intensive, being normally implemented in software. This paper present a new algorithm for fingerprint features localization, that can be easily implemented in hardware (system-on-a-chip, FPGA). This algorithm is composed by 3 stages, first stage read a fingerprint image (255x255pixels, ash tones) and apply a Gaussian Filter, after this, apply a absolute difference mask (ADM) for detector the edges in the image filtered and the last stage look for fingerprint features into the image. The information showed by 3th stage are the coordinate X and Y for each feature detected, asked minutiae. For localization the minutiae, the system pursue the edge detected by ADM, this edge represent ridge edge, and analyzing the information from each pixel pursued is possible to locate the minutiae. The average time for localization all minutiae into the fingerprint image, implemented in hardware (FLEX10KE Family, Altera), was 306 milliseconds. Beyond hardware implementation be fast, is possible create embedded systems.

Customized Regular Channel Design in FPGAs

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In this paper, we study the problem of customized regular segmentation design in FPGA routing channels. We propose a deterministic algorithm for segmentation design problem in which each interval is assigned to only one segment (1-Segmentation). We solve the problem of maximum number of incremental track assignment of intervals by mincost network flow technique for 1-Segmentation design. The general K-Segmentation design problem can also be solved by some modifications in our algorithm. We have experimented our algorithm on a set of MCNC benchmarks and compared the routability of the segmented channels with the routability of different segmentations in FPGA routing architectures, one used by industrial Xilinx TM 4000 FPGA series. The experimental results show that the routability of the segmentation in general-purpose architecture can be as low as 18.4% while the routability of our proposed customized segmentation can be as high as 91%. This result shows the gap between the general FPGA routing architecture and customized architecture for a given application can be very significant and our method is capable of generating such optimized segmentation with high routability for a given application.