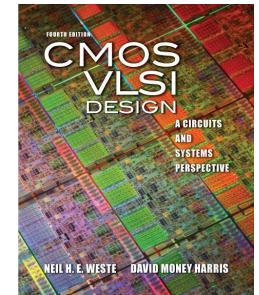
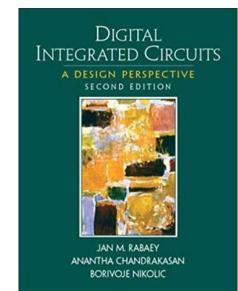


Microeletrônica

Aula #6 → Processo de fabricação CMOS

- Professor: Fernando Gehm Moraes
- Livro texto:
Digital Integrated Circuits a Design Perspective - Rabaey
CMOS VLSI Design - Weste



Companhias

1Q21 Top 15 Semiconductor Sales Leaders (\$M, Including Foundries)

1Q21 Rank	1Q20 Rank	Company	Headquarters	1Q20 Total IC	1Q20 Total O-S-D	1Q20 Total Semi	1Q21 Total IC	1Q21 Total O-S-D	1Q21 Total Semi	1Q21/1Q20 % Change
1	1	Intel	U.S.	19,508	0	19,508	18,676	0	18,676	-4%
2	2	Samsung	South Korea	14,030	767	14,797	16,152	920	17,072	15%
3	3	TSMC (1)	Taiwan	10,319	0	10,319	12,911	0	12,911	25%
4	4	SK Hynix	South Korea	5,829	210	6,039	7,323	305	7,628	26%
5	5	Micron	U.S.	5,004	0	5,004	6,580	0	6,580	31%
6	7	Qualcomm (2)	U.S.	4,050	0	4,050	6,281	0	6,281	55%
7	6	Broadcom Inc. (2)	U.S.	3,673	409	4,082	4,355	485	4,840	19%
8	9	Nvidia (2)	U.S.	3,074	0	3,074	4,630	0	4,630	51%
9	8	TI	U.S.	2,974	190	3,164	3,793	235	4,028	27%
10	16	MediaTek (2)	Taiwan	2,022	0	2,022	3,849	0	3,849	90%
11	18	AMD (2)	U.S.	1,786	0	1,786	3,445	0	3,445	93%
12	11	Infineon	Europe	1,828	876	2,704	2,170	1,083	3,253	20%
13	10	Apple* (2)	U.S.	2,770	0	2,770	3,080	0	3,080	11%
14	14	ST	Europe	1,483	745	2,228	2,011	994	3,005	35%
15	13	Kioxia	Japan	2,567	0	2,567	2,585	0	2,585	1%
— — Top-15 Total				80,917	3,197	84,114	97,841	4,022	101,863	21%

(1) Foundry (2) Fabless

Source: Company reports, IC Insights' *Strategic Reviews* database

*Custom processors/devices for internal use.

<https://www.icinsights.com/data/articles/documents/1376.pdf>

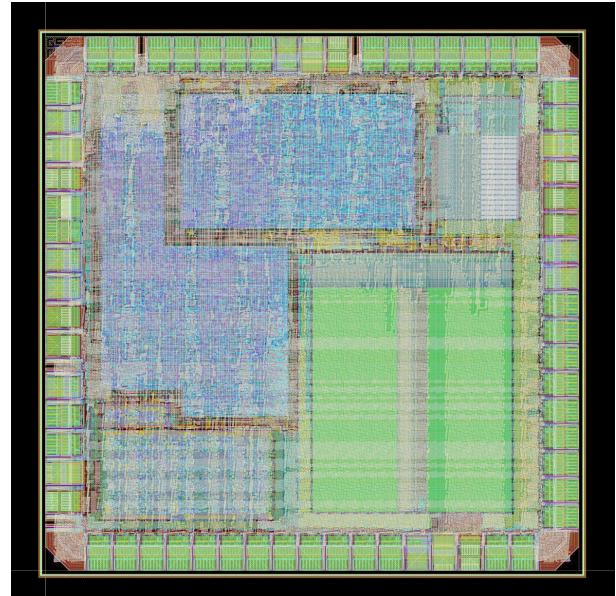
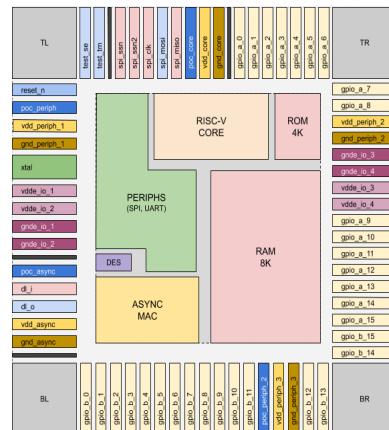
PMU – Projeto Multi Usuário

Permite a pequenos clientes prototipar circuitos integrados

Possuem programas especiais para universidades que permitem fabricar CIs gratuitamente

Principais atores

- MOSIS (EUA)
- EUROPRACTICE (**IMEC – Bélgica**)
- CMP (França)

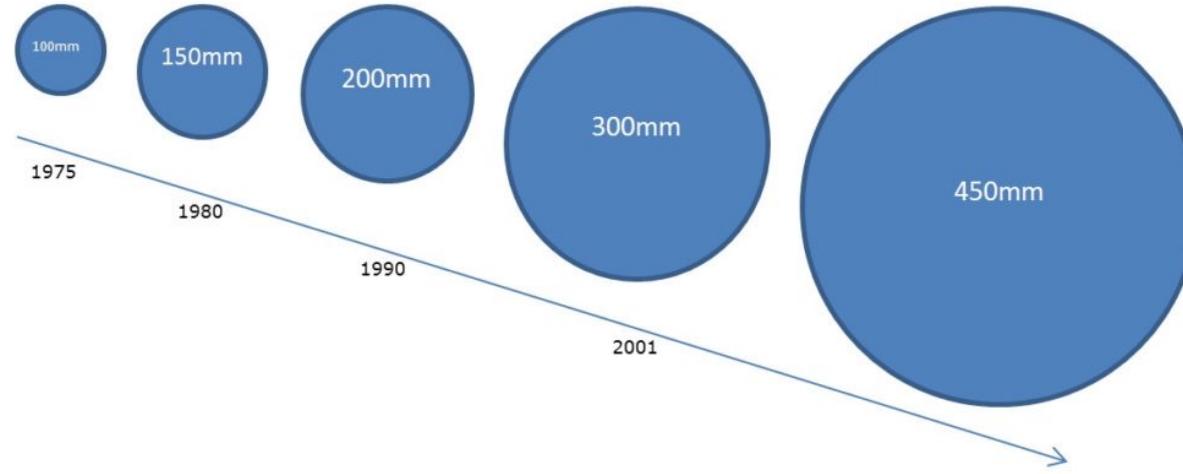


2020

A-SOC (PUCRS), com dimensão de 1660 um x 1660 um (2,76 mm²)

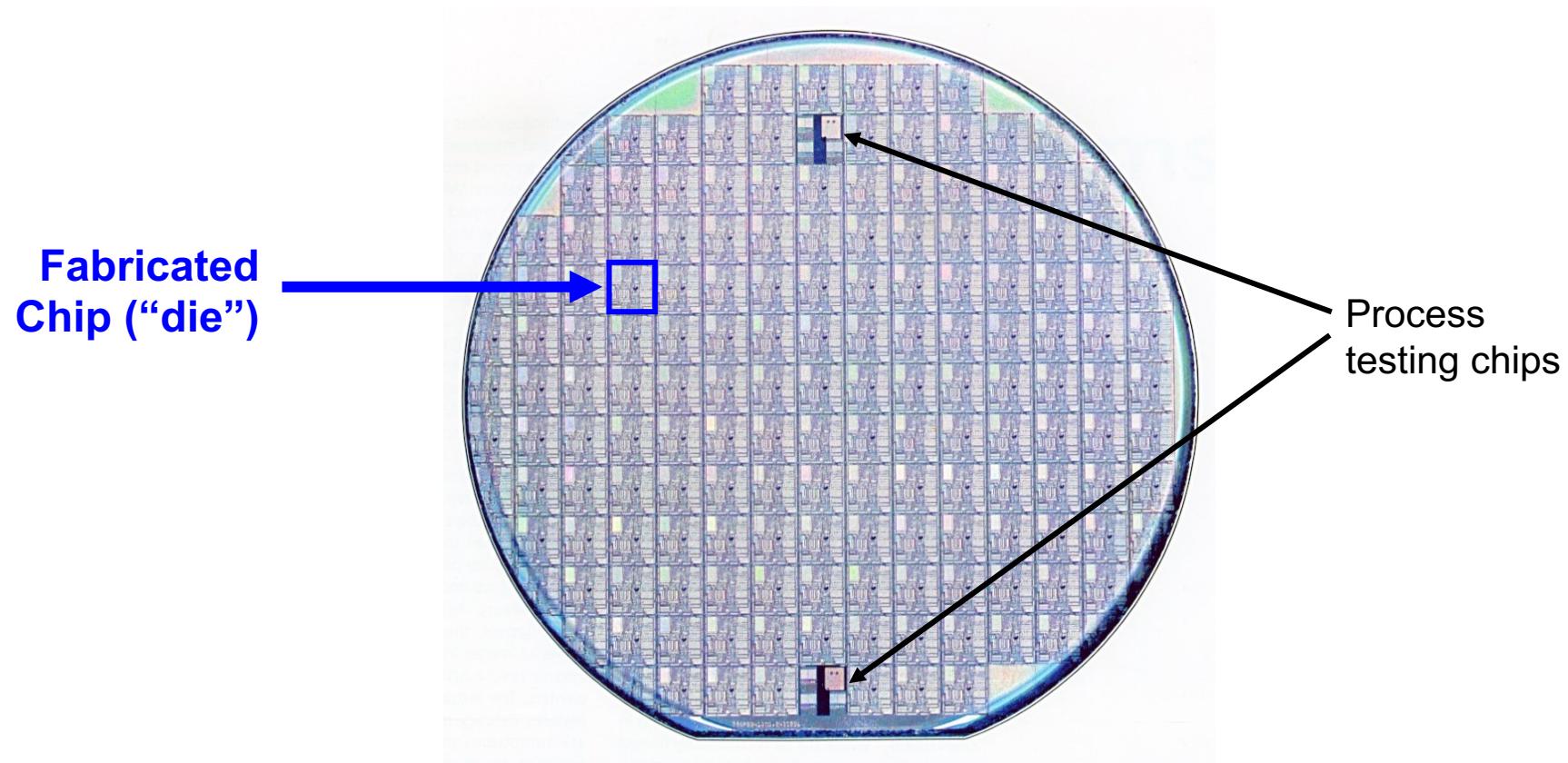
Características de um wafer

- O wafer varia de 100mm a 450mm de diâmetro
- Espessura do wafer: 0,25mm a 1 mm
- Wafer é cortado de um lingote de silício de cristal simples
- Impurezas são adicionadas para as propriedades elétricas requeridas

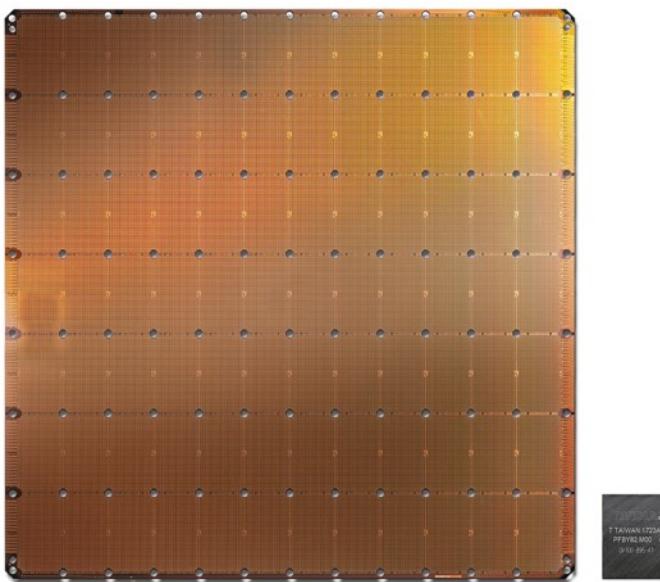


Características de um wafer

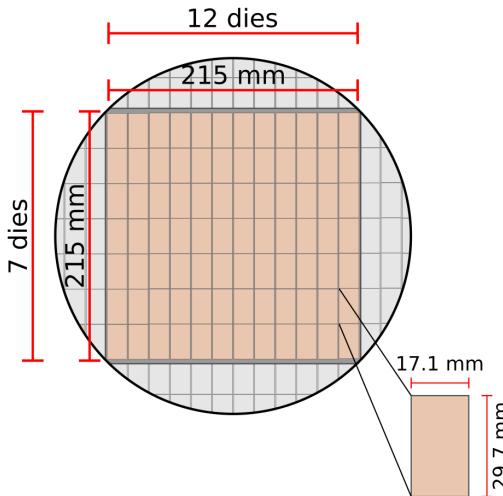
**Wafer com vários circuitos integrados idênticos
(antes de serem testados e encapsulados)**



Cerebras – <https://www.cerebras.net>



- TSMC 16nm, 84 dies
- The WSE (Wafer Scale Engine) is 215 mm by 215 mm



CS-1 is powered by the Cerebras Wafer Scale Engine - the largest chip ever built

56x the size of the largest Graphics Processing Unit

The Cerebras Wafer Scale Engine is 46,225 mm² with 1.2 Trillion transistors and 400,000 AI-optimized cores.

By comparison, the largest Graphics Processing Unit is 815 mm² and has 21.1 Billion transistors.

Consumo de potência máxima: 20 kW

Purpose-built for Deep Learning: enormous compute, fast memory and communication bandwidth

46,225 mm² chip

56x larger than the biggest GPU ever made

400,000 core

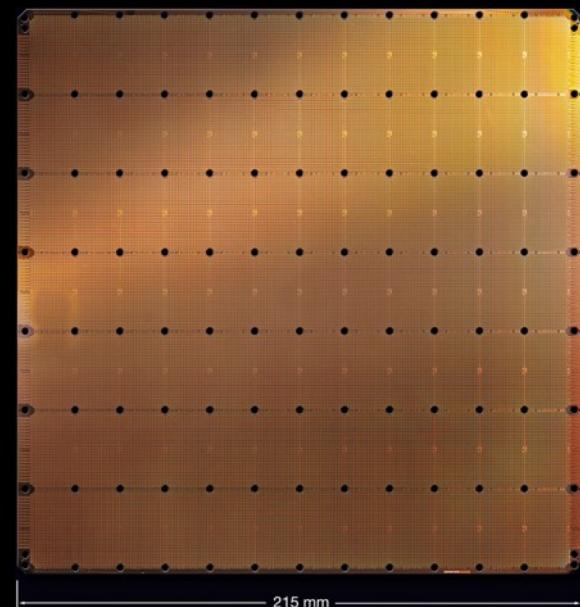
78x more cores

18 GB on-chip SRAM

3000x more on-chip memory

100 Pb/s interconnect

33,000x more bandwidth

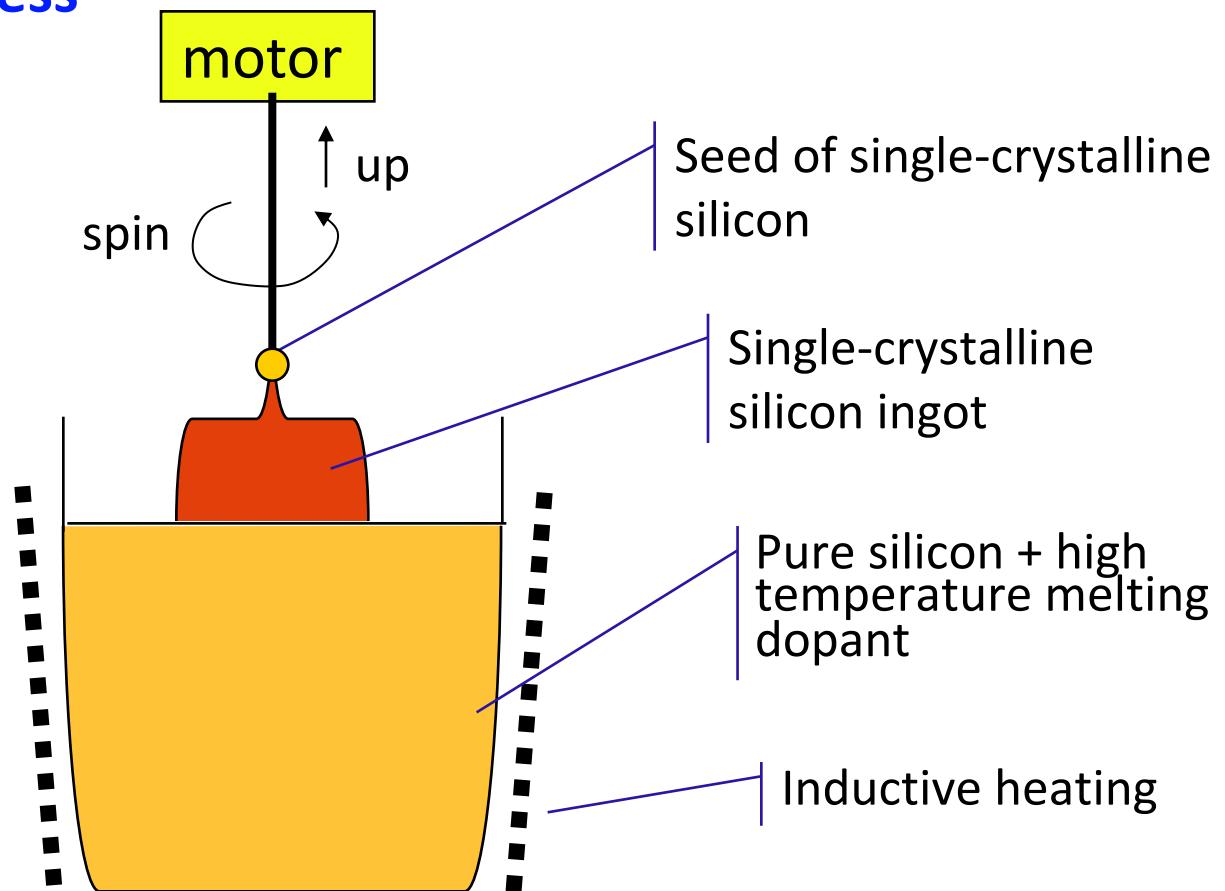


FABRICAÇÃO DOS WAFERS

Processo de Fabricação

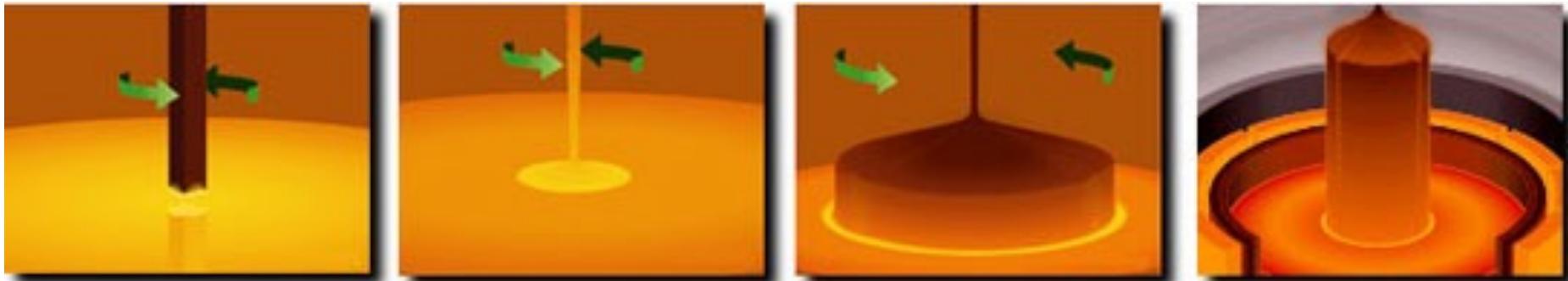
Obtaining the Single-Crystalline Silicon Ingot

The Czochralski Process



Processo de Fabricação

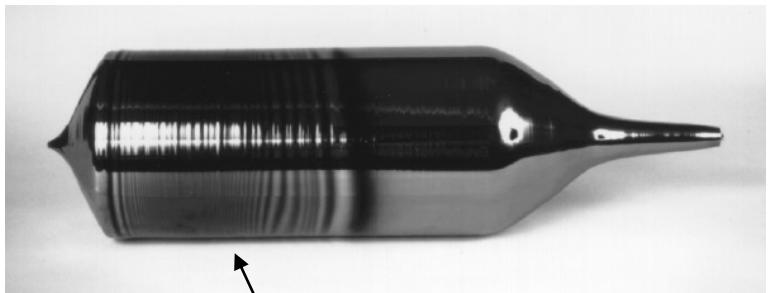
Obtenção de Silício Monocristalino



Processo de Fabricação



Silicon Ingot

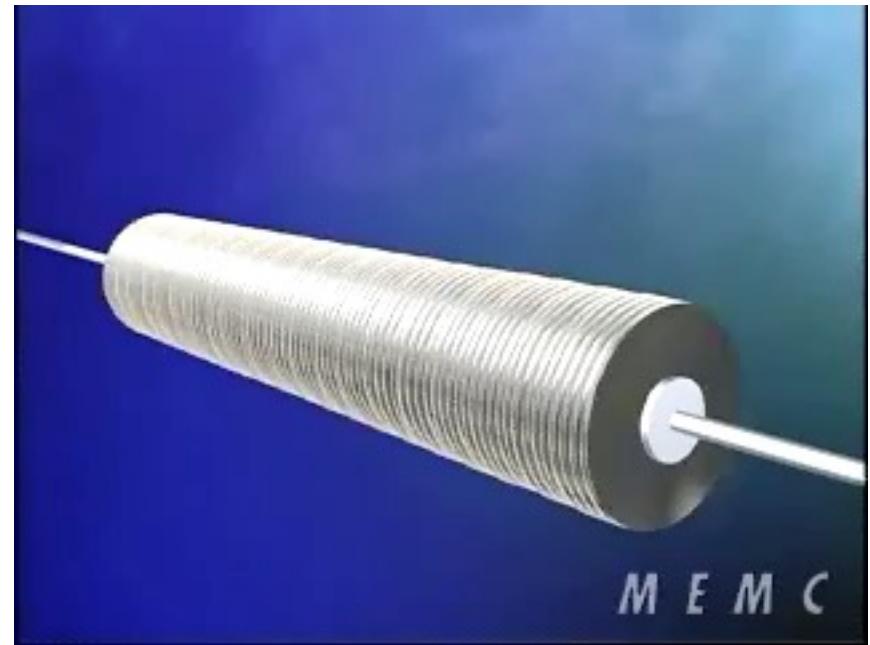


A single crystal of silicon, a silicon ingot, grown by the Czochralski technique. The diameter of the ingot is 6 inches – 15 cm (courtesy of Texas Instruments).

← **ATUAL!**

Processo de Fabricação

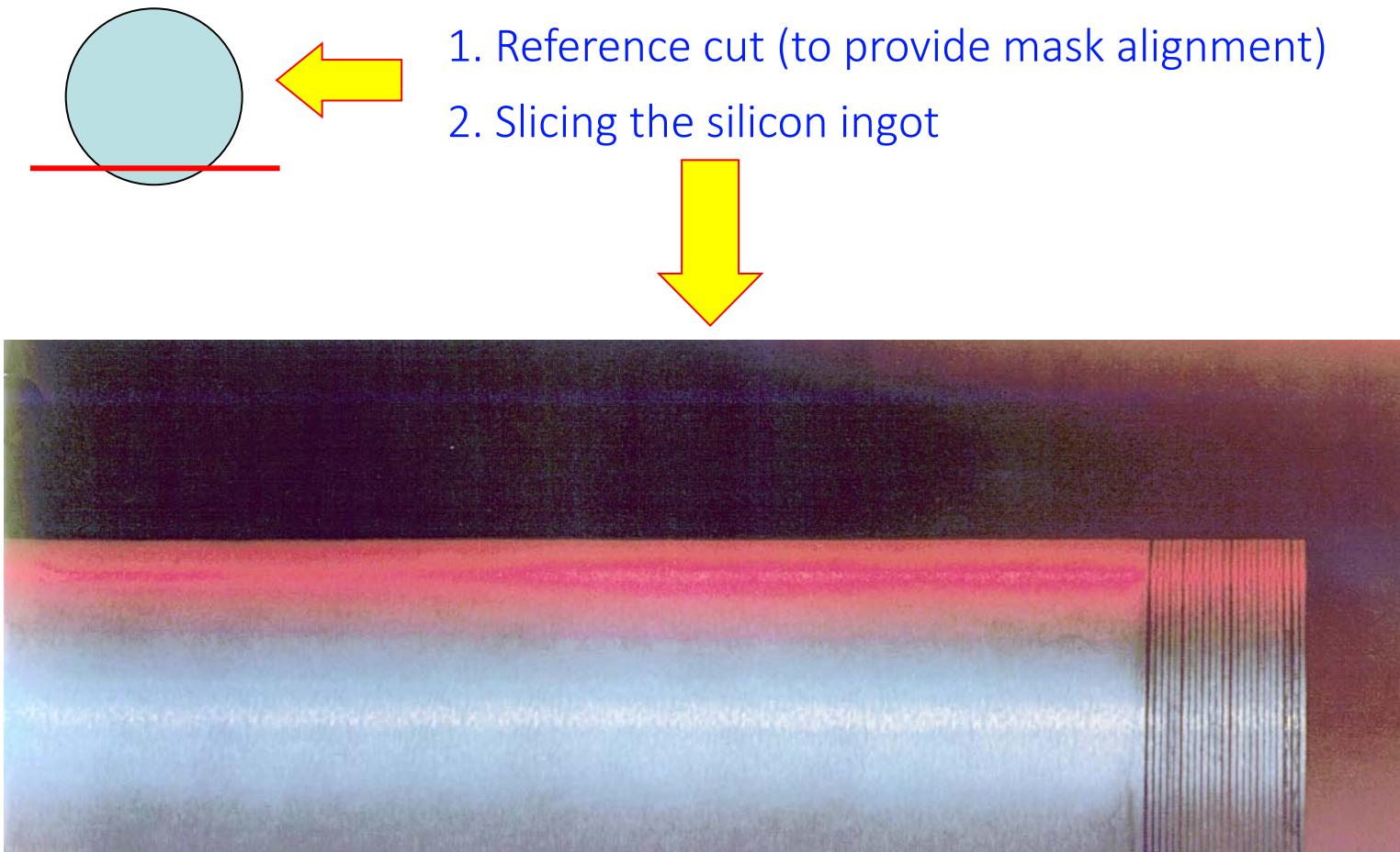
Polimento dos lingotes de silício monocristalino



Após o crescimento do lingote de silício monocristalino, este passa por um processo de polimento, antes do corte em fatias

Processo de Fabricação

Obtaining the Silicon Wafer



Processo de Fabricação

Polimento dos wafers de silício monocristalino



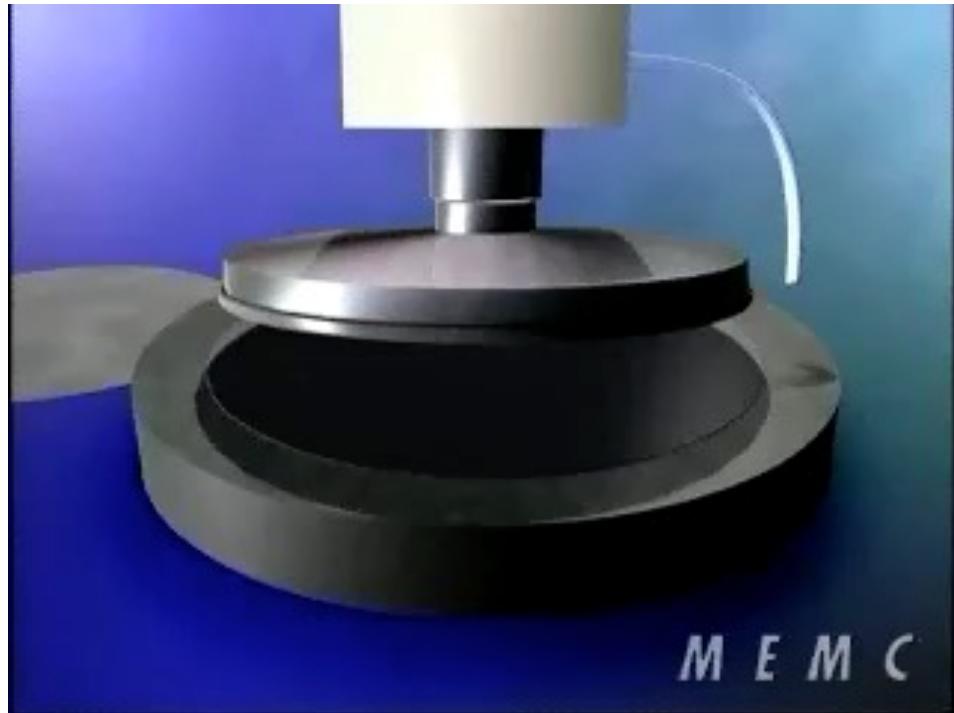
Cada *wafer* passa individualmente por um processo de polimento, tanto das bordas como de suas superfícies.

Processo de Fabricação

Planarization: Polishing the Wafers

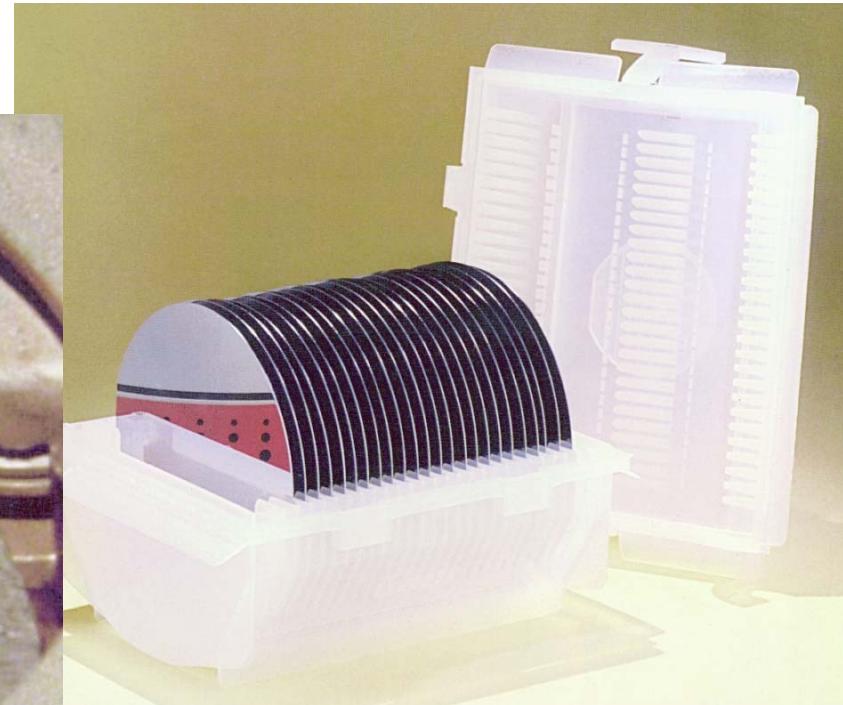
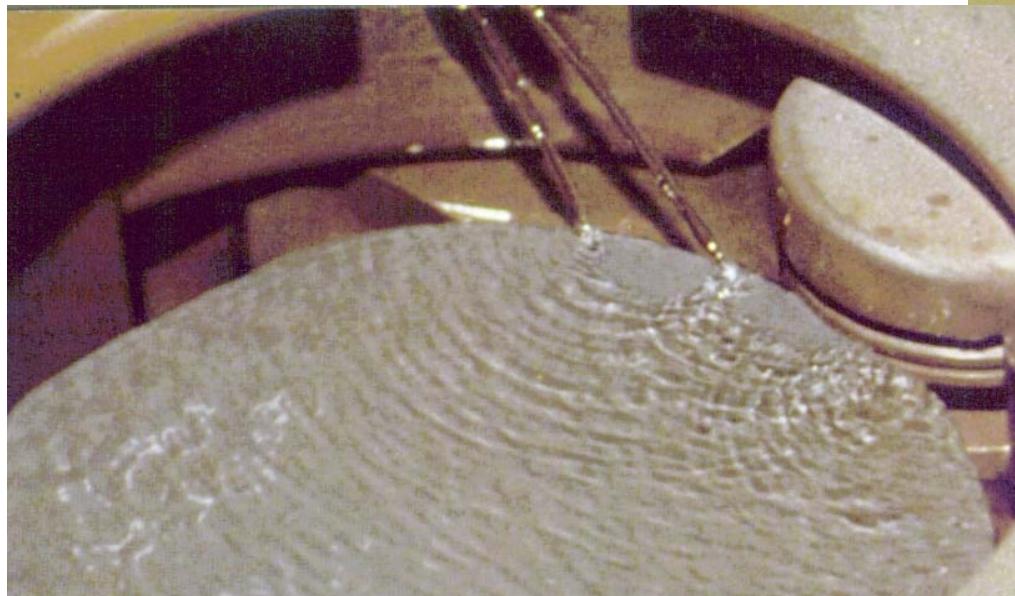


From *Smithsonian*, 2000



Processo de Fabricação

Polimento e limpeza dos wafers de silício monocristalino

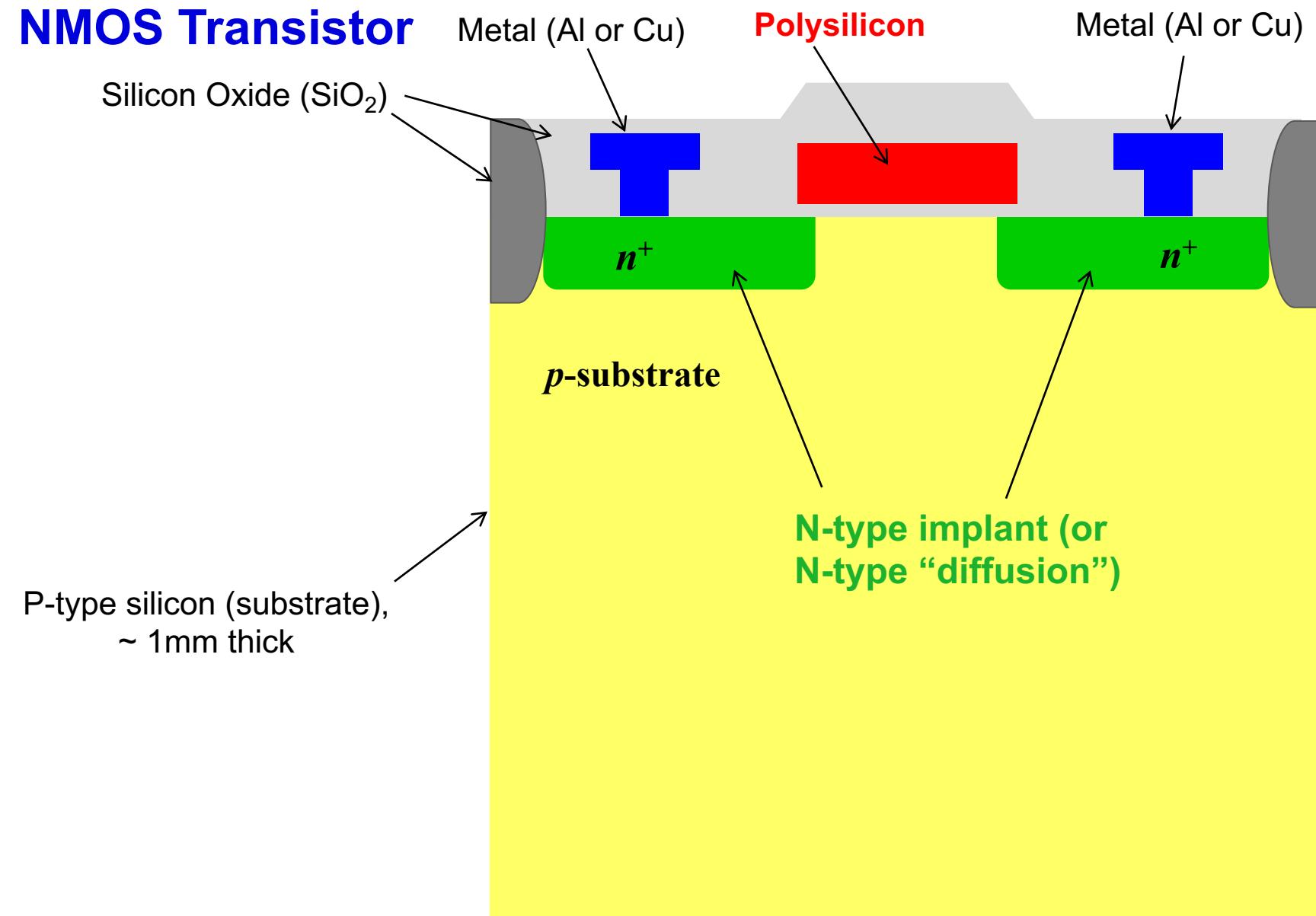


FABRICAÇÃO DOS CIRCUITOS INTEGRADO

Obrigados os professores José Luís Güntzel (UFSC) e
Gilson Inacio Wirth (UFRGS) por compartilharem
suas apresentações neste tema

CMOS Process

NMOS Transistor



CMOS Fabrication

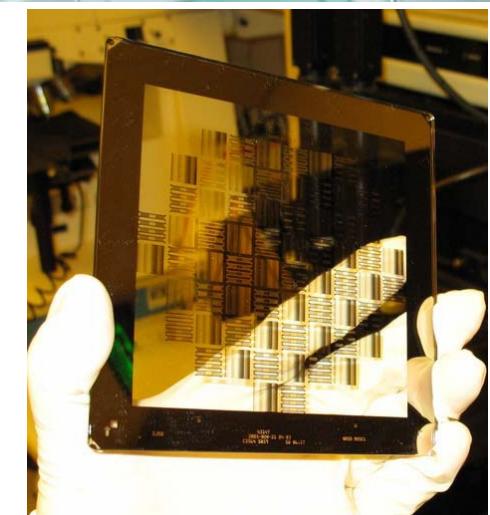
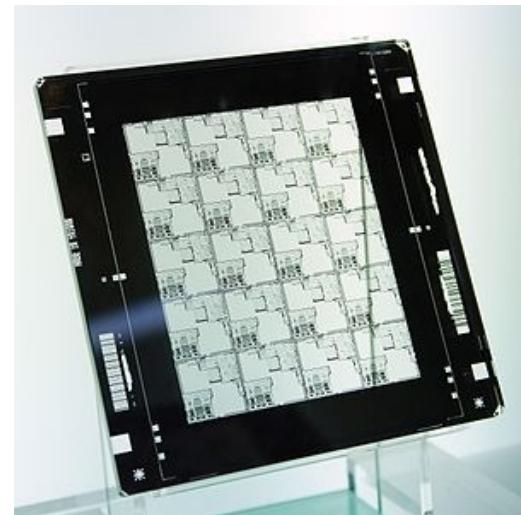
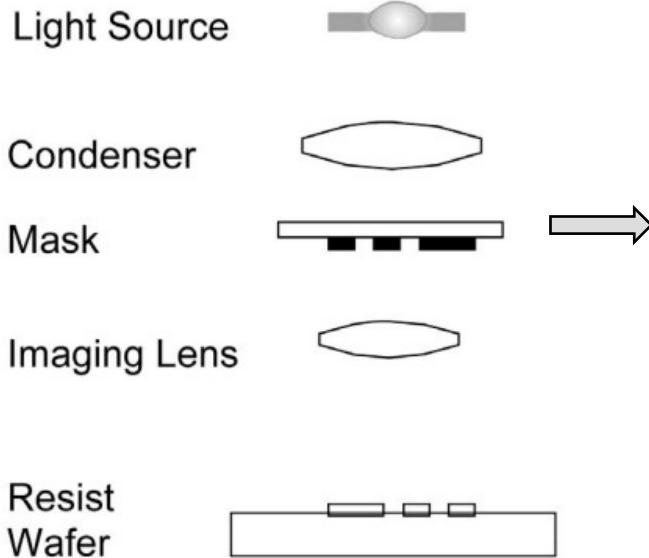
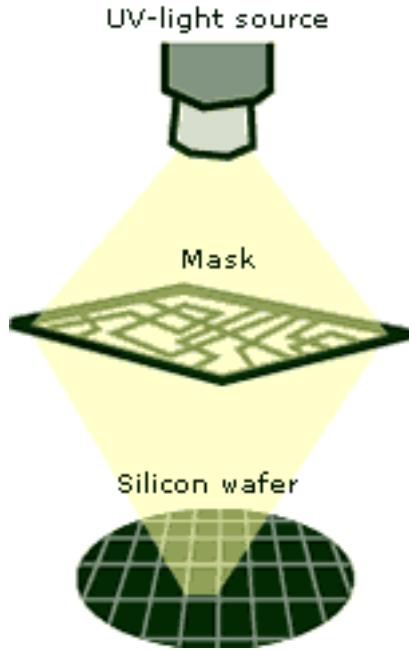
CMOS transistors are fabricated on silicon wafer

Lithography process similar to printing press

On each step, different materials are deposited or etched

Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Princípio de base: litografia



FONTE:

http://www.nobelprize.org/educational/physics/integrated_circuit/history/

<http://spie.org/samples/PM190.pdf>

Light-field photomask

Processo de Fabricação de Cls

Photoresist Coating

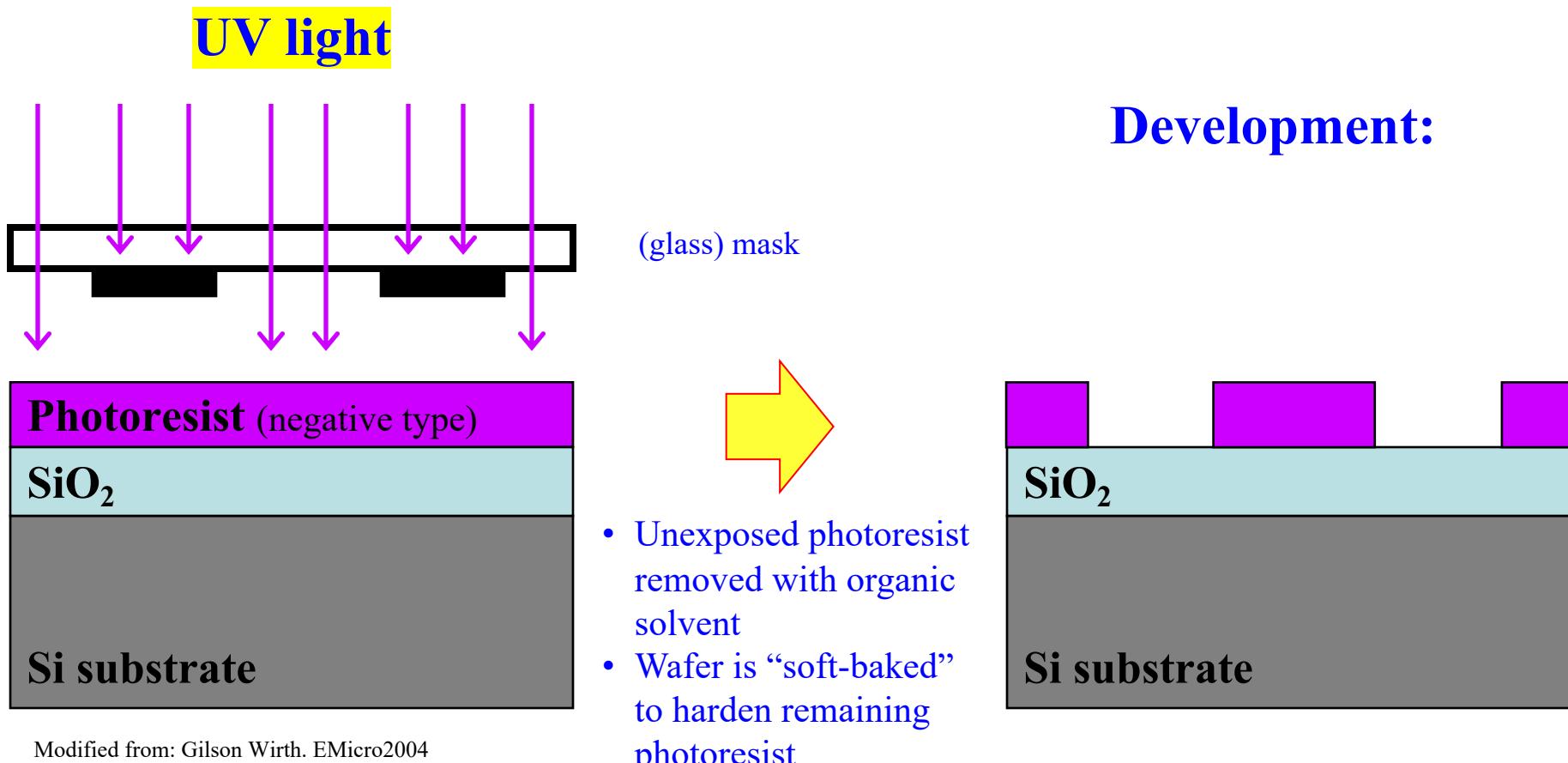
A light sensitive **polymer** is evenly applied by spinning the wafer (thickness ~ $1\mu\text{m}$)

Negative photoresist: when exposed to light, it becomes insoluble

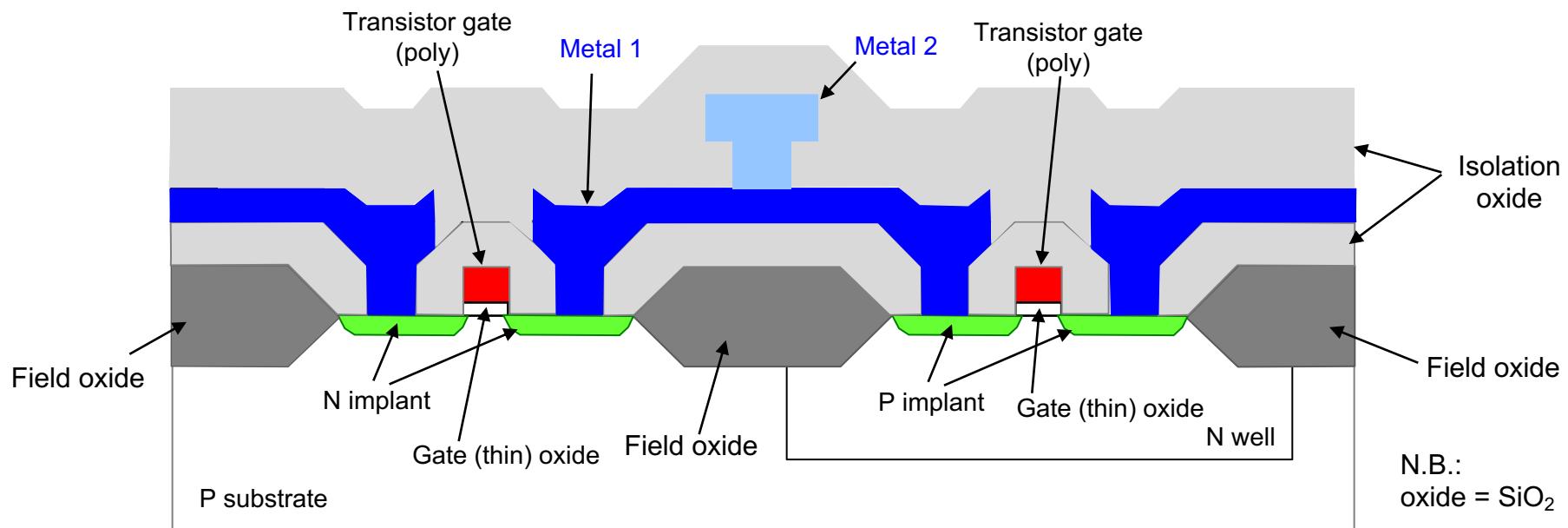
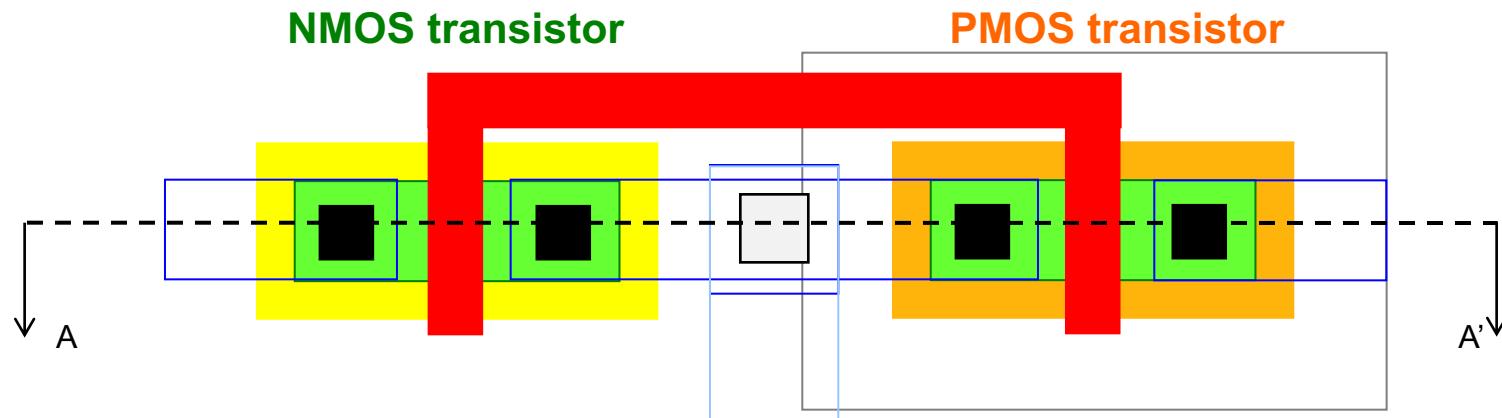


Processo de Fabricação de Cls

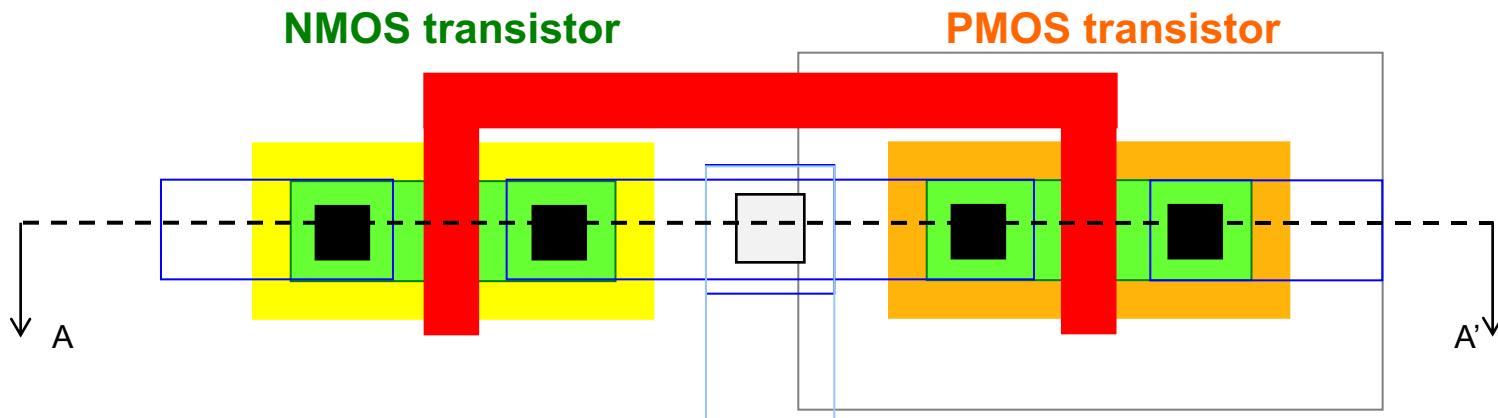
Stepper Exposure & Photoresist Development



Layout vs. AA' Cross on Fabricated Structure

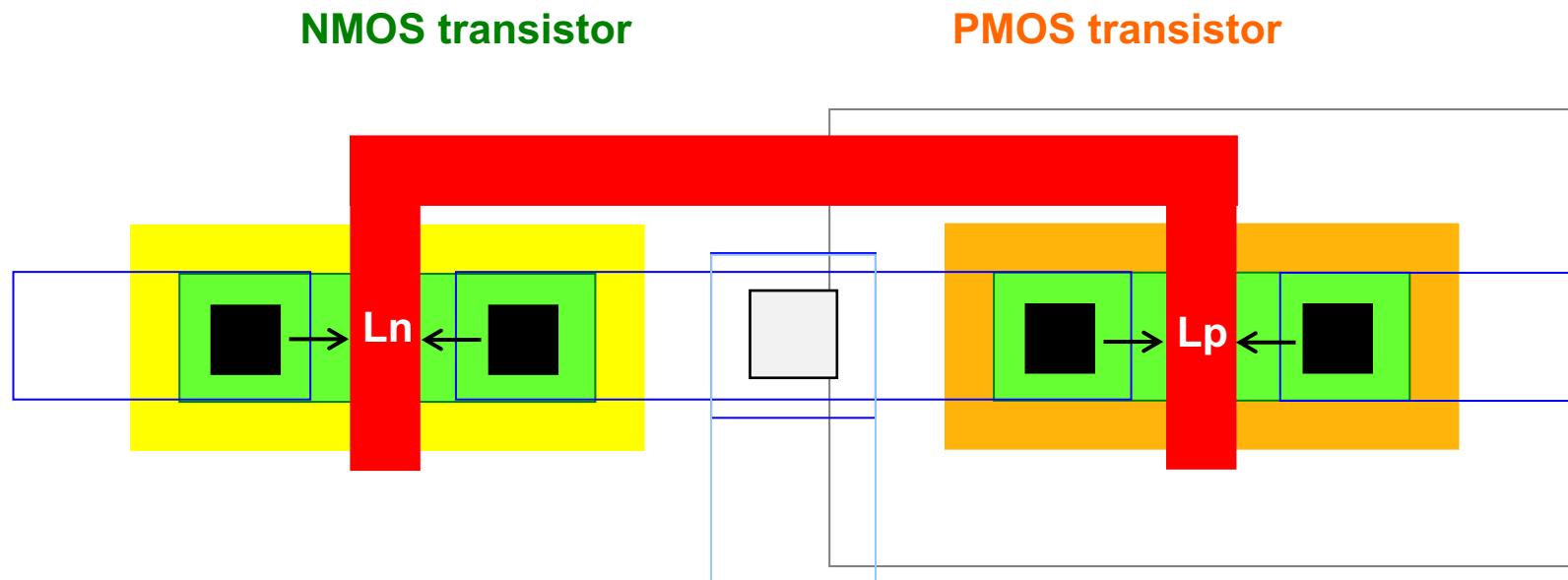


Layout vs. AA' Cross on Fabricated Structure



- Designers define only the top view geometries
- The vertical geometries (thickness of the various materials) are consequence of the fabrication process

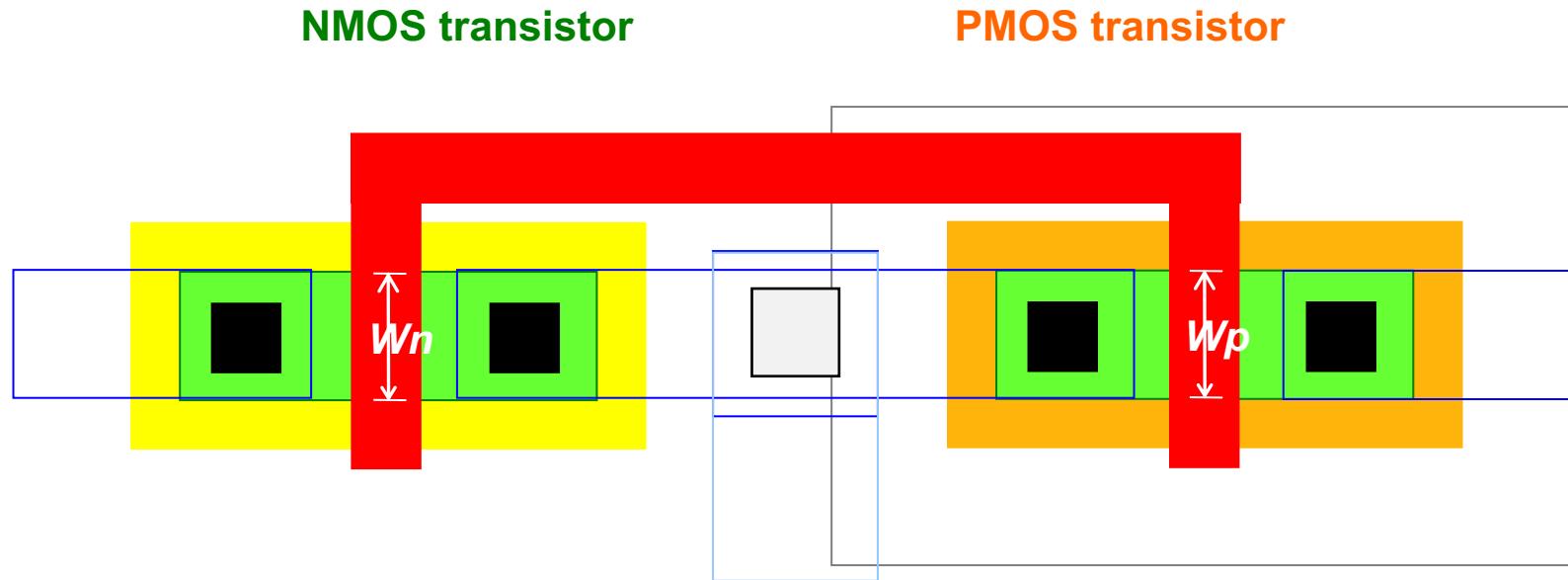
Process Features: Gate Length



L_n, L_p : NMOS, PMOS transistor channel length

L_{min} : minimum channel length allowed by a given fabrication process. Examples: 350nm, 180nm, 130nm, 90nm, 65nm, 45nm, 32nm, 22nm ...

Process Features: Gate Width



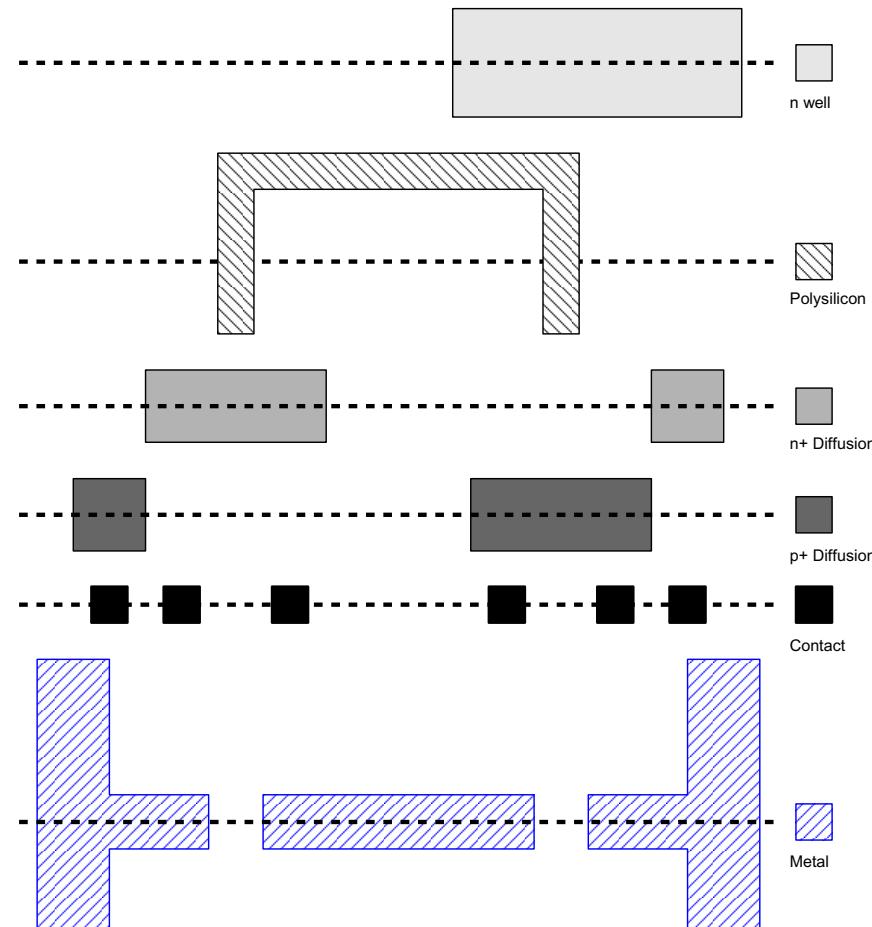
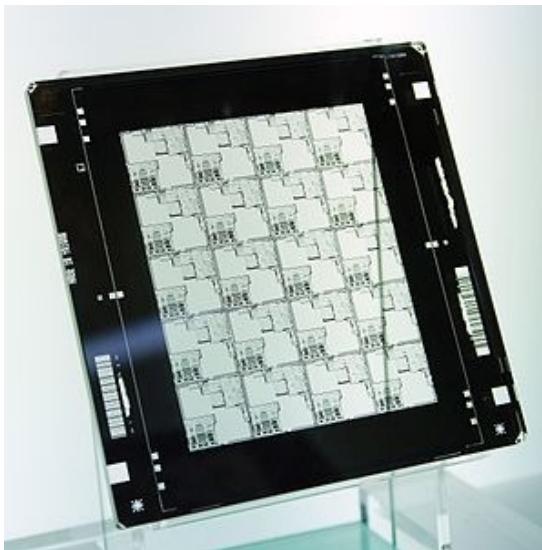
W_n, W_p : NMOS, PMOS channel width

W_{min} : minimum channel width allowed by a given fabrication process
(generally, is the same value for both NMOS and PMOS)

Detailed Mask Views

□ Six masks

- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal



ORDEM DE FABRICAÇÃO

Processo de Fabricação CMOS

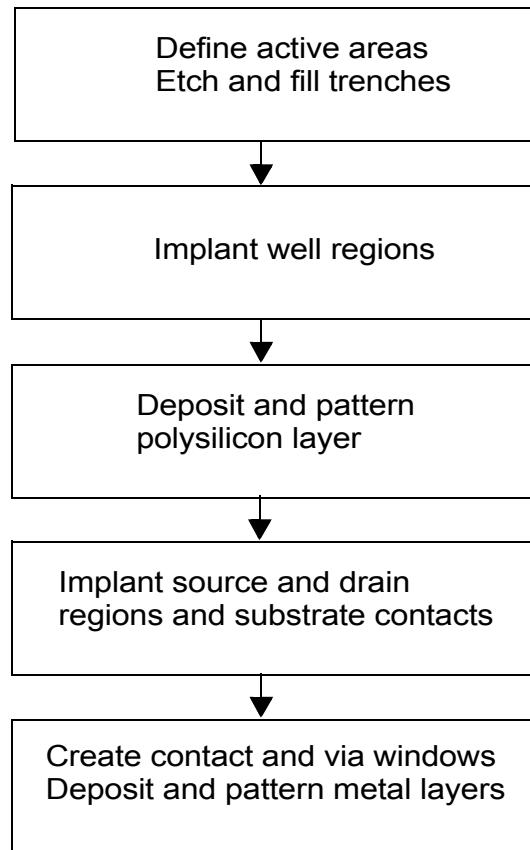
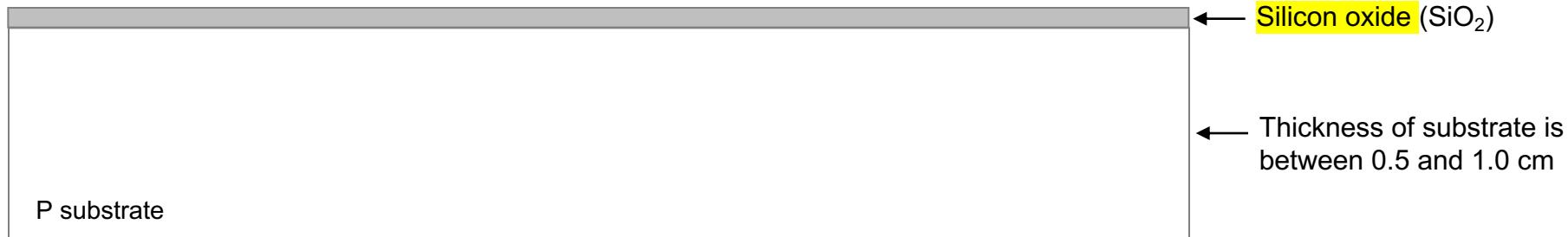


Figure 2.6 Simplified process sequence for the manufacturing of a n-dual-well CMOS circuit.

Processo de Fabricação CMOS

N Well Creation (1/12)

A thin layer (“film”) of oxide (SiO_2), typically with 10nm, is deposited through dry oxidation (which is slow, but allows for a good thickness control)



Processo de Fabricação CMOS

N Well Creation (2/12)

Deposition

Any CMOS process requires the repetitive deposition of layers of a material over the complete wafer, to either act as buffers for a processing step, or as insulating or conducting layers. We have already discussed the oxidation process, which allows a layer of SiO_2 to be grown. Other materials require different techniques. For instance, silicon nitride (Si_3N_4) is used as a sacrificial buffer material during the formation of the field oxide and the introduction of the stopper implants. This silicon nitride is deposited everywhere using a process called *chemical vapor deposition* or CVD, which uses a gas-phase reaction with energy supplied by heat at around 850°C .

A thicker layer (“film”) of “sacrificial” silicon nitride (Si_3N_4) is deposited through Plasma CVD (Chemical Vapor Deposition)

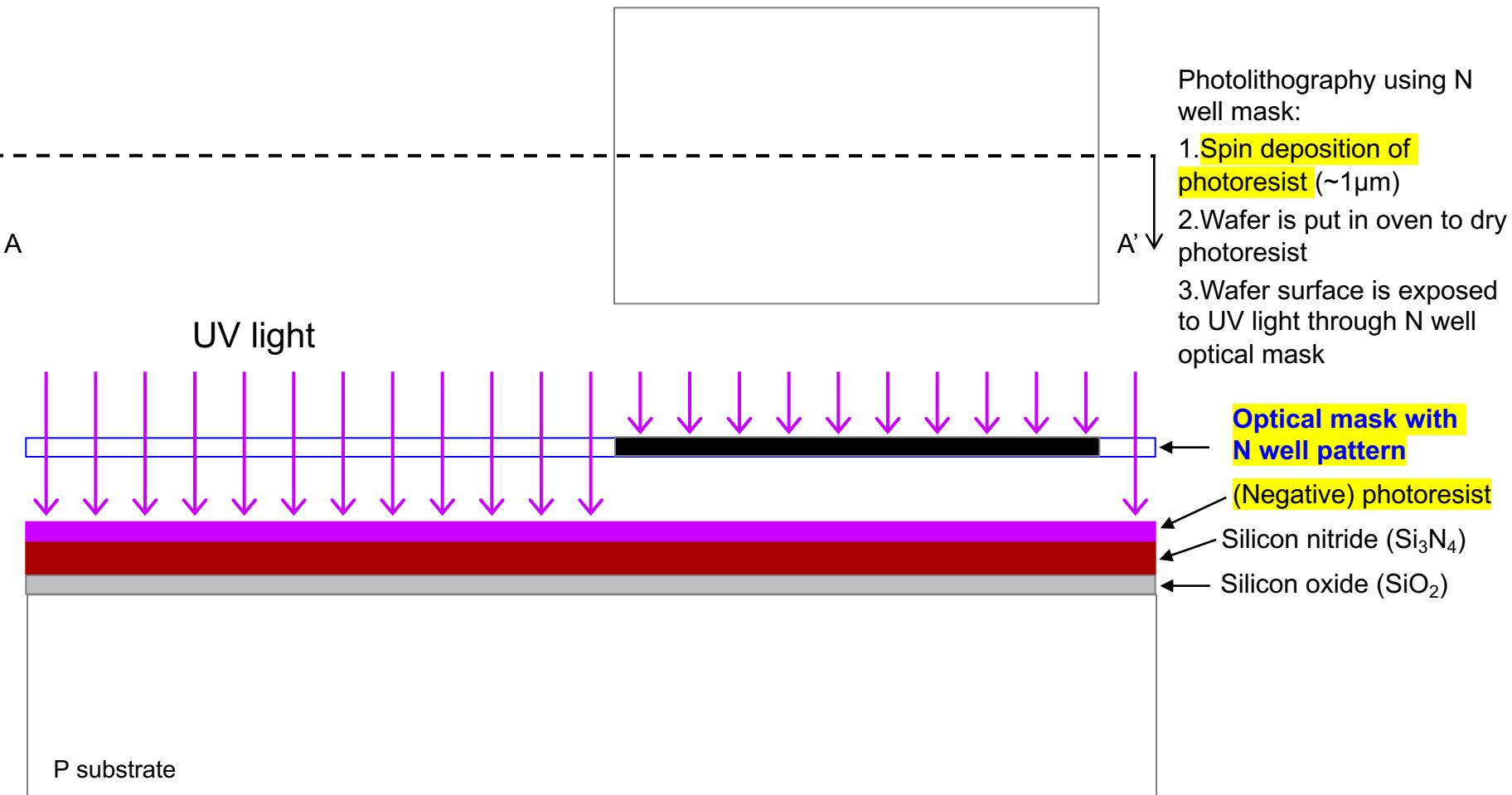
Cap. 2 – Rabaey



Processo de Fabricação CMOS

N Well Creation (3/12)

“N well layer” (pattern)



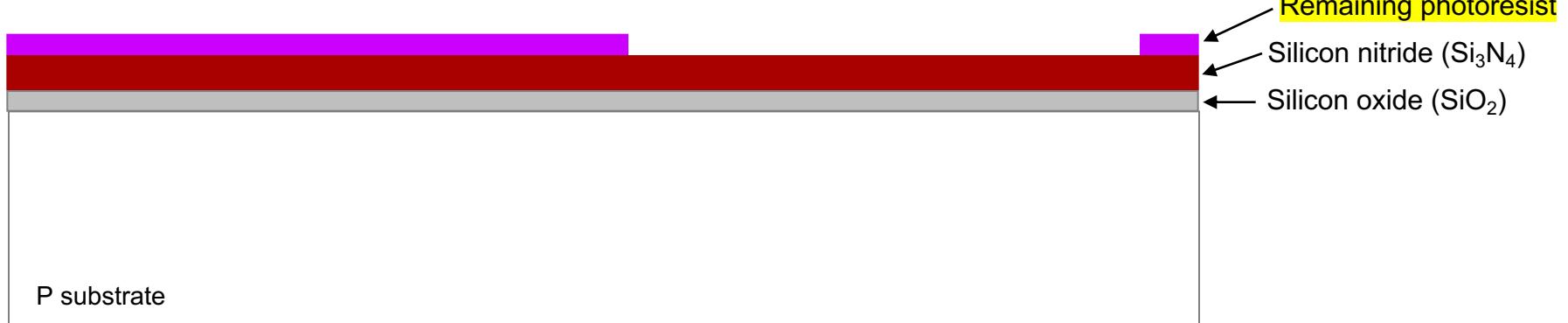
Processo de Fabricação CMOS

N Well Creation (4/12)

Photolithography using N well mask:

4. Unexposed photoresist is removed by using organic solvent

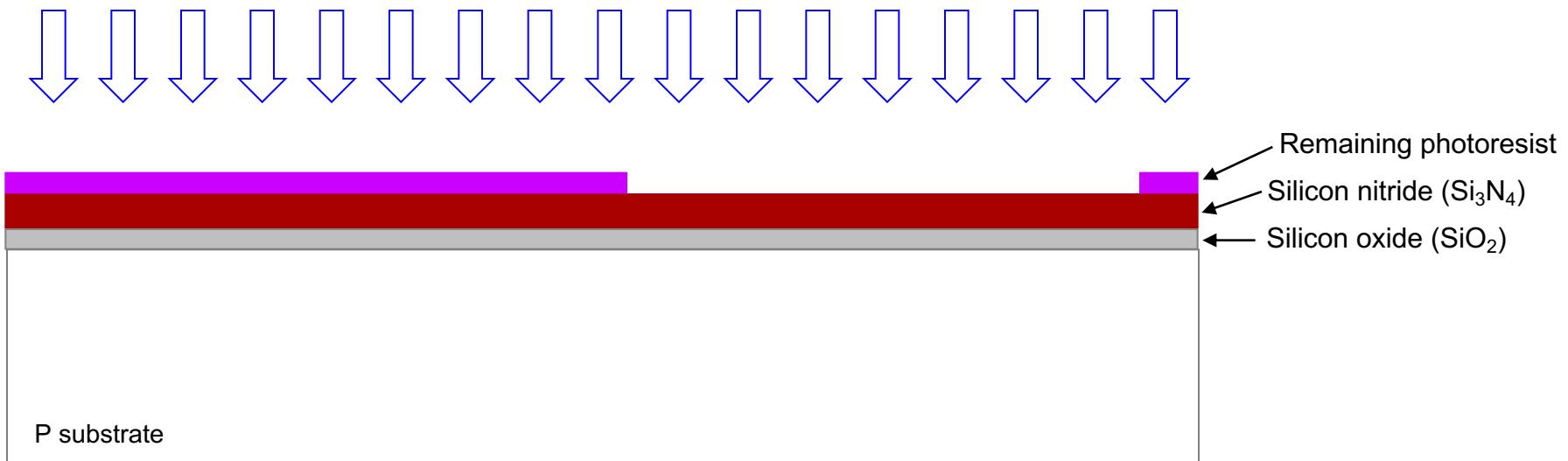
5. Wafer is “soft baked” at low temperature to hard remaining photoresist



Processo de Fabricação CMOS

N Well Creation (5/12)

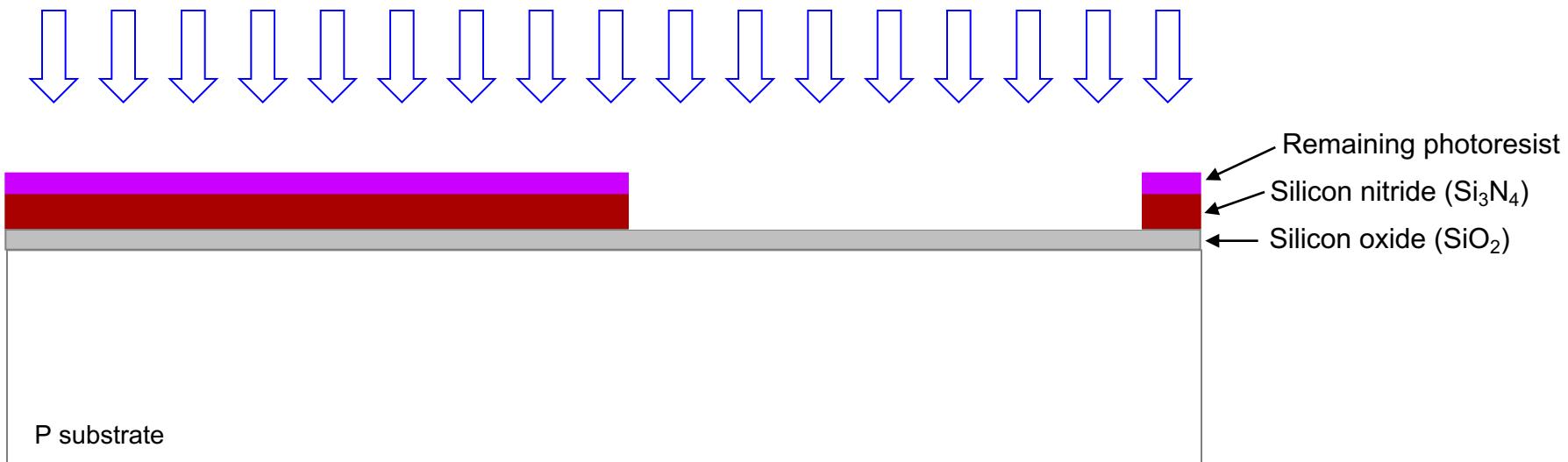
Nitride is selectively removed by plasma etching (photoresist serves as coat)



Processo de Fabricação CMOS

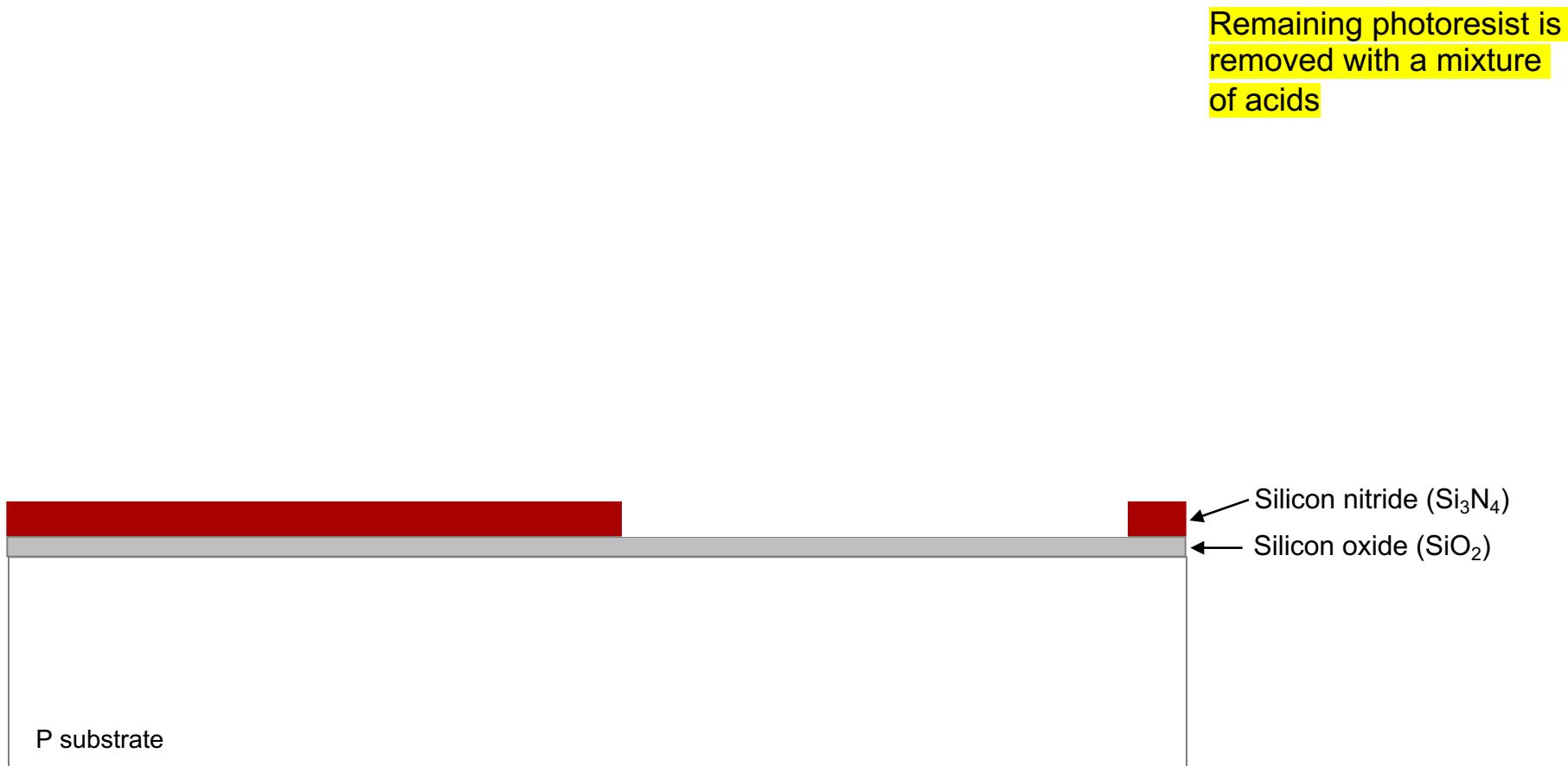
N Well Creation (6/12)

Nitride is selectively removed by plasma etching (photoresist serves as coat)



Processo de Fabricação CMOS

N Well Creation (7/12)

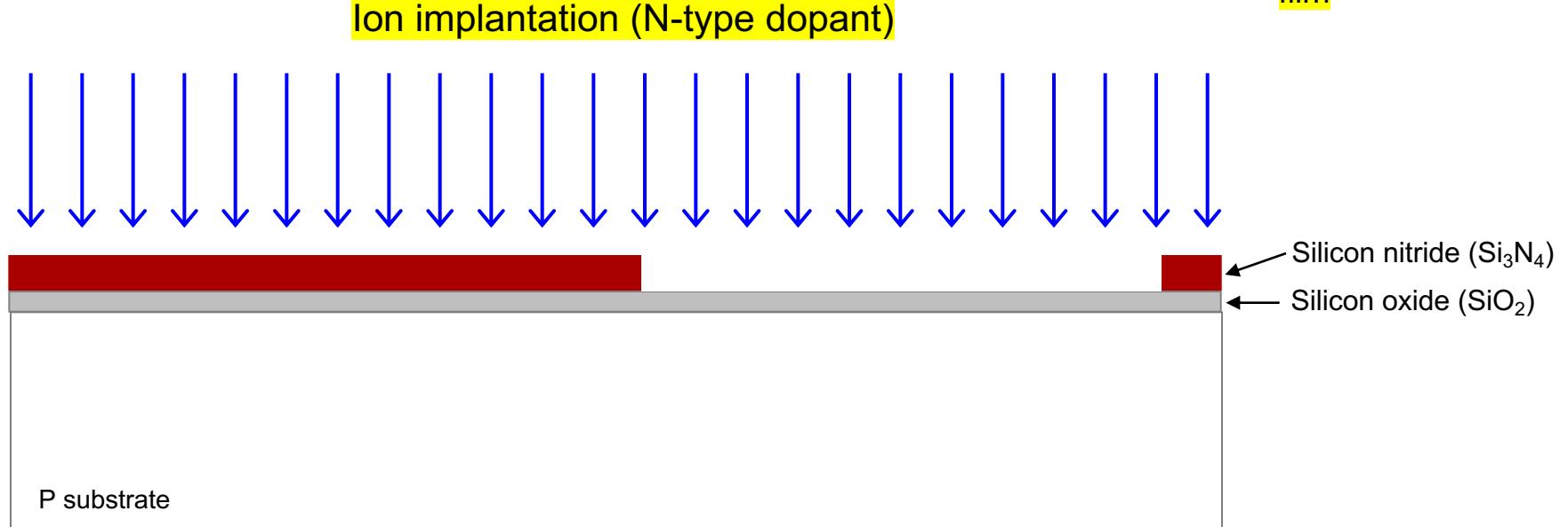


Processo de Fabricação CMOS

N Well Creation (8/12)

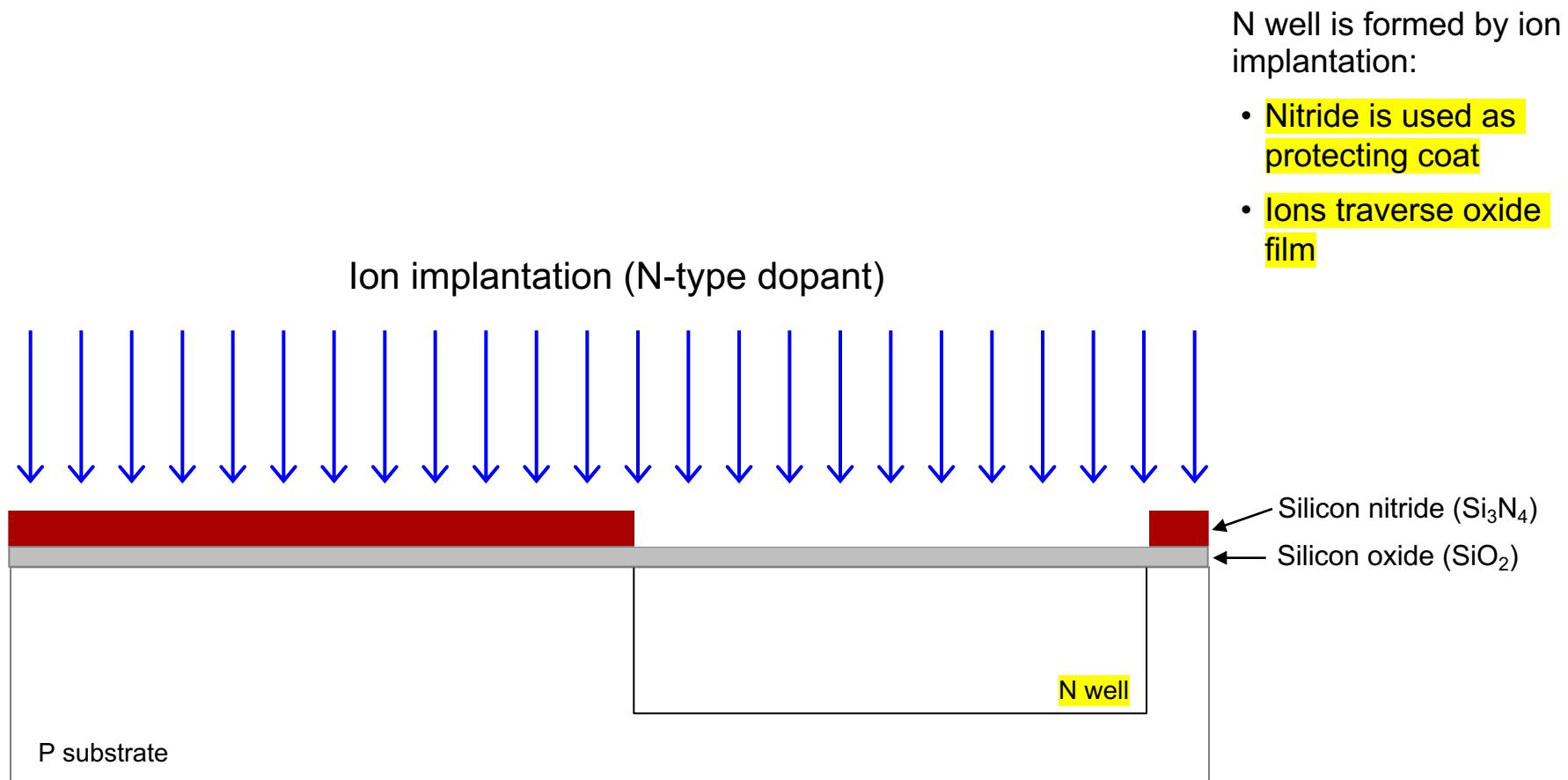
N well is formed by ion implantation:

- Nitride is used as protecting coat
- Ions traverse oxide film



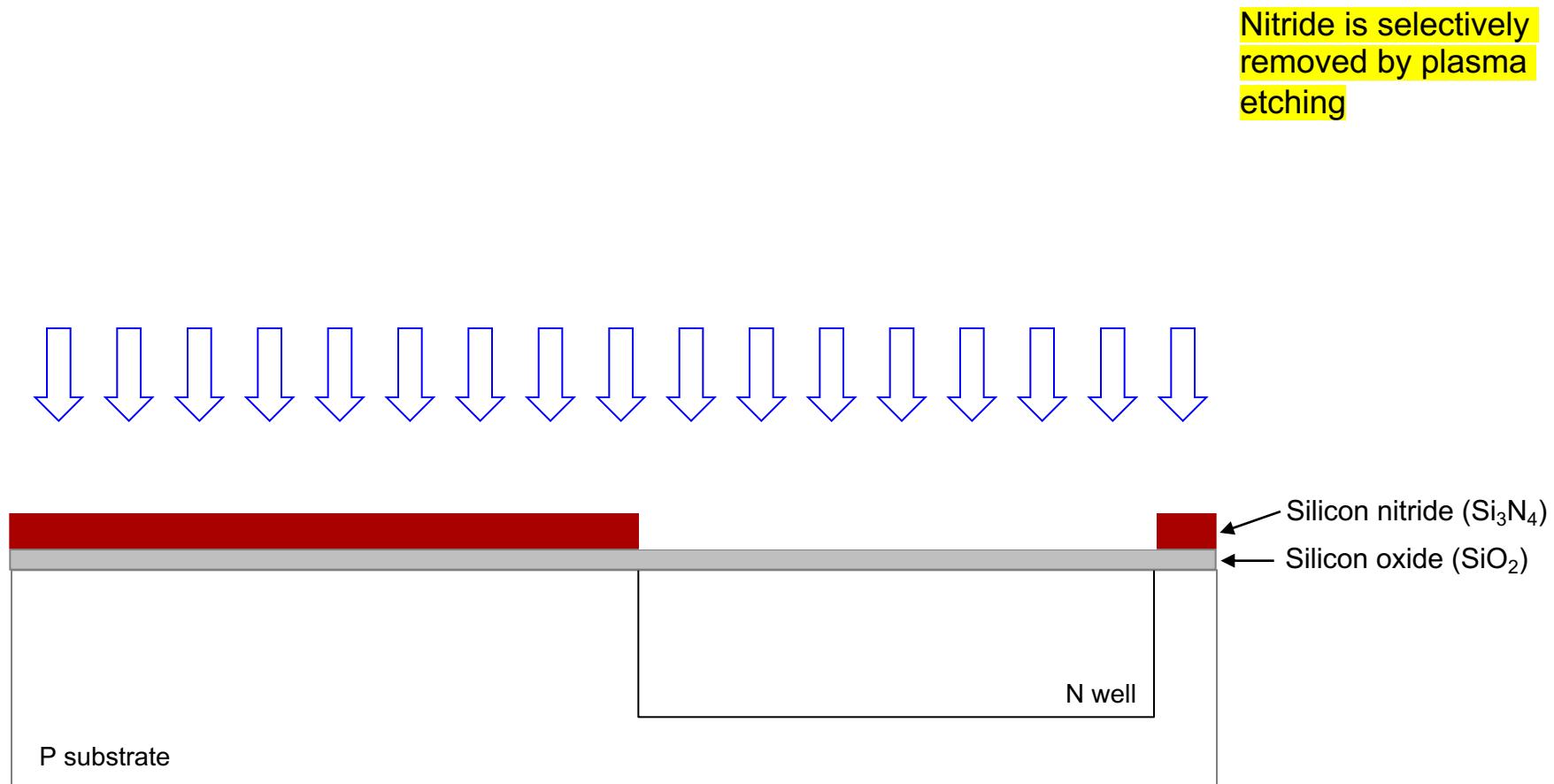
Processo de Fabricação CMOS

N Well Creation (9/12)



Processo de Fabricação CMOS

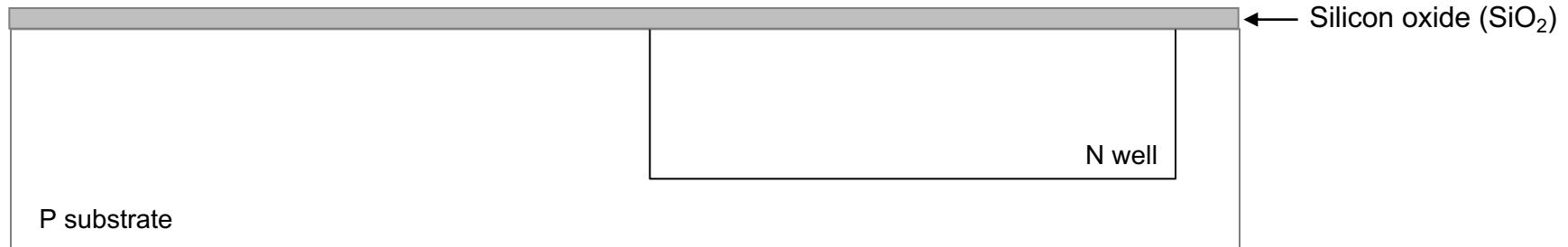
N Well Creation (10/12)



Processo de Fabricação CMOS

N Well Creation (11/12)

Oxide is removed by using Hydrofluoric acid (HF)



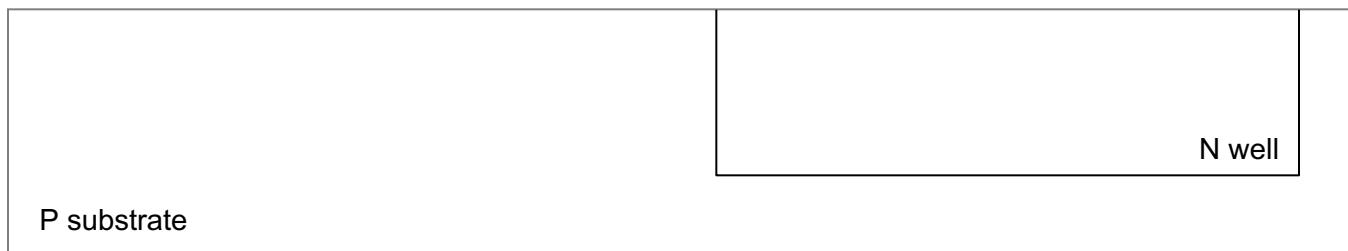
Processo de Fabricação CMOS

N Well Creation (12/12)

Resumo

1. Deposita óxido
2. Deposita nitrito
3. Deposita photoresist
4. Exposição UV
5. Remove photoresist
6. Remove nitrito (parcial)
7. **Implantação iônica**
8. Remove nitrito (total)
9. Remove óxido
10. “Limpa” o wafer

The wafer is cleaned
(SRD - spin, rinse and
dry with nitrogen)

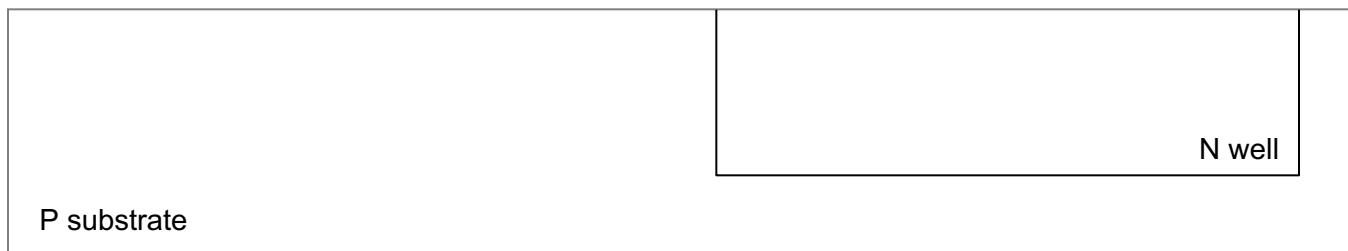


Processo de Fabricação CMOS

Field Oxide Growth (1/5)

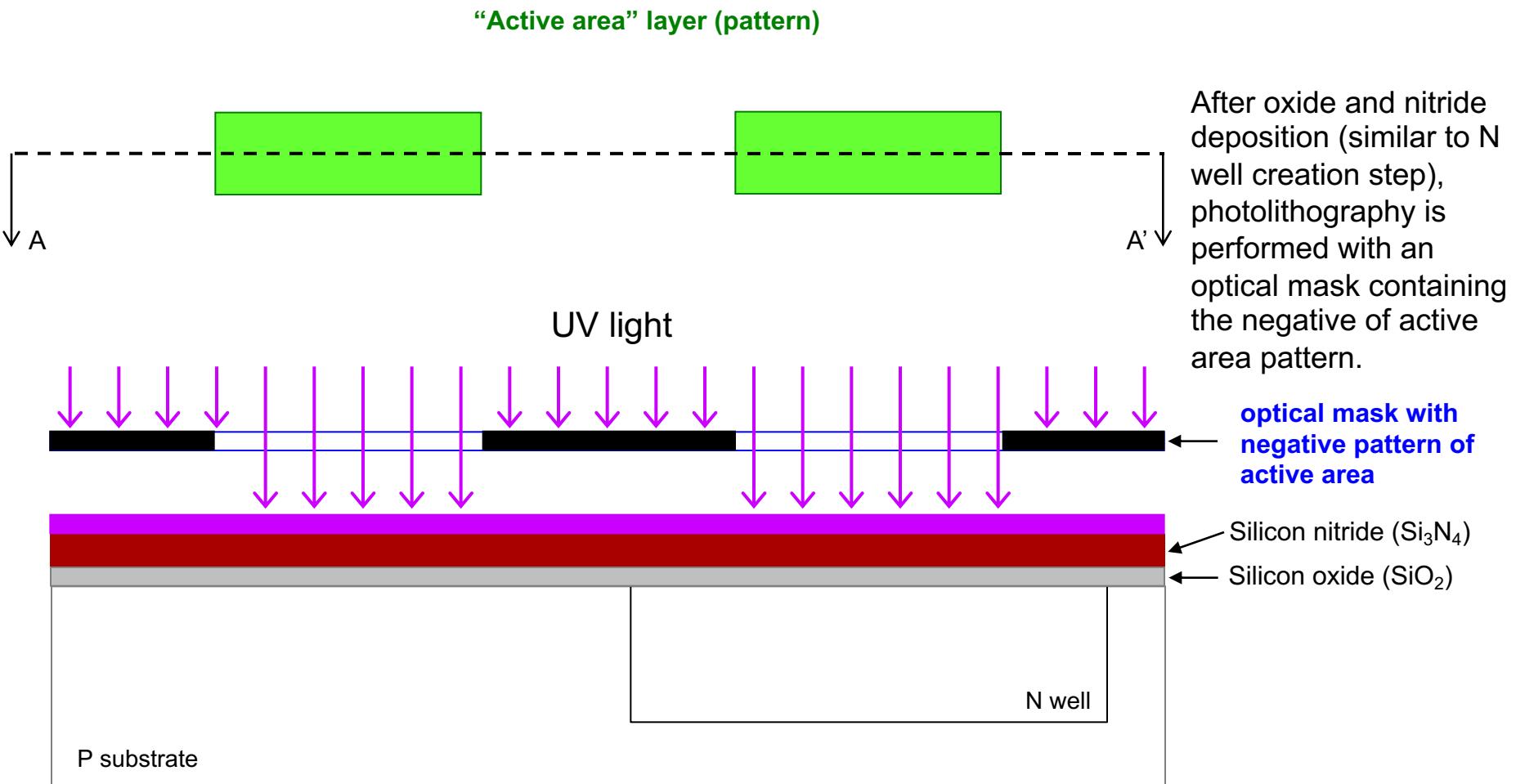
There are two types of regions ion wafer surface:

- Active area (where transistors are)
- Field area (must isolate transistors)



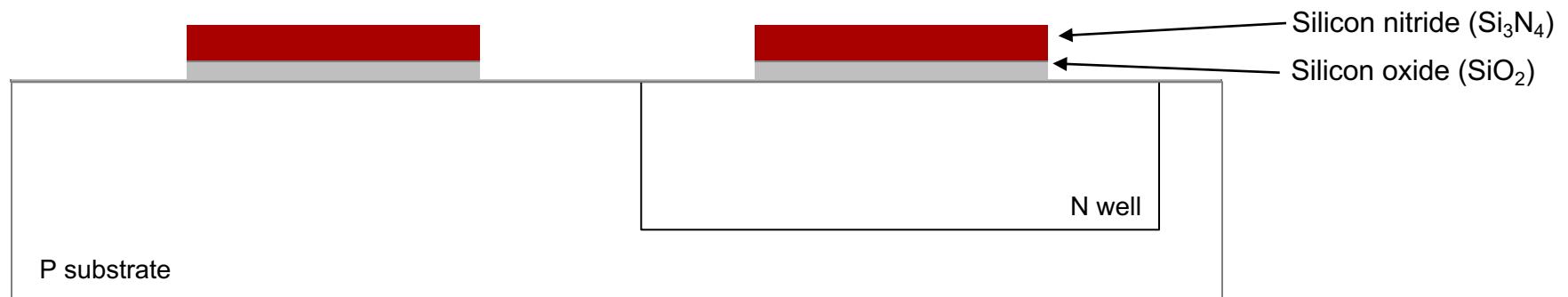
Processo de Fabricação CMOS

Field Oxide Growth (2/5)



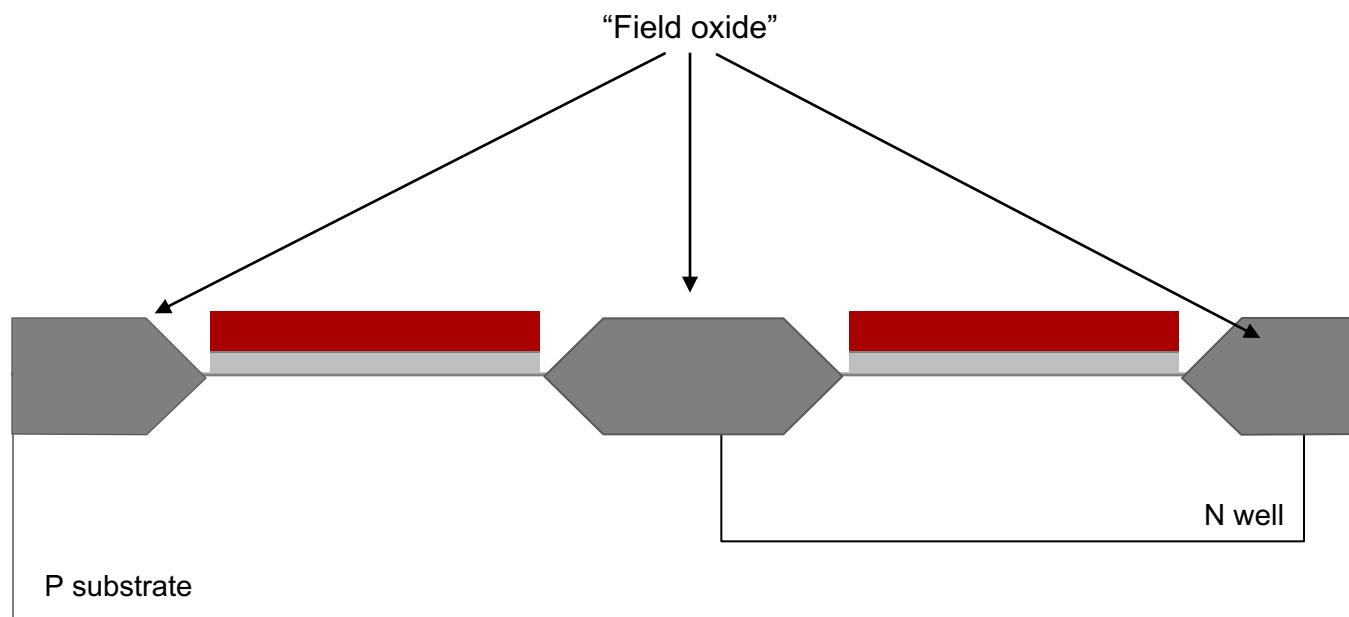
Processo de Fabricação CMOS

Field Oxide Growth (3/5)



Processo de Fabricação CMOS

Field Oxide Growth (4/5)



Wet oxidation is used to grow a thick layer of oxide (with a few hundreds of nanometers), that will serve as isolation between transistors

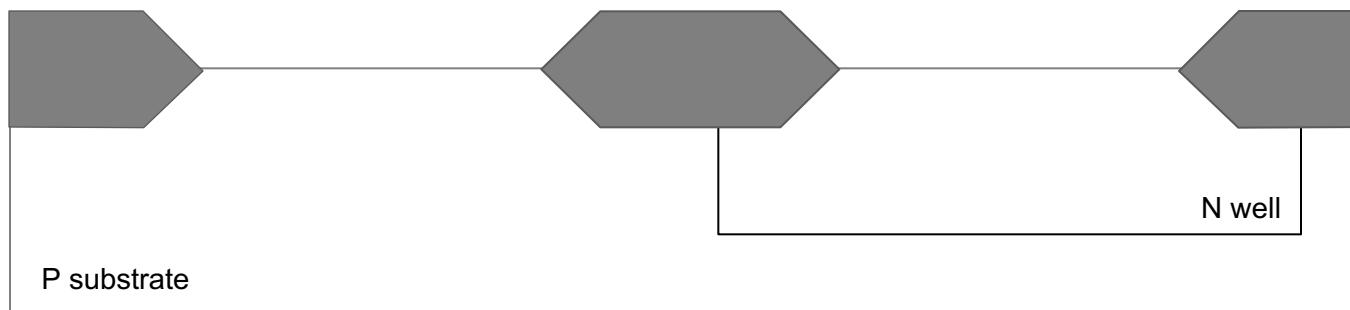
Processo de Fabricação CMOS

Field Oxide Growth (5/5)

Nitride is selectively removed by plasma etching

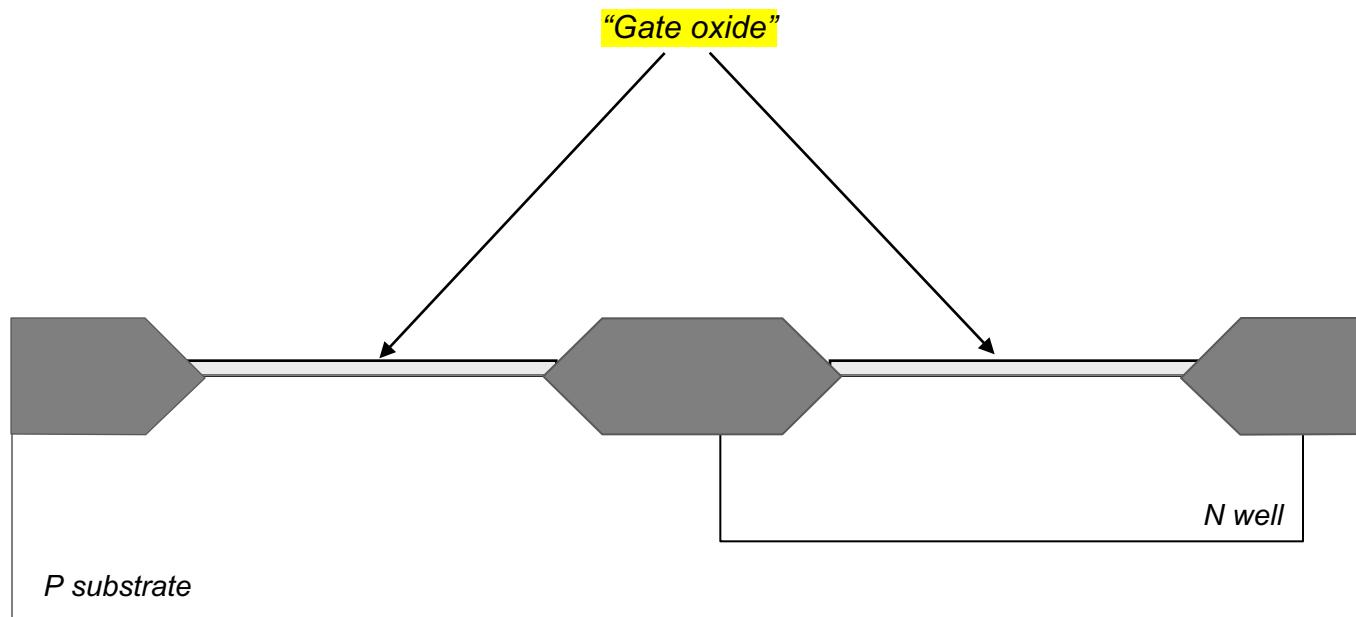
Oxide is removed by using Hydrofluoric acid (HF)

The wafer is cleaned (SRD - spin, rinse and dry with nitrogen)



Processo de Fabricação CMOS

Gate Oxide Formation

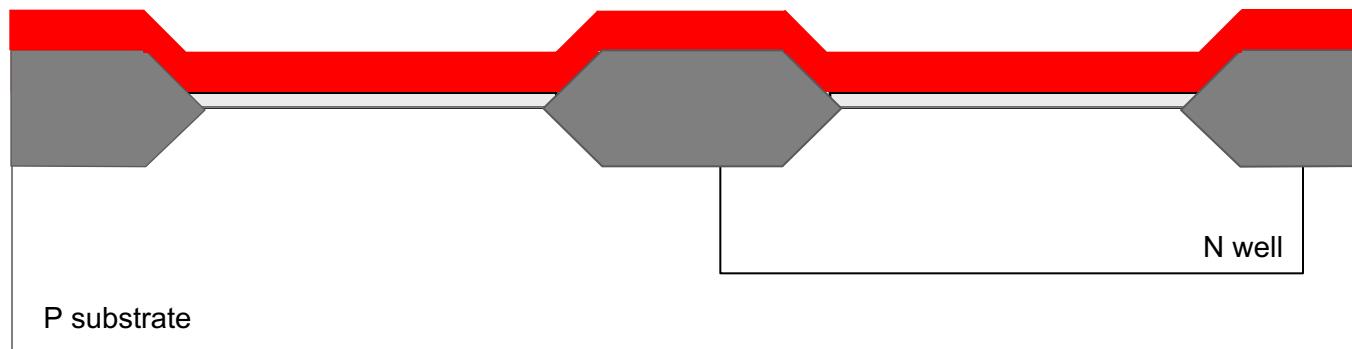


Wafer surface is submitted to **dry oxidation** to grow a thin film of oxide (~100 Angstrom), referred to as "gate oxide"

Processo de Fabricação CMOS

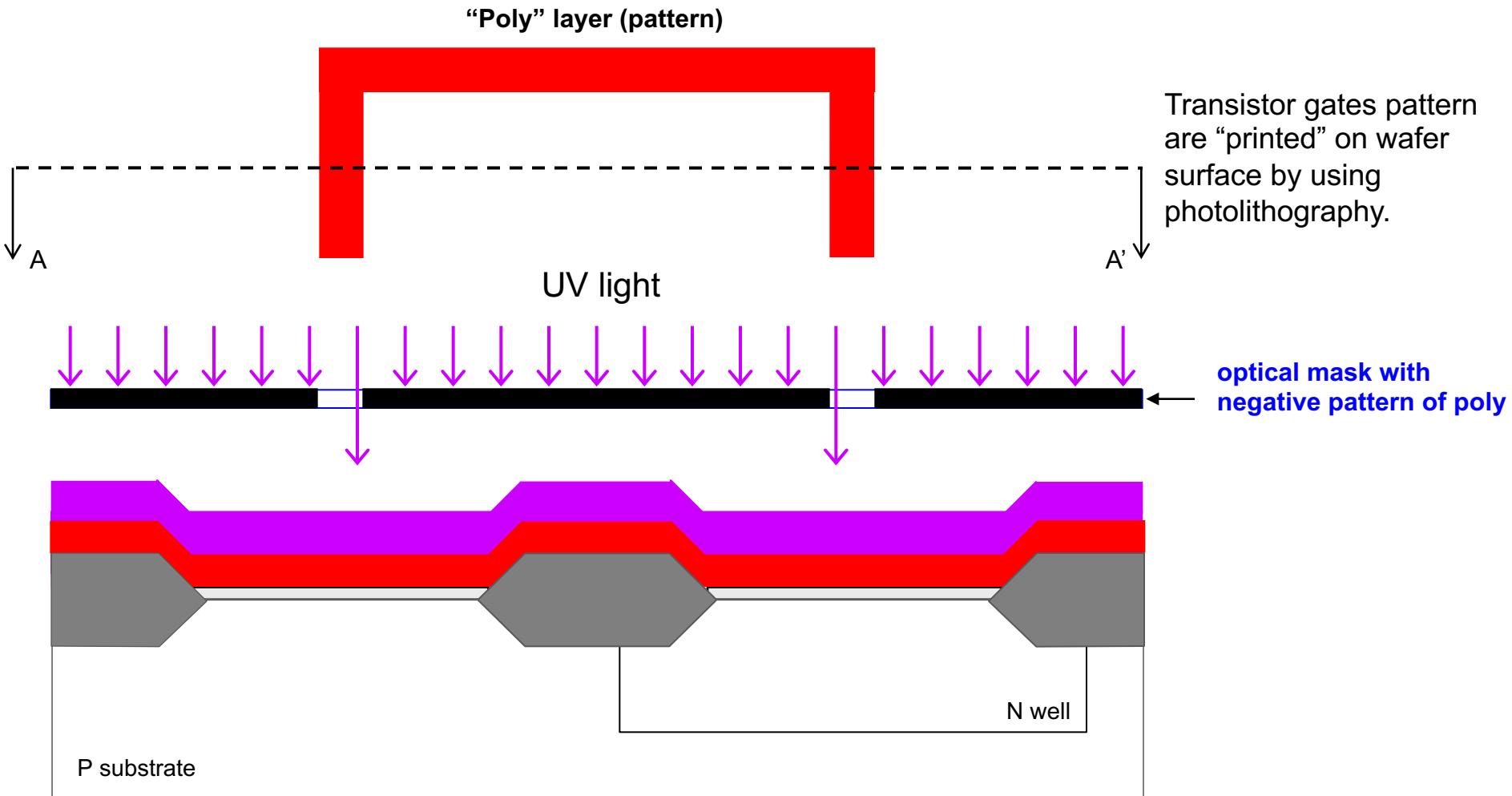
Polysilicon Deposition (1/7)

Poly is deposited by CVD process using silane gas



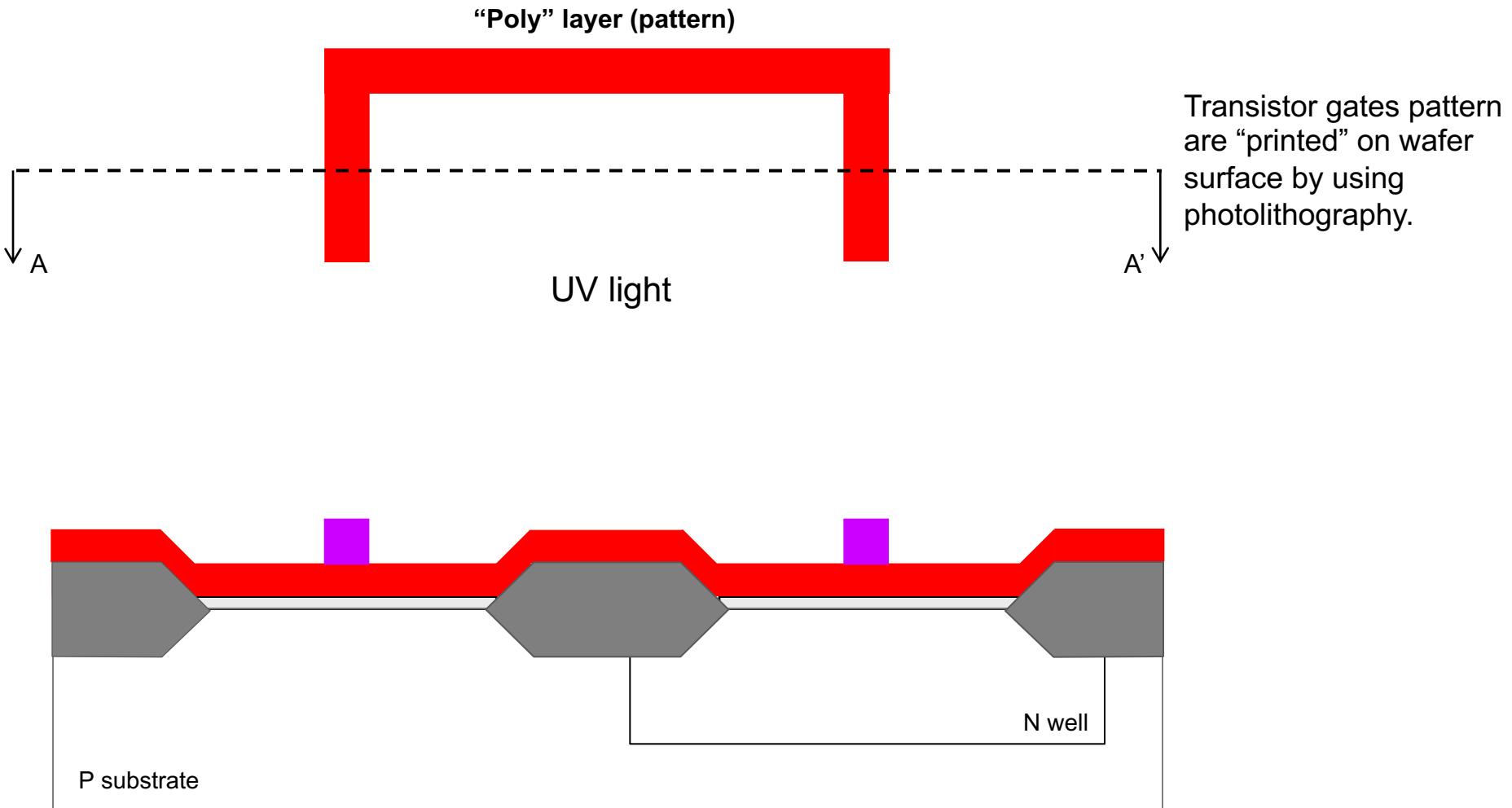
Processo de Fabricação CMOS

Polysilicon Shaping (2/7)



Processo de Fabricação CMOS

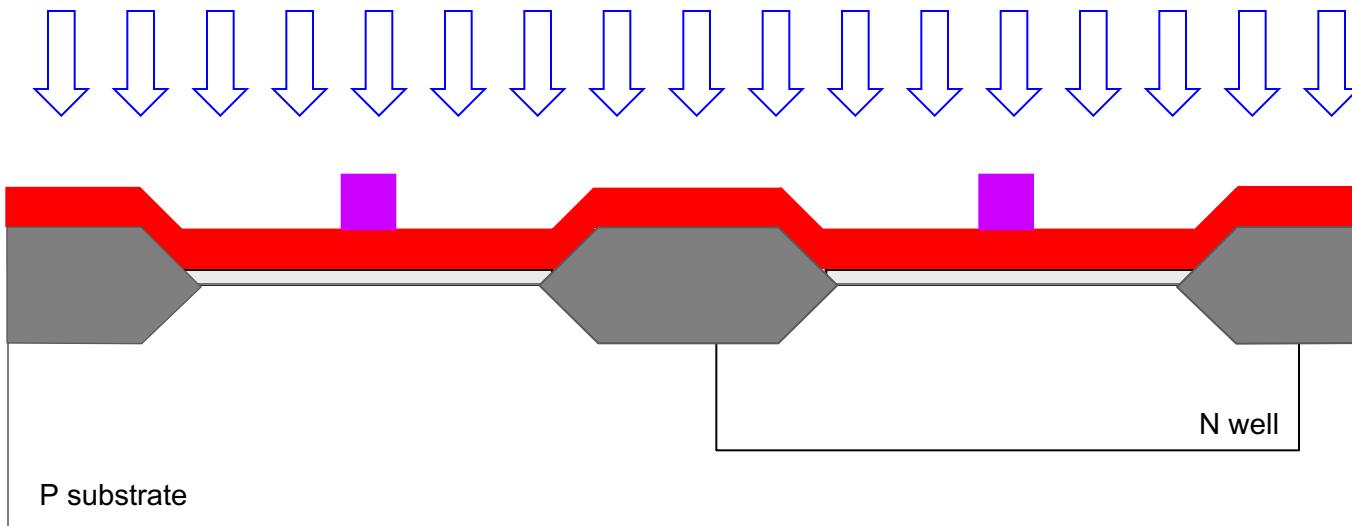
Polysilicon Shaping (3/7)



Processo de Fabricação CMOS

Polysilicon Shaping (4/7)

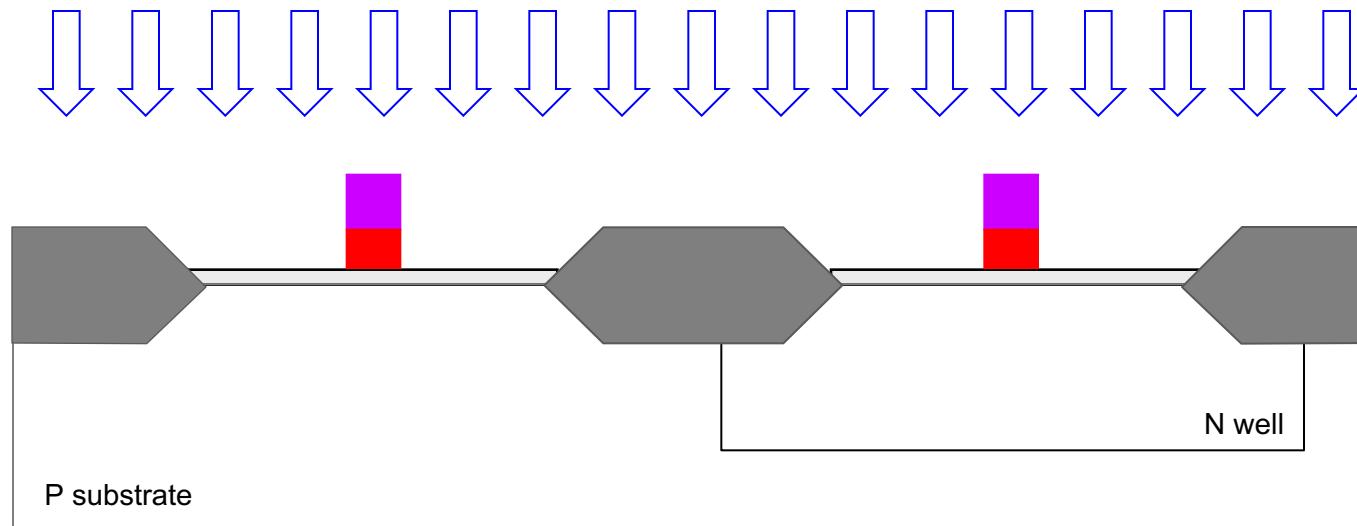
Poly is selectively removed by etching. The photoresist serves as coating.



Processo de Fabricação CMOS

Polysilicon Shaping (5/7)

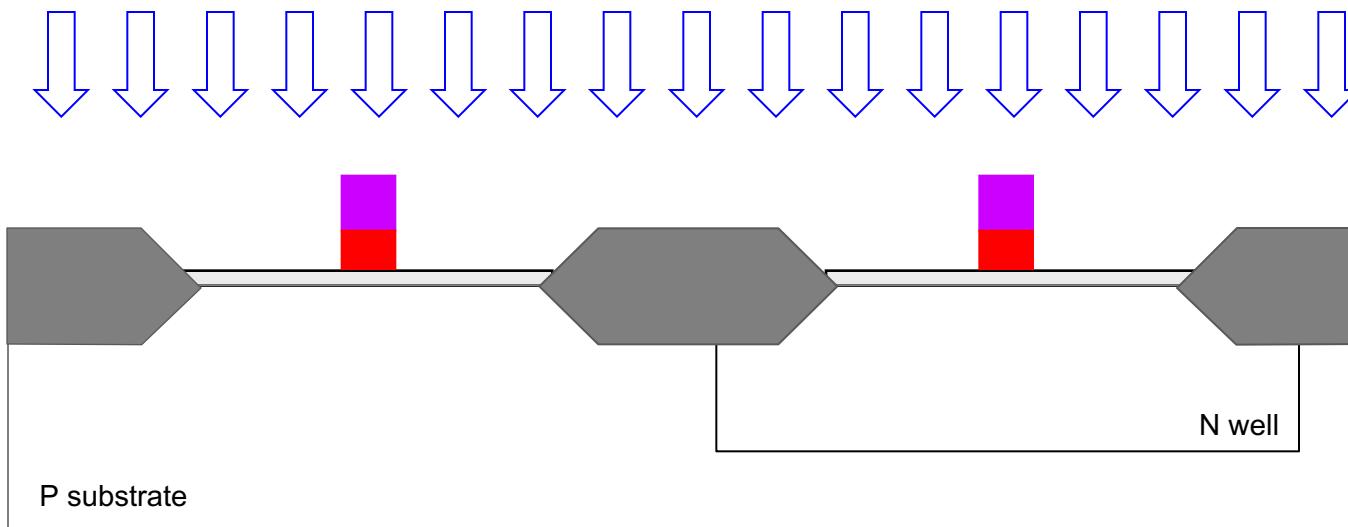
Poly is selectively removed by etching. The photoresist serves as coating.



Processo de Fabricação CMOS

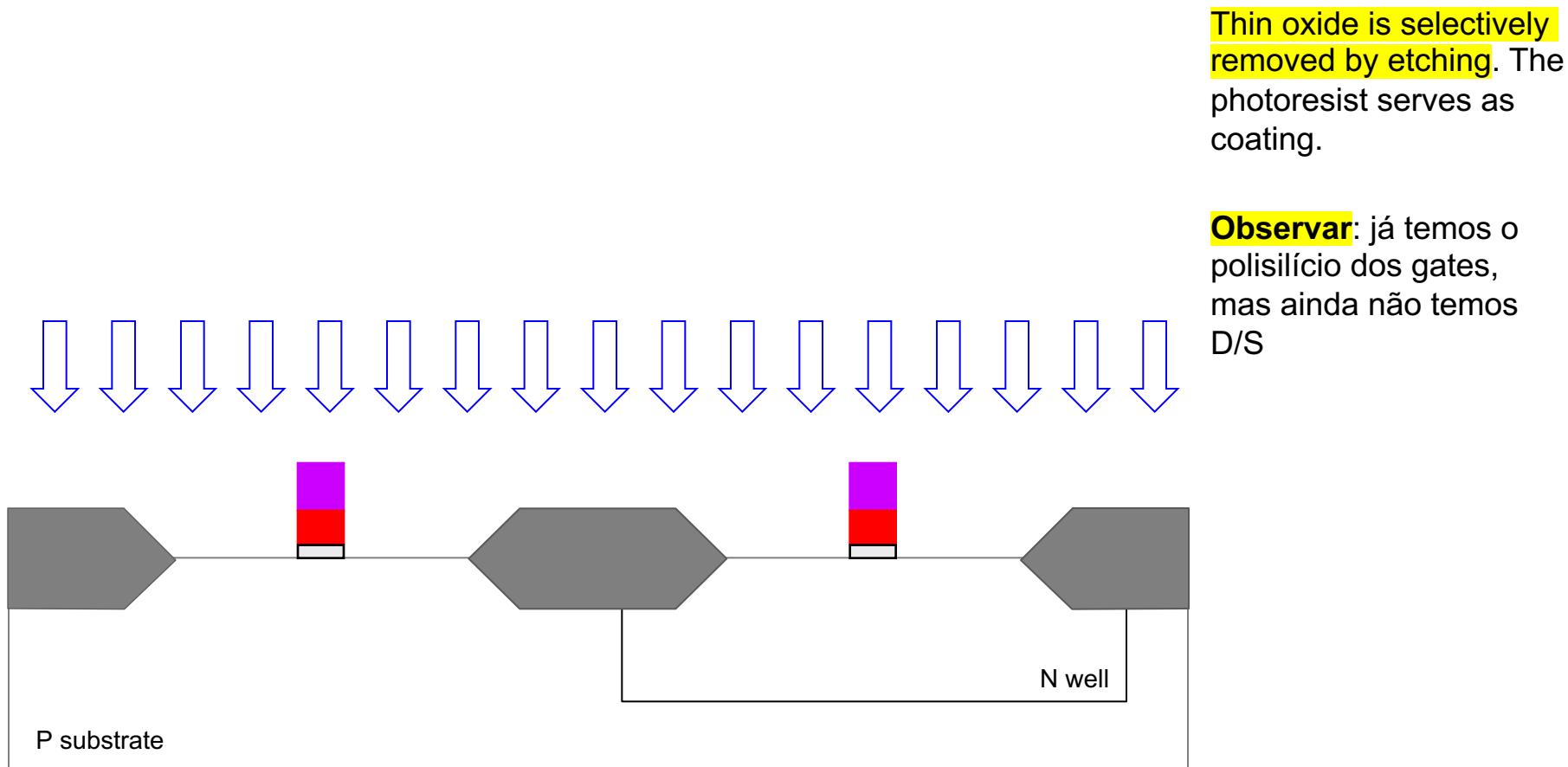
Polysilicon Shaping (6/7)

Thin oxide is selectively removed by etching. The photoresist serves as coating.



Processo de Fabricação CMOS

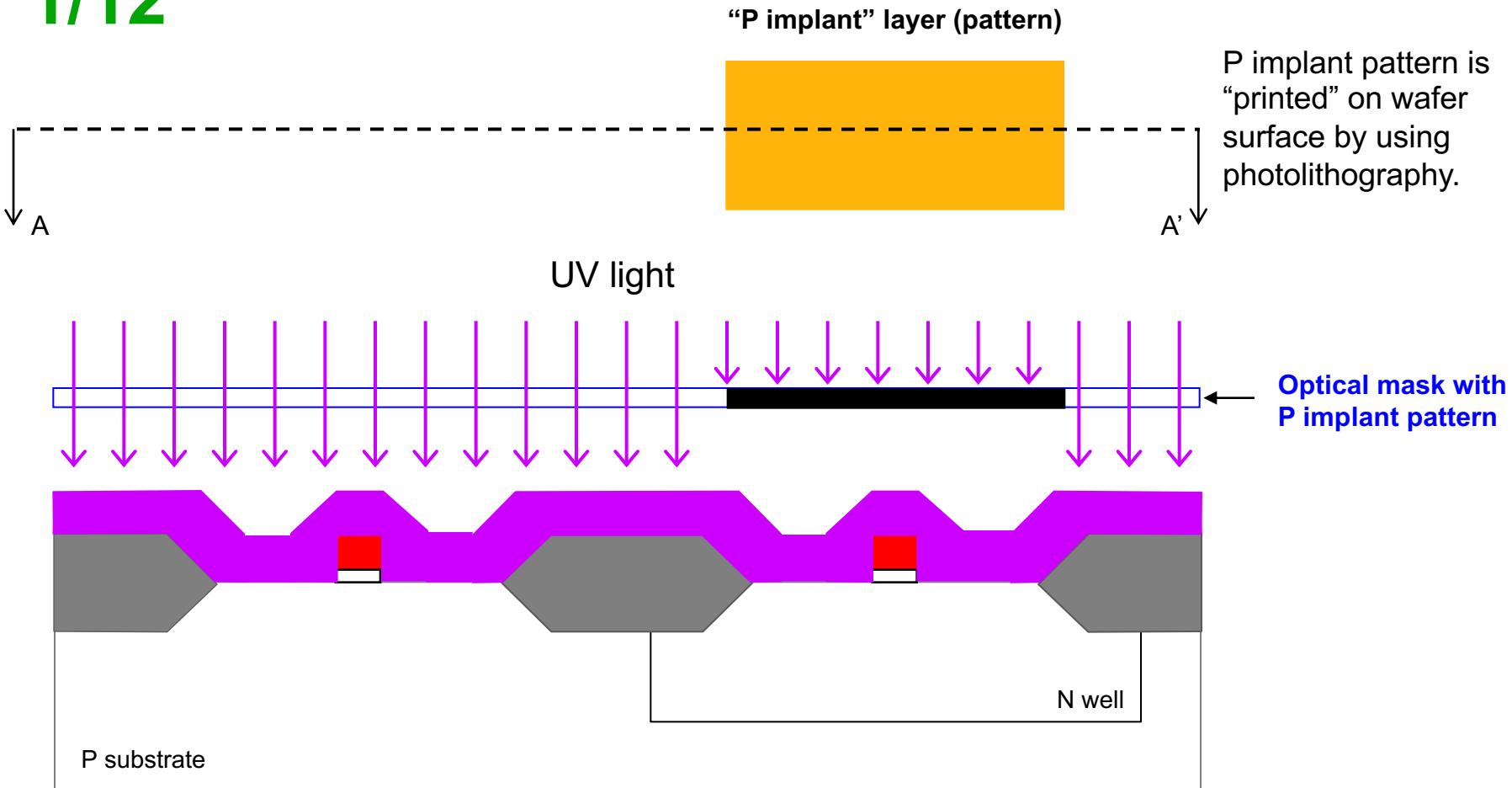
Polysilicon Shaping (7/7)



Processo de Fabricação CMOS

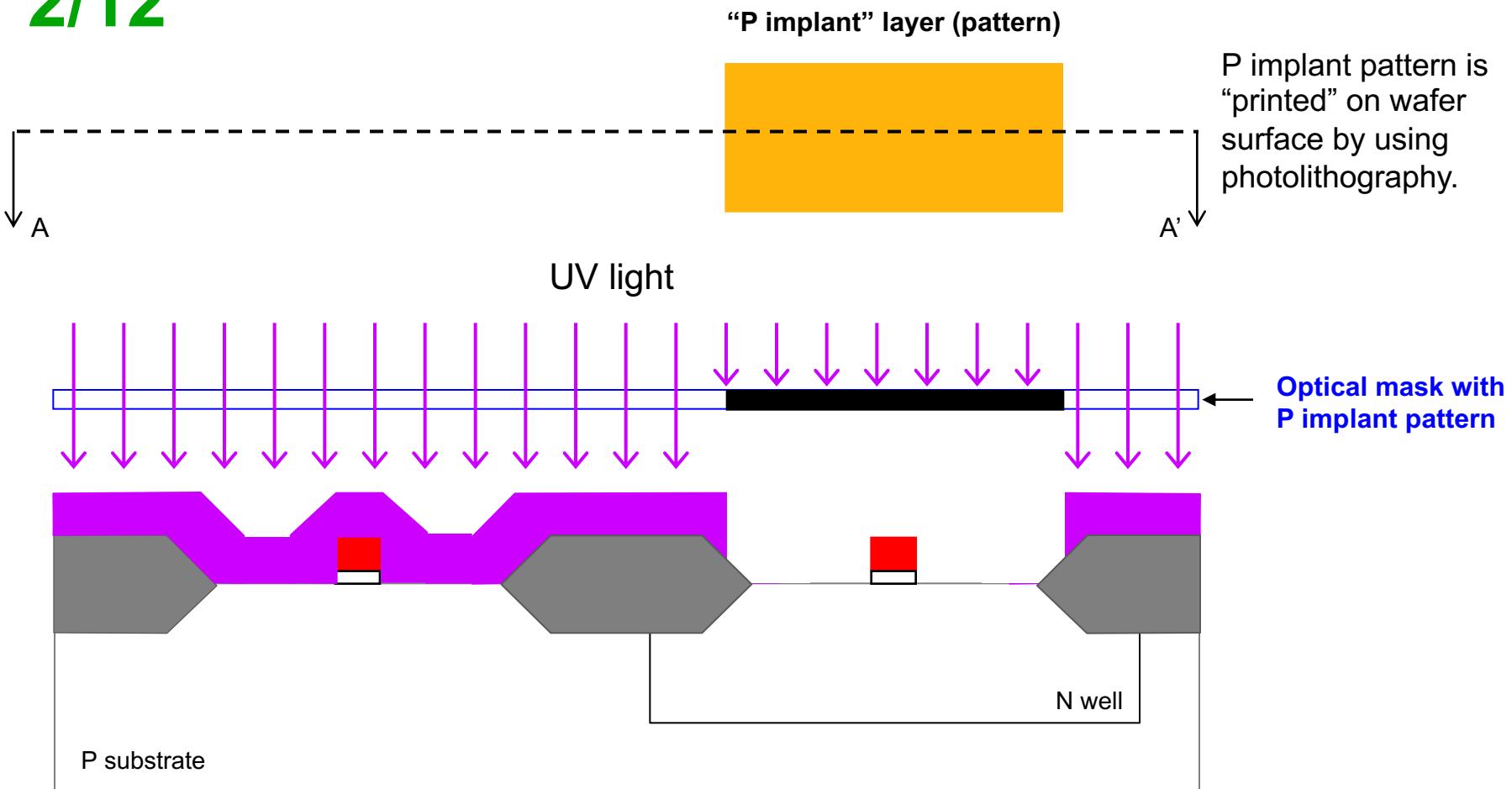
PMOS Transistor Drain and Source Creation

1/12



Processo de Fabricação CMOS

PMOS Transistor Drain and Source Creation 2/12



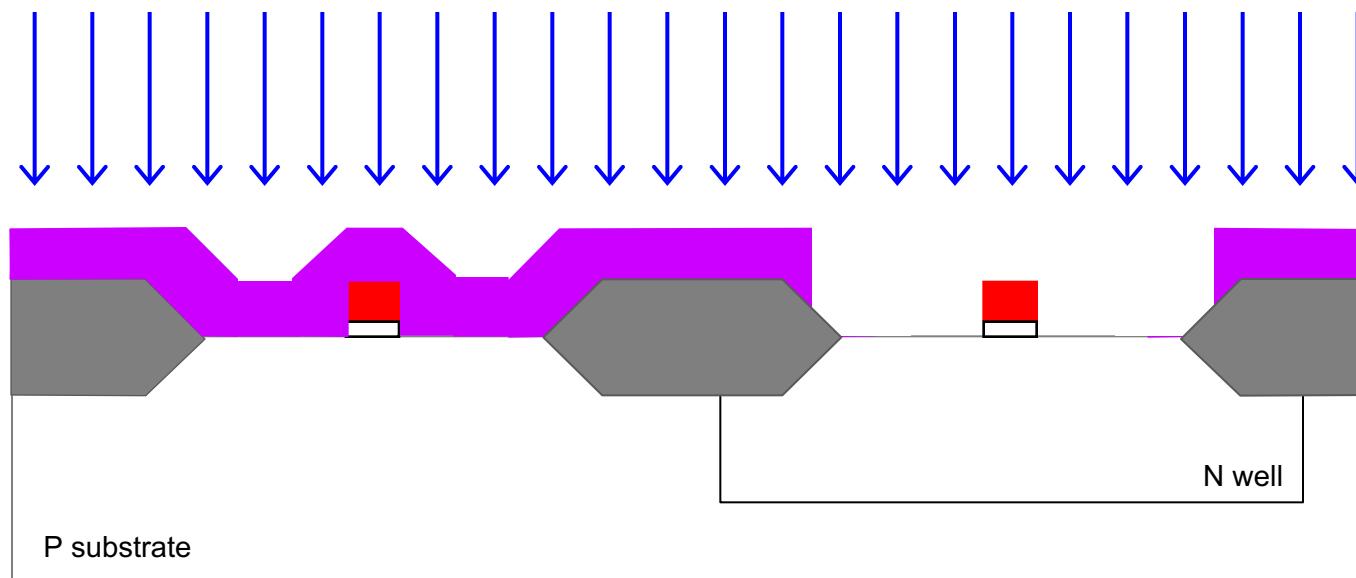
Processo de Fabricação CMOS

PMOS Transistor Drain and Source Creation 3/12

P-type dopants are implanted through ion implantation.

Photoresist serves as coating (implants are shallow).

Ion implantation (P-type dopant)



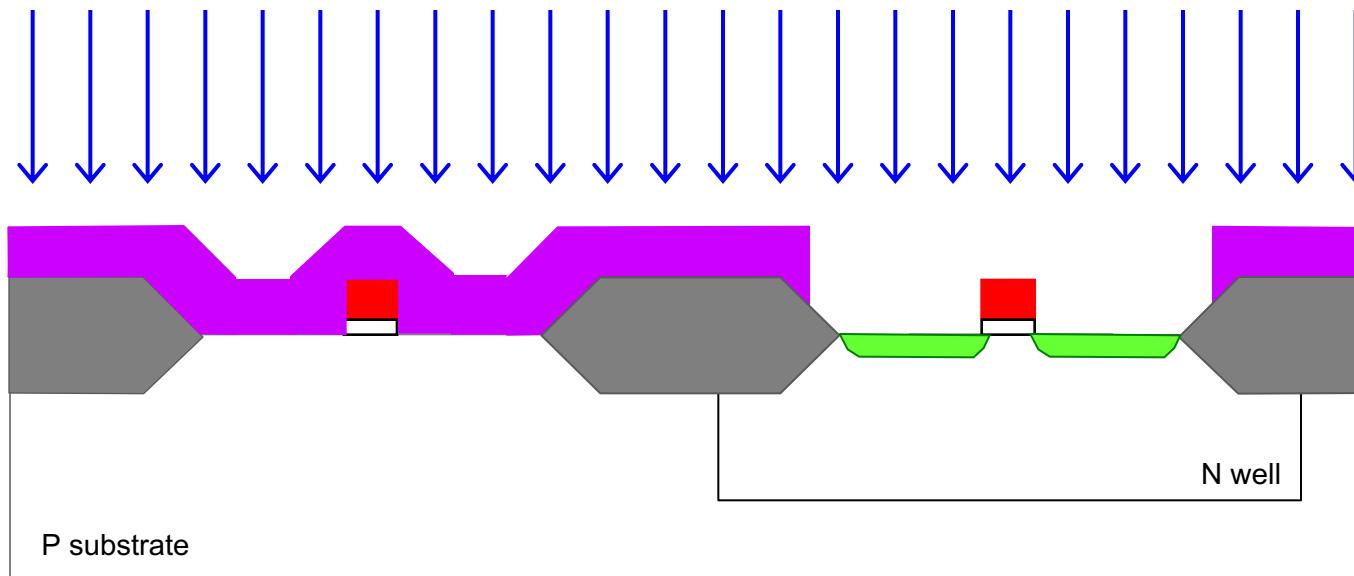
Processo de Fabricação CMOS

PMOS Transistor Drain and Source Creation 4/12

P-type dopants are implanted through ion implantation.

Photoresist serves as coating (implants are shallow).

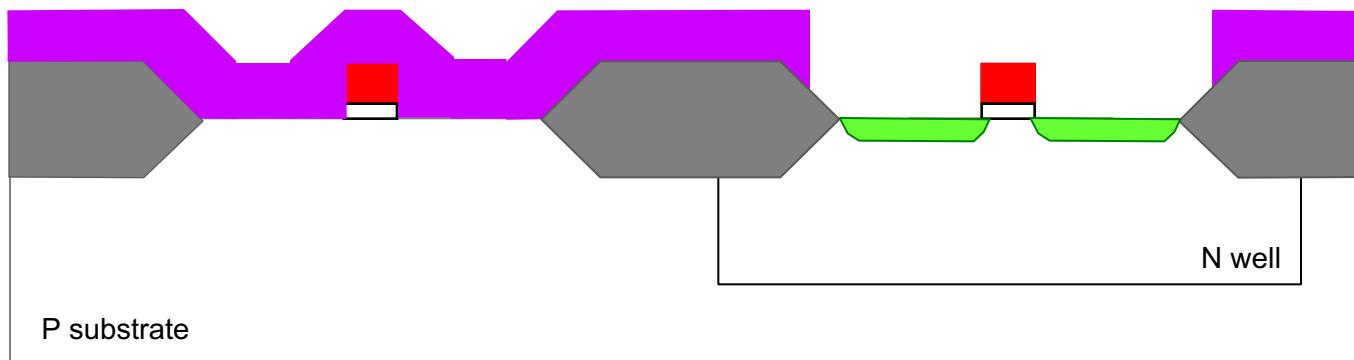
Ion implantation (P-type dopant)



Processo de Fabricação CMOS

PMOS Transistor Drain and Source Creation 5/12

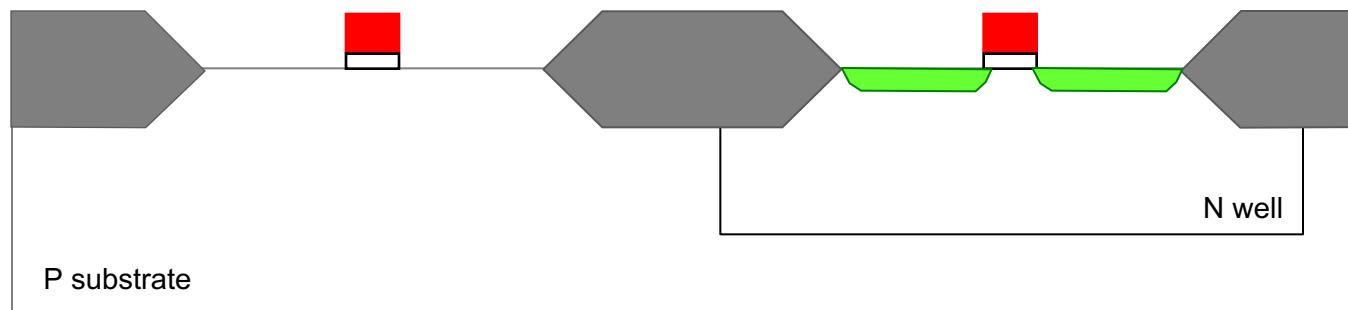
Remaining photoresist is removed with a mixture of acids.



Processo de Fabricação CMOS

PMOS Transistor Drain and Source Creation 6/12

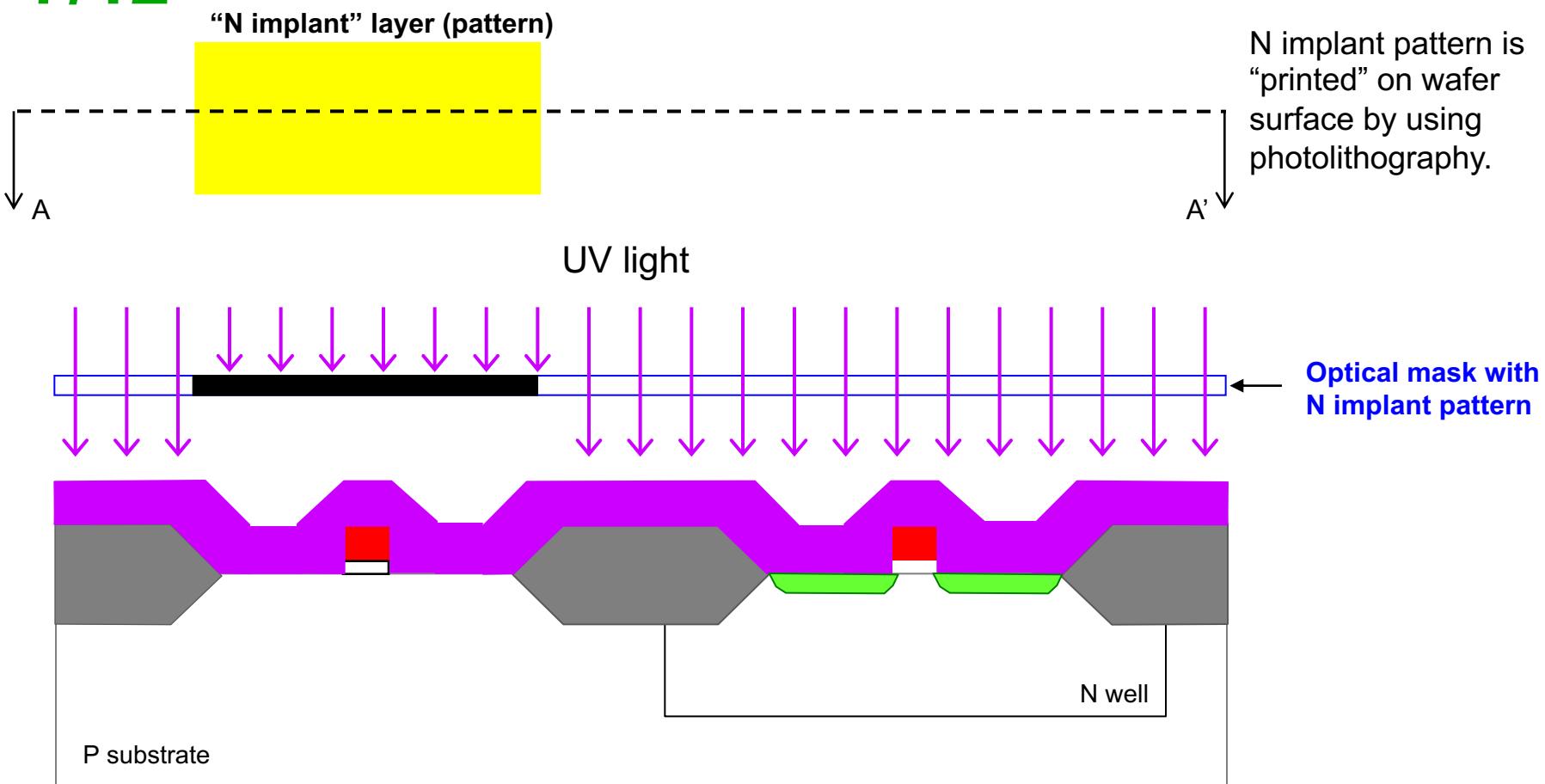
Remaining photoresist is removed with a mixture of acids.



Processo de Fabricação CMOS

NMOS Transistor Drain and Source Creation

7/12

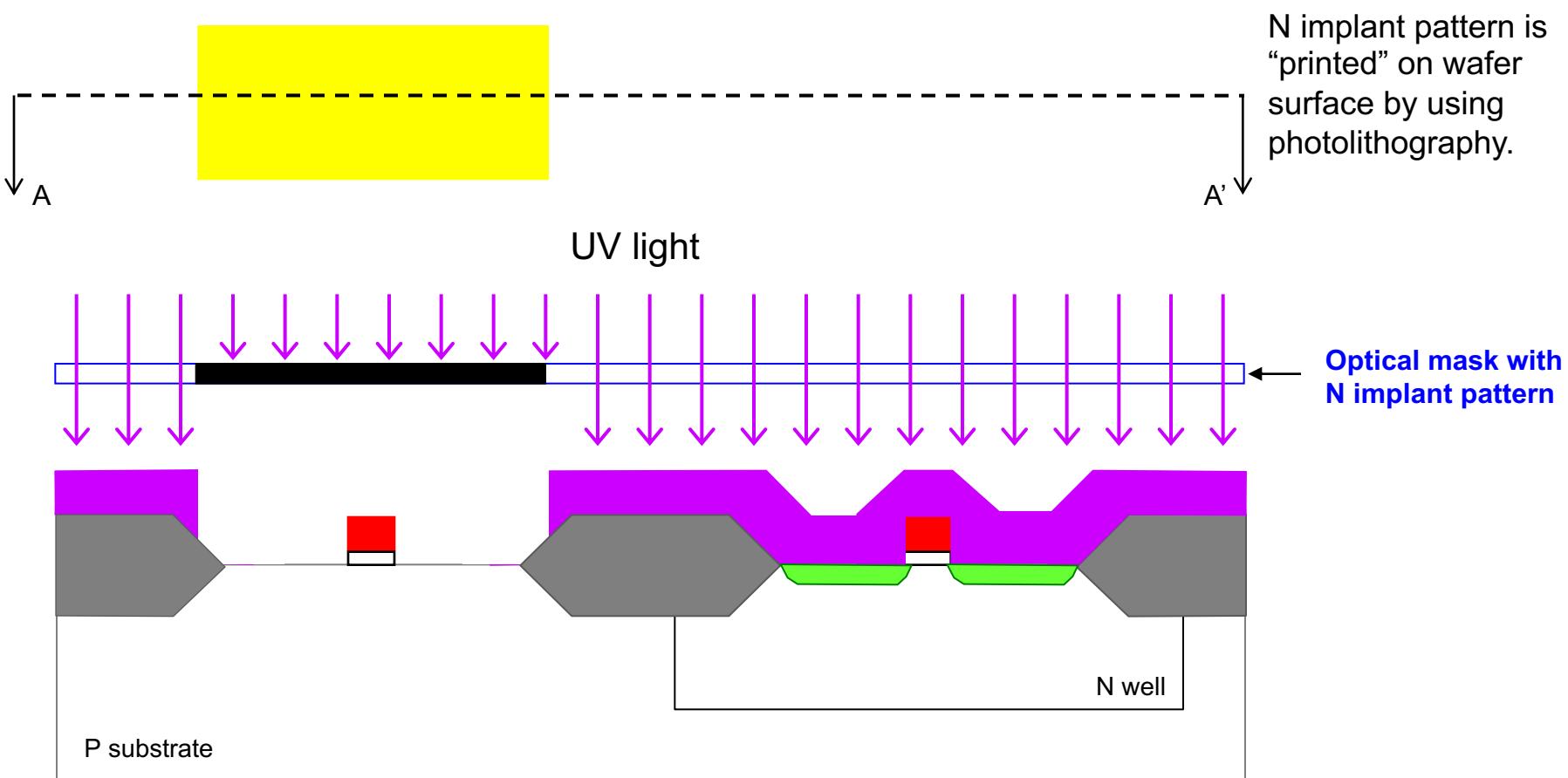


Processo de Fabricação CMOS

NMOS Transistor Drain and Source Creation

8/12

“N implant” layer (pattern)

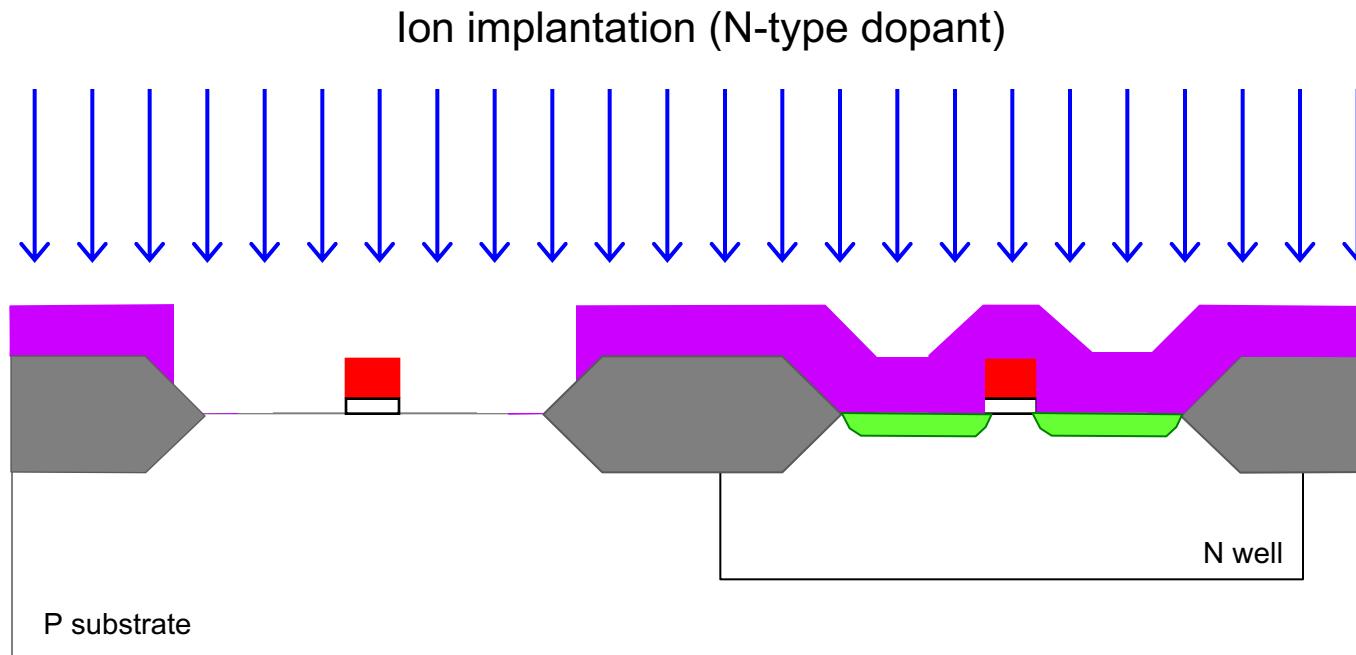


Processo de Fabricação CMOS

NMOS Transistor Drain and Source Creation 9/12

N-type dopants are implanted through ion implantation.

Photoresist serves as coating (implants are shallow).

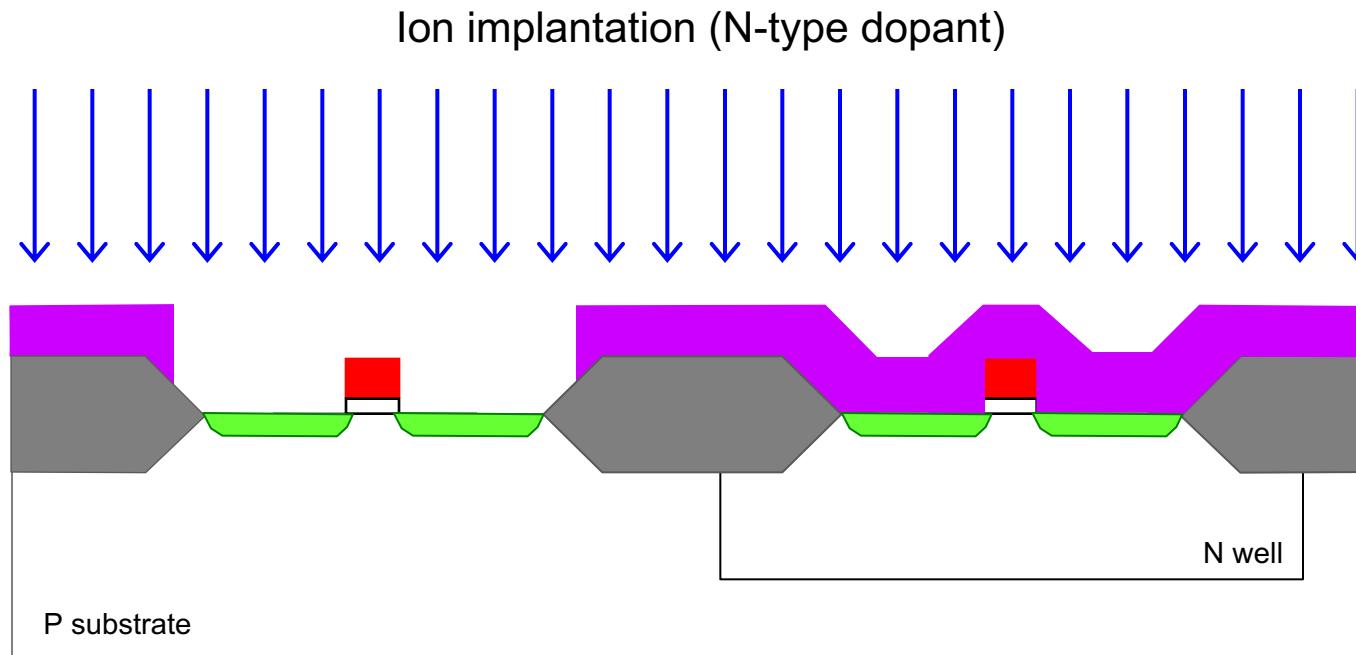


Processo de Fabricação CMOS

NMOS Transistor Drain and Source Creation 10/12

N-type dopants are implanted through ion implantation.

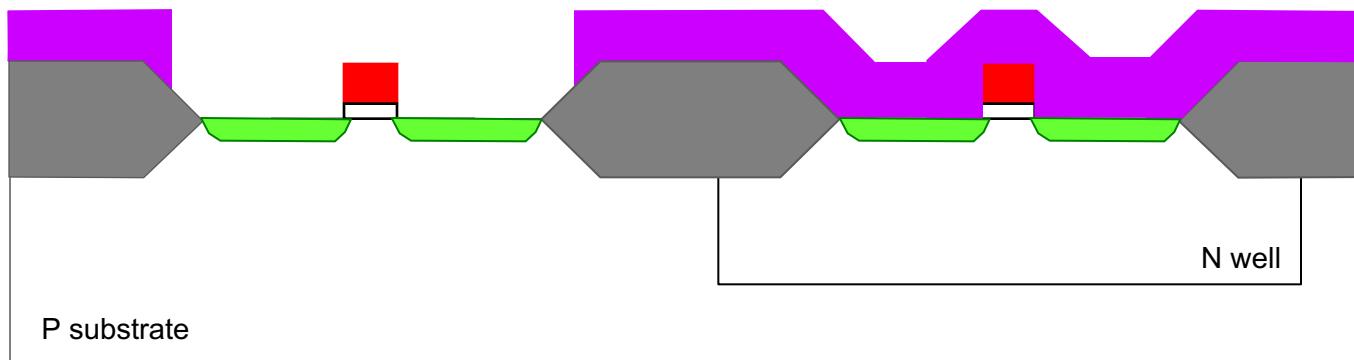
Photoresist serves as coating (implants are shallow).



Processo de Fabricação CMOS

NMOS Transistor Drain and Source Creation 11/12

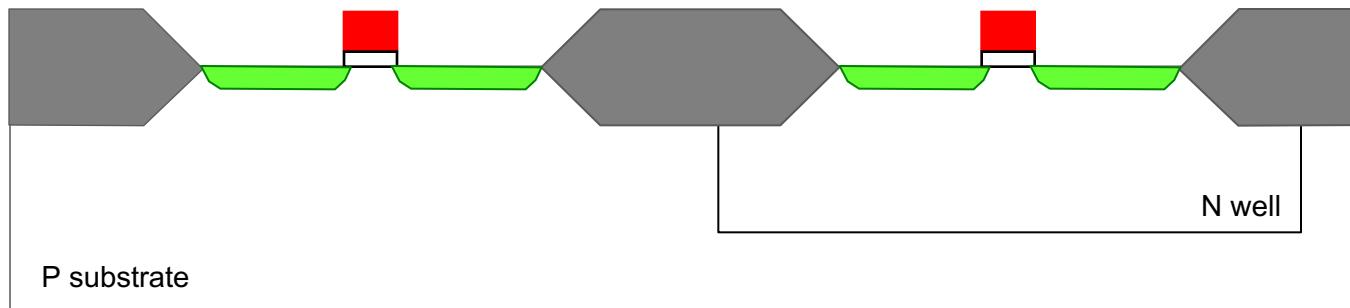
Remaining photoresist is removed with a mixture of acids.



Processo de Fabricação CMOS

NMOS Transistor Drain and Source Creation 12/12

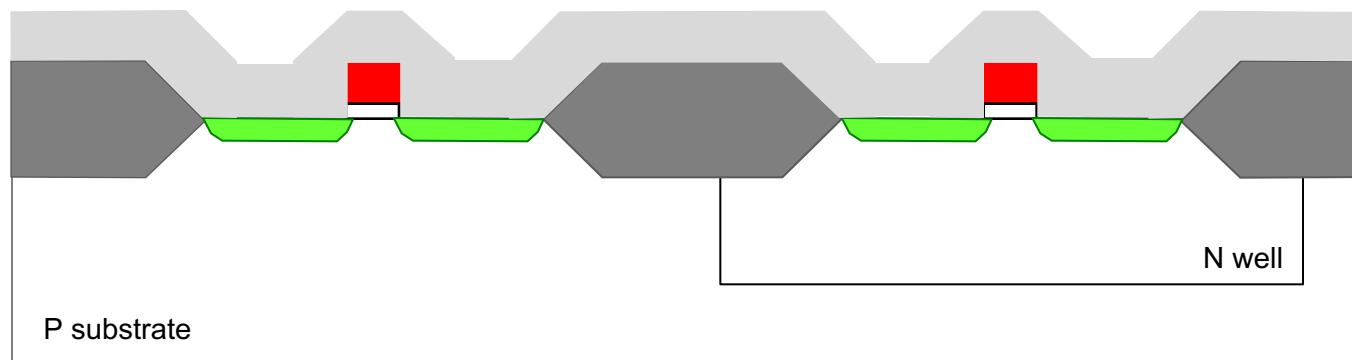
Remaining photoresist is removed with a mixture of acids.



Processo de Fabricação CMOS

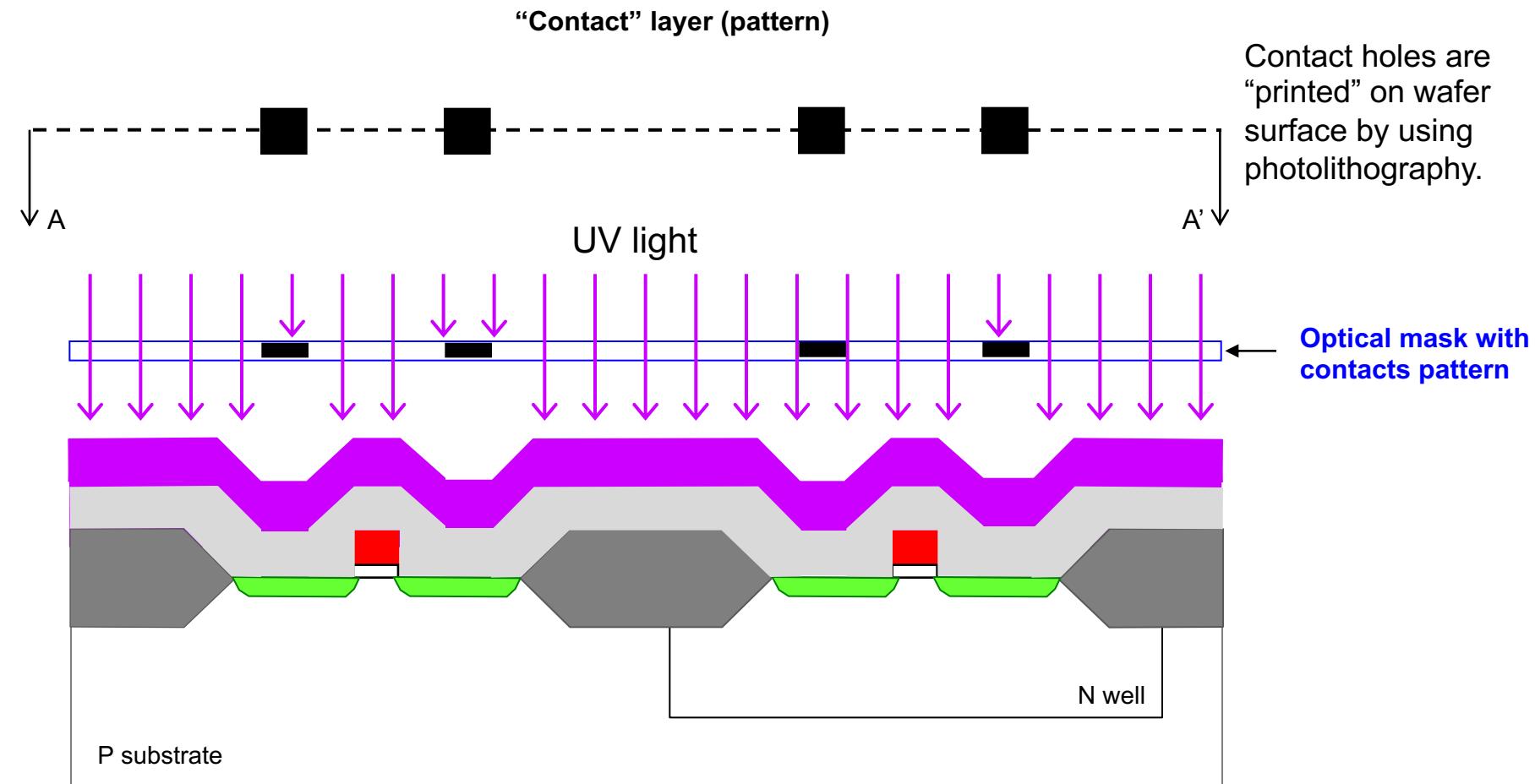
Isolation Oxide Deposition

A thick film of oxide is deposited through CVD.



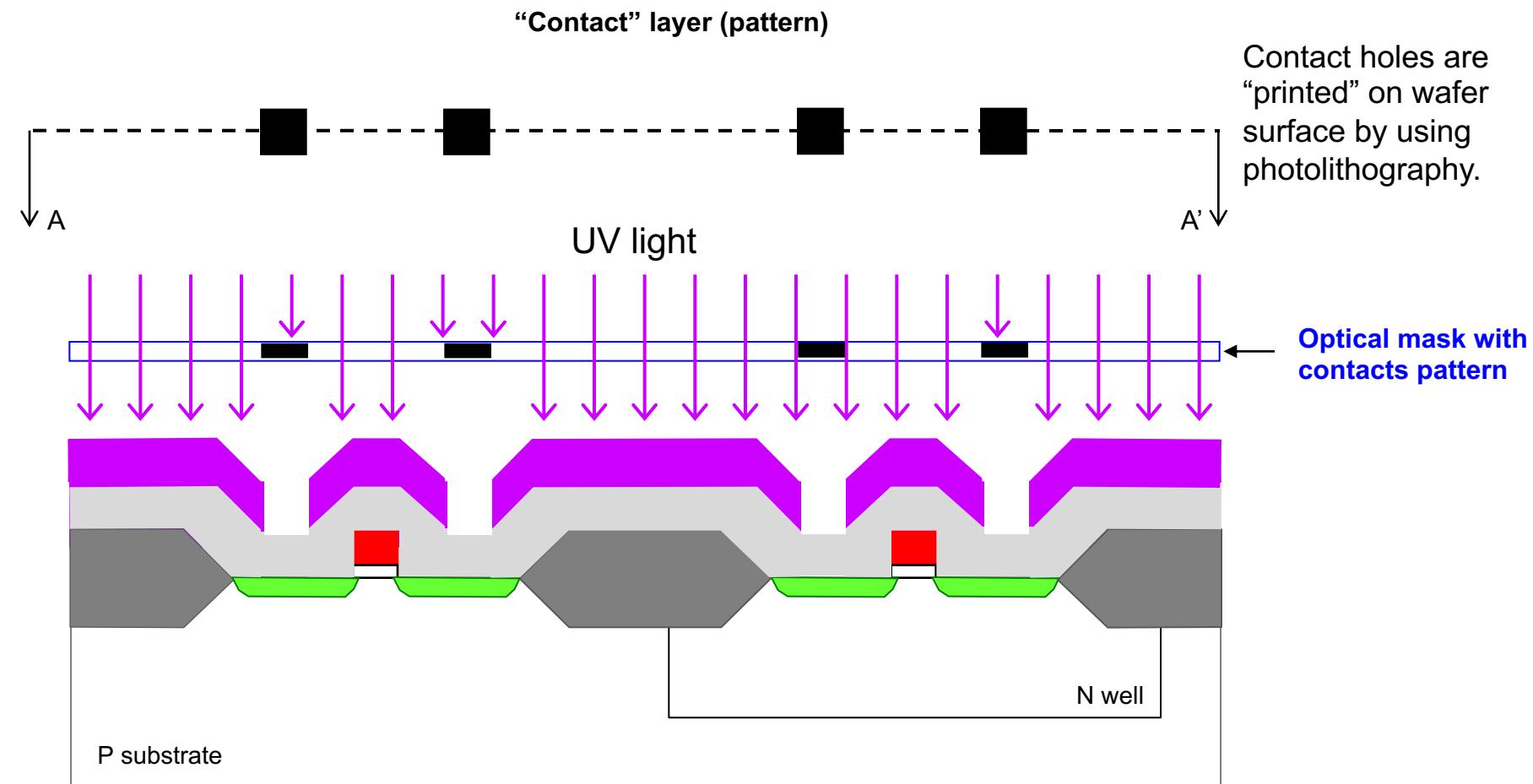
Processo de Fabricação CMOS

Contact Wholes Opening (1/6)



Processo de Fabricação CMOS

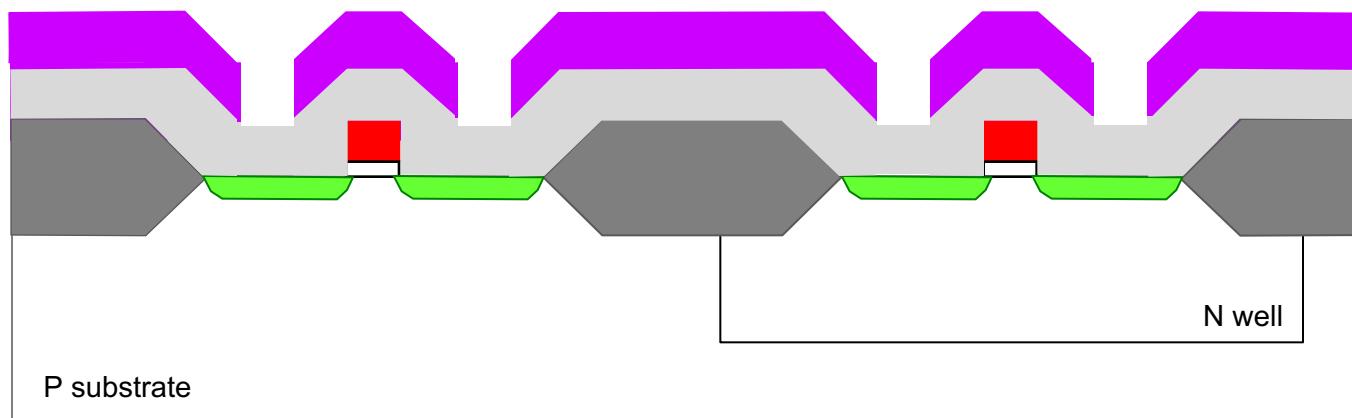
Contact Wholes Opening (2/6)



Processo de Fabricação CMOS

Contact Wholes Opening (3/6)

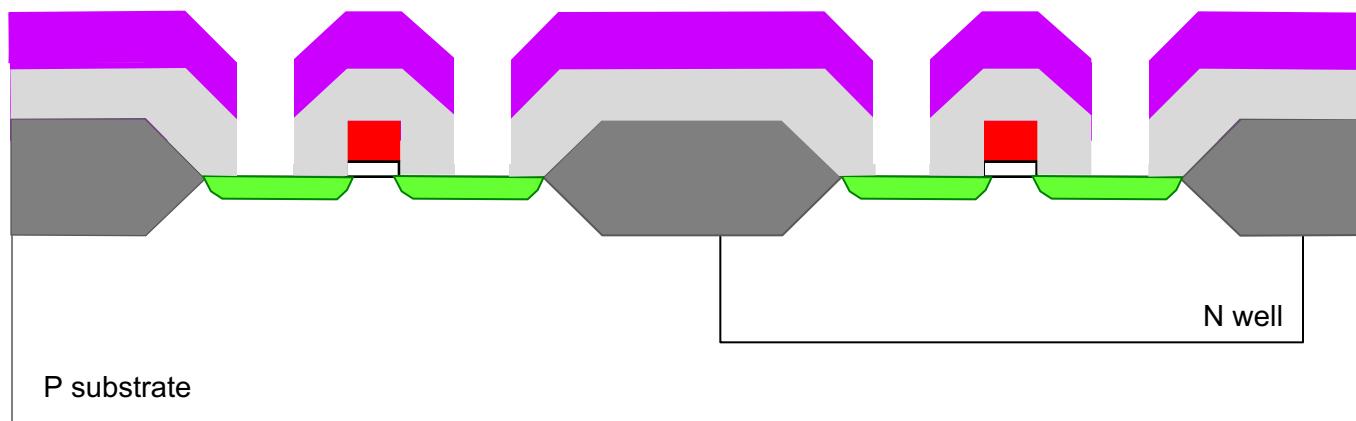
Contact holes are dug on isolation oxide through etching.



Processo de Fabricação CMOS

Contact Wholes Opening (4/6)

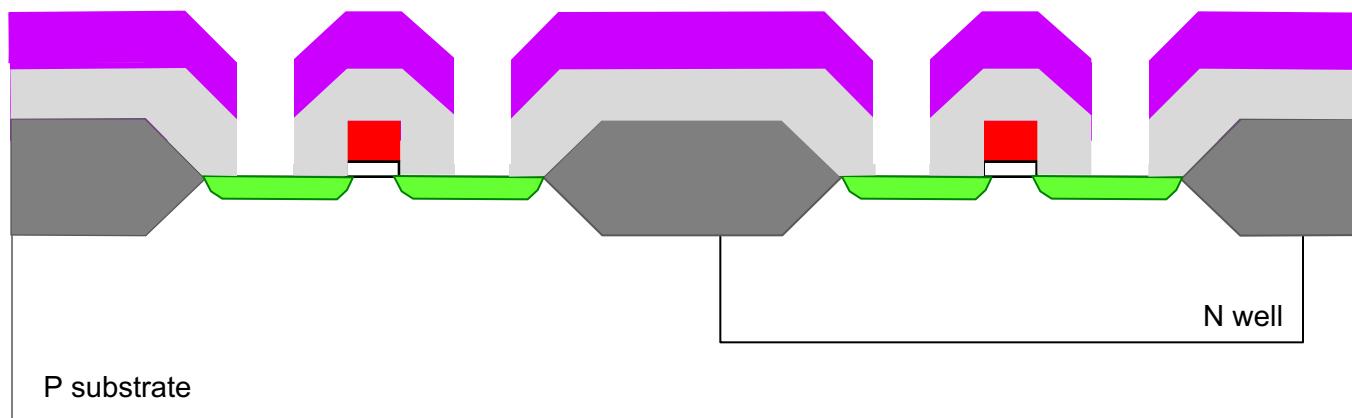
Contact holes are dug on isolation oxide through etching.



Processo de Fabricação CMOS

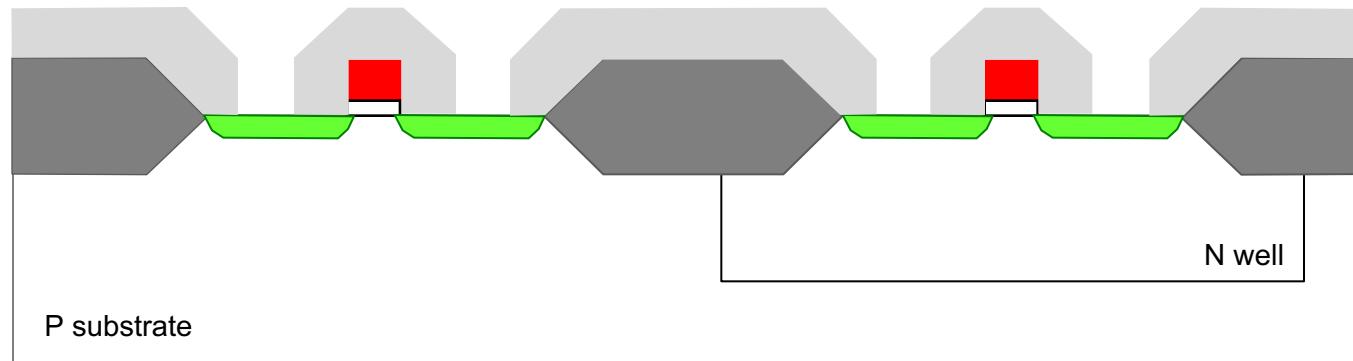
Contact Wholes Opening (5/6)

Remaining photoresist is removed.



Processo de Fabricação CMOS

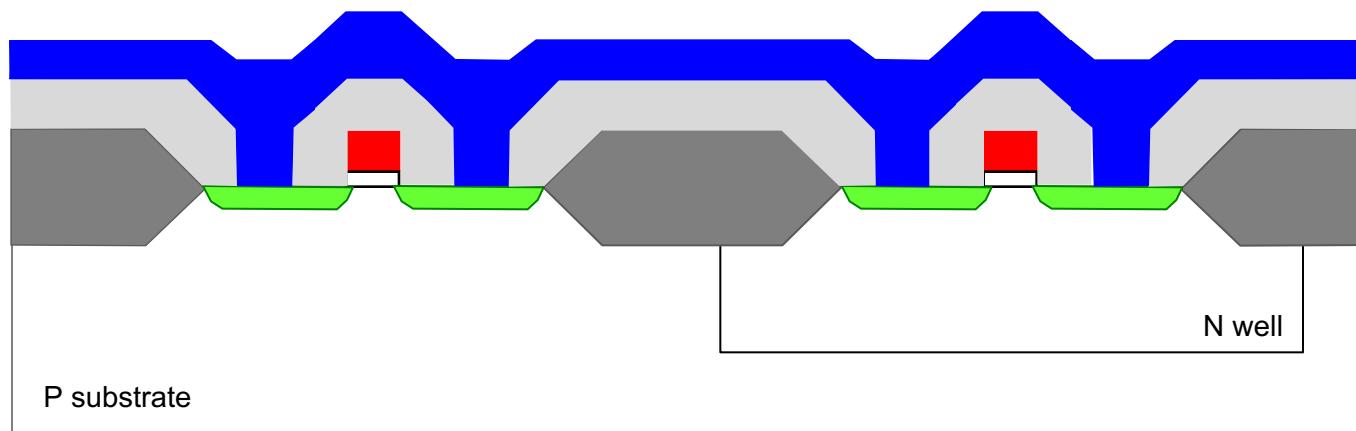
Contact Wholes Opening (6/6)



Processo de Fabricação CMOS

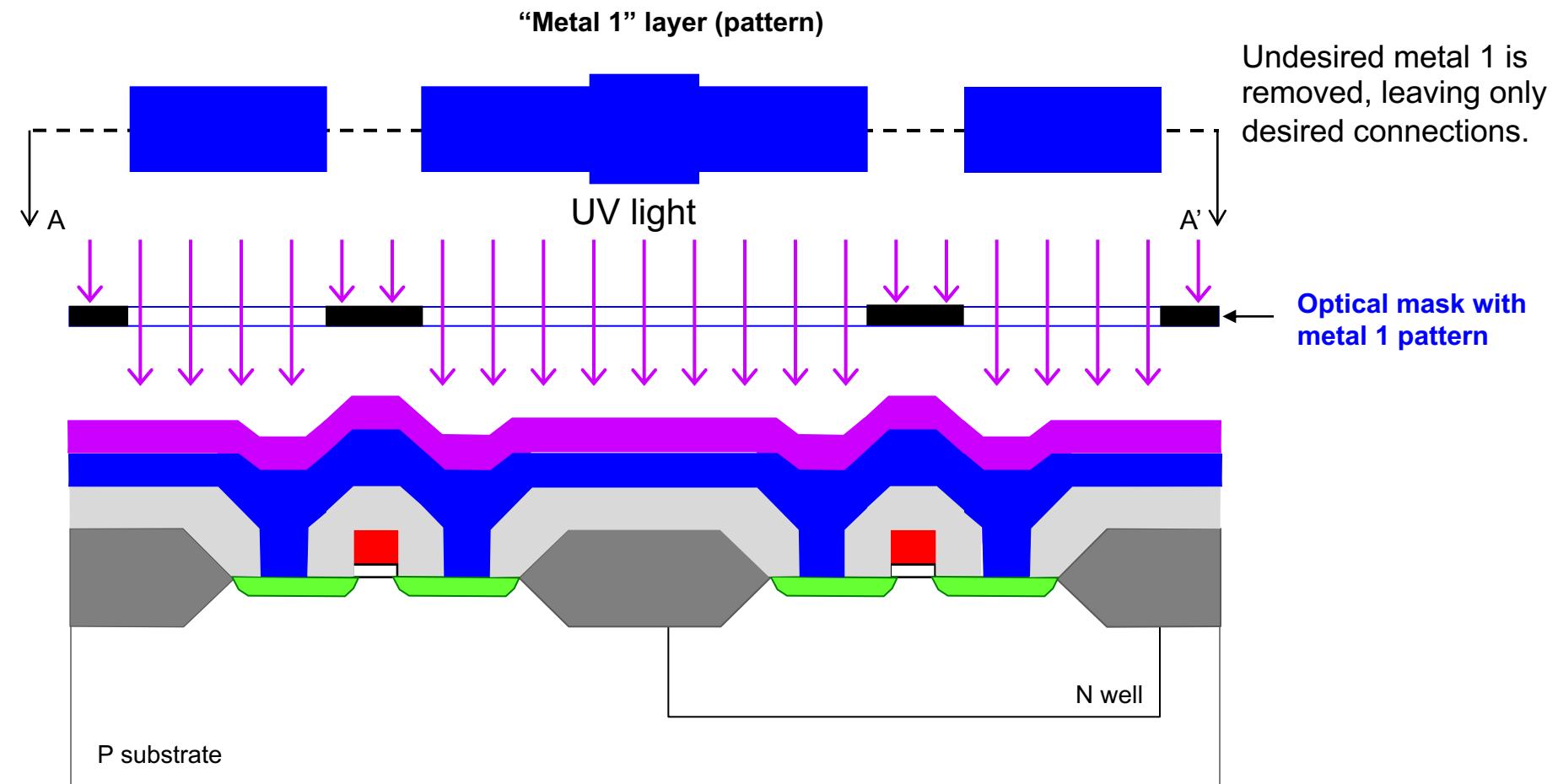
Metal 1 Deposition (1/6)

Metal 1 is deposited through sputtering.



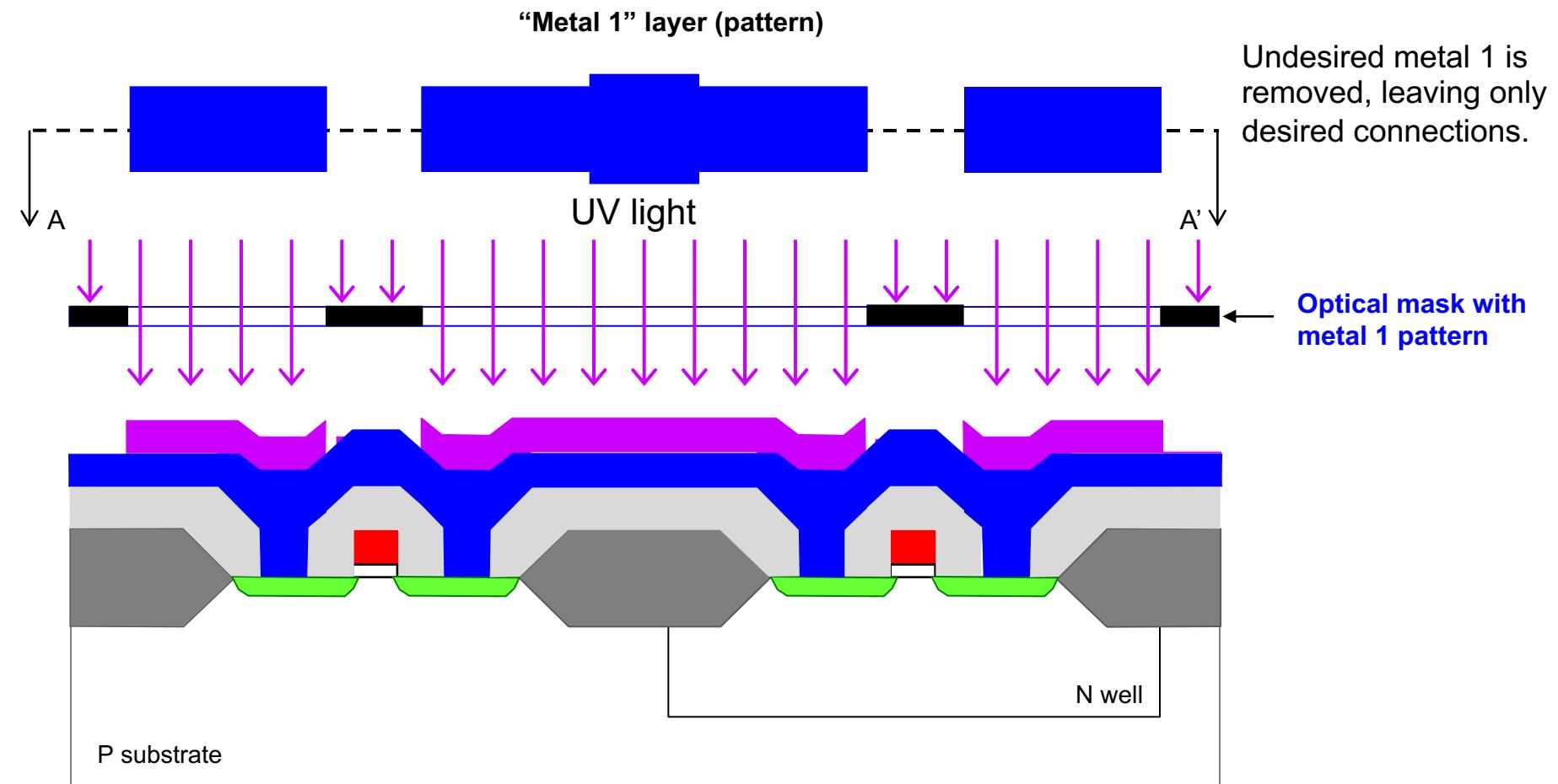
Processo de Fabricação CMOS

Metal 1 Deposition (2/6)



Processo de Fabricação CMOS

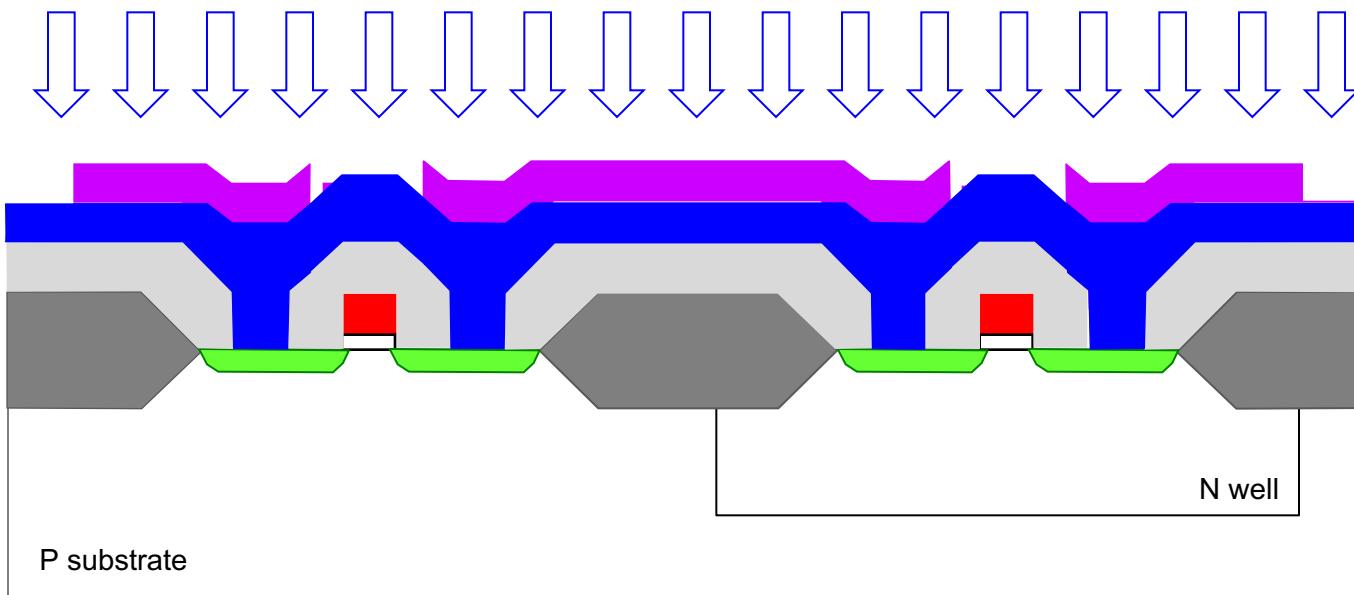
Metal 1 Deposition (3/6)



Processo de Fabricação CMOS

Metal 1 Deposition (4/6)

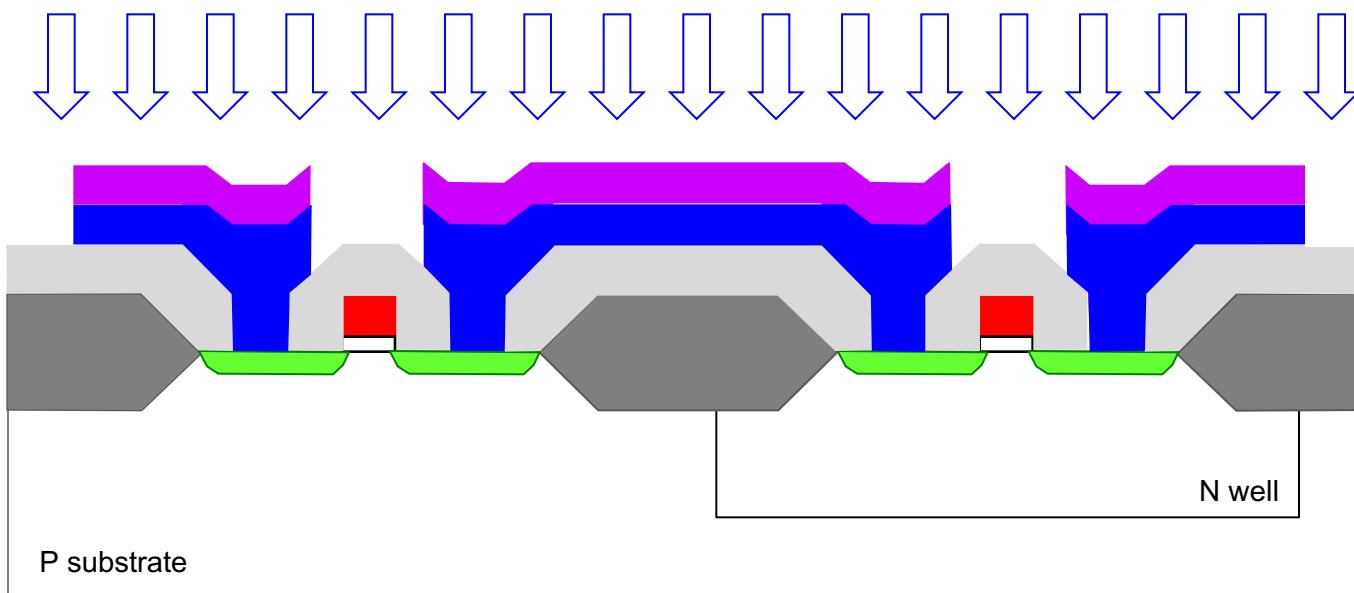
Undesired metal 1 is removed through etching.



Processo de Fabricação CMOS

Metal 1 Deposition (5/6)

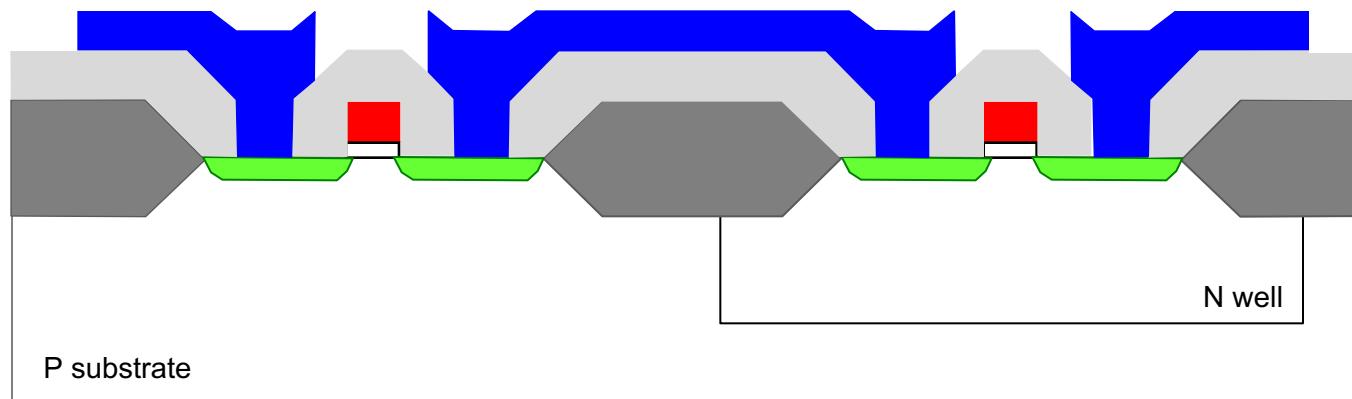
Undesired metal 1 is removed through etching.



Processo de Fabricação CMOS

Metal 1 Deposition (6/6)

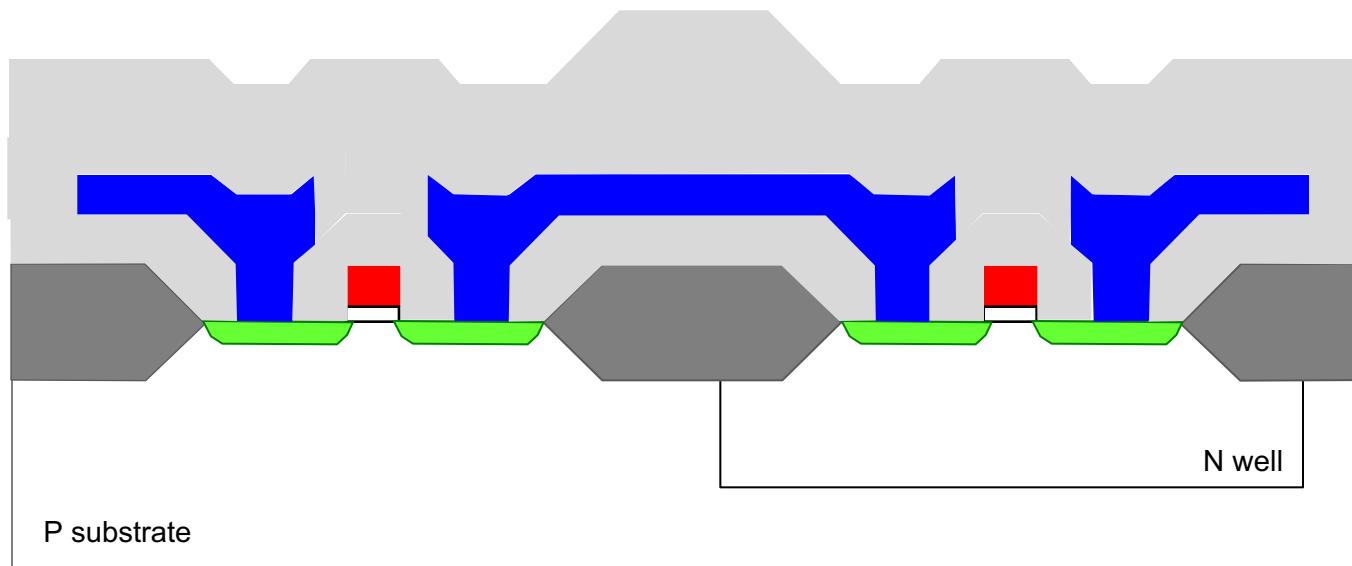
Photoresist is removed.



Processo de Fabricação CMOS

Isolation Oxide Deposition

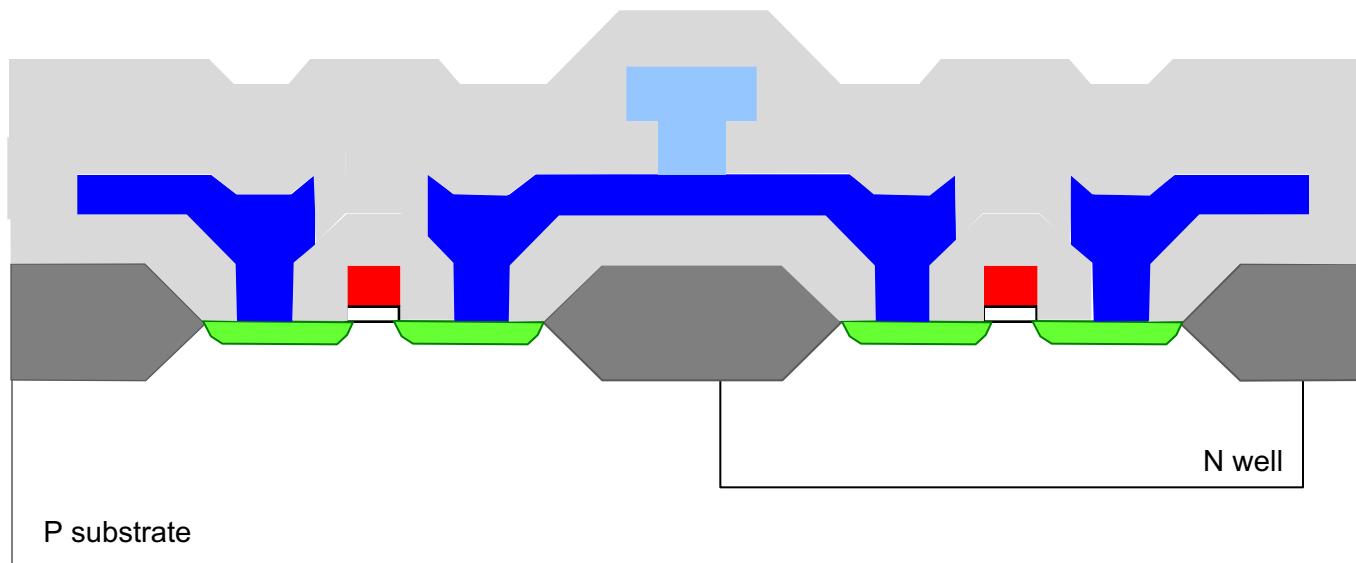
Another thick film of oxide is deposited through CVD to isolate metal 1 from metal 2.



Processo de Fabricação CMOS

Metal 2 Deposition

Similarly to metal 1 deposition.

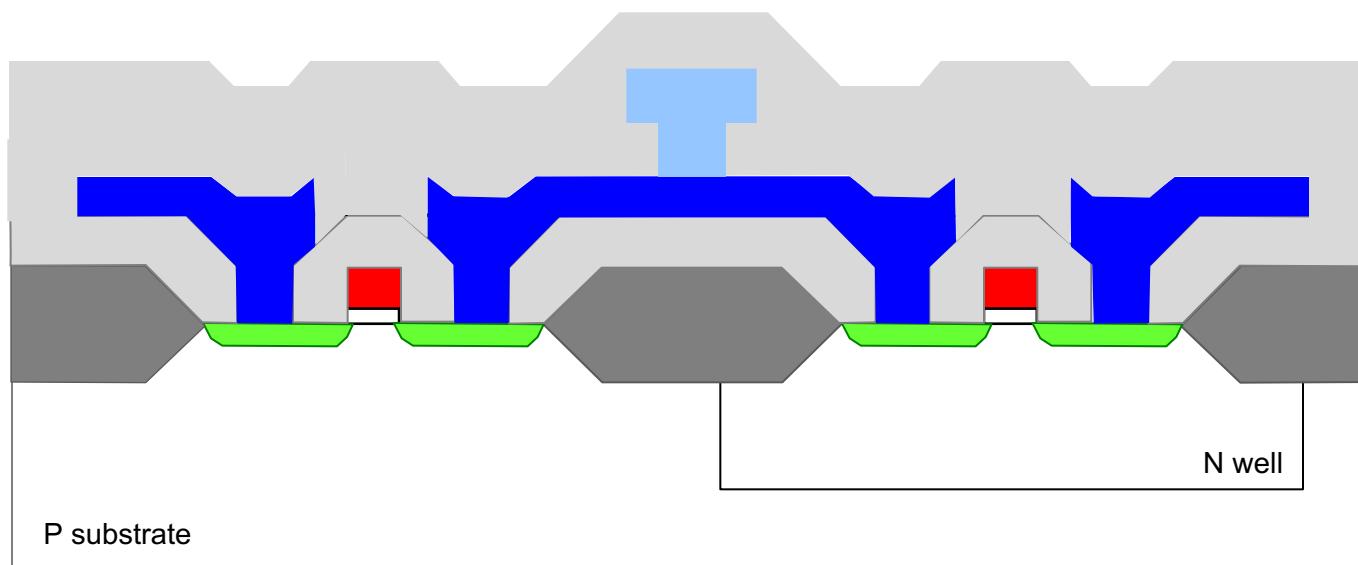
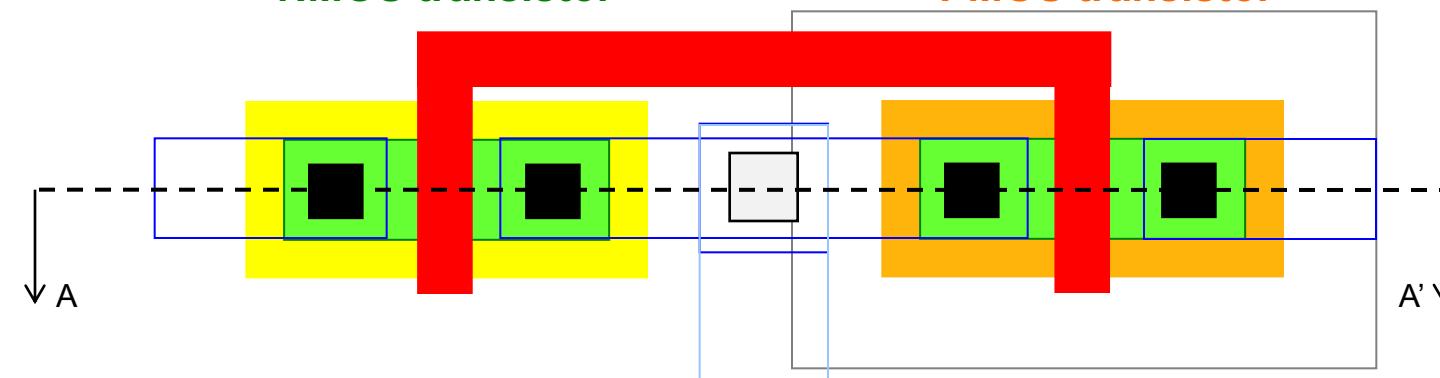


Processo de Fabricação CMOS

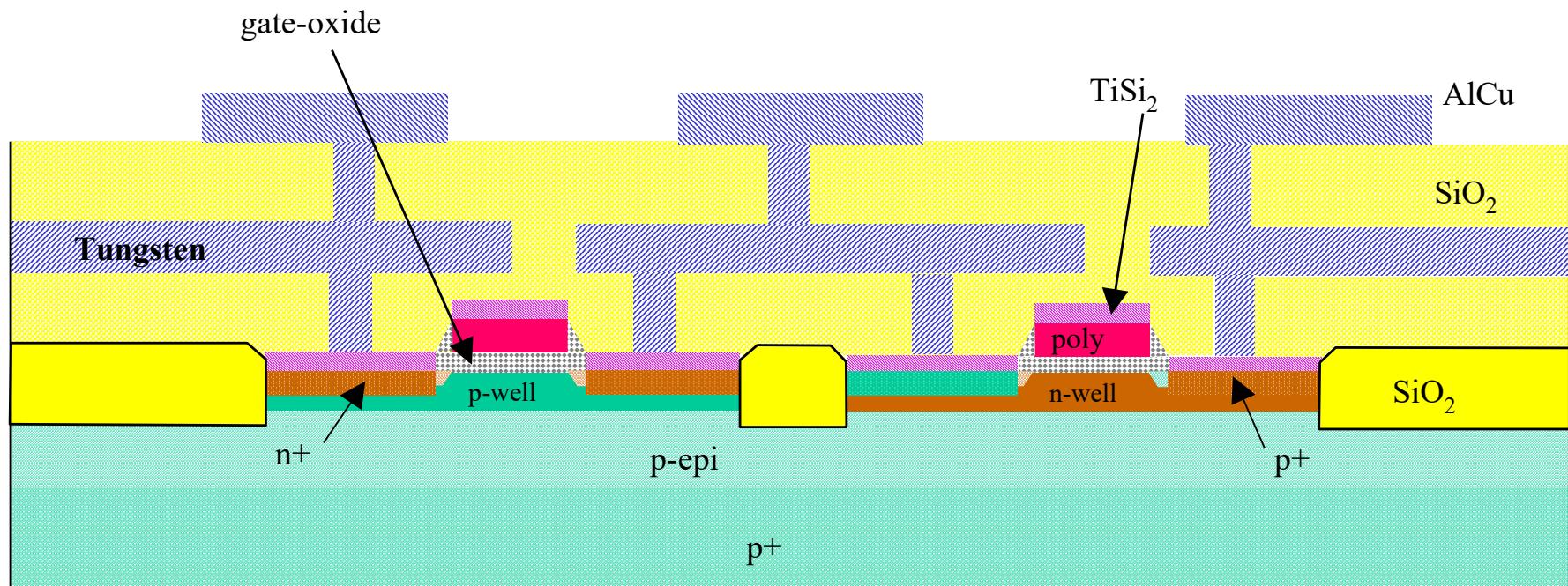
Layout vs. AA' Cross on Fabricated Structure

NMOS transistor

PMOS transistor



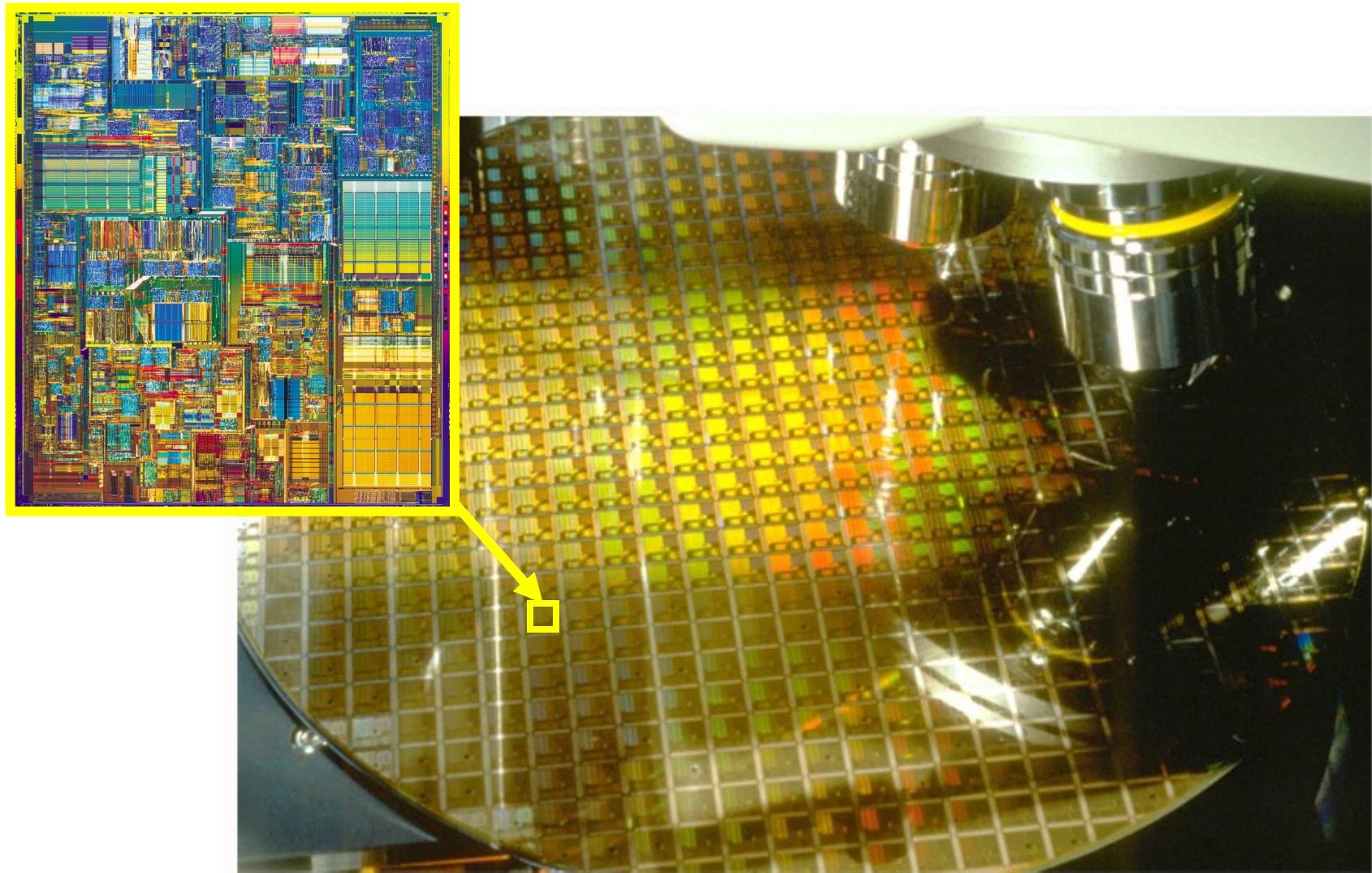
A Modern CMOS Process



Dual-Well Trench-Isolated CMOS Process

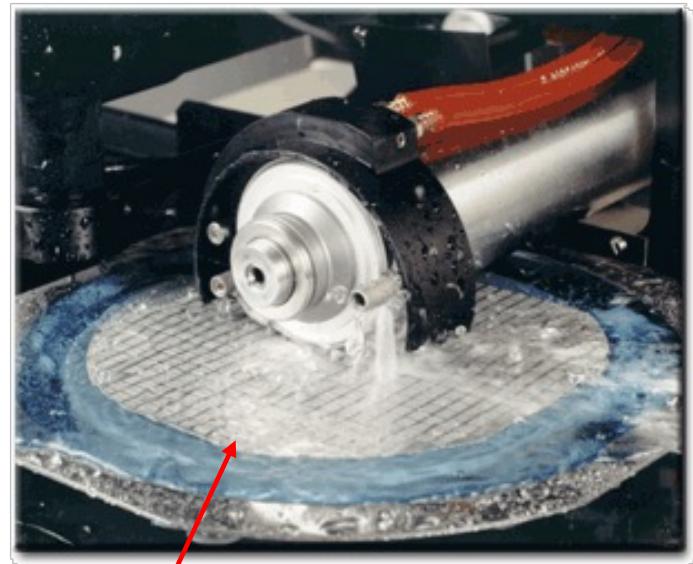
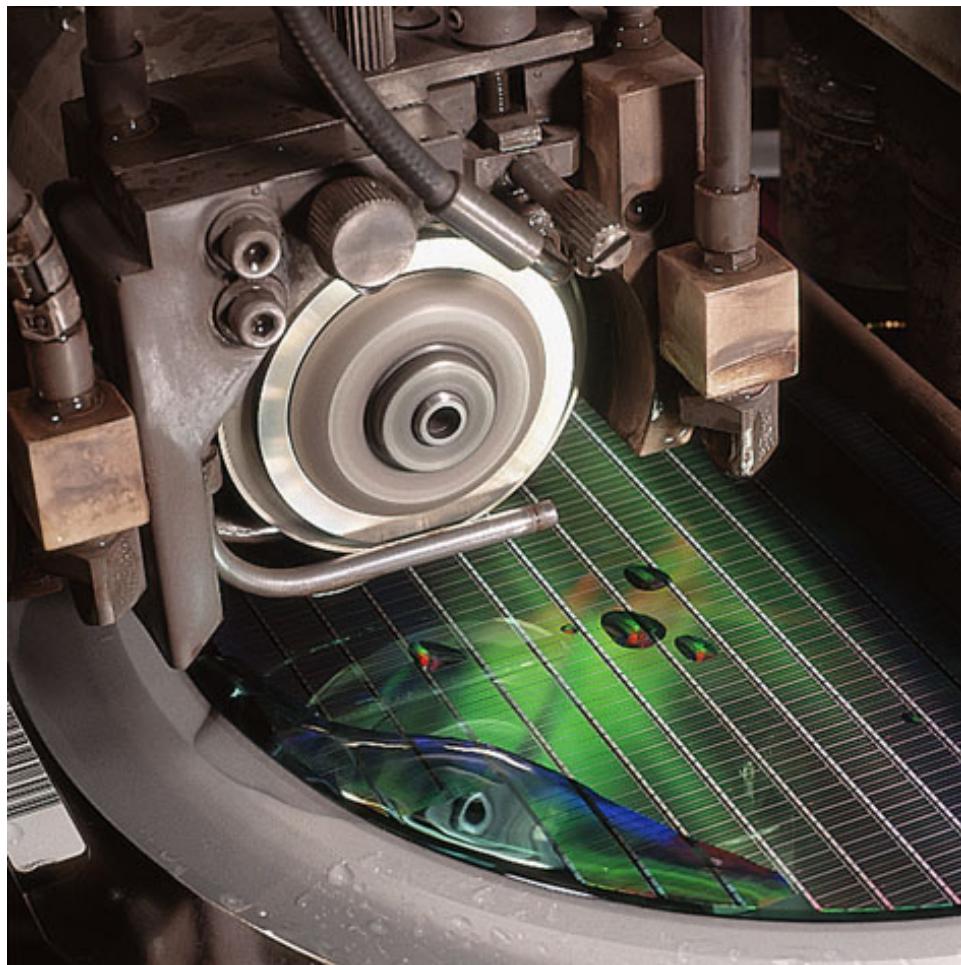
Processo de Fabricação CMOS

Final Result



Processo de Fabricação CMOS

Corte dos wafers



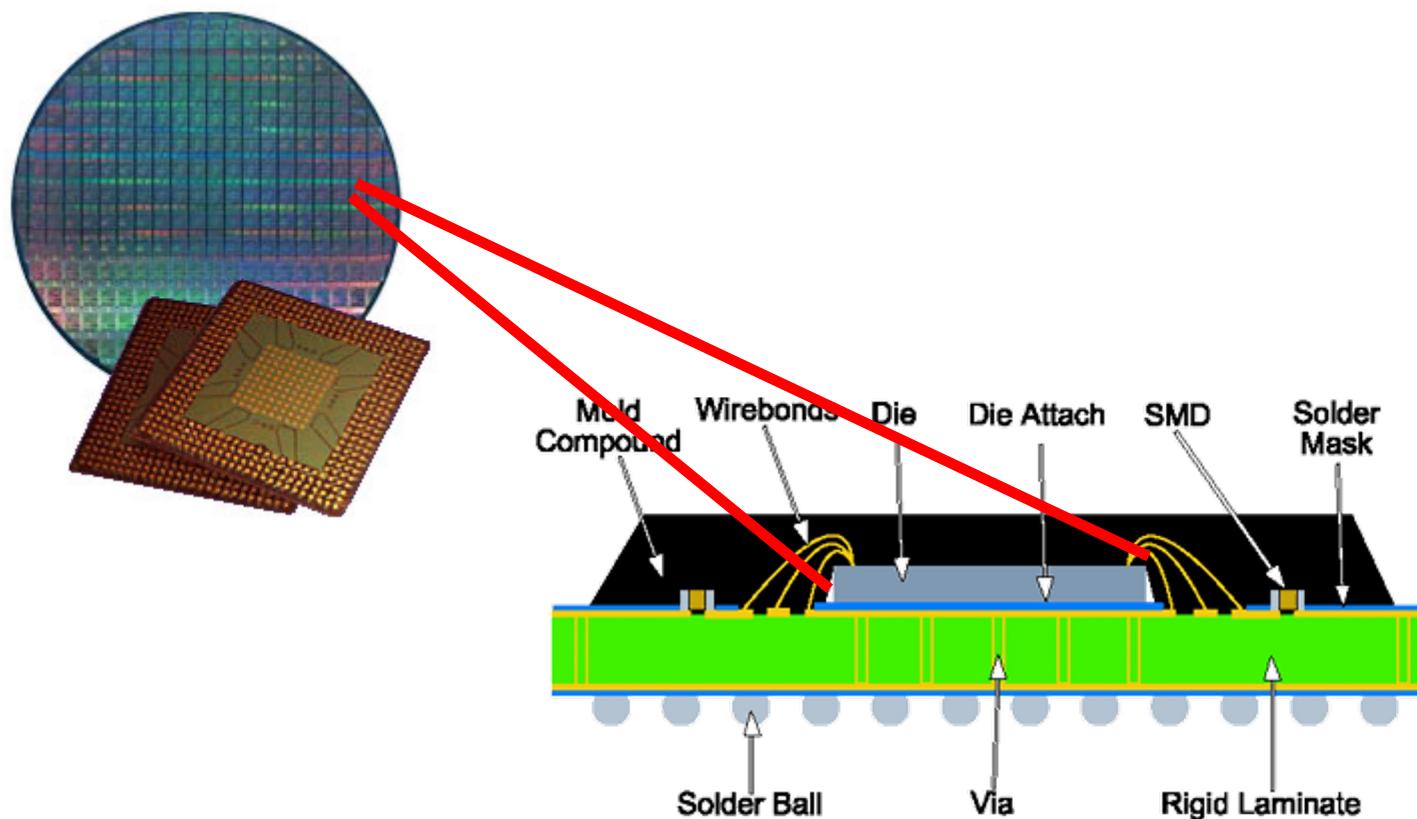
Die

Teste Final



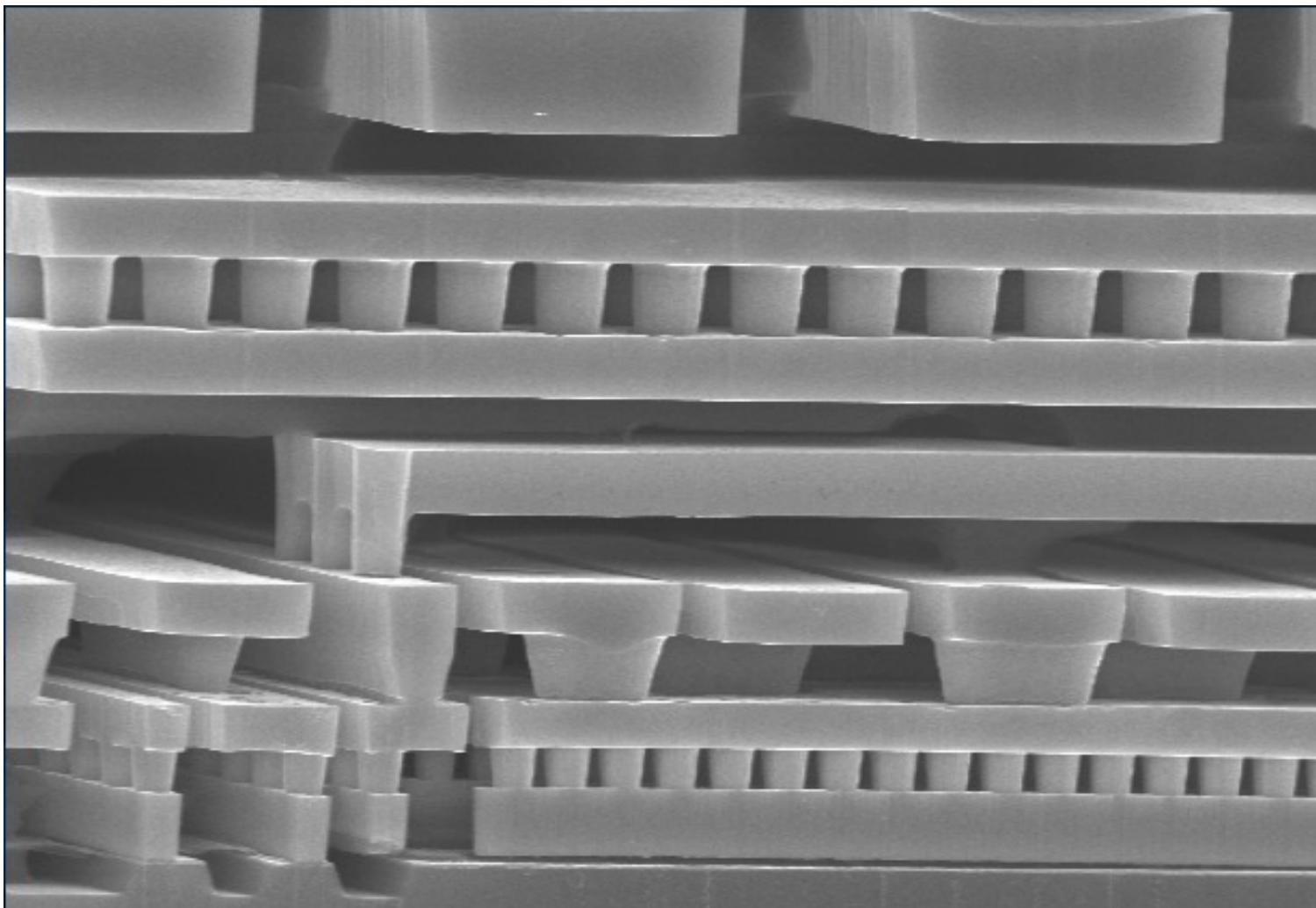
Agilent Versatest
V5500 test cell

Encapsulamento

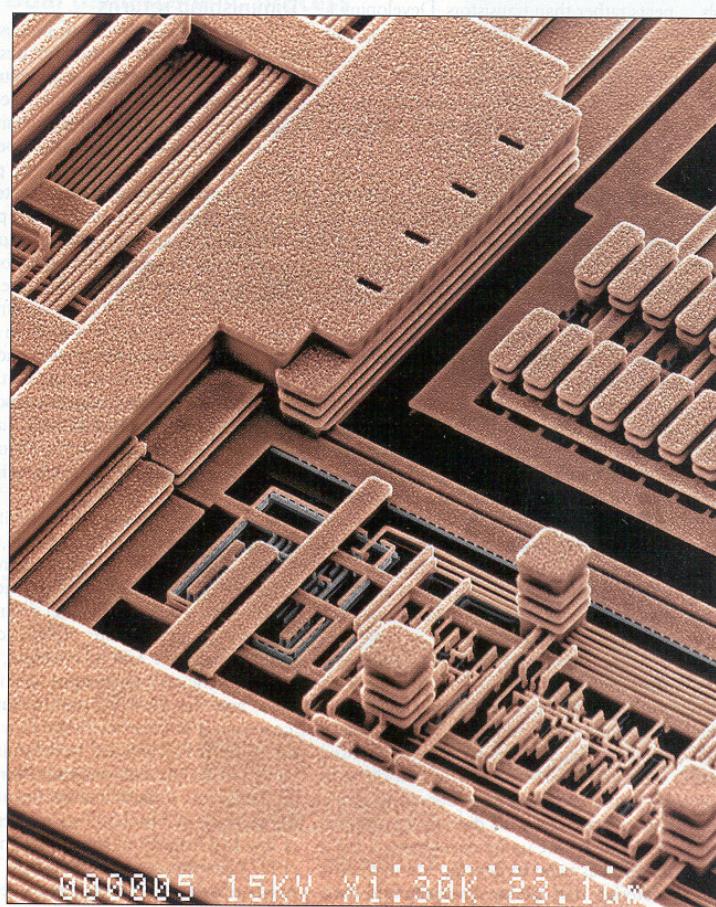


SiP-PBGA Cross Section

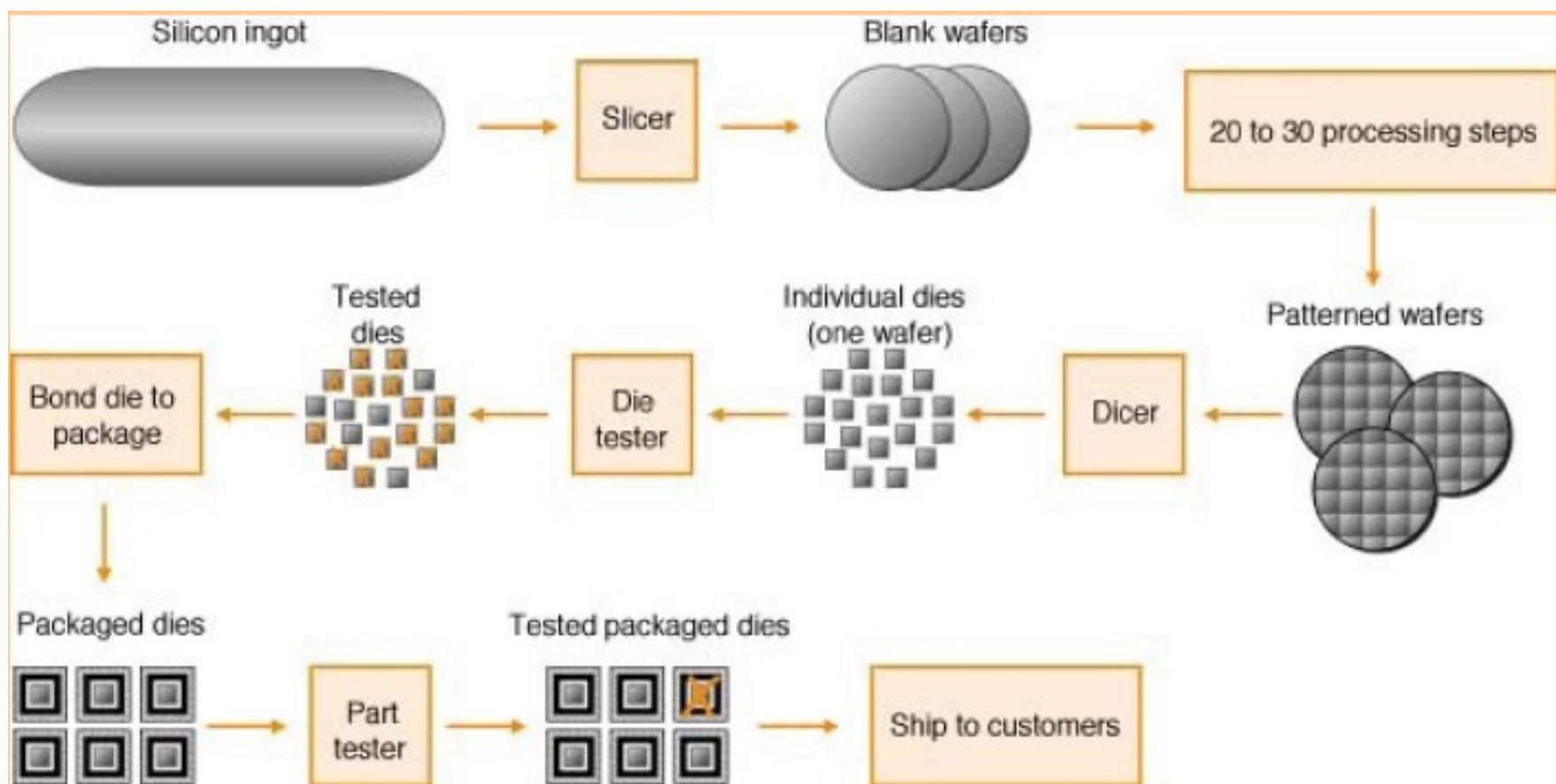
Camadas de metal



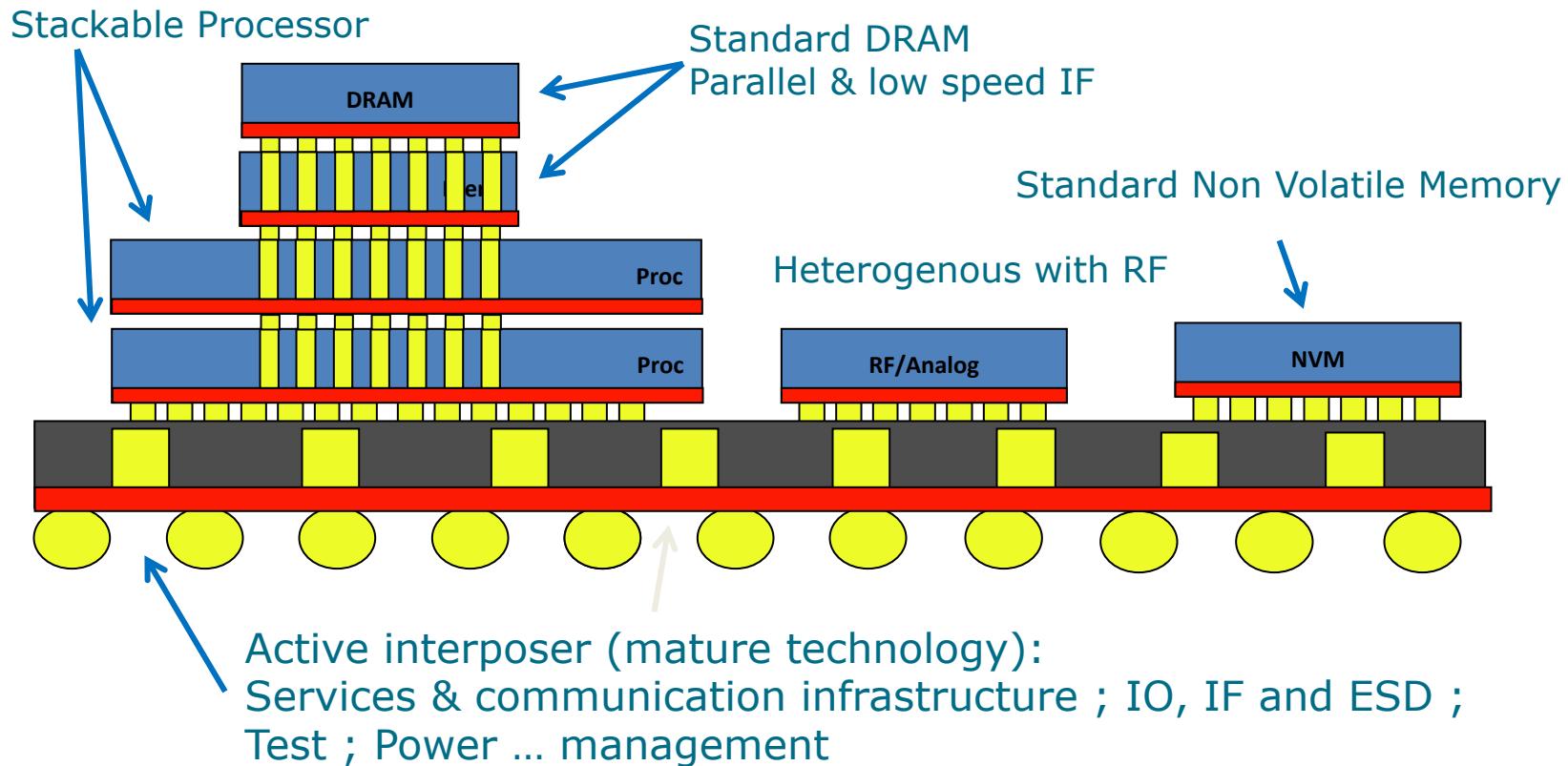
Advanced Metallization



Fluxo de Fabricação - Resumo



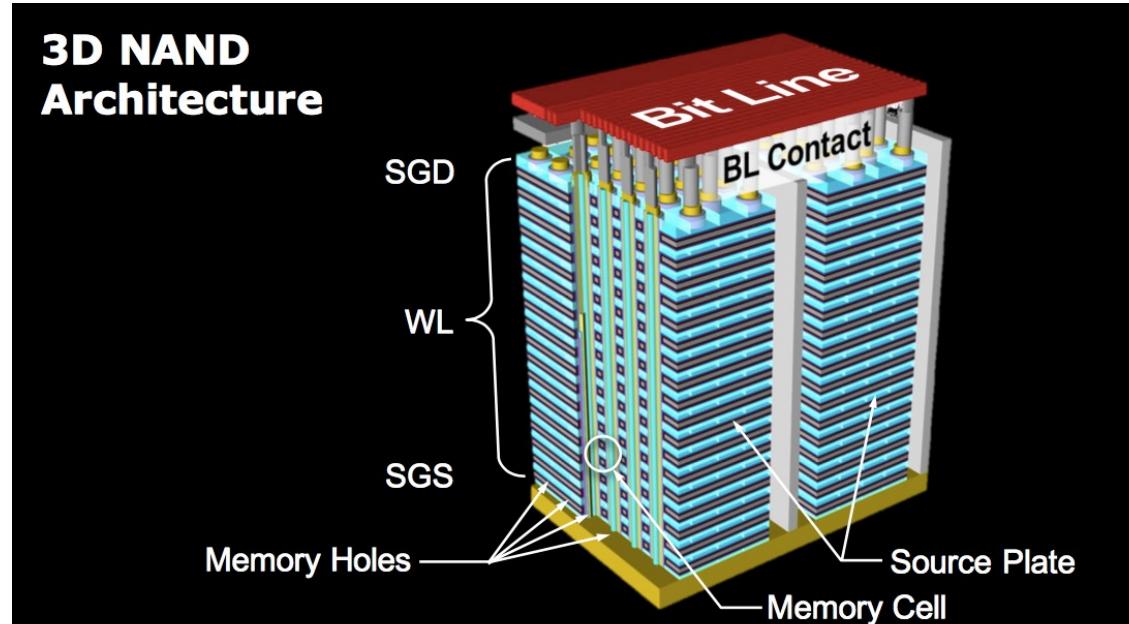
3D Design



3D NAND architecture

3D NAND is quantified by the number of layers stacked in a device. As more layers are added, the bit density increases. Today, 3D NAND suppliers are shipping 64-layer devices, although they are now ramping up the next technology generation, which has 96 layers. And behind the scenes vendors are racing to develop and ship the next iteration, 128-layer products, by mid-2019, analysts said.

<https://semiengineering.com/3d-nand-flash-wars-begin/>

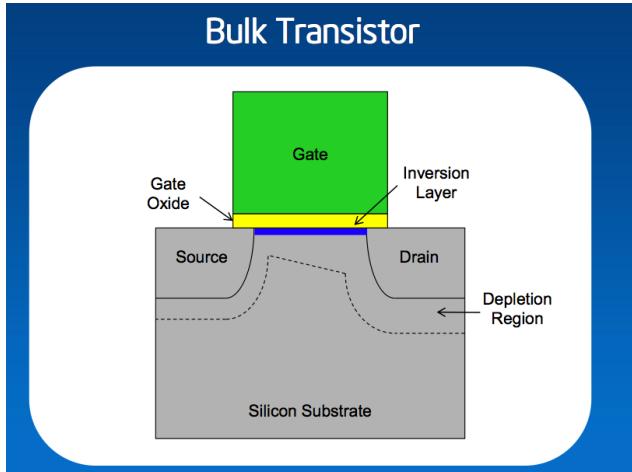


Year	2016-2017	2018-2019		2020-2021	2022-2023
Generation 3D	L48	L64	L96	L128	512
Die size (3b/cell)	256-512 Gb	512Gb – 1Tb	512Gb-2Tb	1-3Tb	2-6 Tb
Hole CD	65-100	65-100	65-100	65-100	65-100
Slit pitch (# holes)	4	4	4-8	8	8
Vertical pitch	50-70nm	40-60	40-60	40-50	40-50
BL CD	20	20	20 - 40	~40	~40
Multiple stacks	No	No	No	No	Yes (2-4)
					Yes (4-8)

Novos processos de fabricação

Até +- 32 nm

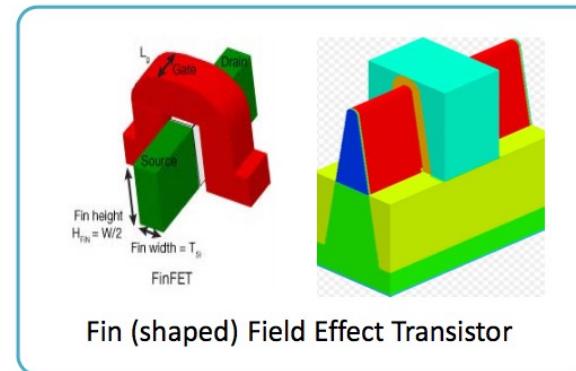
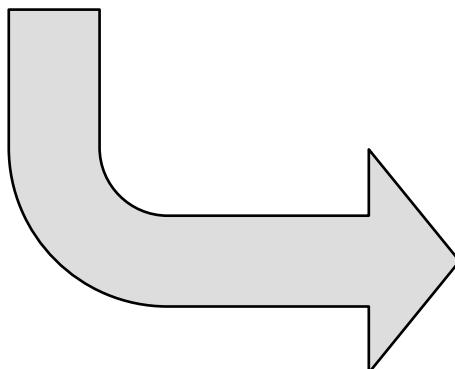
http://maltiel-consulting.com/Intel_22nm_3D_Tri-Gate_FinFETs_Transistors_maltiel_semiconductor_consulting.html



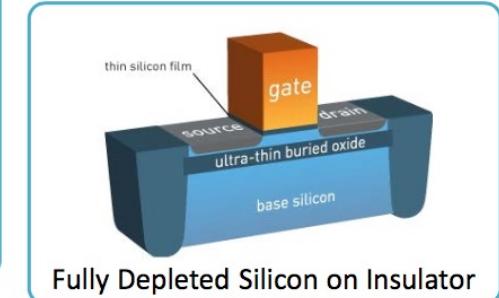
Possible Solutions

FinFET

FD-SOI



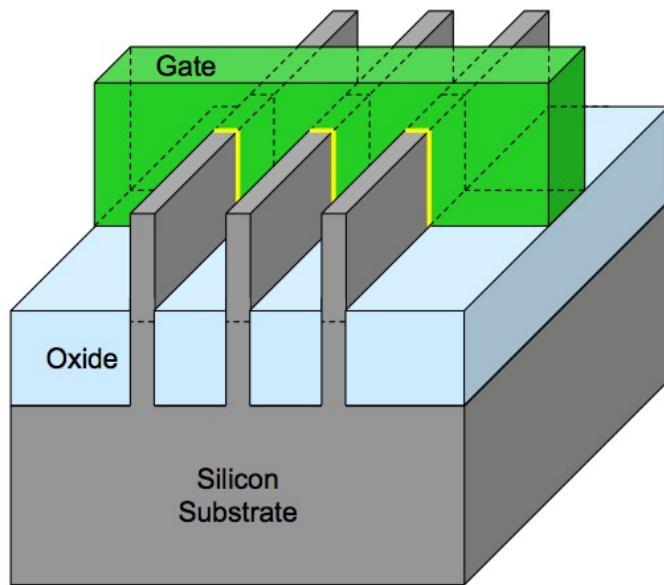
Fin (shaped) Field Effect Transistor



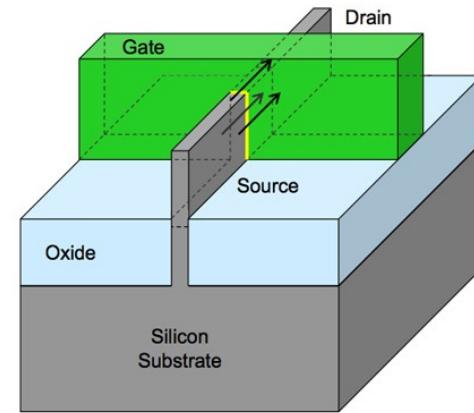
Fully Depleted Silicon on Insulator

FinFET - Intel 3D Tri-Gate Transistor

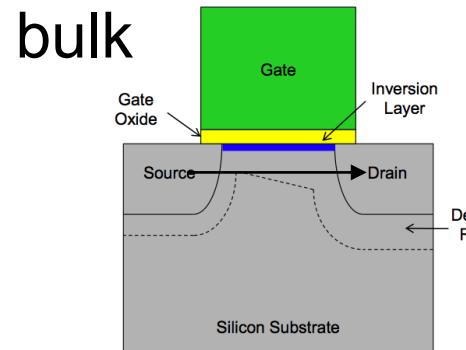
22 nm Tri-Gate Transistor



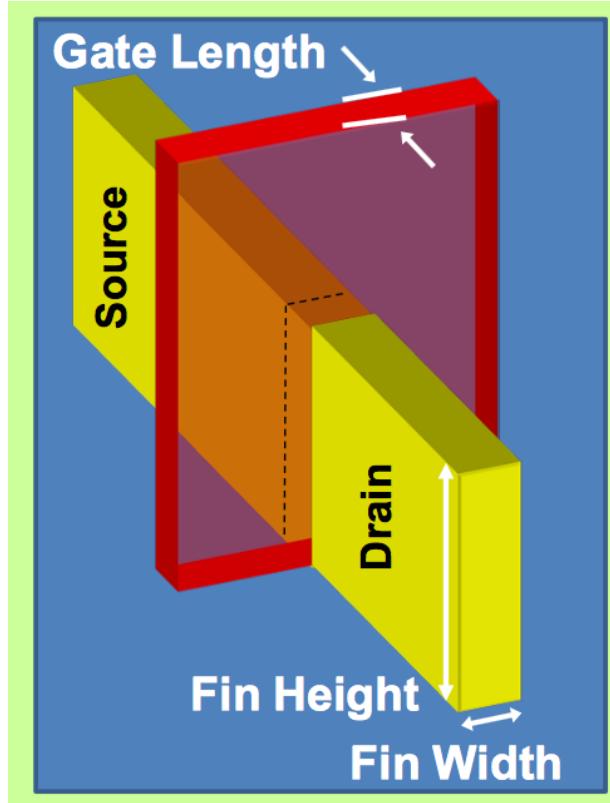
22 nm Tri-Gate Transistor



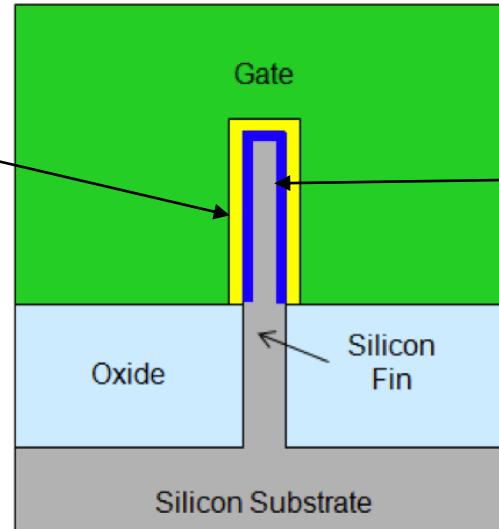
Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance



FinFET

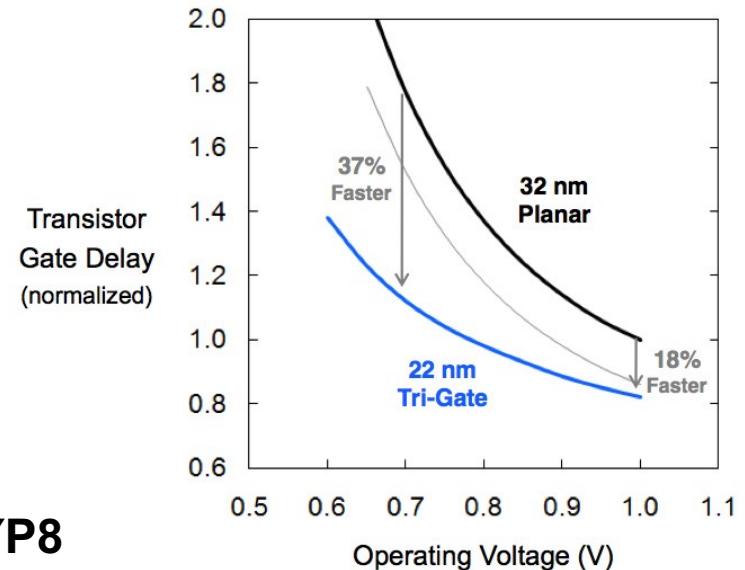


Isolante

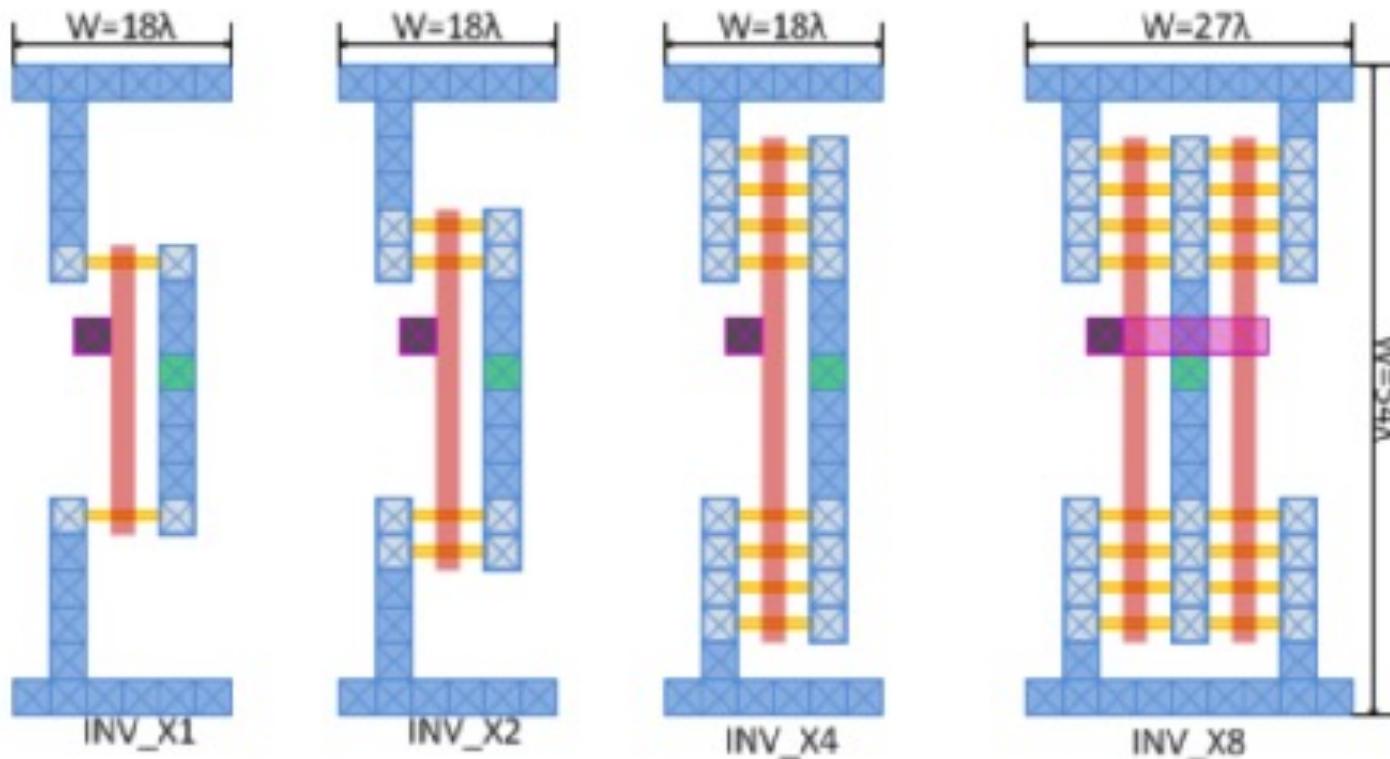
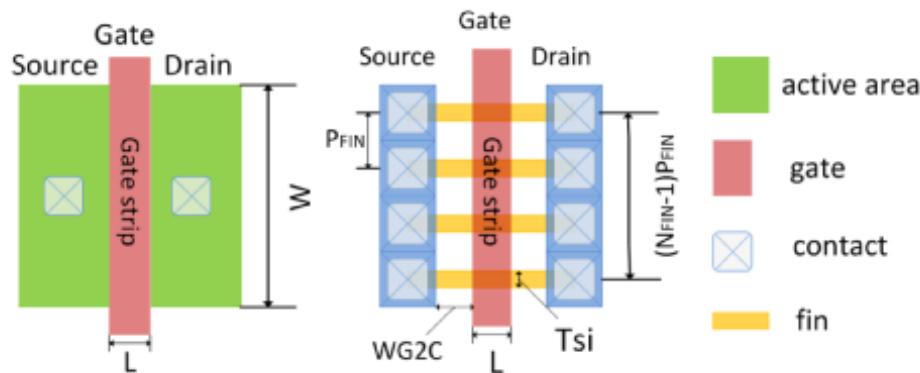


Dopante N ou P

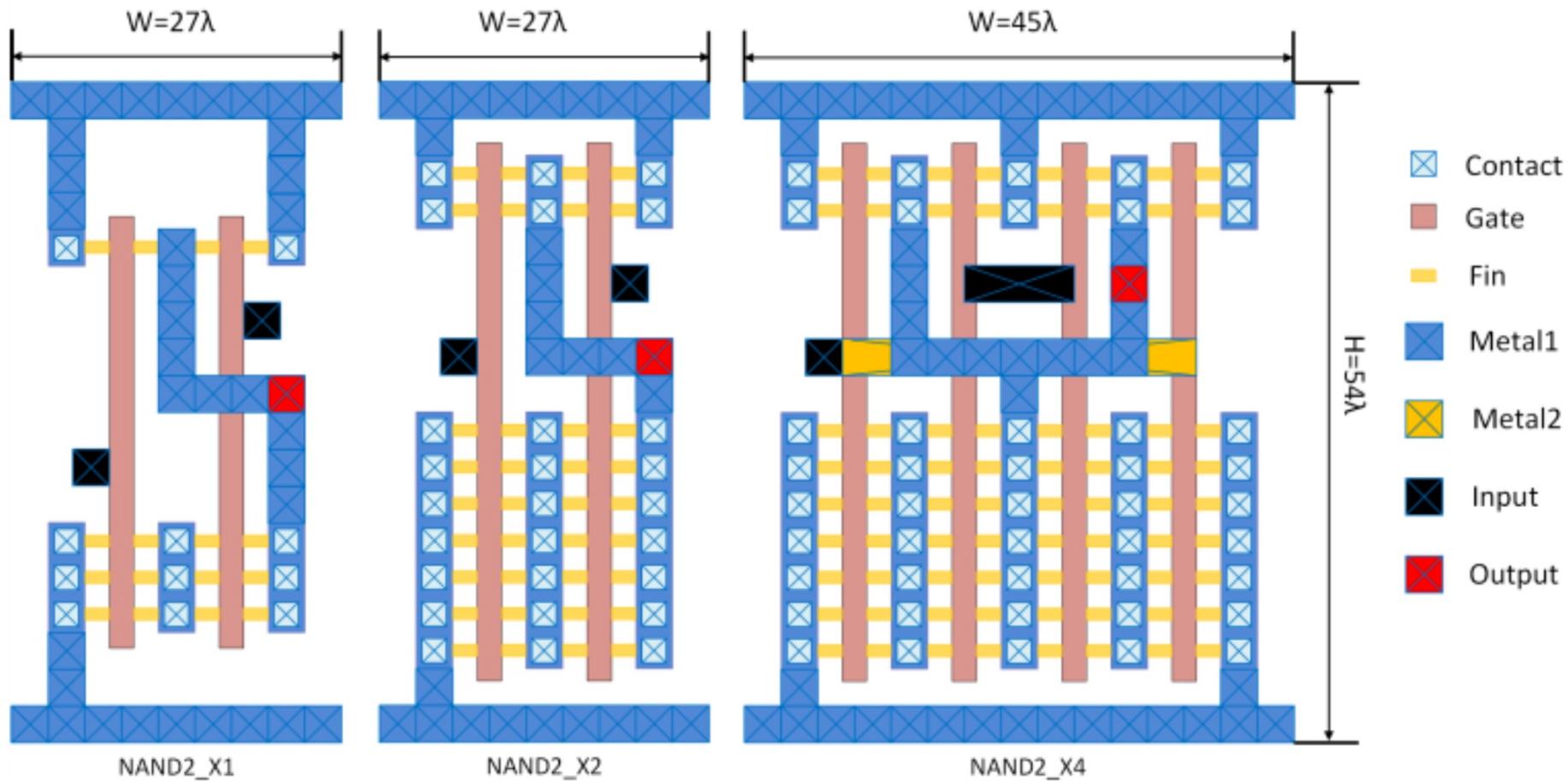
Transistor Gate Delay



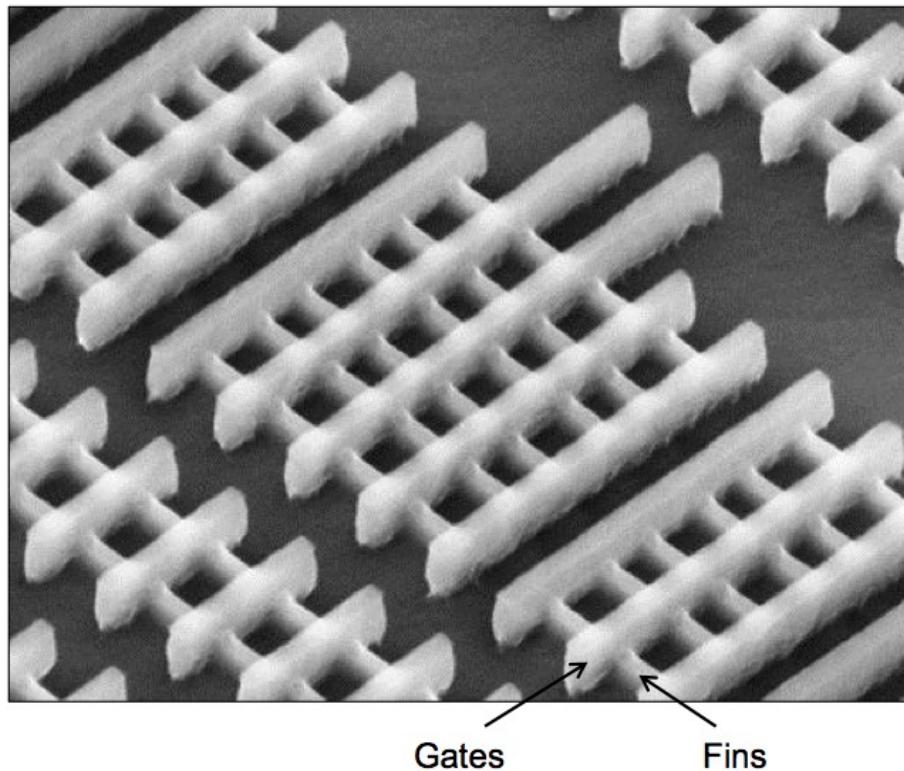
FinFET Layout



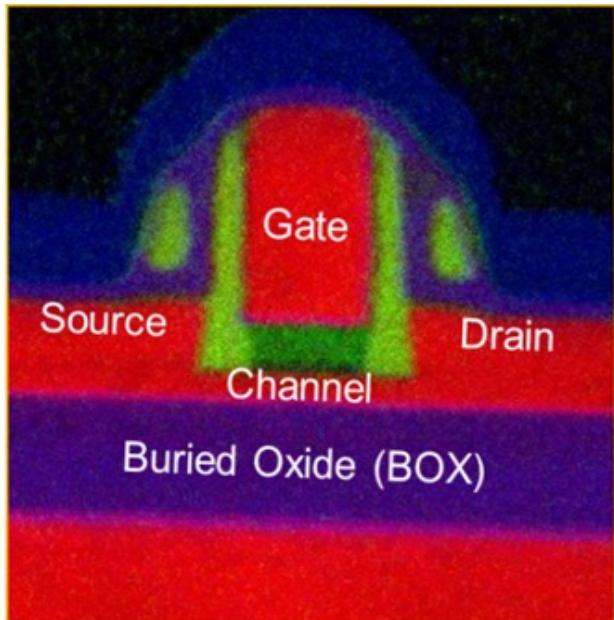
FinFET Layout



22 nm Tri-Gate Transistor

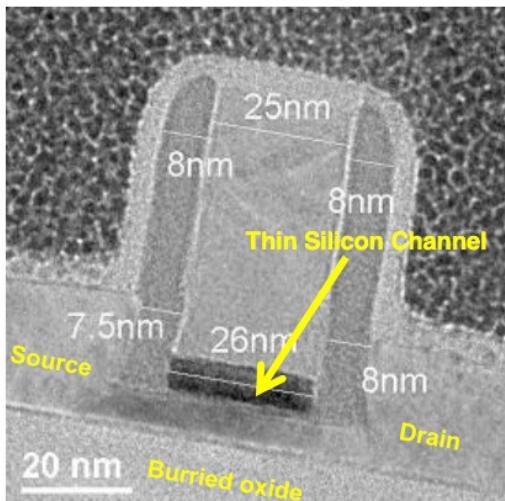


SOI – Silicon on Insulator



Fully Depleted Silicon On Insulator, or FD-SOI:

- planar process technology
- an ultra-thin layer of insulator, called the buried oxide, is positioned on top of the base silicon.
- a very thin silicon film implements the transistor channel.
- Thanks to its thinness, there is no need to dope the channel, thus making the transistor Fully Depleted.
- Device: “ultra-thin body and buried oxide Fully Depleted SOI” or UTBB-FD-SOI



<https://www.youtube.com/watch?v=uvV7jcpQ7UY>

SOI – Silicon on Insulator

- The buried oxide layer lowers the parasitic capacitance between the source and the drain.
- It also efficiently confines the electrons flowing from the source to the drain, reducing performance-degrading leakage currents.

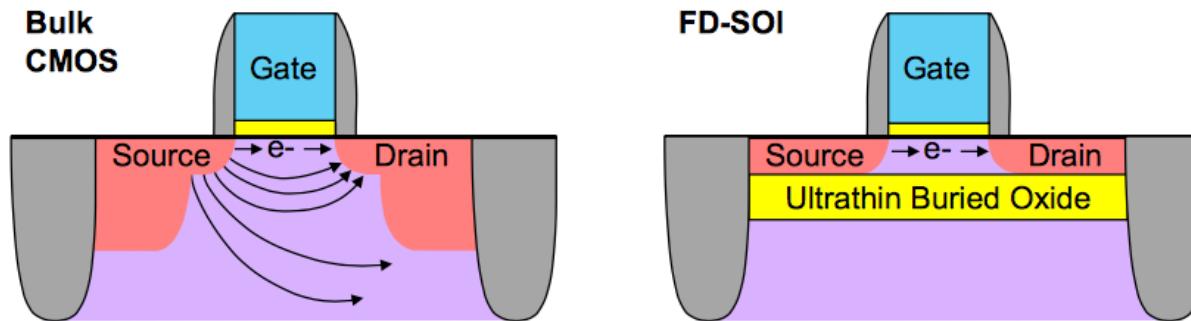
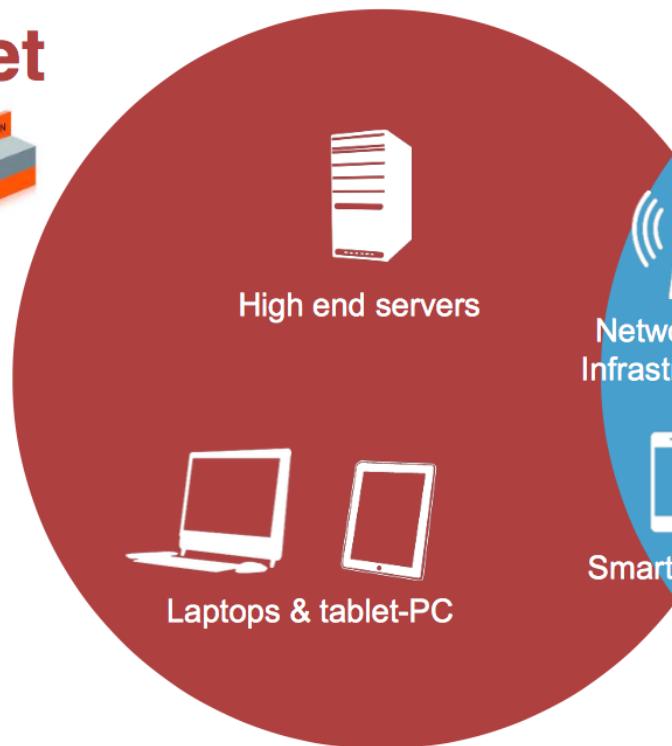
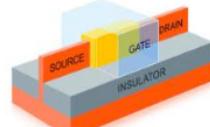


Figure 1. Traditional CMOS versus FD-SOI. As a bulk-CMOS transistor gets smaller, electrons can jump from the source to the drain even when the gate is off, creating leakage current. In the FD-SOI transistor, the buried oxide layer blocks most of the leakage.

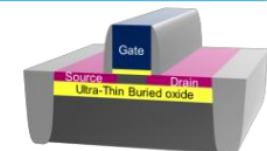
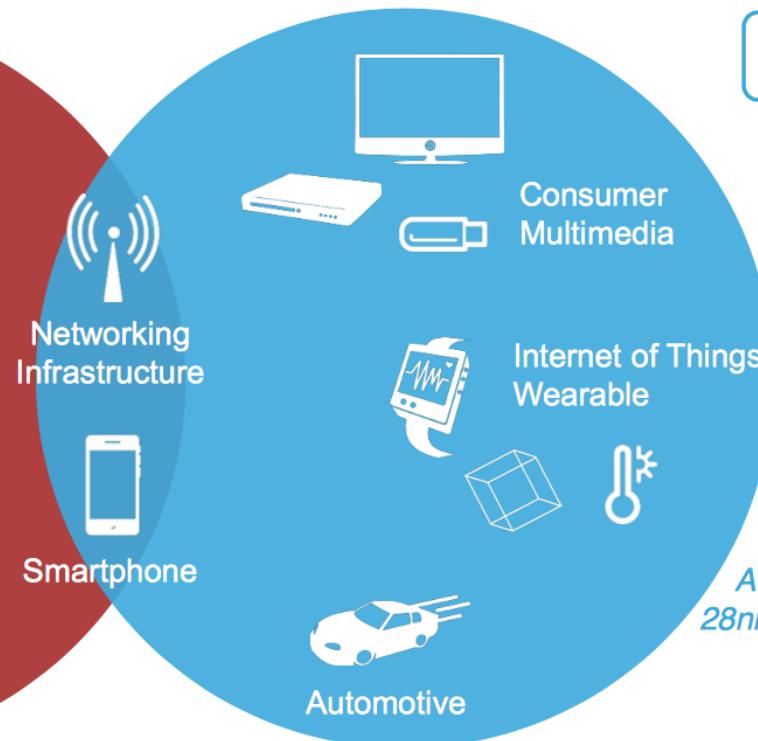
<http://globalfoundries.com/docs/default-source/PDF/FD-SOI-Offers-Alternative-to-FinFET.pdf>

Addressing Digital Markets

FinFet



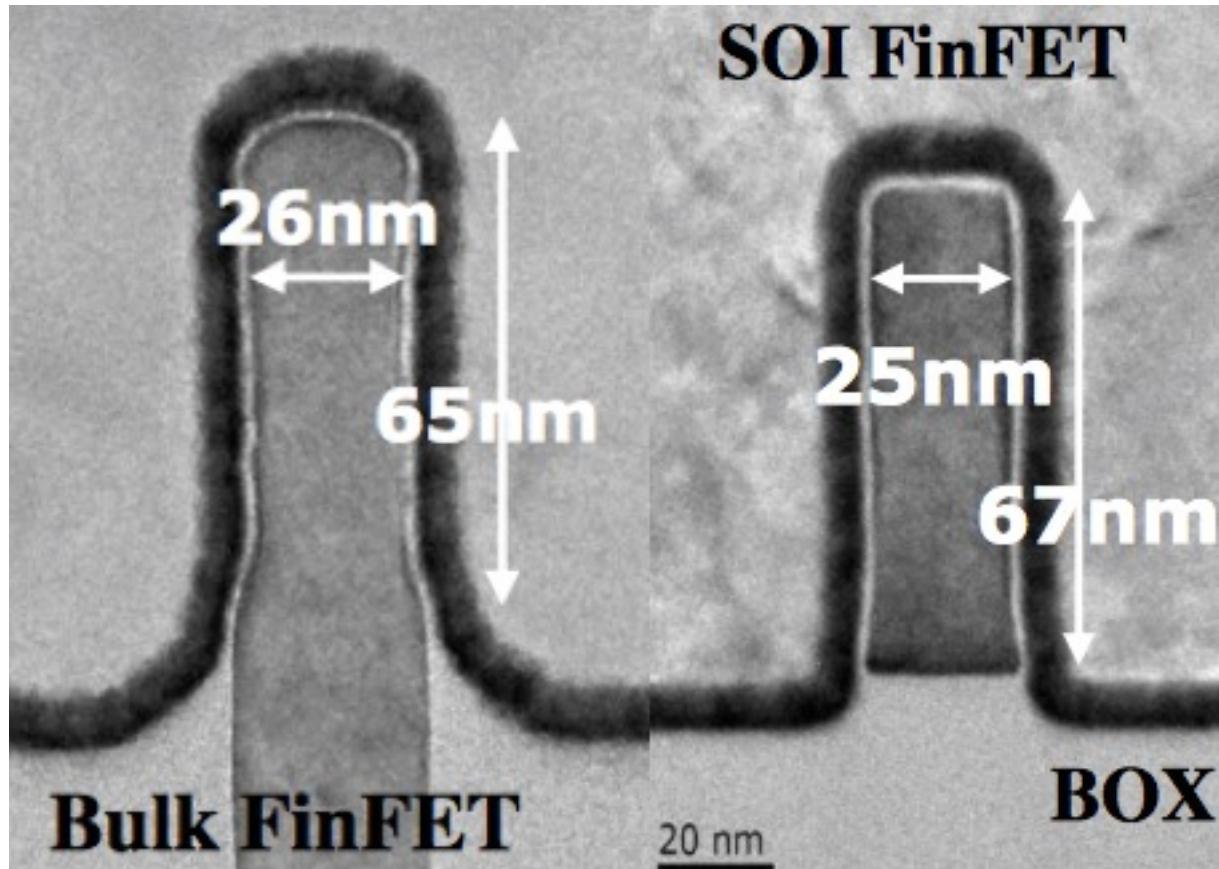
Ultimate Digital Integration



FD-SOI



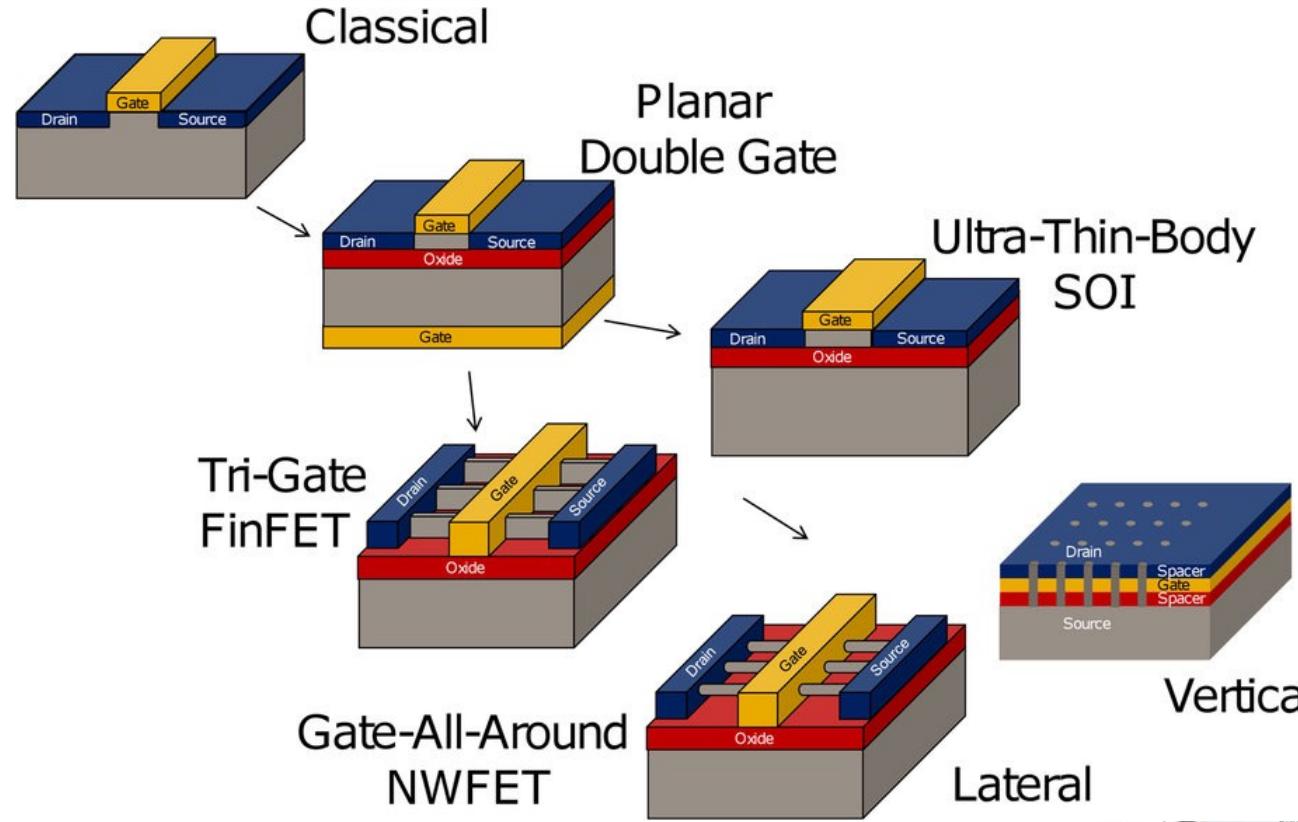
Mais uma opção - SOI FinFET



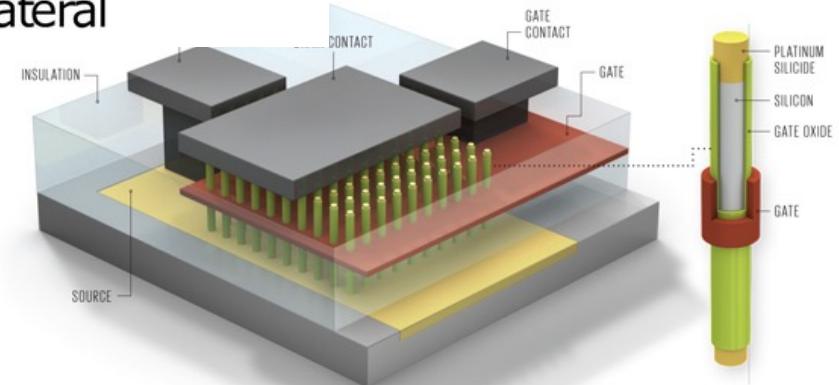
The SOI Industry Consortium (including IBM, Imec, Soitec, and Freescale) has been experimenting with combining FinFETs with SOI, here showing the buried-oxide (BOX, right) which is thinned for FD-SOI.

(Source: SOI Industry Consortium)

Para vai a tecnologia?

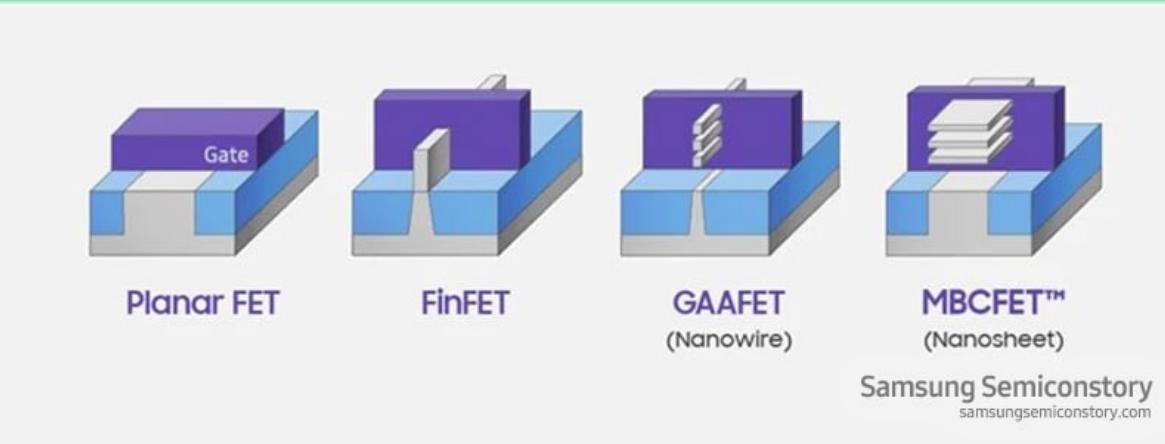


Gate-All-Around Transistors: the transistor channel is made up of an array of vertical nanowires.



GAA Transistors

<https://www.youtube.com/watch?v=3otqUu-7WUQ>



Multi Bridge Channel FET

3nm Samsumg

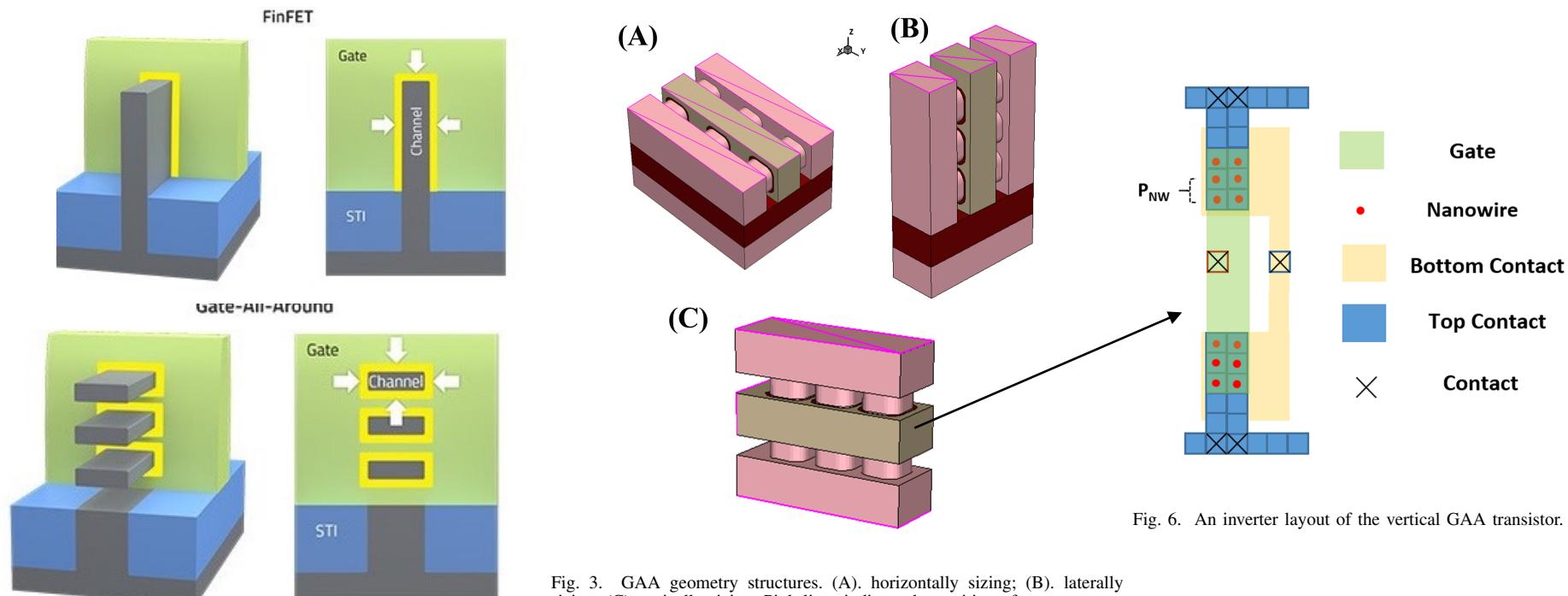


Fig. 6. An inverter layout of the vertical GAA transistor.

Fig. 3. GAA geometry structures. (A). horizontally sizing; (B). laterally sizing; (C).vertically sizing. Pink lines indicate the position of contacts.

Exemplos de equipamentos

Corredor principal da sala limpa



Corredor principal da sala limpa



Corredor lateral (fora da sala limpa)



Equipamentos para monitoramento de gases tóxicos



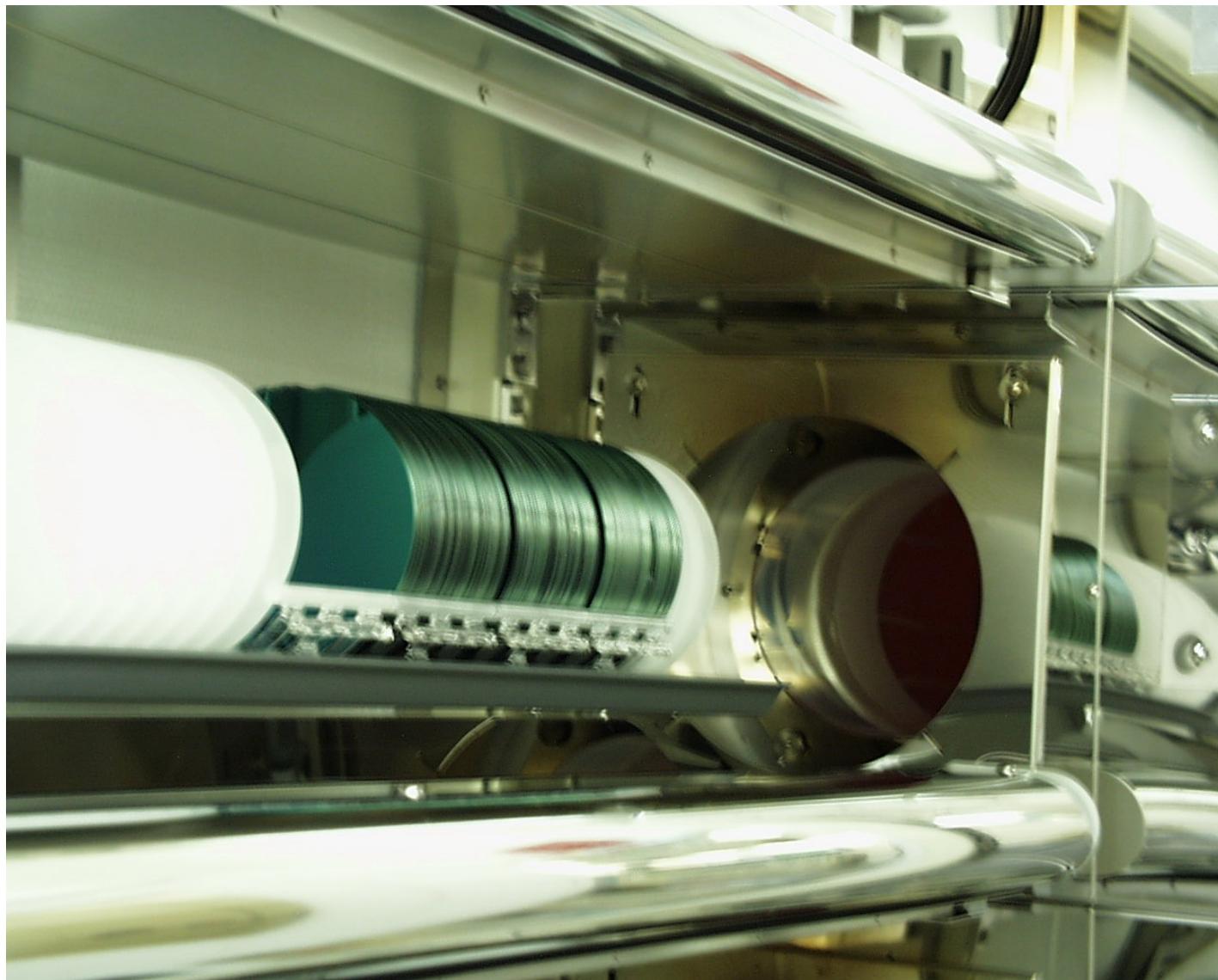
Sala de litografia



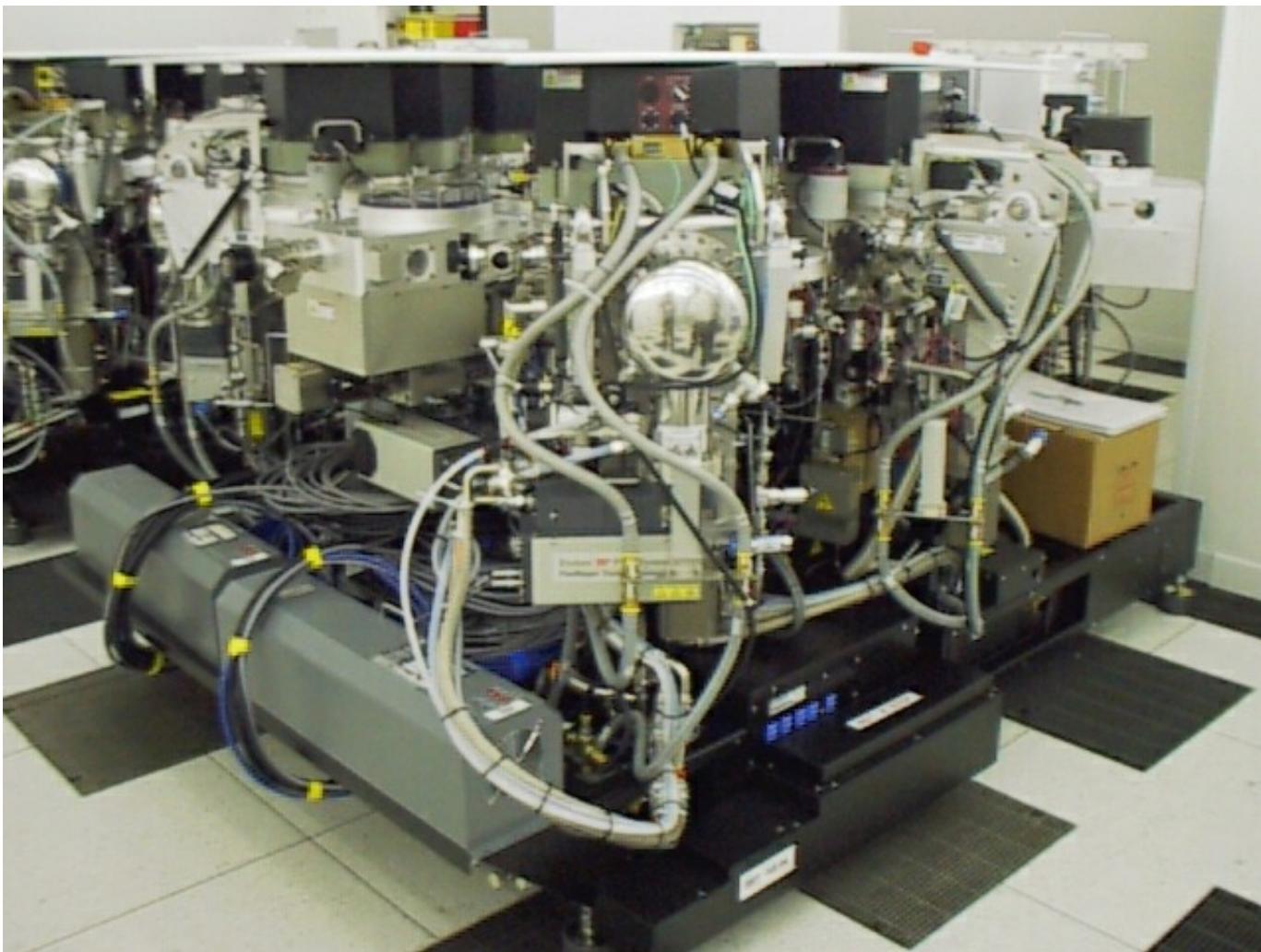
Forno de difusão



Forno de difusão



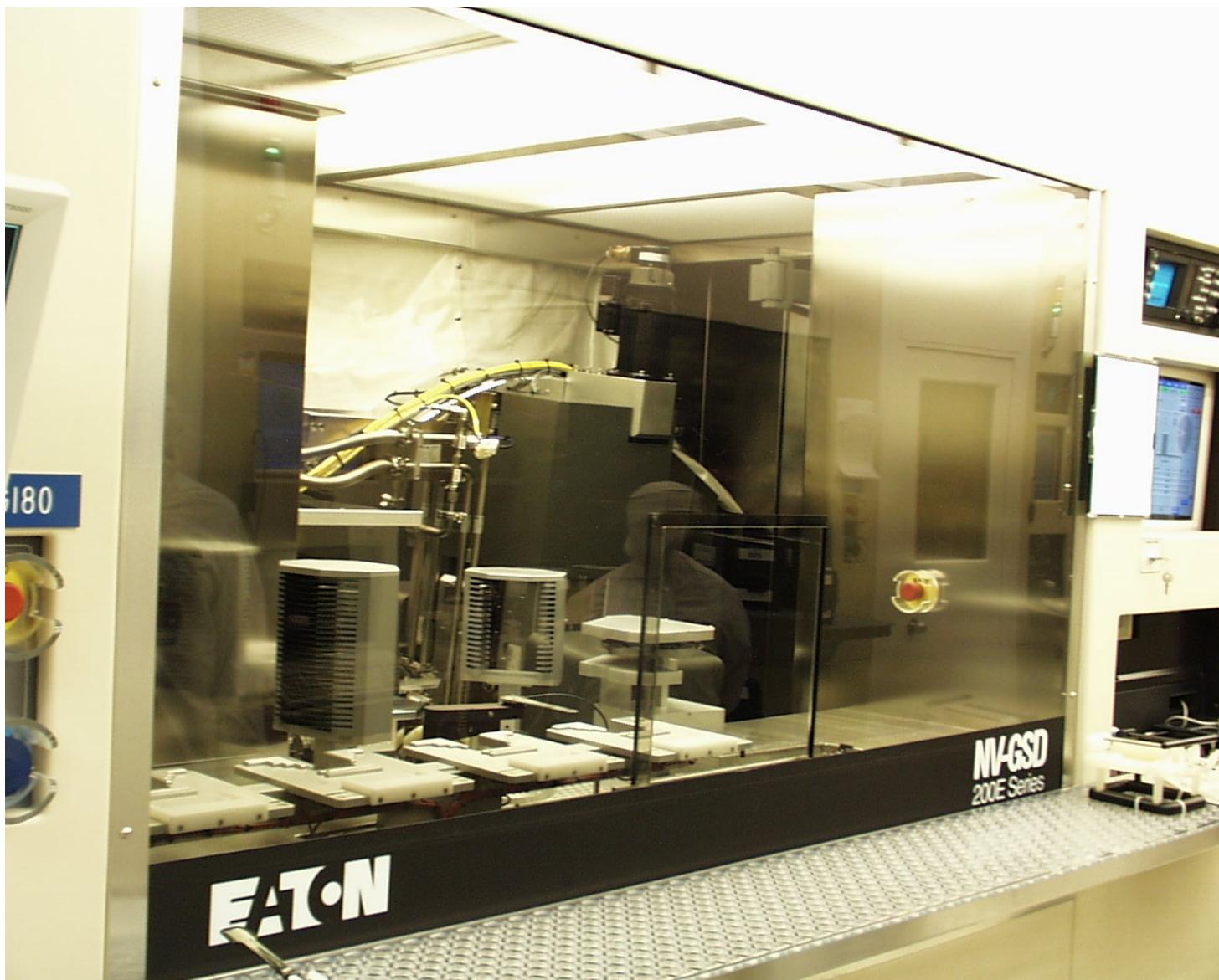
Equipamento para deposição de metal



Equipamento de etching

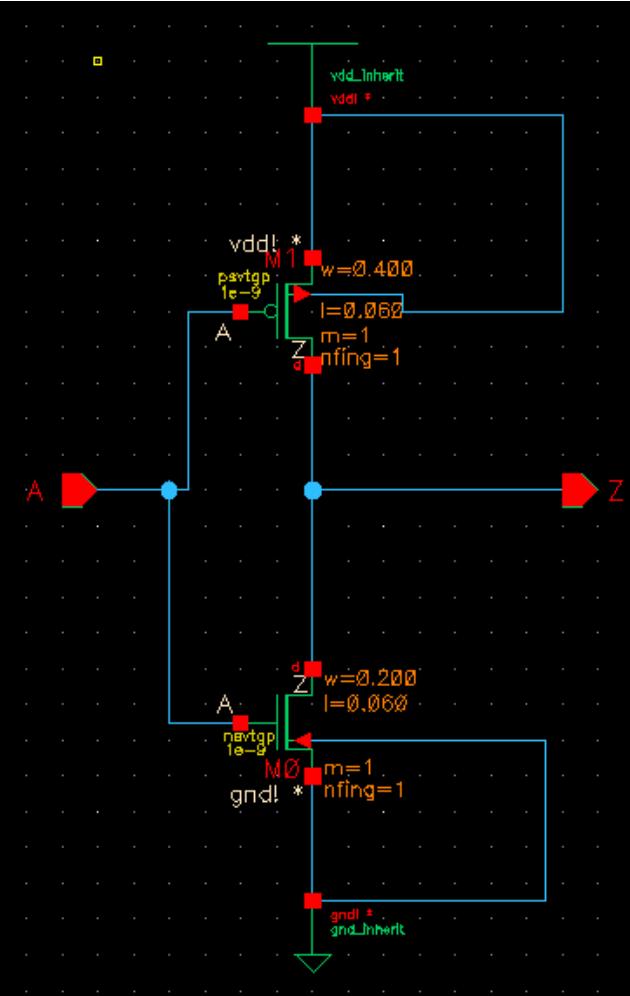


Painel do implantador iônico

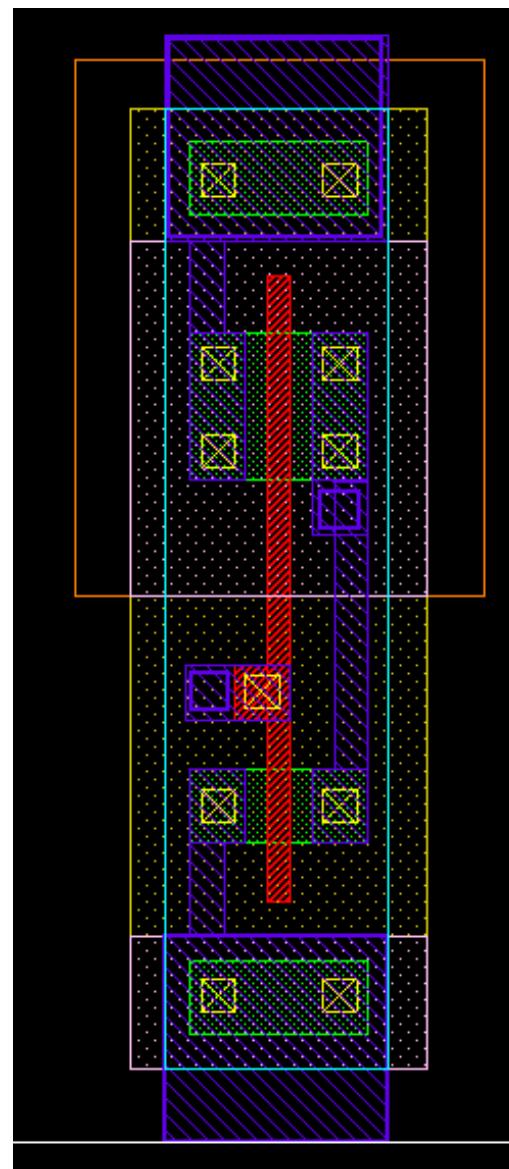


LAB4

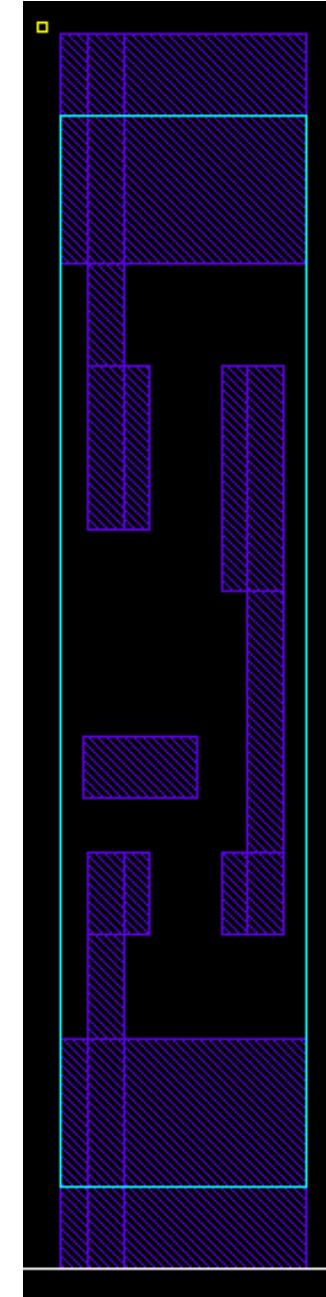
DRC, LVS, extração,
simulação



ESQUEMÁTICO



LAYOUT



ABSTRACT 115

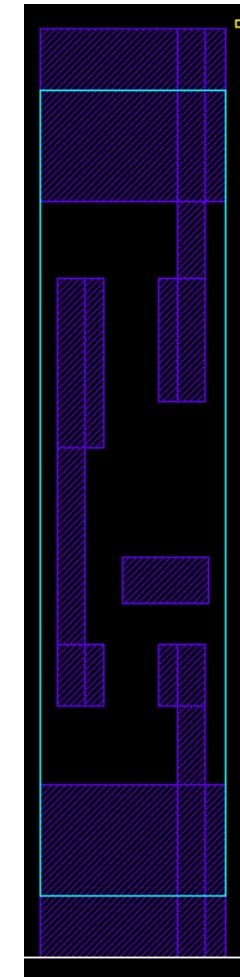
LAB4

PROBLEMA 1: inserção nos pinos do layout – erro na camada PIN e por consequência LVS falha

PROBLEMA 2: passo 7 ABSTRACT

SEGUIR OS PASSO ‘a’ – ‘e’

```
*****  
# Preview export LEF  
#  
# Preview sub-version  
5.10.41_USR5.90.69  
#  
# REF LIBS: lab3  
# TECH LIB NAME: cmos065  
# TECH FILE NAME: techfile.cds  
*****  
....  
MACRO inv  
    CLASS CORE ; Lembrar de substituir  
    ...  
    PIN A  
    ....  
END A
```



LAB4 - Final

