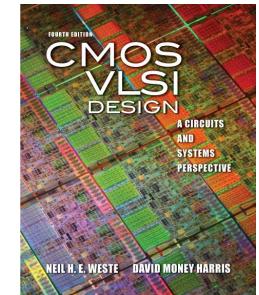
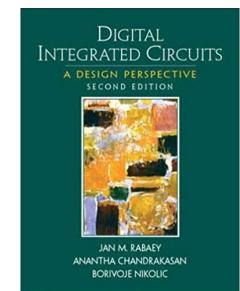


# Microeletrônica

## Aula #8 → Circuitos sequenciais dinâmicos

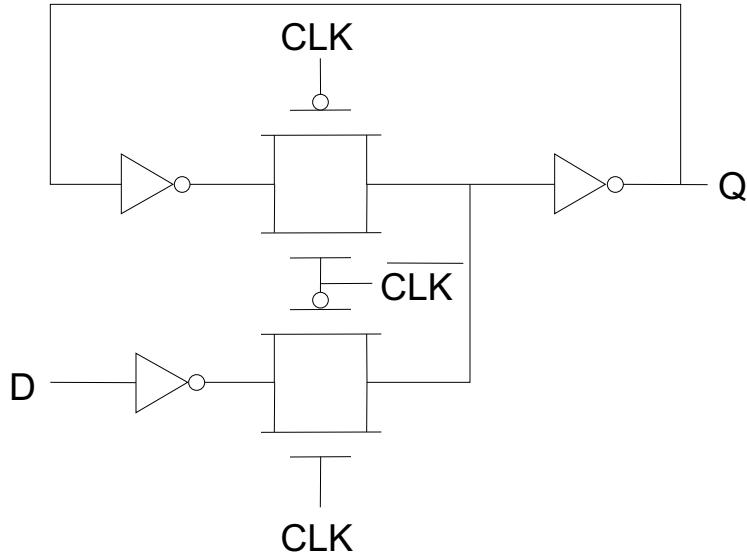
- Professor: Fernando Gehm Moraes
- Livro texto:  
Digital Integrated Circuits a Design Perspective - Rabaey  
C MOS VLSI Design - Weste



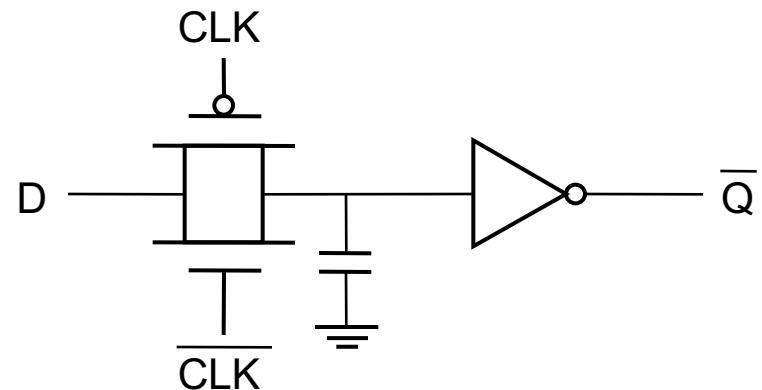
**Revisão das lâminas: 10/outubro/2023**

# Storage Mechanisms

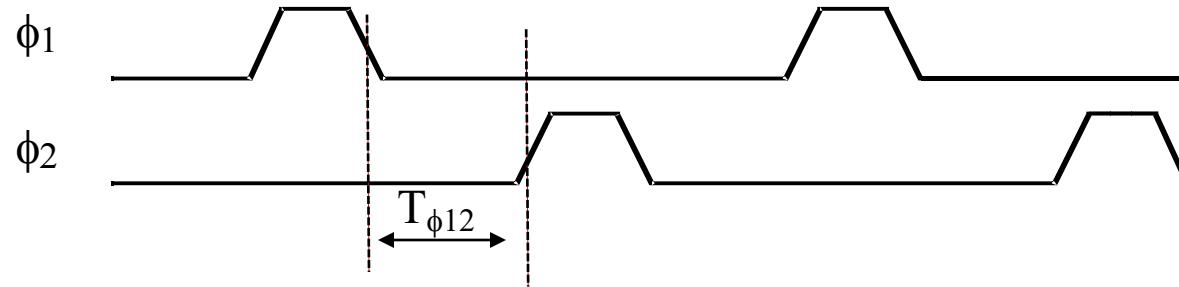
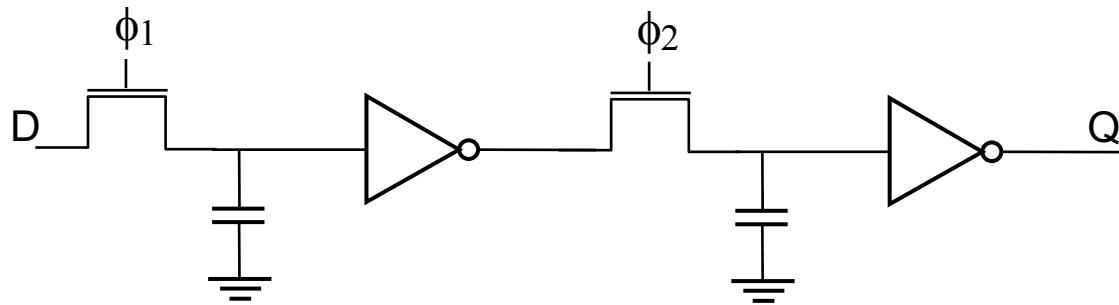
Static (mux-based latch)



Dynamic (charge-based)

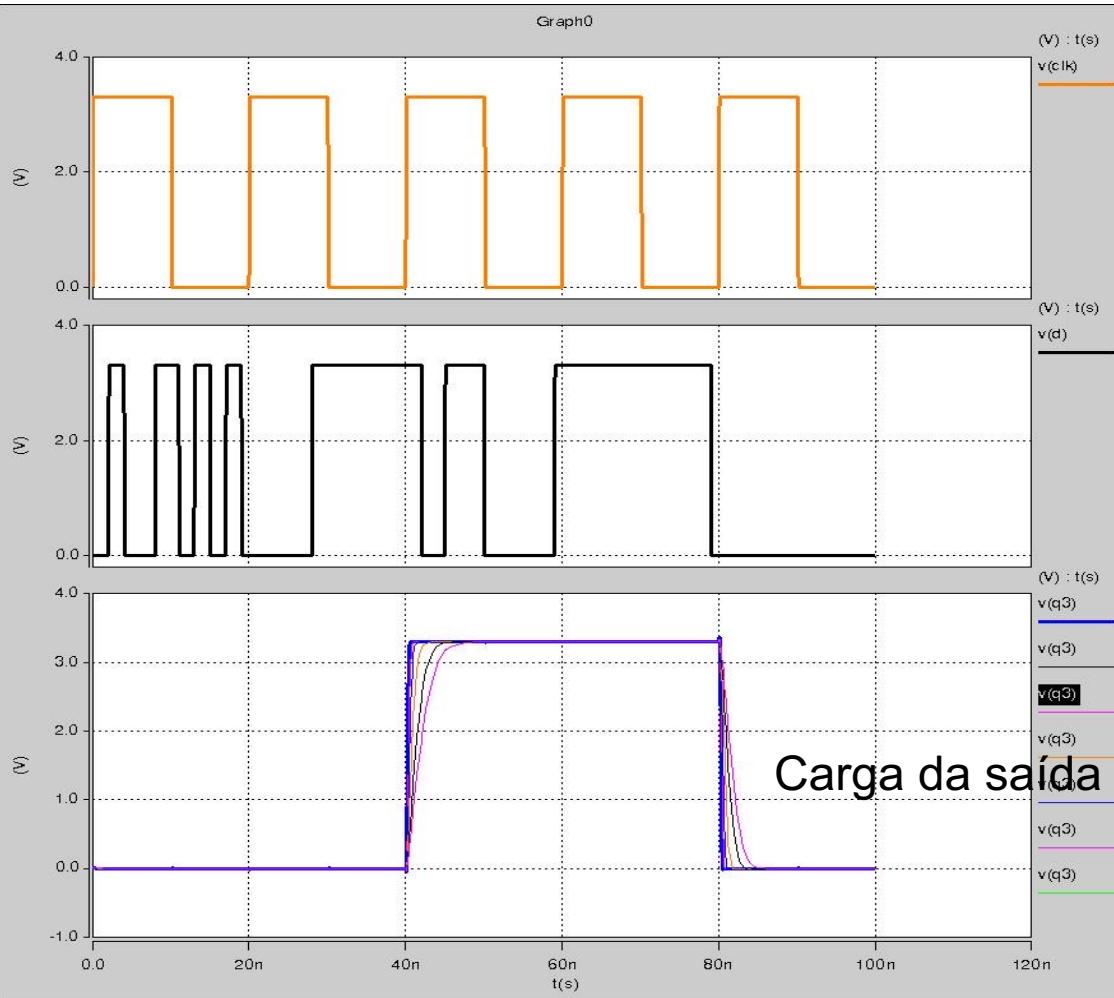
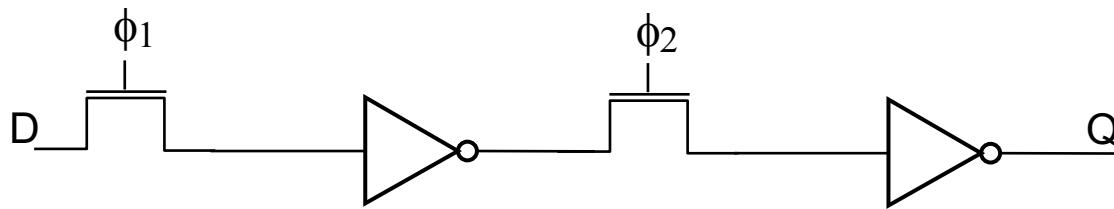


# Flip Flop MS Dinâmico de 2 Fases



- Reduzida complexidade dos circuitos dinâmicos
- A implementação necessita somente 6 transistores
- Necessita relógios sem sobreposição
- $T_{\phi_{12}}$  pode ocasionar perda de desempenho

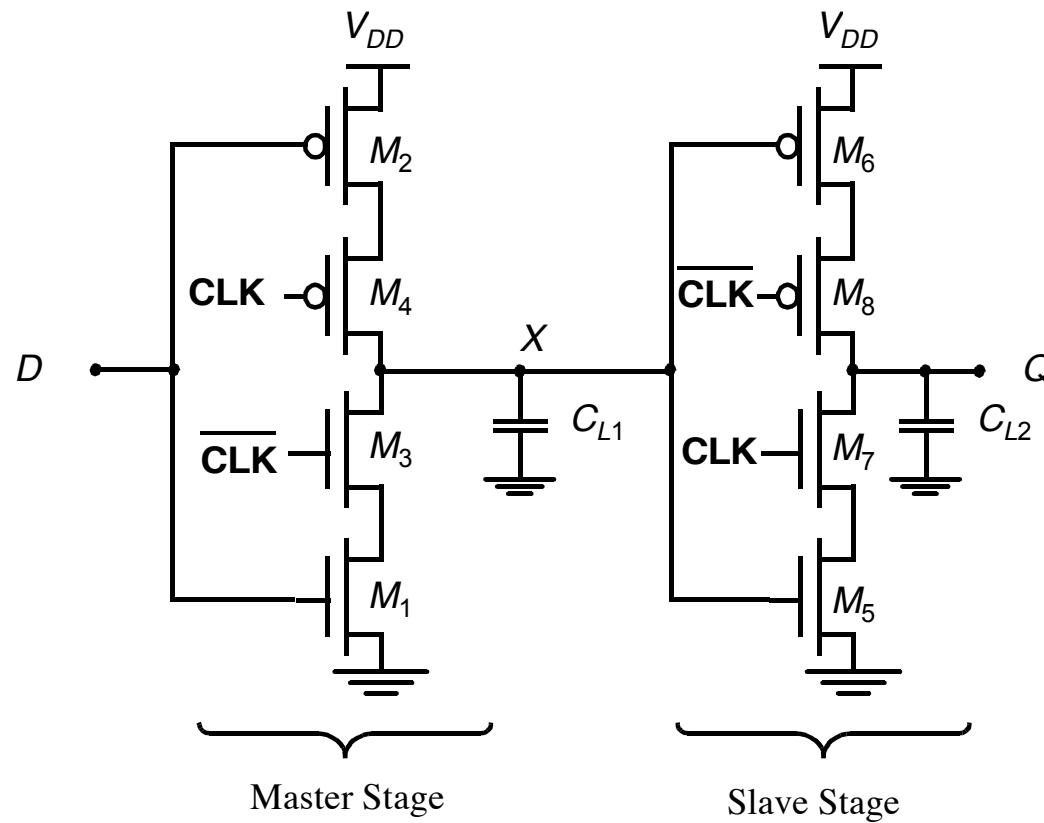
# Simulação



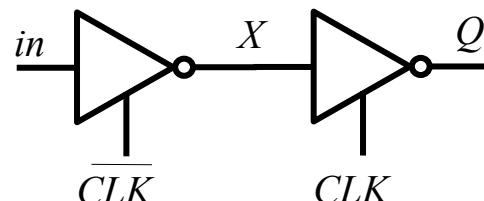
```
.subckt din d q ck vcc
X1 d nck ck A vcc tg
X2 A B vcc inv
X3 B ck nck C vcc tg
X4 C q vcc inv
X5 ck nck vcc inv
.ends din
```

# FF Mestre-Escravo: C<sup>2</sup>MOS

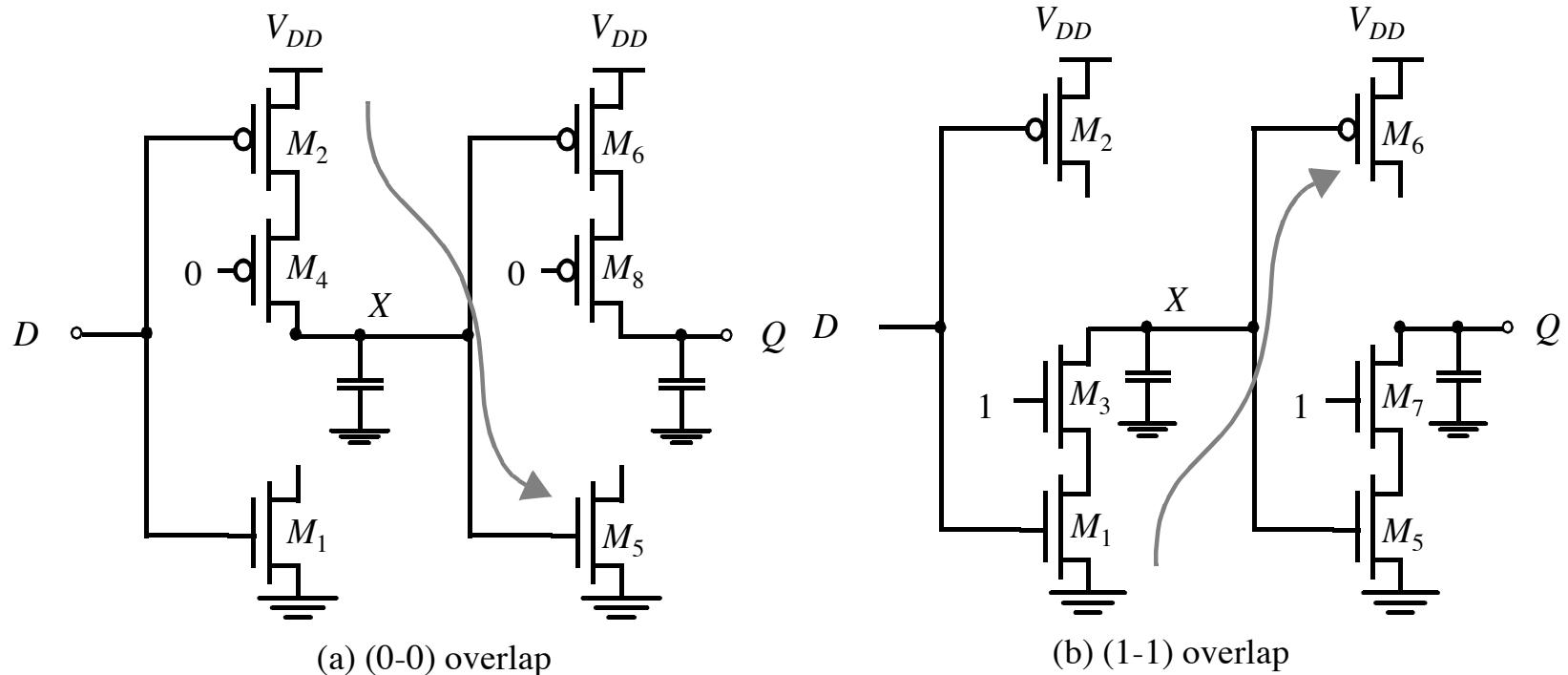
MS dinâmico insensível à sobreposição das fases de clock



**Figure 7.26** C<sup>2</sup>MOS master-slave positive edge-triggered register.



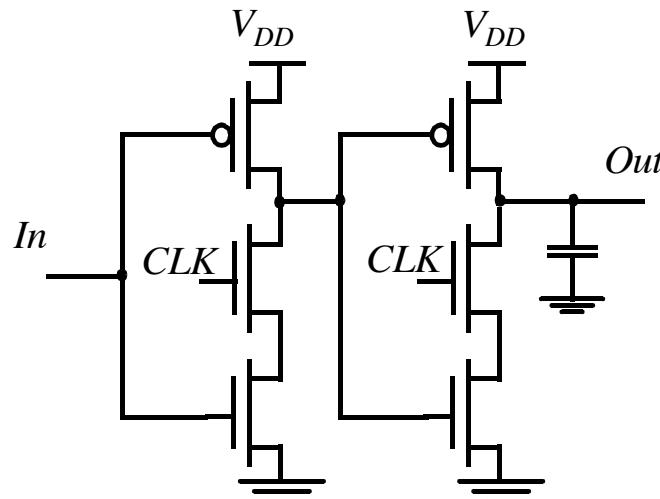
# Insensitive to Clock-Overlap



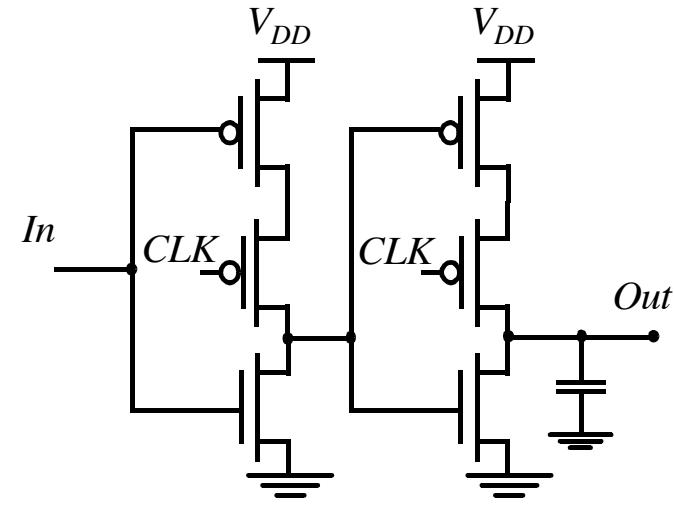
**Figure 7.27** C<sup>2</sup>MOS D-FF during overlap periods. No feasible signal path can exist between *In* and *D*, as illustrated by the arrows.

# Latch TSPC

TSPC → True Single-Phase Clocked



Positive Latch

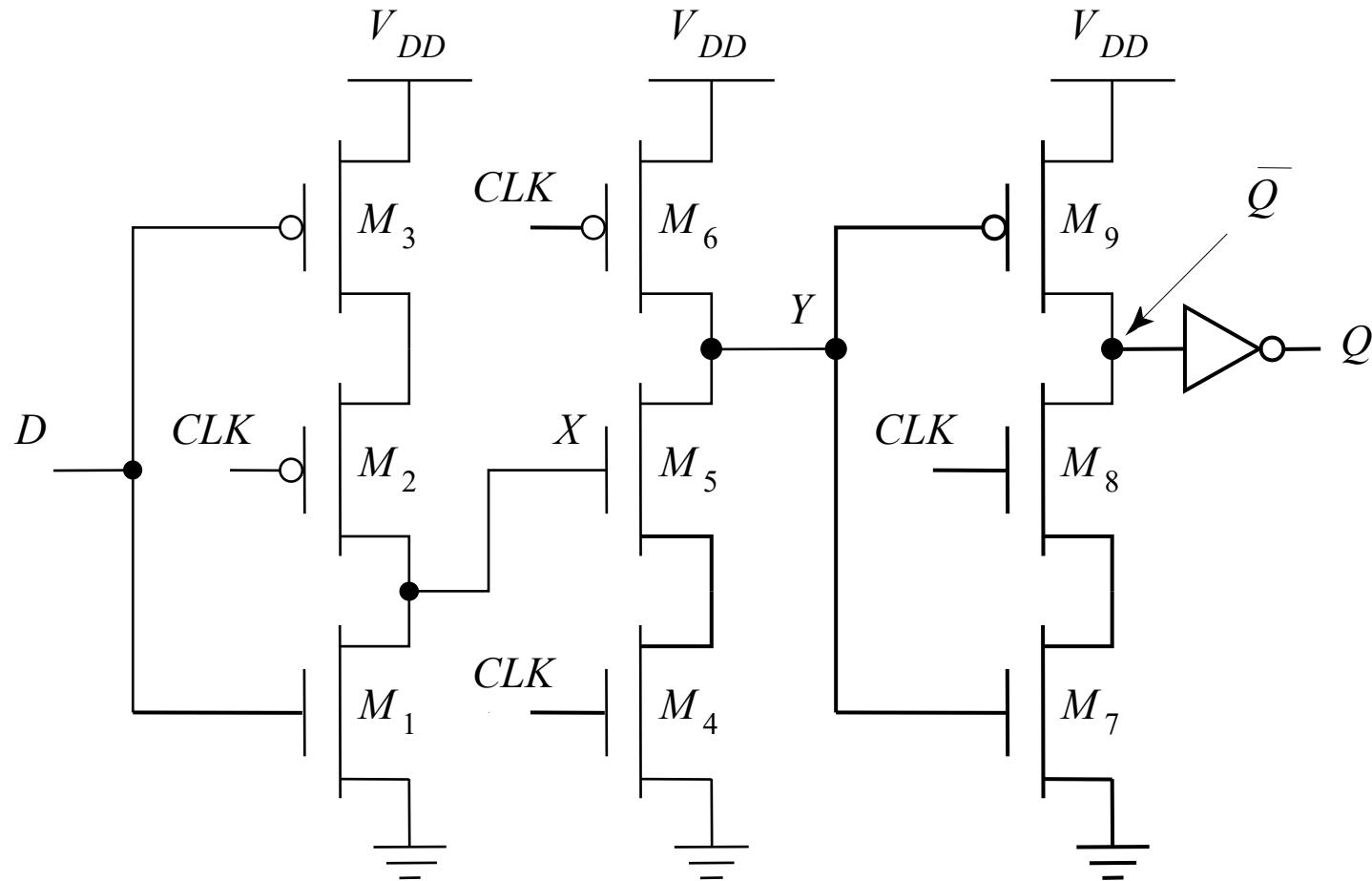


Negative Latch

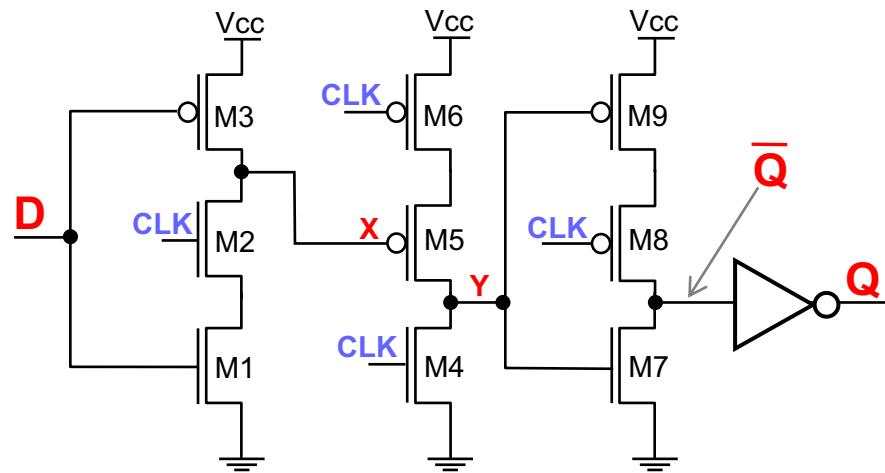
Figure 7.30 True Single Phase Latches.

Positive latch  
(transparent when  $CLK=1$ )      Negative latch  
(transparent when  $CLK=0$ )

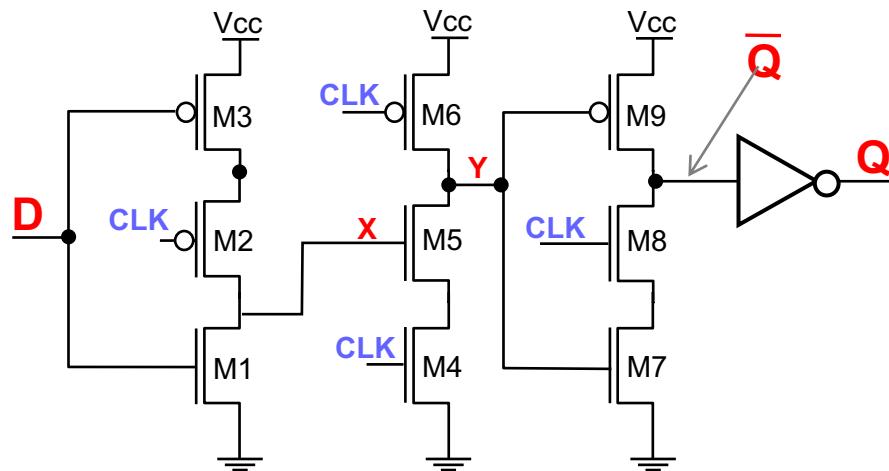
# Mestre-escravo TSPC - subida



# Mestre-escravo TSPC



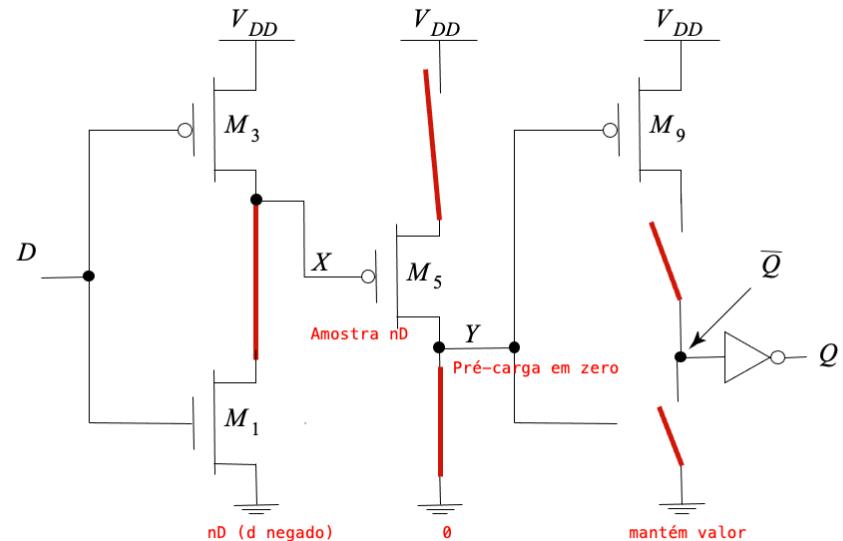
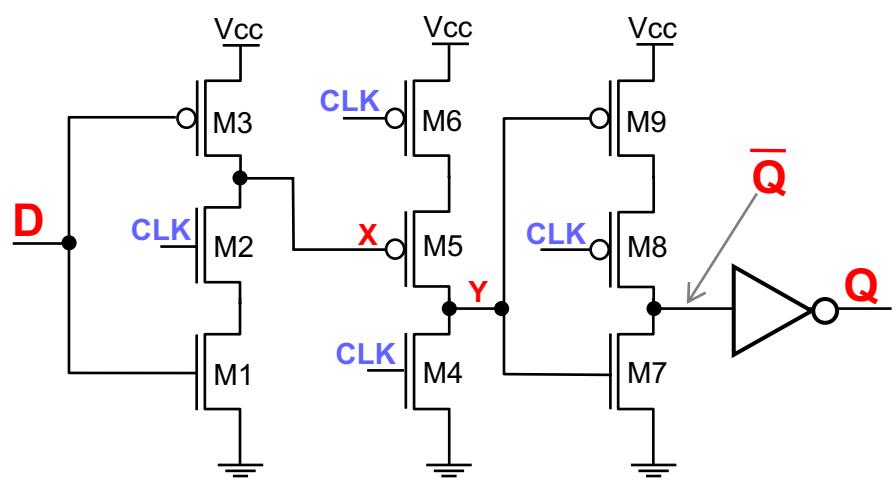
descida



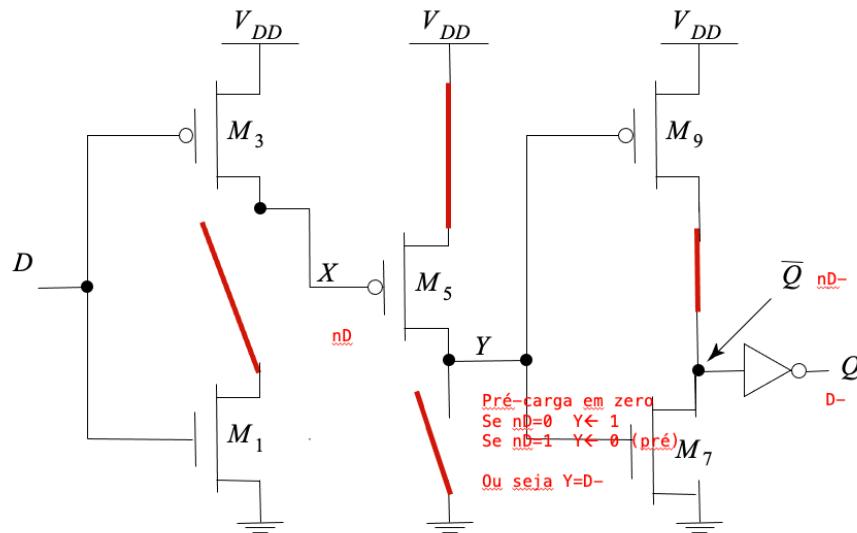
subida

Possui a vantagem de necessitar um único relógio

# CK=1: amostra em M5, pré-carga 0 em Y, mantém Q



CK= ↓: Y recebe D antes da borda, e transfere para saída



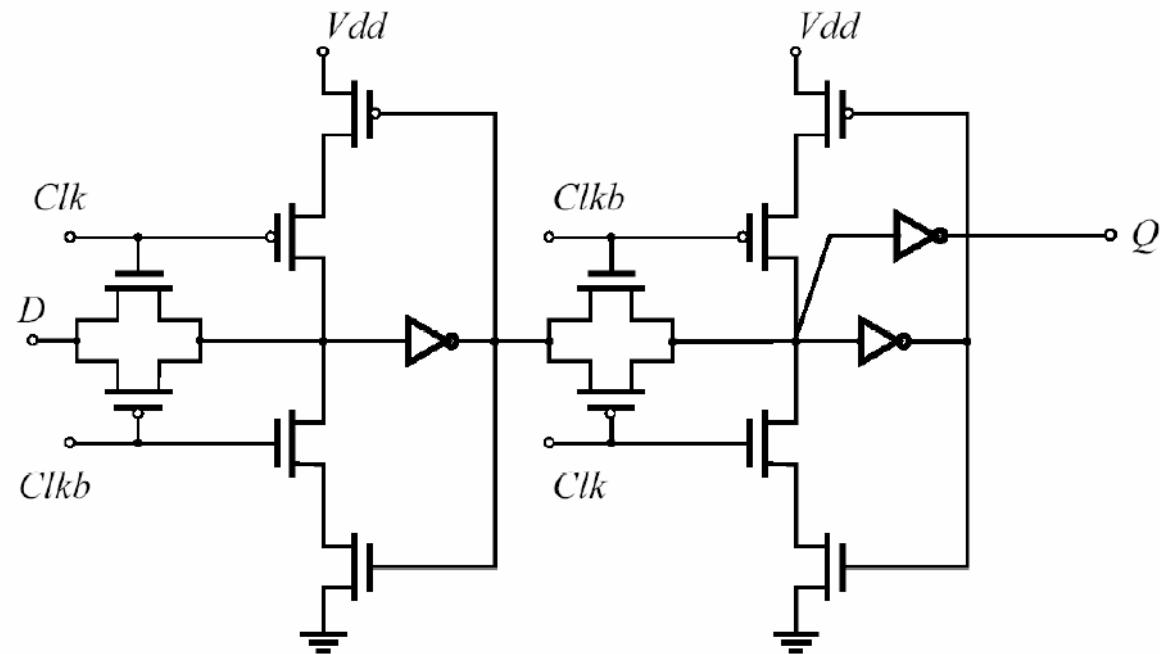
# Exercício – analise o seguinte FF

Fonte: <http://www.ece.ncsu.edu/asic/ece733/2008/docs/FlipFlops1up.pdf>

## Transmission Gate Master-Slave

### PowerPC 603

- Clock Load
  - ♦ High
- Power
  - ♦ Low
  - ♦ low power feedback
- Positive setup

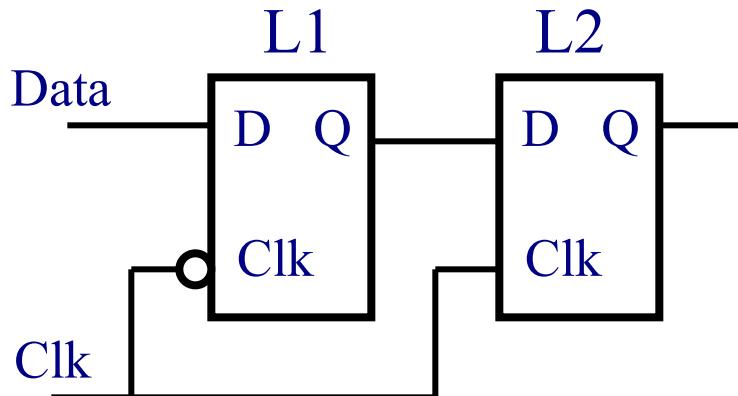


# Pulse-Triggered Latches

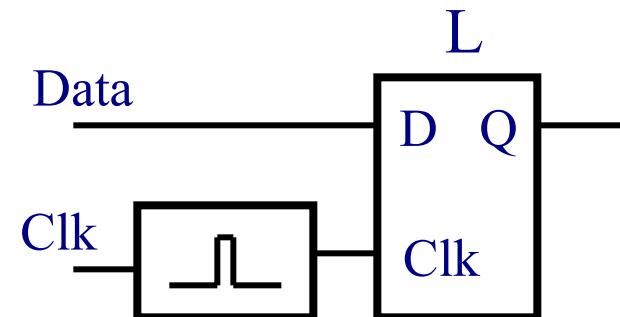
## An Alternative Approach

Ways to design an edge-triggered sequential cell:

Master-Slave  
Latches

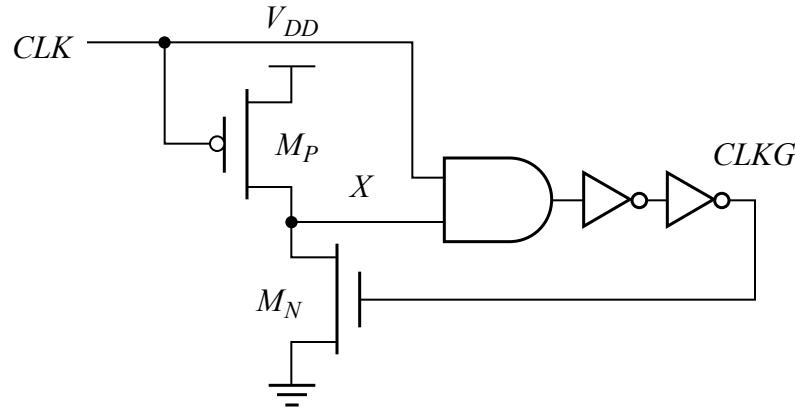


Pulse-Triggered  
Latch



# Circuito Gerador de Pulso

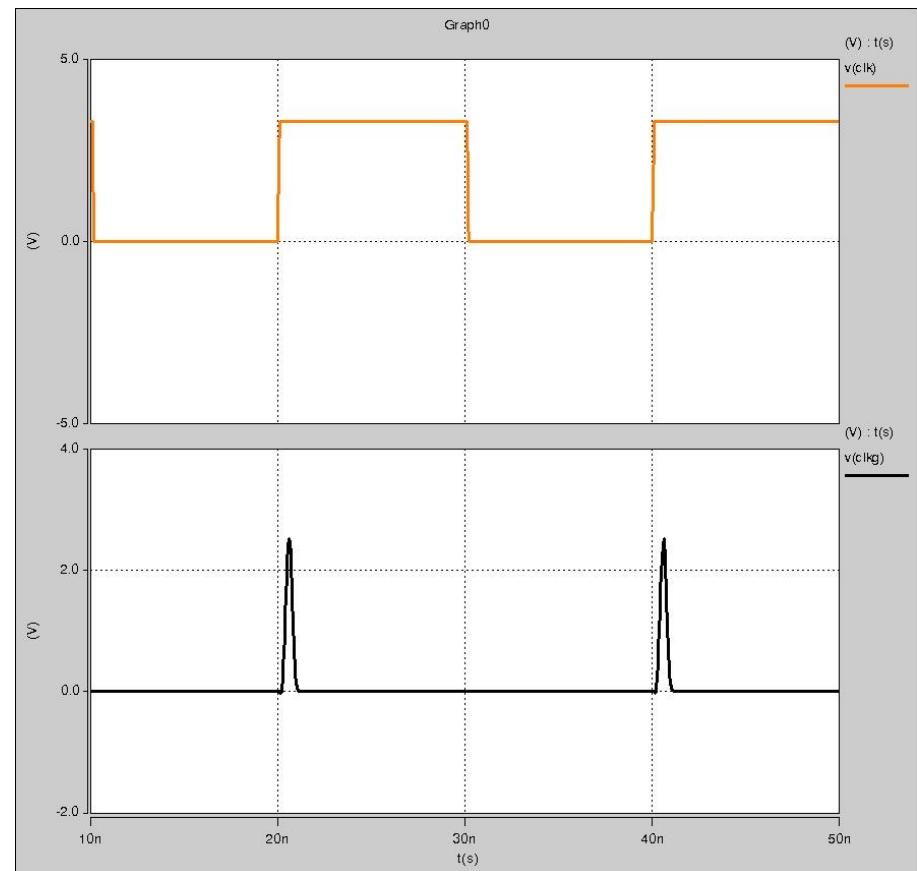
- A idéia é não usar MS, e sim latches, usando como gatilho pulsos muito rápidos



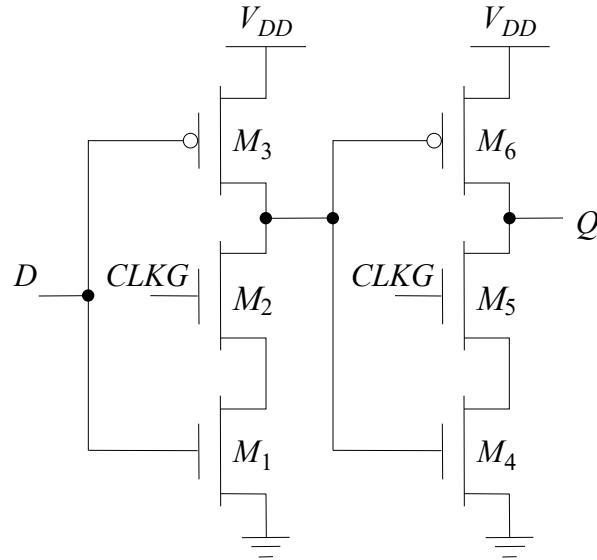
```

.subckt pulso clk clkg vcc
X1 clk X n1 vcc nand2
X2 n1 clkg vcc inv
MP2 X clk vcc vcc pmos l=0.35U W=3.0U
MN2 X clkg 0 0 nmos l=0.35U W=1.5U
.ends pulso

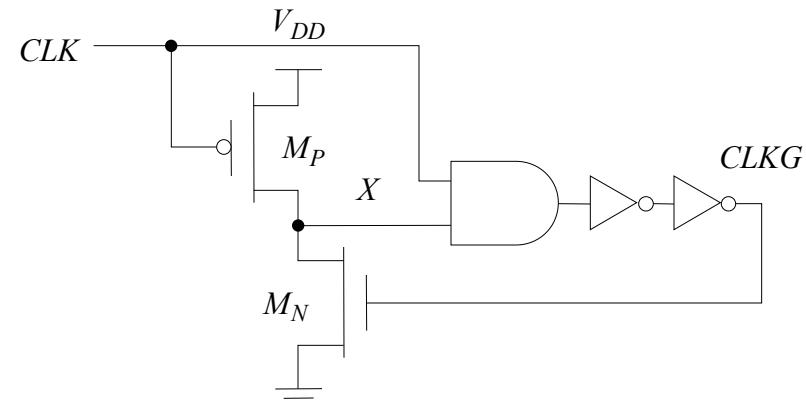
```



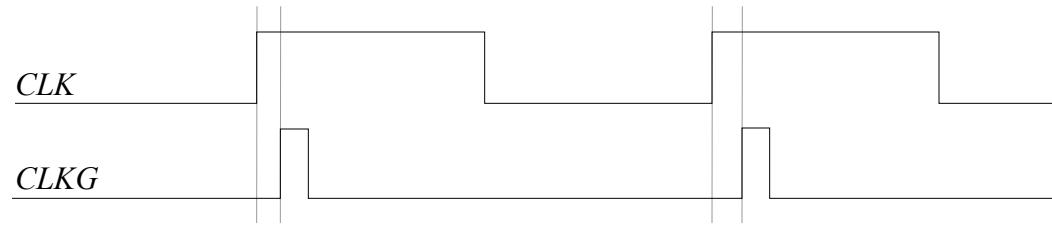
# Pulsed Latches



(a) register



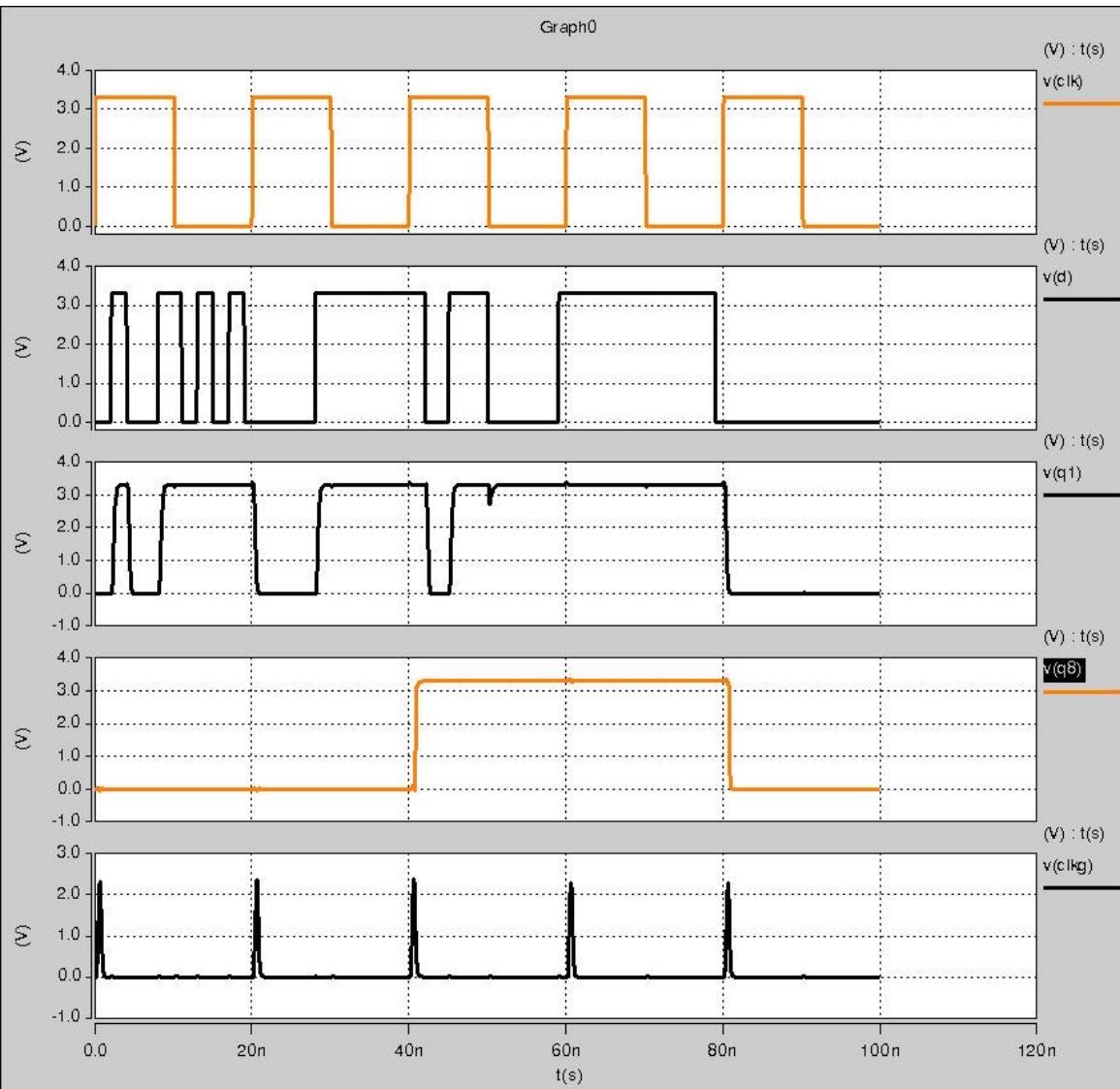
(b) glitch generation



(c) glitch clock

# Comparação

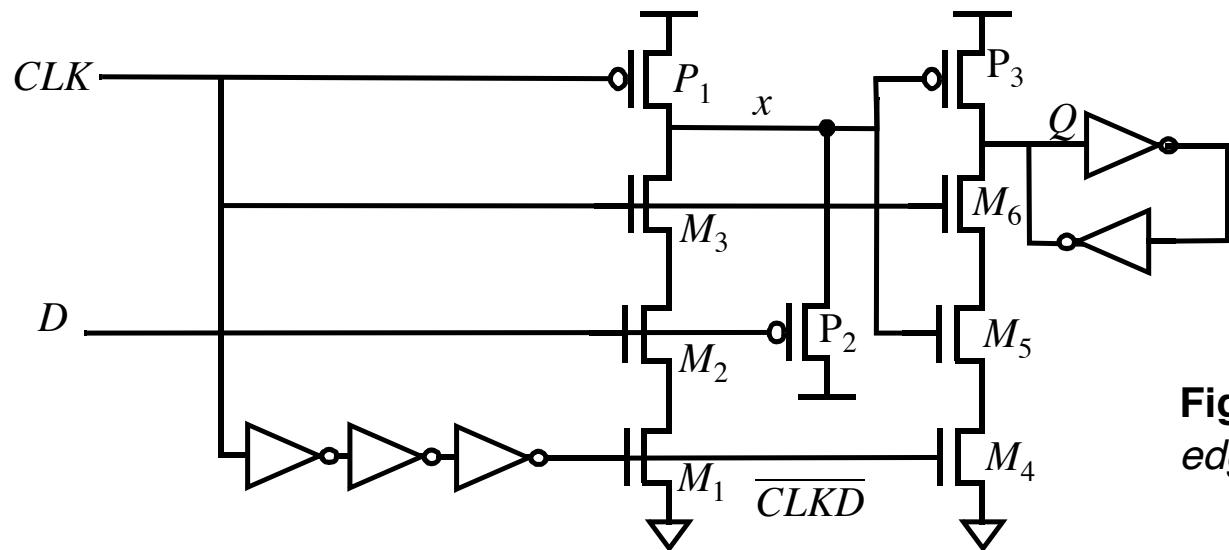
x1 D q1 clk vcc latch1  
x8 D q8 clkg vcc latch1



- Mesma latch, transparente no nível alto, controlada por un clock e por um glitch
- **EFEITO:** quando controlada por glitch atua como mestre escravo
- Razão: tempo que a latch fica transparente é muito curto, não ocorredo “race”
- Menor carga na linha do clock

# Pulsed Latches

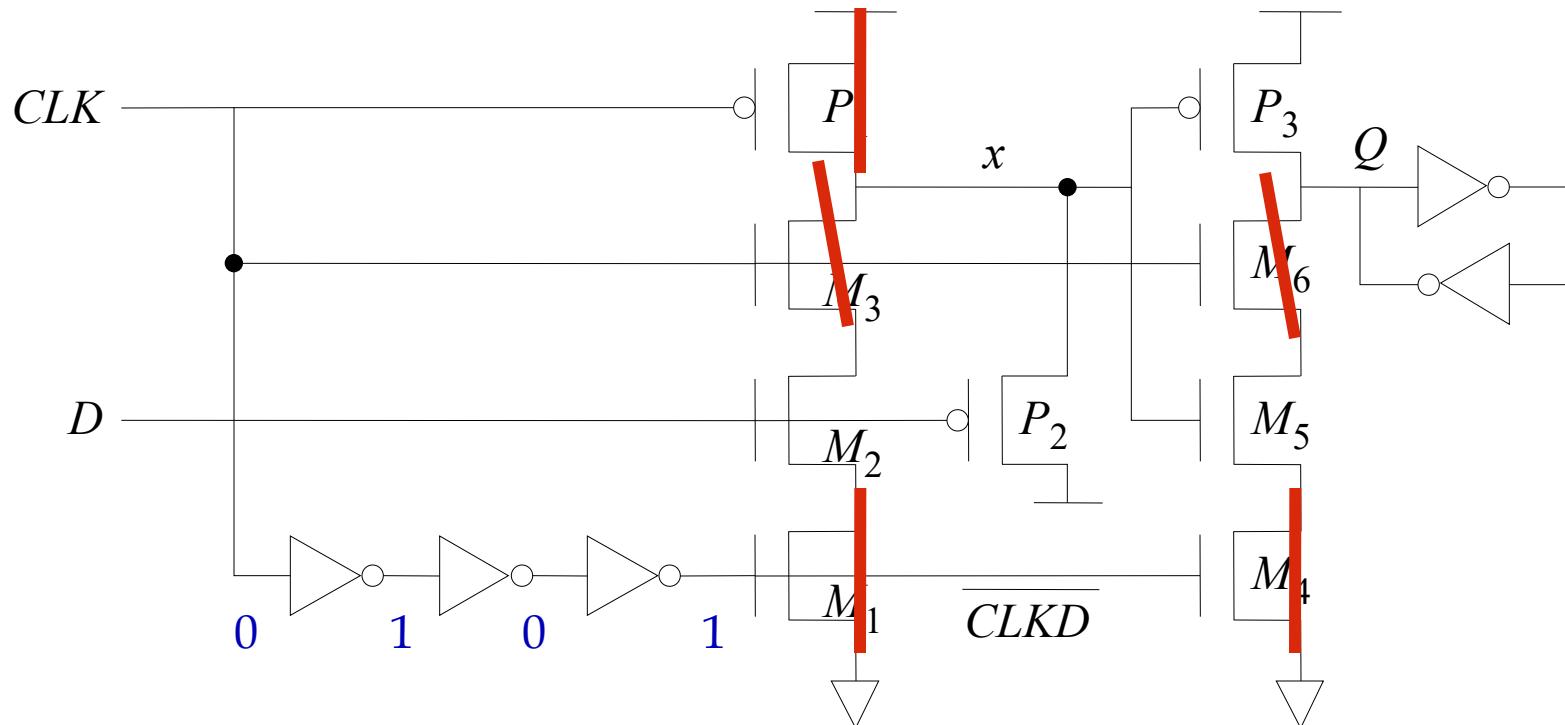
Hybrid Latch - Flip-flop (HLFF), AMD K-6 and K-7 :



**Figure 7.36** Flow-through positive edge-triggered register.

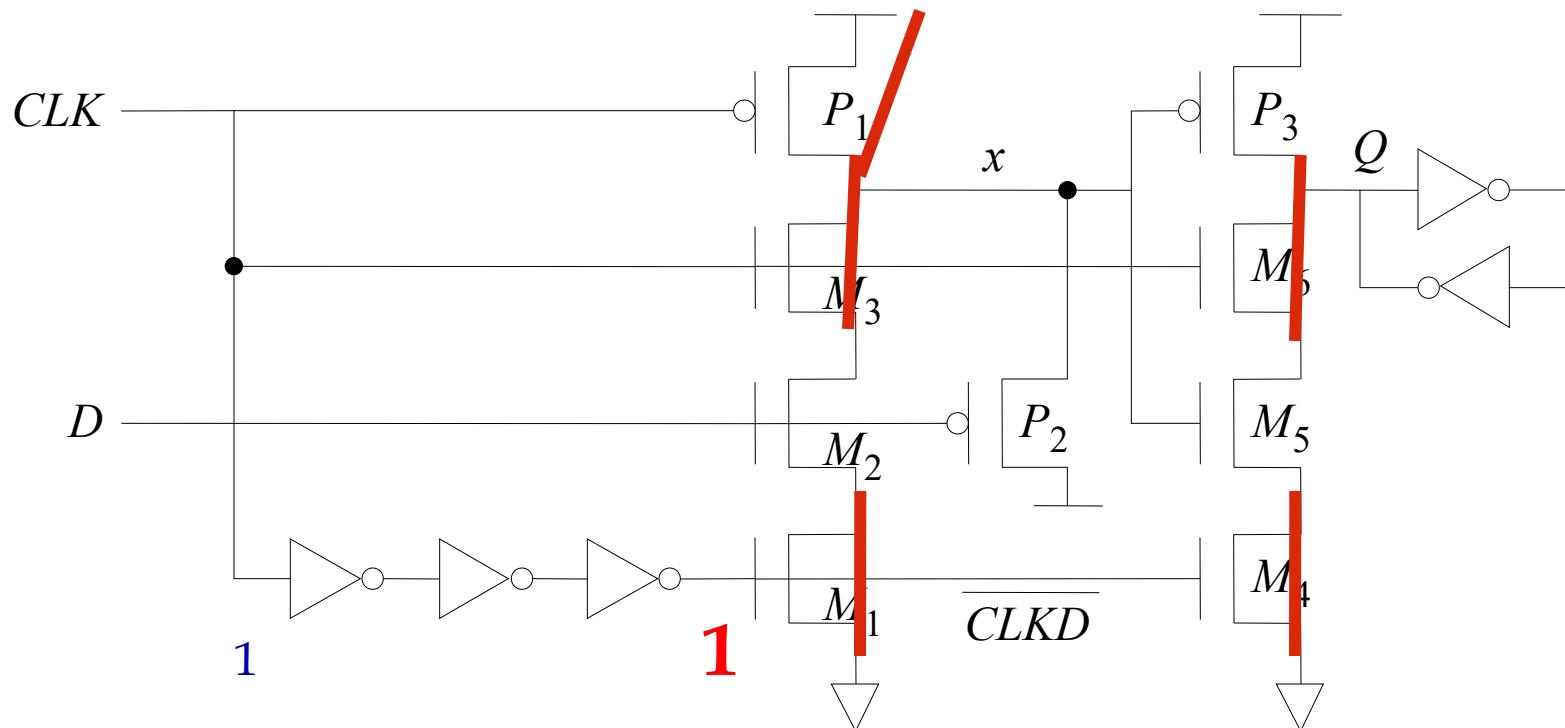
# Clock = 0

X em pré-carga 1 (notar P2, não incomoda pois se conduzir leva x a 1)  
Saída Q mantém o estado



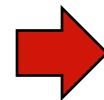
# Clock sobe por um curto tempo clk=1 e clkd=1

Se D=1 descarrega x, se d=0 x=1. Na prática P2-M2 é um inverter de D. Par P3-M5 atuam com inverter, e forçam estado de x no par de inversores

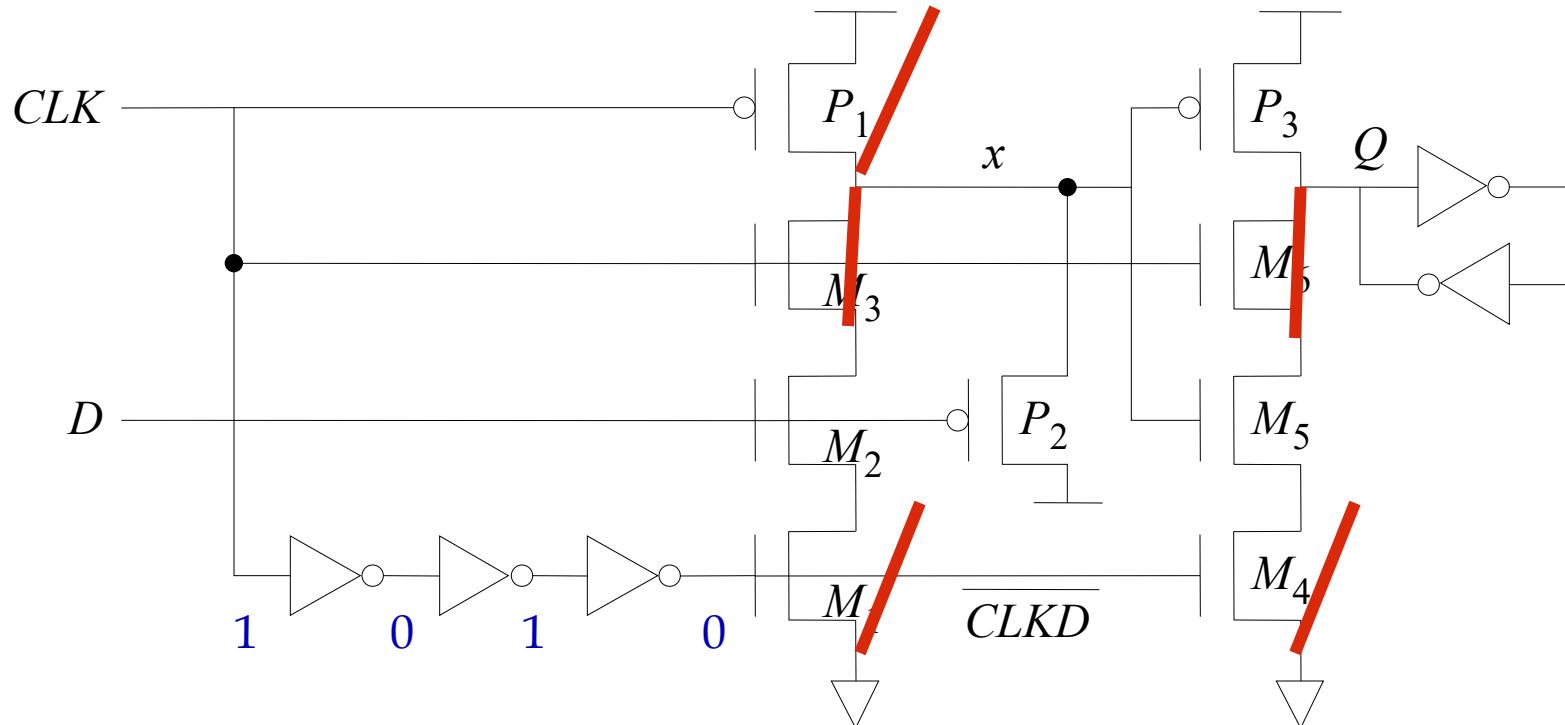


# Clock = 1

Se  $D=0$   $x \leftarrow 1$ , não faz P3 conduzir  
Se  $D=1$  não altera o estado de  $x$

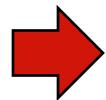


Mantém o estado

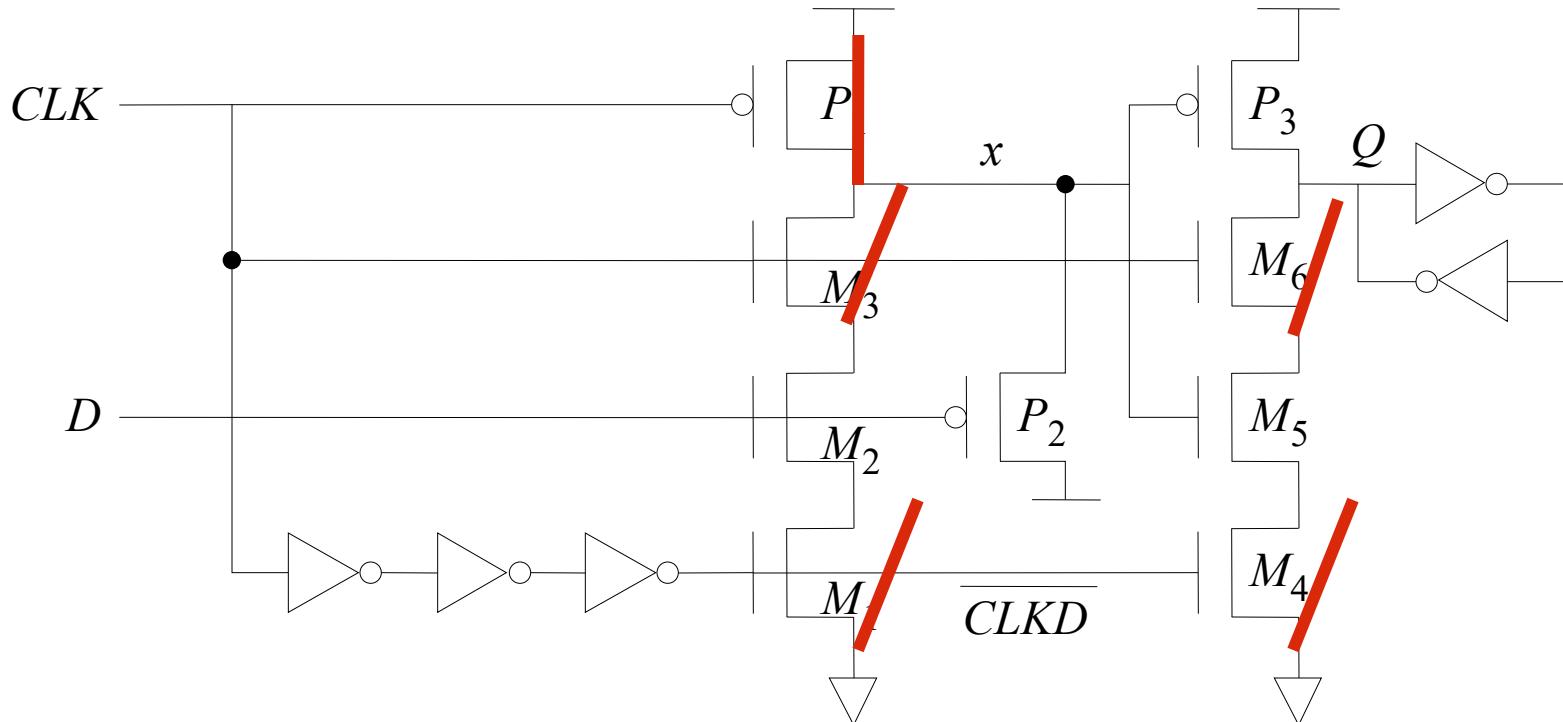


# Clock desce clk e clkd iguais a zero (glitch)

Se  $D=0$   $x \leftarrow 1$ , não faz  $P_3$  conduzir  
Se  $D=1$  não altera o estado de  $x$

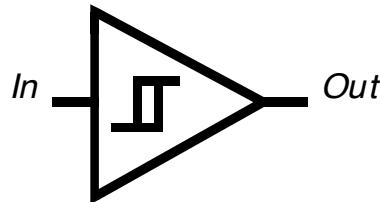


Mantém o estado

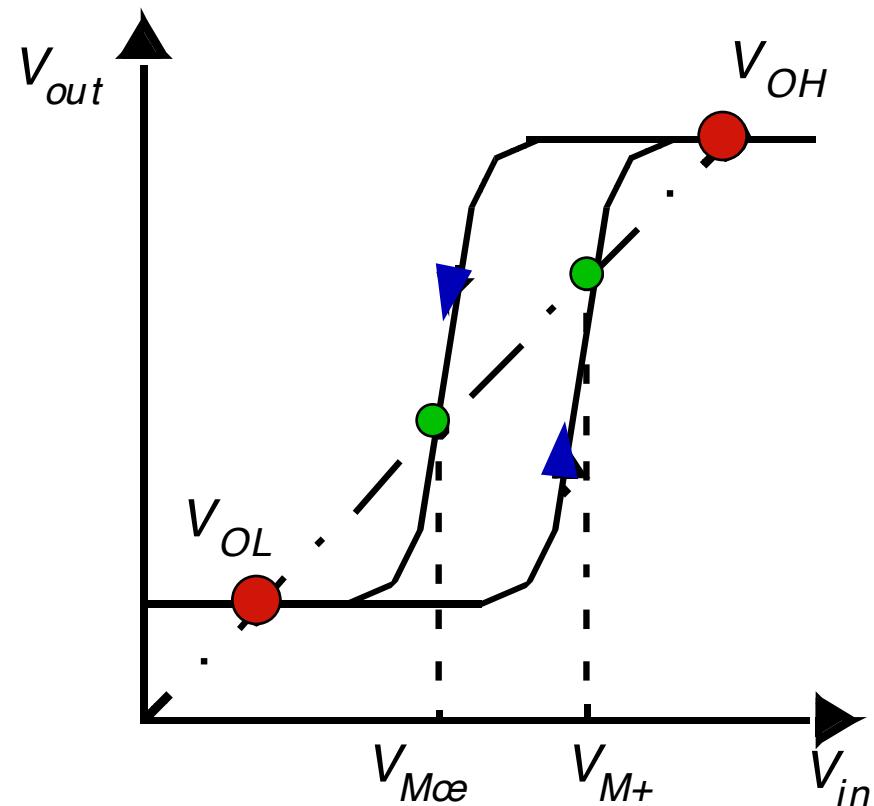


# Non-Bistable Sequential Circuits

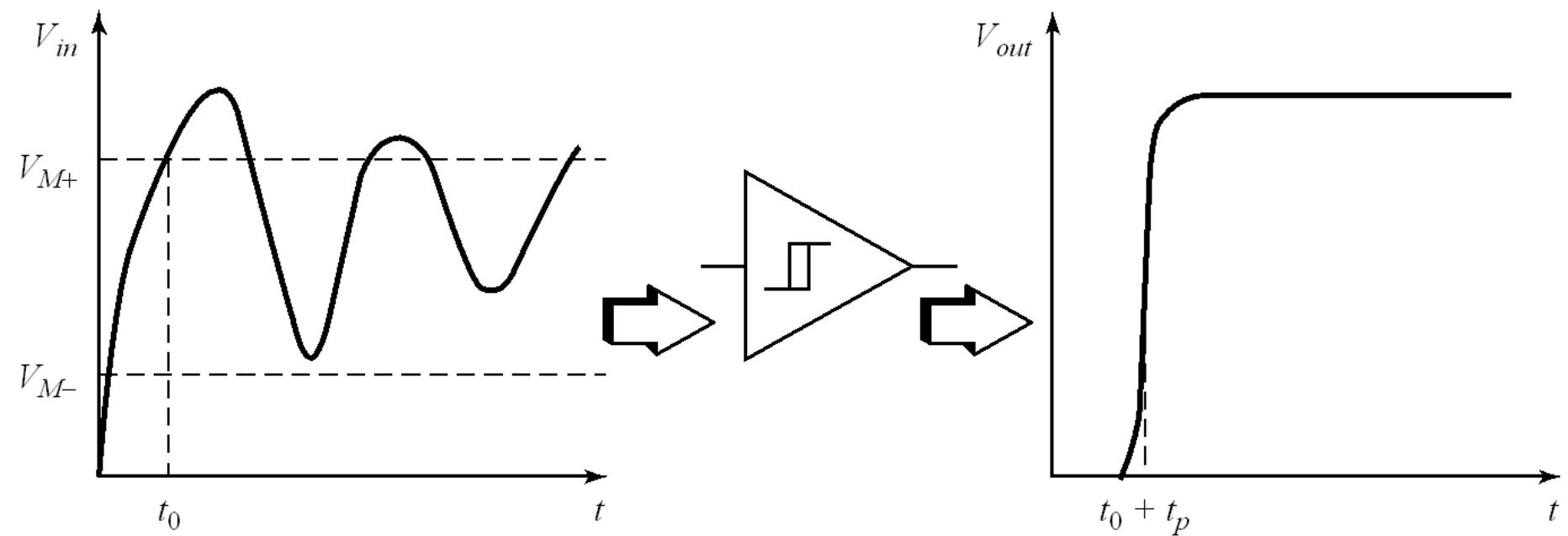
## Schmitt Trigger



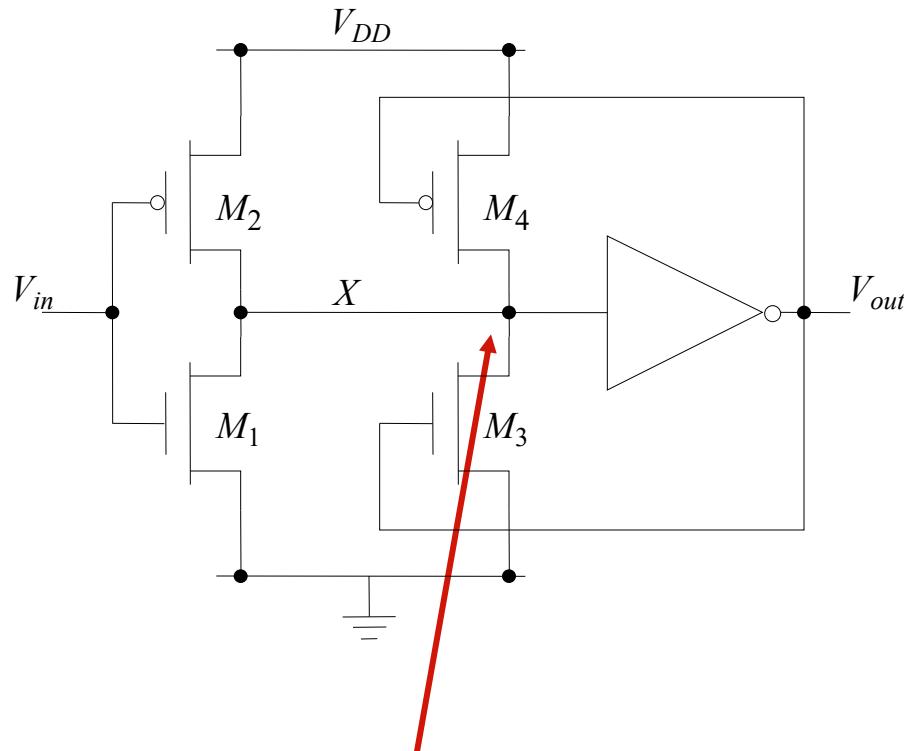
- VTC with hysteresis
- Restores signal slopes



# Noise Suppression using Schmitt Trigger



# CMOS Schmitt Trigger

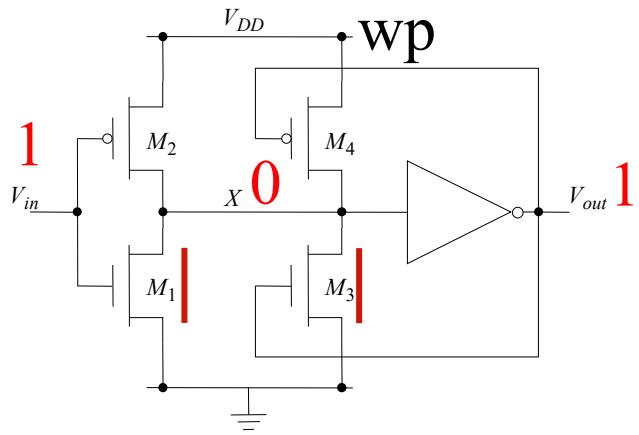
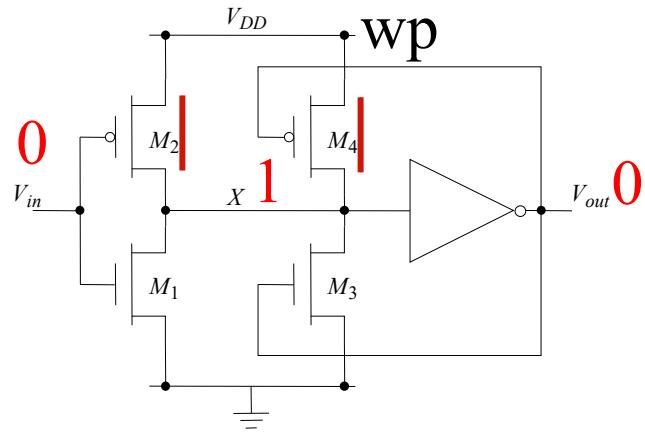


Moves switching threshold  
of the first inverter

```
.subckt inv in out vcc
MP1  out in vcc vcc pmos l=0.35U w=5.5U
MN2  out in 0 0 nmos l=0.35U w=2.0U
.ends inv

.subckt SCHMITTRIGGER in out vcc
X1 in X vcc inv
X2 X out vcc inv
MP2 X out vcc vcc pmos l=0.35U w=4U
MN2 X out 0 0 nmos l=0.35U w=2U
.ends SCHMITTRIGGER
```

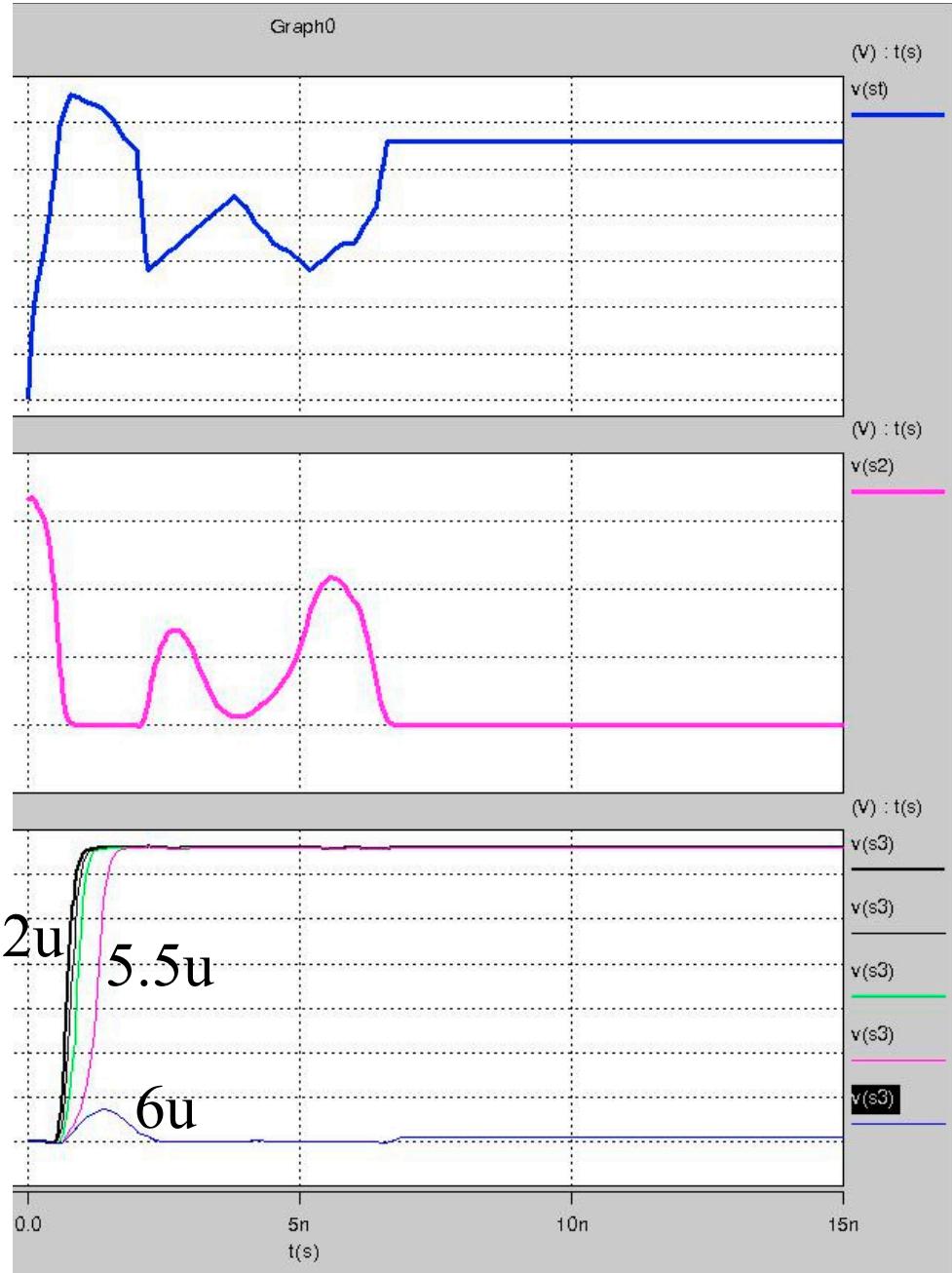
Opera de 2u a 5.5u – mais que 6  
microns muito ganho no P e fica em 0



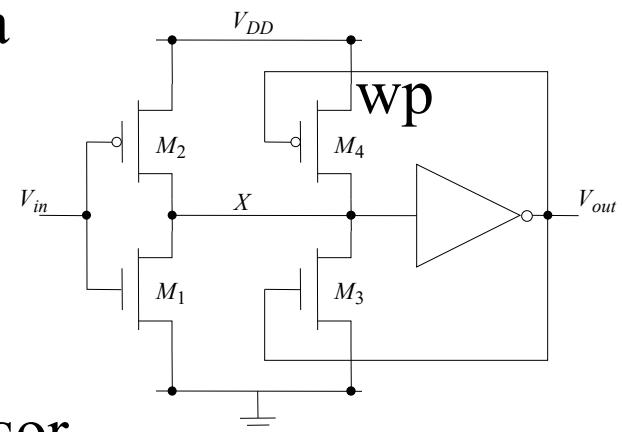
Para passar de 0 para 1:

$$W(M2) > W(M4)$$

Se ganho de M4 for maior que o ganho de M2 a saída fica presa em 0



Entrada

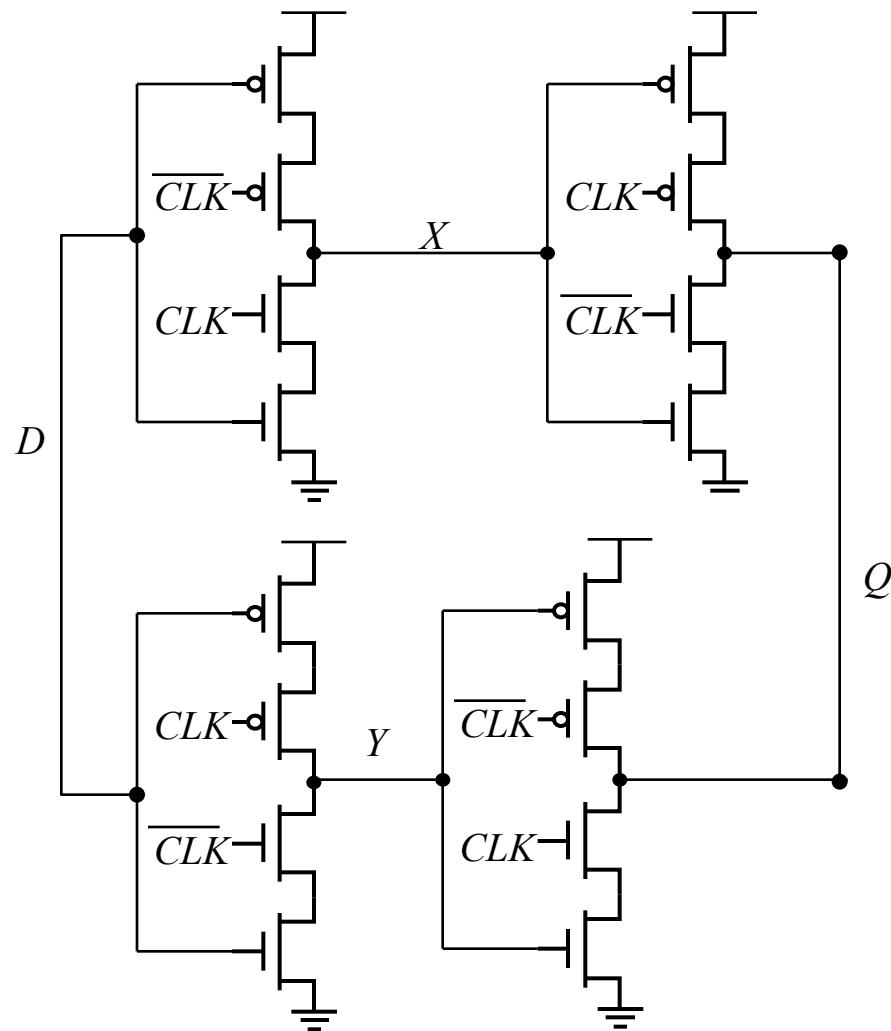


1 inversor

Schmitt Trigger  
Parâmetro que varia: wp

# Dual – edge flip flop (dinâmico)

- Dual-edge triggered storage element is an edge-sensitive element that captures the value of the input after both low-to-high and high-to-low clock transitions.

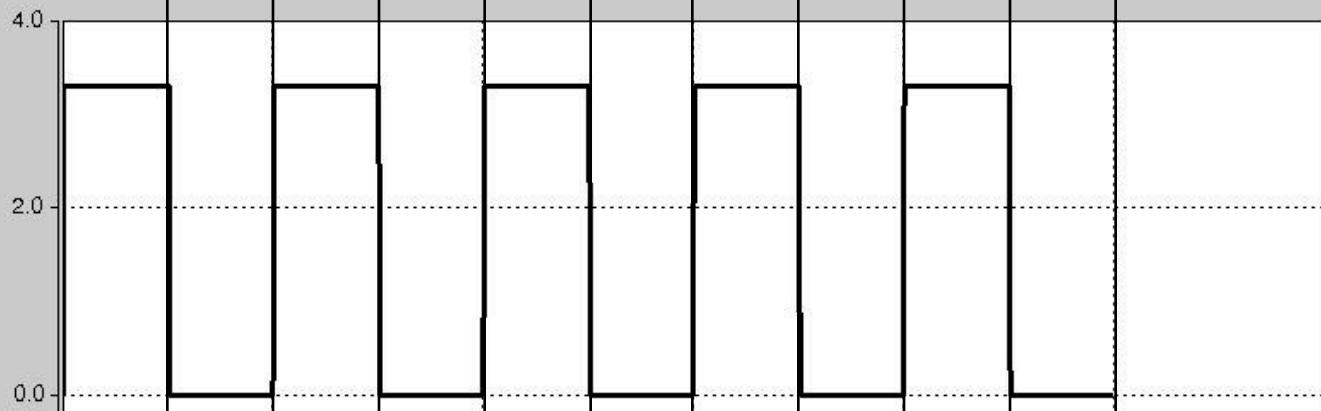


Analizar o circuito ao lado

Graph0

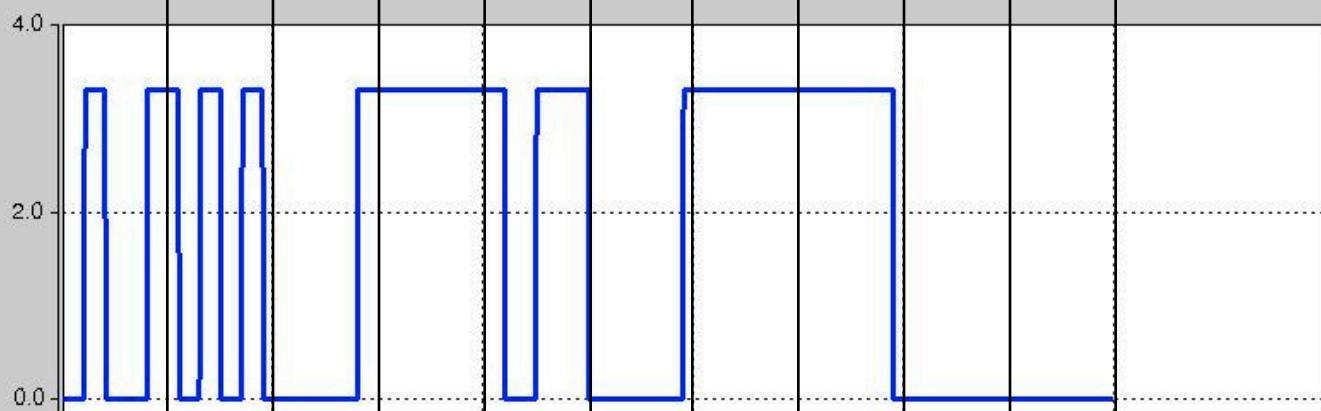
(V) : t(s)

v(clk)

 $\Sigma$ 

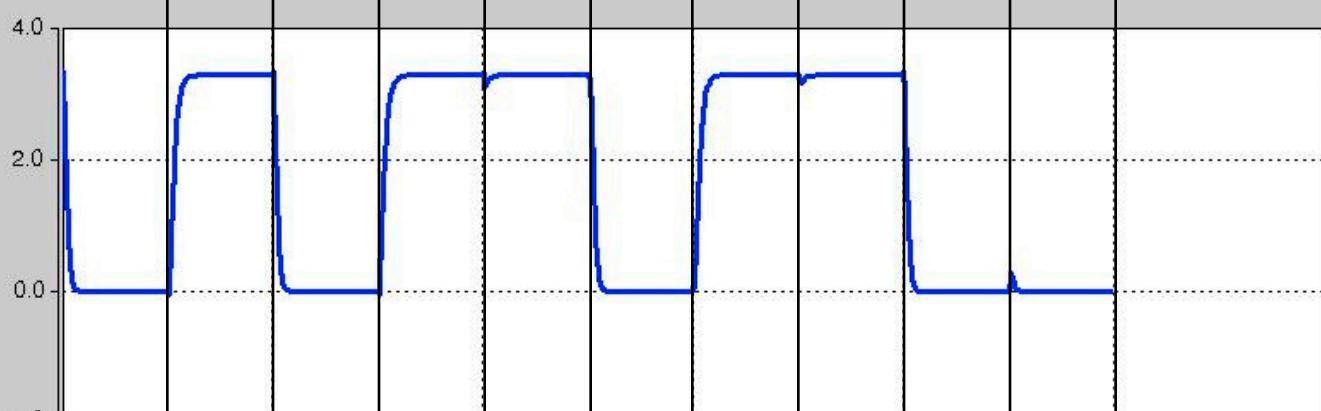
(V) : t(s)

v(d)

 $\Sigma$ 

(V) : t(s)

v(qddr)

 $\Sigma$ 

0.0

20n

40n

60n

80n

100n

120n

t(s)