Interconnection Length Estimation at Logic-Level

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Abstract

Accurate and fast interconnection length estimation of CMOS circuits during the design phase is essential to evaluate placement, routing and power estimation. The goal of this work is to estimate the average interconnection length of the nets for a given circuit at the logic level. We propose a look-up-table method, taking into account three parameters available at the logic level: number of cells, number of nets and fanout of each cell. To validate the method we use an automatic layout generator, TROPIC3, which generates the circuit layout from a SPICE netlist, reporting the net lengths after synthesis. The proposed method is compared with the values obtained after layout synthesis. The difference between estimated length and real length are lower then 10%.

Keywords *– power estimation, parasitic capacitances.*

1. Introduction

In the physical design of integrated circuits, a critical problem is related to the amount of wires required for the implementation of interconnections. Quite often, the total interconnection length is used as a measure of quality of the placement [6]. So, the knowledge and management of the interconnection length is important from several points of view:

- the amount of space required for a circuit is largely governed by the total length of wires that must be accommodated into the layout;
- time delay for signals depends on the wiring length because the wiring capacitance slows down the circuit and also because the interconnection acts as a transmission line;
- power requirements depend on the amount of load capacitance of a gate which depends on wire length.

In [7] is described a relationship between the average number of terminals T of a block for a given circuit and the average number of logic gates inside this circuit. This relationship is given by $T=t.B^p$ and it is know as the Rent's rule. The parameter t is the average number of terminals per logic gate and the exponent p is the Rent exponent. Its value depends on the complexity of the interconnect topology and on the quality of the placement. The maximal value of the Rent exponent p is 1 for a very complex topology or a random placement [2],[3],[9].

Several authors were concerned with the problem of a priori length estimation. In [4], Rent's rule has been used for length interconnection estimation. They derived upper bounds for interconnection lengths of linear and square arrays of components. In [5], the problem of determining the distribution of wire lengths is considered. In both works, the effect of placement is introduced by assuming that Rent's rule holds true at all levels of the partition hierarchy.

The interconnection estimation at the logic level is used to predict the capacitance interconnection. Therefore, it is possible to evaluate the feasible operating frequency in the critical path of the circuit at the logic level [1], [3]. This estimation can compute the number of wiring layers needed for a circuit in a given technology. Accurate routing estimation can also be used to guide layout design tools to provide improved solutions and fast power consumption estimation of CMOS circuits

This paper is organized as follows. In Section 2, we describe our method to estimate the average interconnection length. In the section 3 is presented the resultant look-up-table, which lets interconnection estimation at logic level. In Section 4, we describe the experimental results to validate the proposed method. In Section 5, we give some conclusions and some highlights of future research.

2. Interconnection Length Estimation

The interconnection length estimation starts with the layout synthesis of a set of circuits. These circuits are the MCNC'91 benchmarks (Table 1), containing only combinational logic. The gates used in these circuits are only standard logic gates: inverters, NANDs and NORs. Table 1 presents the number of logic gates, number of transistor, number of inverter, number of NANDs and number of NORs. The complexity of benchmarks, in function of the transistor number, ranges from 192 to 2690 transistors.

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Table 1 – MCNC'91 benchamrks.

Circuits Name	Number of Logic Gates	Number of Transistors	Number of Inverter	Number of NAND	Number of NOR
cmb_a	48	192	18	18	12
parity_a	75	240	30	45	0
pcler8_a	127	412	58	35	34
frg1_a	151	536	64	37	50
count_a	174	602	79	33	62
comp_a	224	656	78	87	59
5xp1	299	798	199	54	46
C432a	259	902	102	85	72
9sym	409	1092	272	70	67
9sym_3x3	339	1156	100	124	115
bw	468	1256	308	94	66
C880a	474	1552	154	158	162
alu2_a	469	1712	184	130	155
C499a	605	2038	223	238	144
x4_a	545	2160	224	156	165
c1355	604	2244	130	472	2
C1908a	728	2690	204	291	233

The layout of each benchmark is generated using the layout synthesis tool TROPIC3 [8]. TROPIC3 is a *macro-cell generator*, i.e., the complete circuit is generated. The main features of the layout style are:

- linear-matrix layout style, each cell row is composed by two horizontal diffusion strips, the width of the transistors are orthogonal to the diffusion strips;
- the routing is implemented with 3 metal layers and stacked contacts, reducing the routing area;
- no layout compaction is used;
- complete parasitic capacitance/resistance evaluation after layout synthesis;
- simple technology file to describe design rules (28 rules) and parasitic capacitances/ resitances (26 rules).

The layouts are generated for a 0.25 μm technology, having 3 metal layers for interconnections. To obtain accurate length estimation it is important to generate the circuit optimizing the routing. If the circuit is wider then higher the horizontal routing dominates, resulting in very long nets. The same for circuits higher than wider. So, it is important to generate circuits with a square shape. This is obtained by selecting the number of rows before layout synthesis.

After layout synthesis, a report is generated, given for each net its length (in microns) and the fanout of the driver. All nets having the same fanout are grouped, and the average length for a given fanout is calculated. As we show after, the fanout is directly related to the net length. It corresponds to the number of terminals that must be connected in the circuit. In our work we considered nets having fanout from 0 to 6 and bigger than 6 (>6). Fanout equal to zero corresponds to cells with no driver, being the primary outputs. Table 2 and Figure 1 present the average interconnection length for nets with fanout 0 to 2.

Table 2 – Average interconnection length of the nets with fanout 0, 1 and 2

Circuit Name	Number of Transistors	fanout 0	fanout 1	fanout 2
cmb_a	192	26,9	33,0	50,6
parity_a	240	17,2	28,5	51,9
pcler8_a	412	35,5	33,1	47,2
frg1_a	536	17,2	36,0	51,9
count_a	602	26,7	41,1	41,5
comp_a	656	16,6	35,4	57,9
5xp1	798	17,2	31,5	52,8
C432a	902	22,2	38,3	75,1
9sym	1092	32,3	34,6	56,3
9sym_3x3	1156	18,1	45,8	91,6
bw	1256	25,3	33,5	57,3
C880a	1552	48,5	43,2	69,9
alu2_a	1712	21,4	42,0	66,8
C499a	2038	63,1	37,9	75,9
x4_a	2160	13,6	39,1	60,4
c1355	2244	81,4	37,0	70,3
C1908a	2690	71,7	43,2	88,6

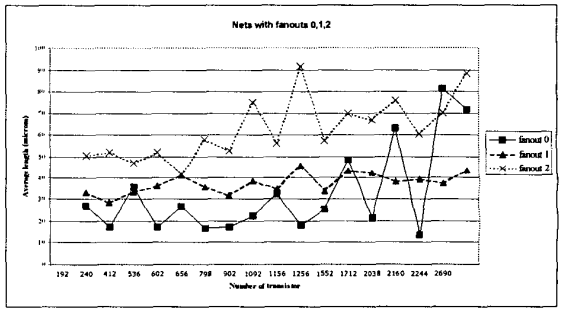

Figure 1 – Number of transistor versus average length (nets with fanout 0, 1, 2)

From Table 1 and Figure 1, we observe:

- nets with fanout equal to zero presents an irregular length distribution (20 to 80 μm), not correlated to the transistor number. The length of these nets is a function of the position of the primary outputs in the circuit boundary;
- the average length of nets with fanout equal the 1 varies between 30μm and 40 μm, practically independent from the number of transistor. This is an **important** observation, since the nets with fanout=1 corresponds to the majority part of nets in all benchmarks (and real circuits). As shown in Table 5, at least 75% of nets have fanout 1. So, for this technology, we can use this value as an accurate length prediction for nets with fanout 1.
- the nets with fanout equal to 2 have an average length between 40μm and 80 μm. In this case the net length

is a function of the fanout and the number of transistors.

Table 3 and Figure 2 present the average interconnection length for nets with fanout 3 to 5. We observe that the net length increases when fanout increases. The obtained average lengths are:

- fanout 3: net length between 50μm and 125μm;
- fanout 4: net length between 100μm and 150μm;
- fanout 5: net length between 100μm and 250μm.

Table 3 – Average interconnection length of the nets with fanouts 3, 4 and 5

Circuit Name	Number of Transistors	fanout 3	fanout 4	fanout 5
cmb_a	192			
parity_a	240			
pcler8_a	412	65,3		
frg1_a	536			
count_a	602	58,7		
comp_a	656	54,4	81	
5xp1	798	86,9	148	151,4
C432a	902	87,2	140	245,8
9sym	1092	123,4	122	160,8
9sym_3x3	1156	123,4	172	194,2
bw	1256	72,7	146	249
C880a	1552	128,5	108	147,6
alu2_a	1712	101,5	154	141,7
C499a	2038	69,9	123	148,6
x4_a	2160	72,8	160	143,1
c1355	2244		117	
C1908a	2690	110,2	122	122,5

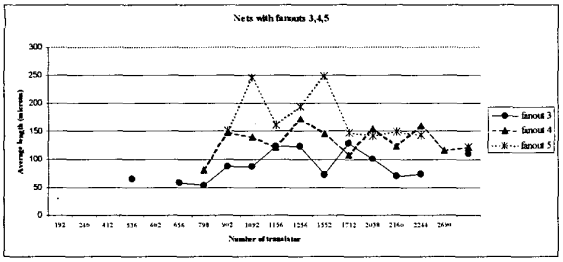

Figure 2 – Number of transistor versus average length (nets with fanout 3, 4, 5)

Table 4 and Figure 3 present the average interconnection length for nets with fanout 6 and bigger than 6. Now, we can see nets having length greater than 500 microns.

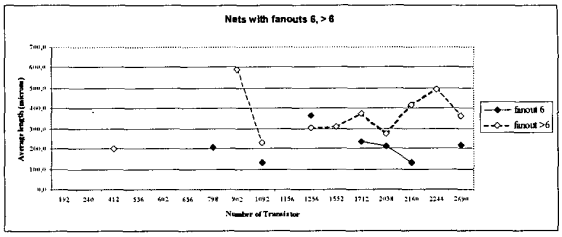

Figure 3 – Transistor number x average length nets fanout equal or bigger than 6.

Table 4 – Average interconnection length of the nets with fanouts 6 and > 6

Circuit Name	Number of Transistors	fanout 6	fanout >6
cmb_a	192		
parity_a	240		
pcler8_a	412		200,1
frg1_a	536		
count_a	602		
comp_a	656		
5xp1	798	205,8	
C432a	902		589,3
9sym	1092	131,2	227,2
9sym_3x3	1156		
bw	1256	362,5	306,3
C880a	1552		312,4
alu2_a	1712	235,1	373,5
C499a	2038	210,2	275,6
x4_a	2160	131,7	415,2
c1355	2244		492,8
C1908a	2690	215,3	360,8

Table 5 presents the distribution of the fanout for each benchmark. Fanout 1 (resulting in nets with quite homogeneous length) and fanout 2 corresponds to, at least, 85% of the nets. Nets with higher fanout values are typically less then 5% of the total number of nets. As shown, higher fanout corresponds to longer nets, being also more difficult to predict accurately its length. Consequently, during the logic synthesis it must be avoided these of nets in the critical path of the circuits. Simple strategies, as buffer insertion, can be used.

Table 5 – Fanout distribution

Circuits	% nets fanout 0	% nets fanout 1	% nets fanout 2	% nets fanout 3	% nets fanout 4	% nets fanout 5	% nets fanout 6	% nets fanout >6
cmb_a	8,33	87,50	4,17					
parity_a	1,33	80,00	18,67					
pcler8_a	13,39	79,53	0,79	4,72				1,57
frg1_a	1,99	95,36	2,65					
count_a	9,20	73,56	9,20	8,05				
comp_a	0,51	79,80	15,66	2,02	2,02			
5xp1	0,33	90,64	3,34	3,01	1,00	1,00	0,67	
C432a	1,67	73,33	21,67	0,83	0,83	0,42		1,25
9sym	0,24	92,42	2,20	1,47	0,98	1,47	0,49	0,73
9sym_3x3	0,29	74,93	4,72	5,60	5,60	8,85		
bw	4,05	85,07	3,84	1,71	2,35	1,28	0,43	1,28
C880a	5,91	74,94	10,17	4,49	2,36	1,42		0,71
alu2_a	1,07	82,52	4,05	4,90	2,99	1,07	1,07	2,35
C499a	5,29	67,11	22,31	0,83	2,15	0,33	0,66	1,32
x4_a	12,09	82,42	1,28	0,37	0,55	0,37	0,55	2,38
c1355	5,30	57,28	33,11		2,98			1,32
C1908a	3,43	72,12	16,35	2,06	3,16	0,14	0,27	2,47

3. Look-up-table for length estimation

Combining the Tables presented in Section 2 we can construct a look-up table having as entry points the number of transistors (or number of cells) and the net fanout. Using the Table 6, we can estimate the length of each net at the logic level, **without** layout synthesis. For example, if a given net in a given benchmark with 2000 transistors have fanout 5, looking the third row and the sixth column we obtain as average length of 175 microns (best case 150, worst case 200, average case 175).

Table 6 – Look-up-table for length estimation

Transis Number.	Fanout 0	Fanout 1	Fanout 2	Fanout 3	Fanout 4	Fanout 5	Fanout 6	Fanout >6
0-800	20-40	30-40	40-60	60-80	80	150	200	100
801-1700	20-40	35-45	60-80	81-120	120-160	150-200	200	200
1701-2500	20-80	40	60-80	81-120	120-160	150-200	200	300-500
2500-3000	70-80	40	80	81-120	120-160	150-200	200	300-500

This Table was obtained for a 0.25 µm technology, using the TROPIC3 layout generator. If the process or the layout synthesis changes, the Table must be generated for the new parameters. Our main contribution in this work is to show that we can accurately predict wire length, at the logic level, using simple data, as fanout and number of transistors (or cells).

4. Experimental Results

The look-up table presented in the previous Section is now used to predict wire length. Table 7 presents compares the total average length obtained **after** layout synthesis, using TROPIC, and the total average length obtained at the **logic level**, using the look-up table obtained in Section 3. We use the average values of the look-up table - (best case + worst case)/2.

Excepting the *9sym_3x3* benchmark (14,65% of nets with fanout greater than 3) the average error is around 8,87%. This shows that the method is accurate, being possible to predict net lengths at the logic level, and consequently the parasitic capacitances associated to the routing. Prediction routing length at this level save CPU time, since the layout synthesis is not executed.

Table 7 – Total average length obtained from layout synthesis and the look-up-table.

Circuit Name	Number of Transistors	TROPIC3	Proposed Method	Error %
cmb_a	192	40,78	35,32	-15,45
parity_a	240	33,31	37,73	13,26
pcler8_a	412	42,37	38,14	-11,1
count_a	602	47,46	40,8	-17,41
comp_a	656	41,92	40,42	-3,71
5xp1	798	40,88	41,38	1,22
C432a	902	56,23	50,56	-11,21
9sym	1092	43,67	45,13	3,34
9sym_3x3	1156	70,9	58,11	22
bw	1256	46,77	49,09	4,96
C880a	1552	60,45	52,32	-15,53
alu2_a	1712	69,59	68,51	-1,57
C499a	2038	58,56	61,1	4,33
x4_a	2160	57,54	59,12	2,74
c1355	2244	63,59	60,15	-5,71
C1908a	2690	68,35	73,61	7,69

5. Conclusion and Future Work

We presented in this paper a method to estimate interconnect length at logic level using a look-up-table strategy. The net fanout and the number of transistors are the entry points for look-up-table. The average interconnect length allows power, routing and capacitance estimation.

The results of experimental application to standard logic gates validated the proposed procedure. It was done a comparison between circuits from MCNC'91 benchmark, in comparison with TROPIC3. The average error is in turn 10%. The next step of this research will consist in capacitance interconnect and power estimation.

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