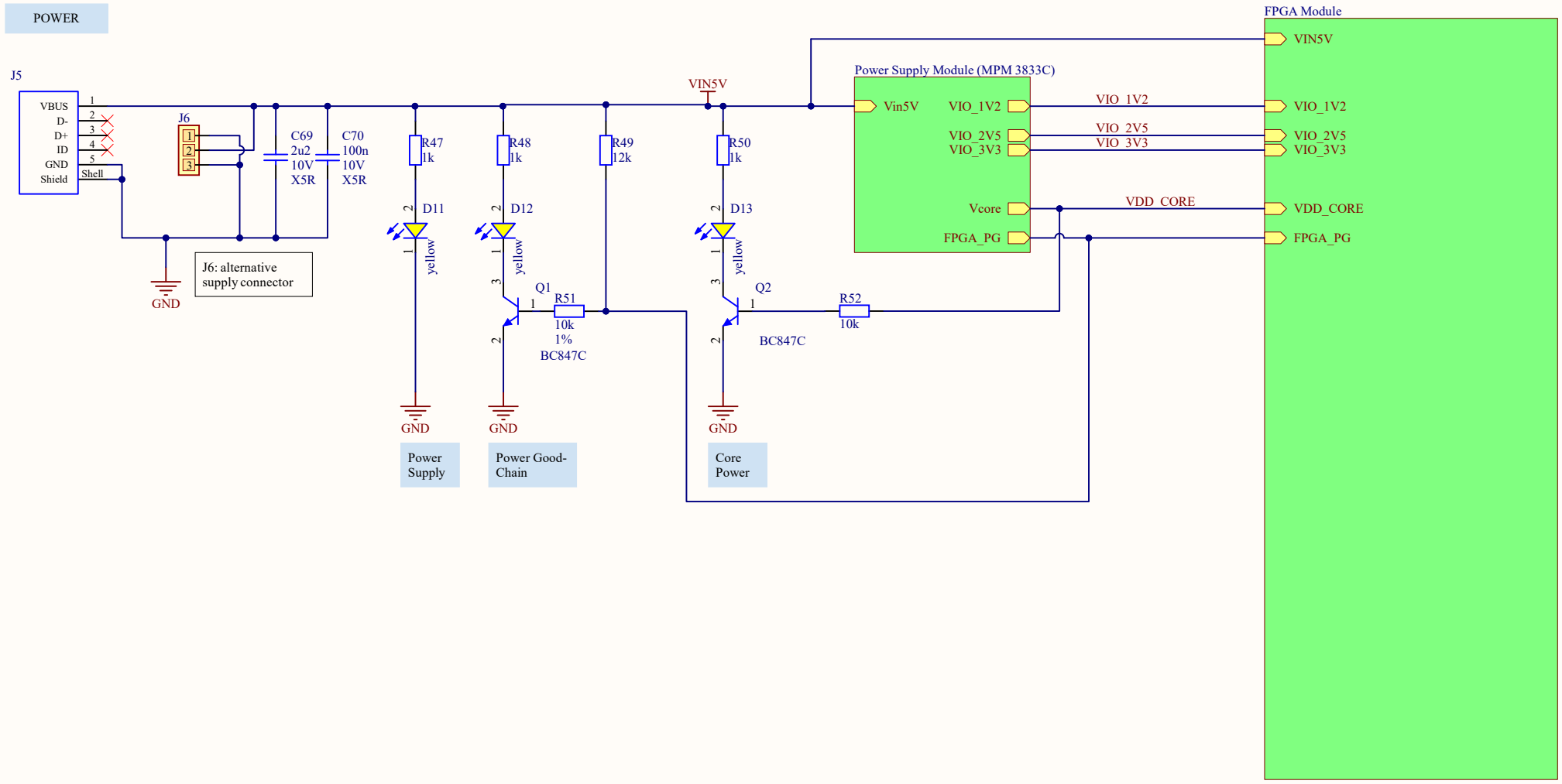

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	Top Level Sheet				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 1 of 21	
File:	GateMate1_CamBoard_1.SchDoc				

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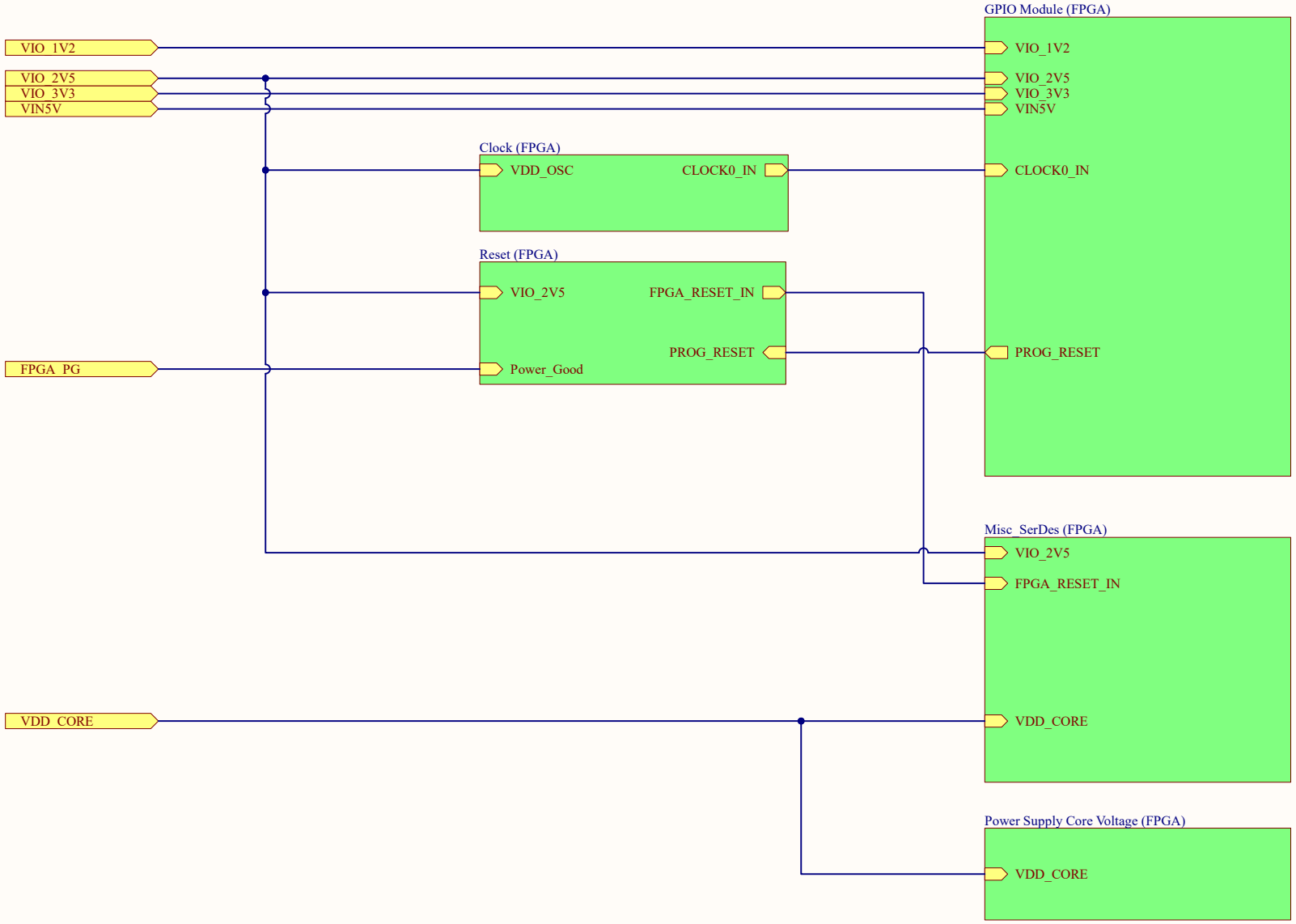

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	FPGA Module				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 2	of 21
File:	FPGA.SchDoc				

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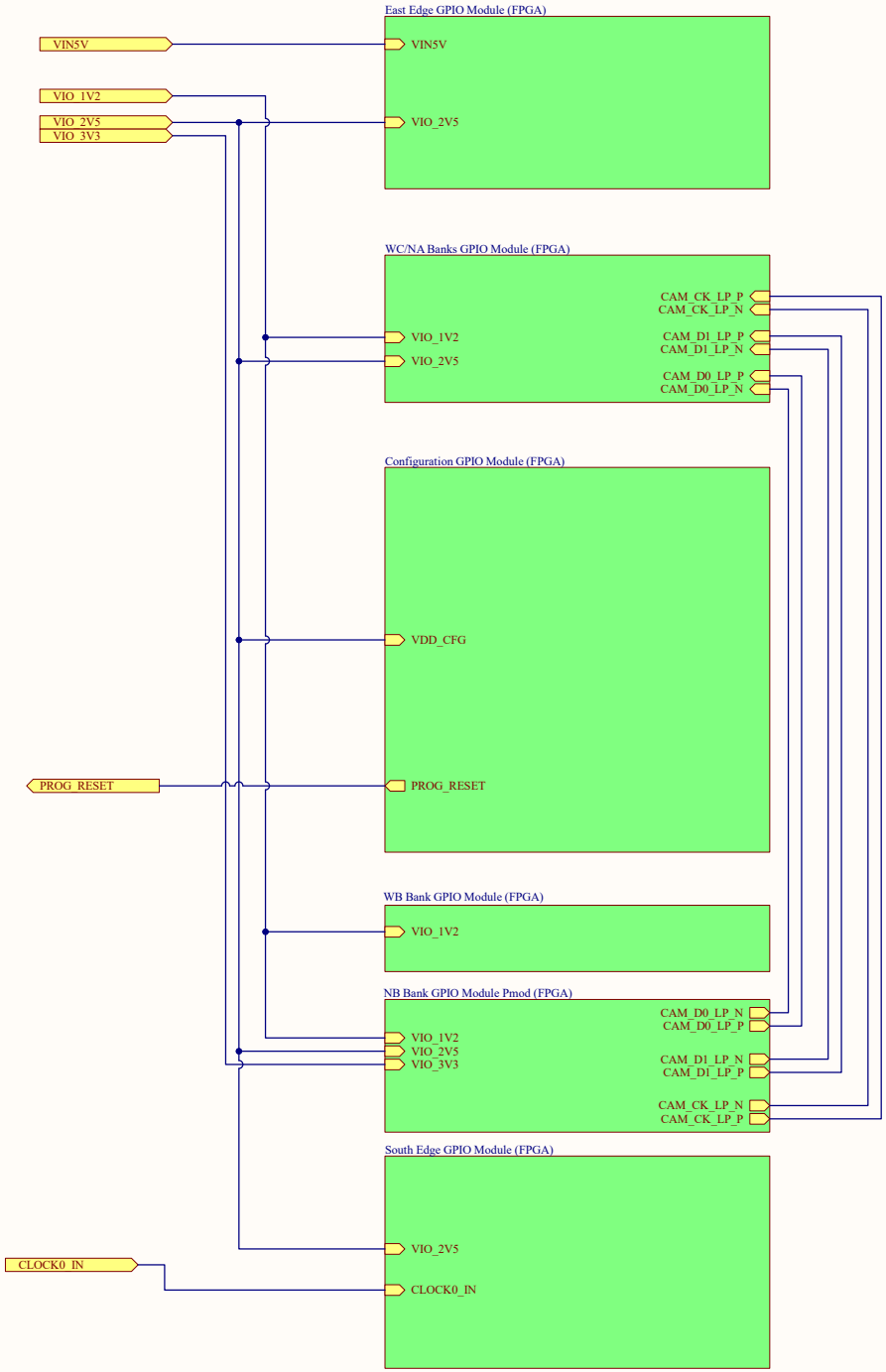

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	GPIO Module (FPGA)				
Size:	A3	Author: CCAG	Date: 26.07.2024	Sheet 3 of 21	
File:	FPGA_GPIO.SchDoc				

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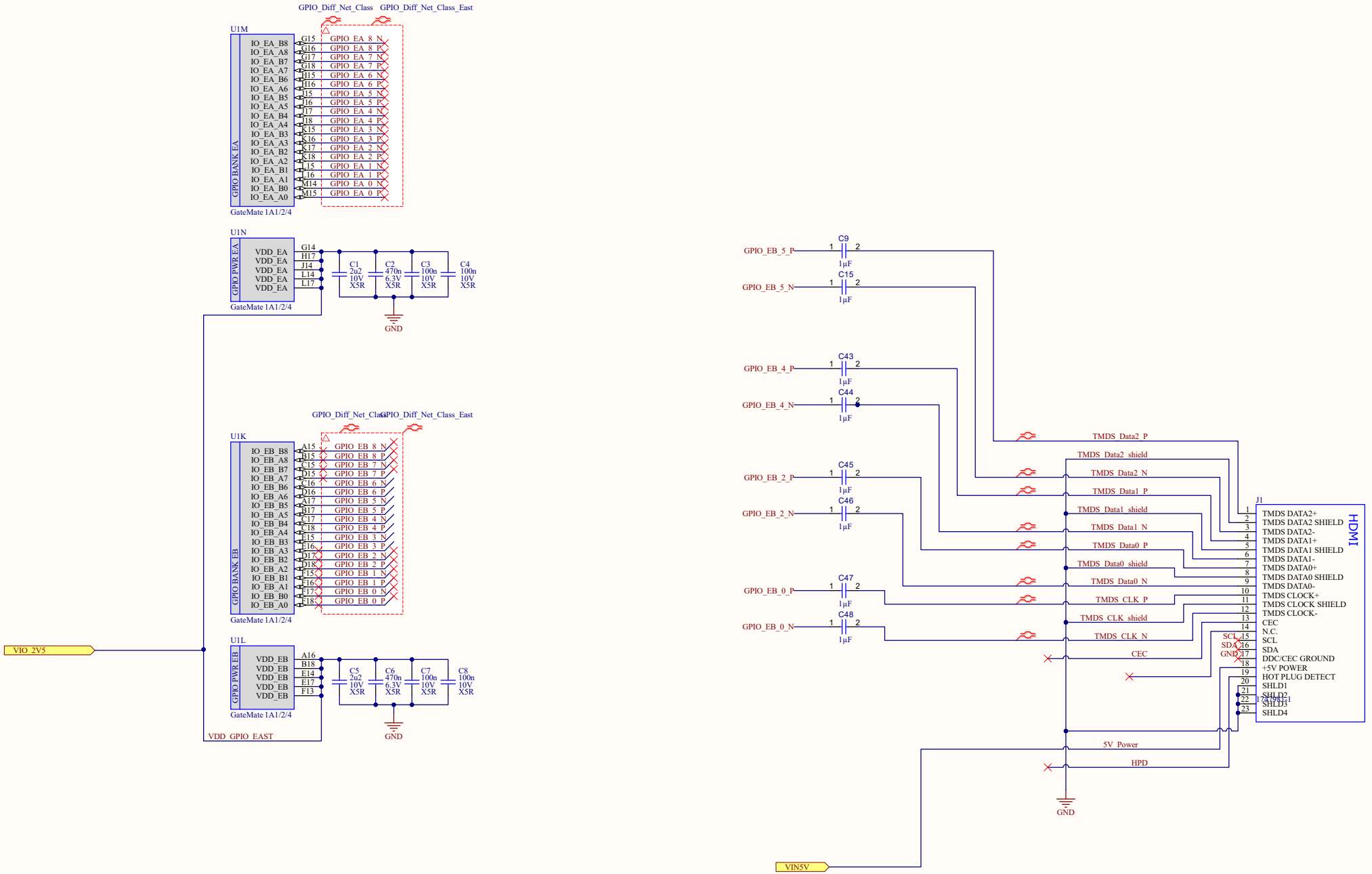

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	East Edge GPIO Module (FPGA)				
Size:	A3	Author: CCAG	Date: 26.07.2024	Sheet 4 of 21	
File:	FPGA_GPIO_East.SchDoc				

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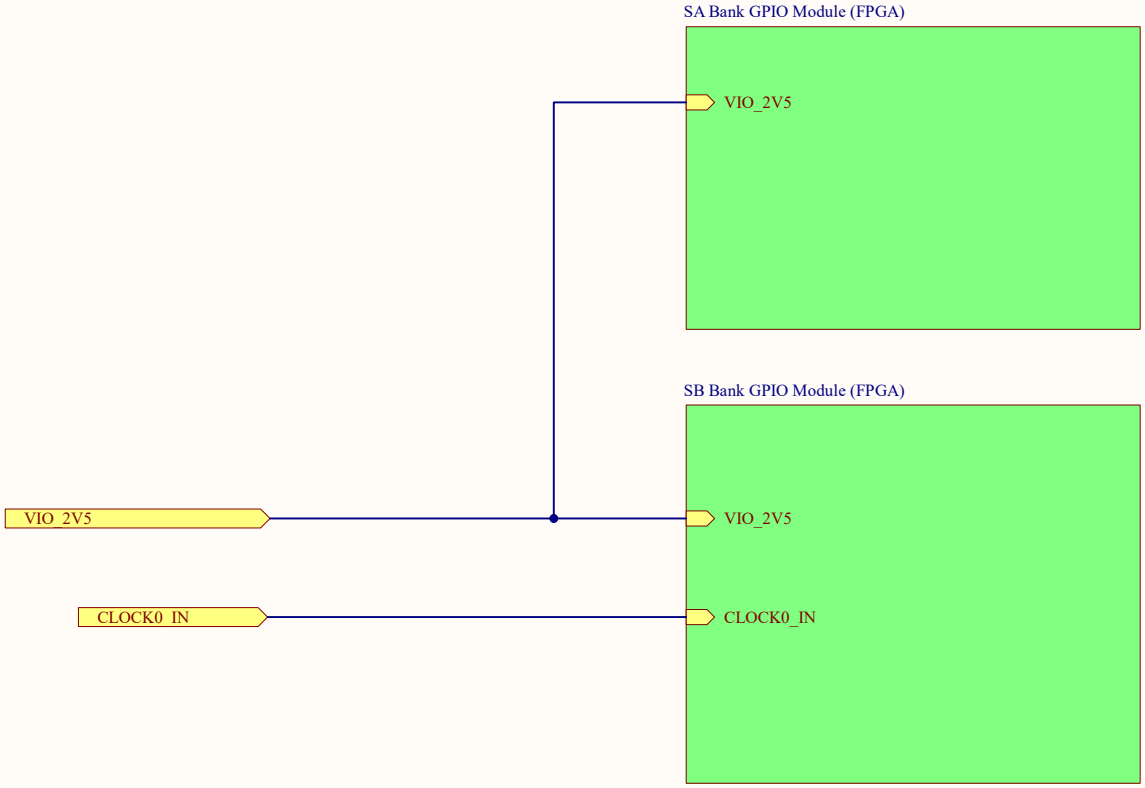

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	South Edge GPIO Module (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 5	of 21
File:	FPGA_GPIO_South.SchDoc				

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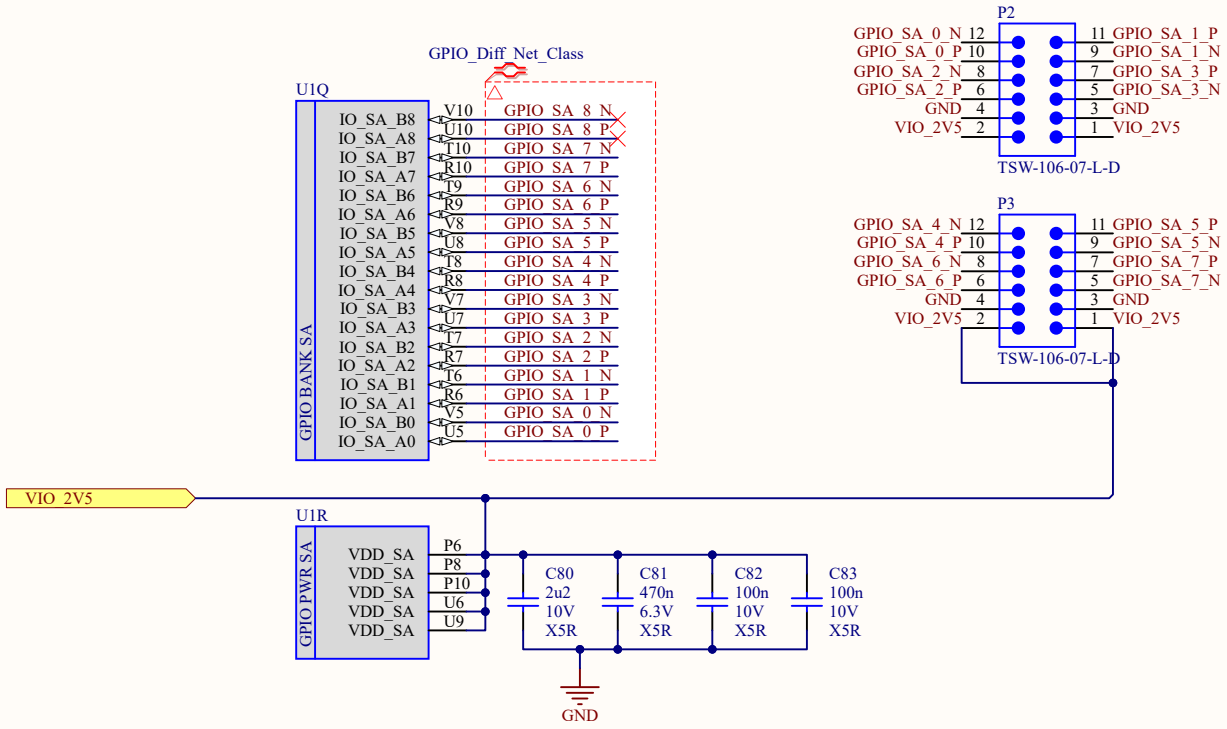

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	SA Bank GPIO Module (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 6	of 21
File:	FPGA_GPIO_SA.SchDoc				

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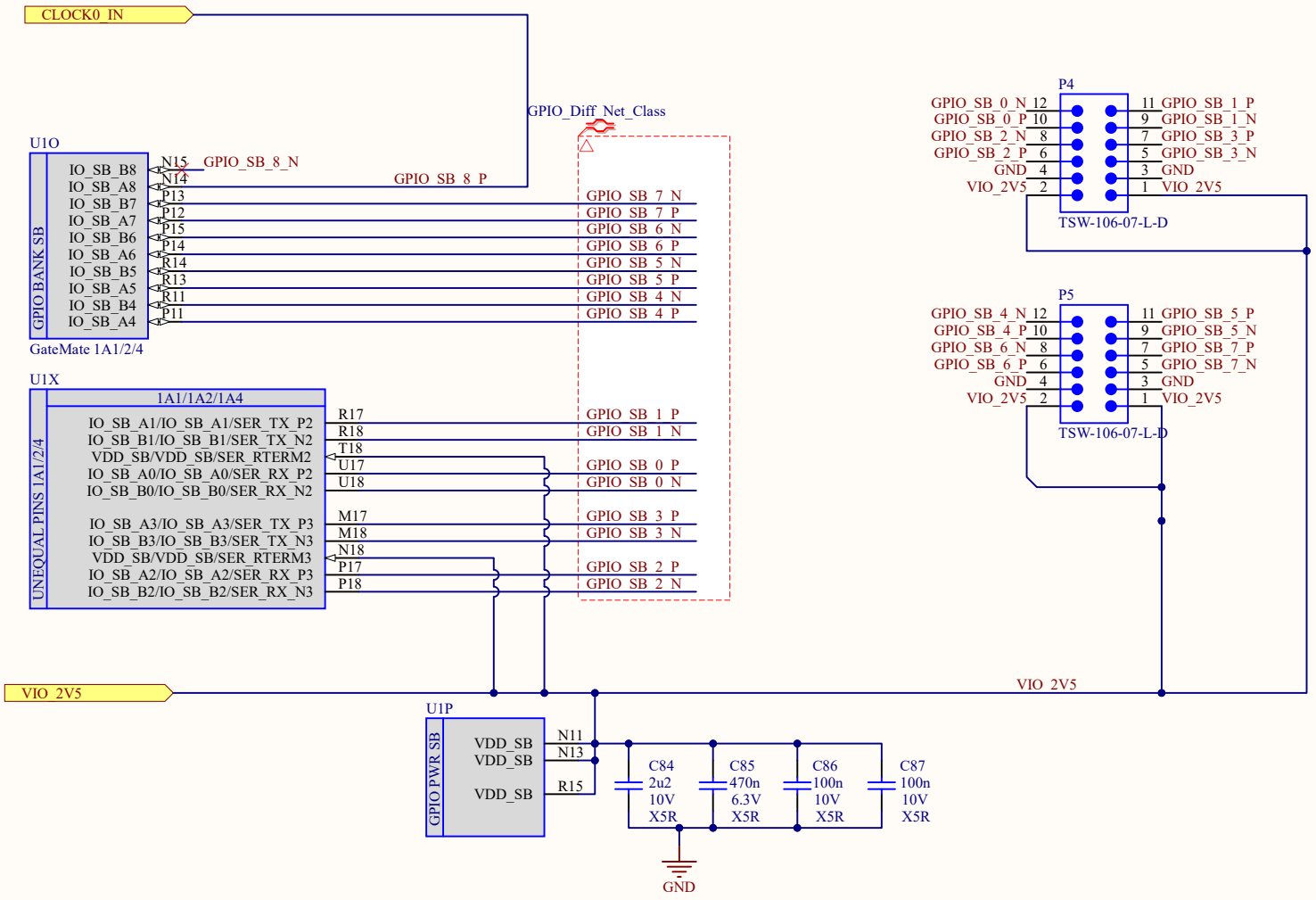

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	SB Bank GPIO Module (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 7	of 21
File:	FPGA_GPIO_SB.SchDoc				

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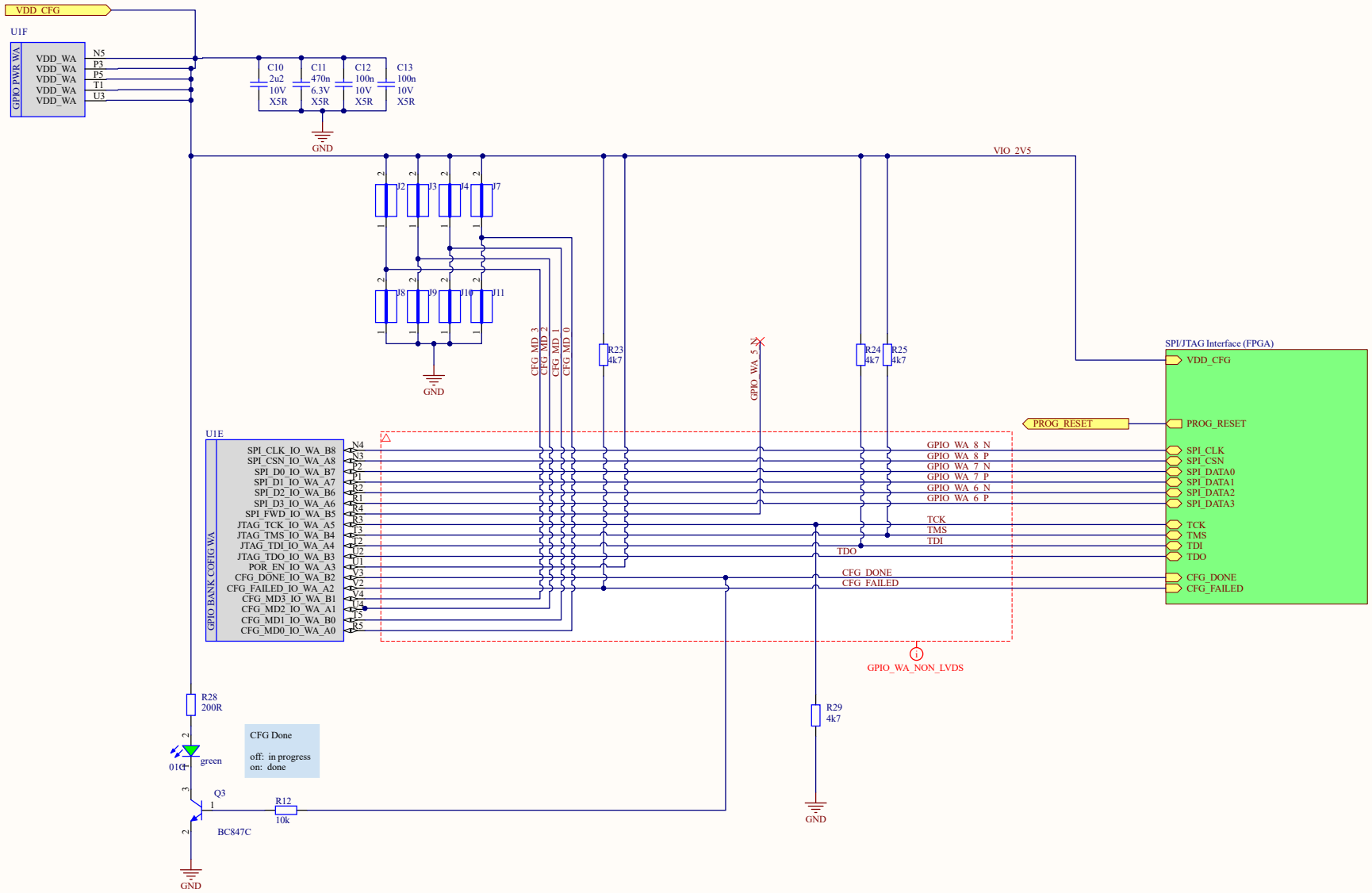

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	Configuration GPIO Module (FPGA)				
Size:	A3	Author: CCAG	Date: 26.07.2024	Sheet 8 of 21	
File:	FPGA_GPIO_Config.SchDoc				

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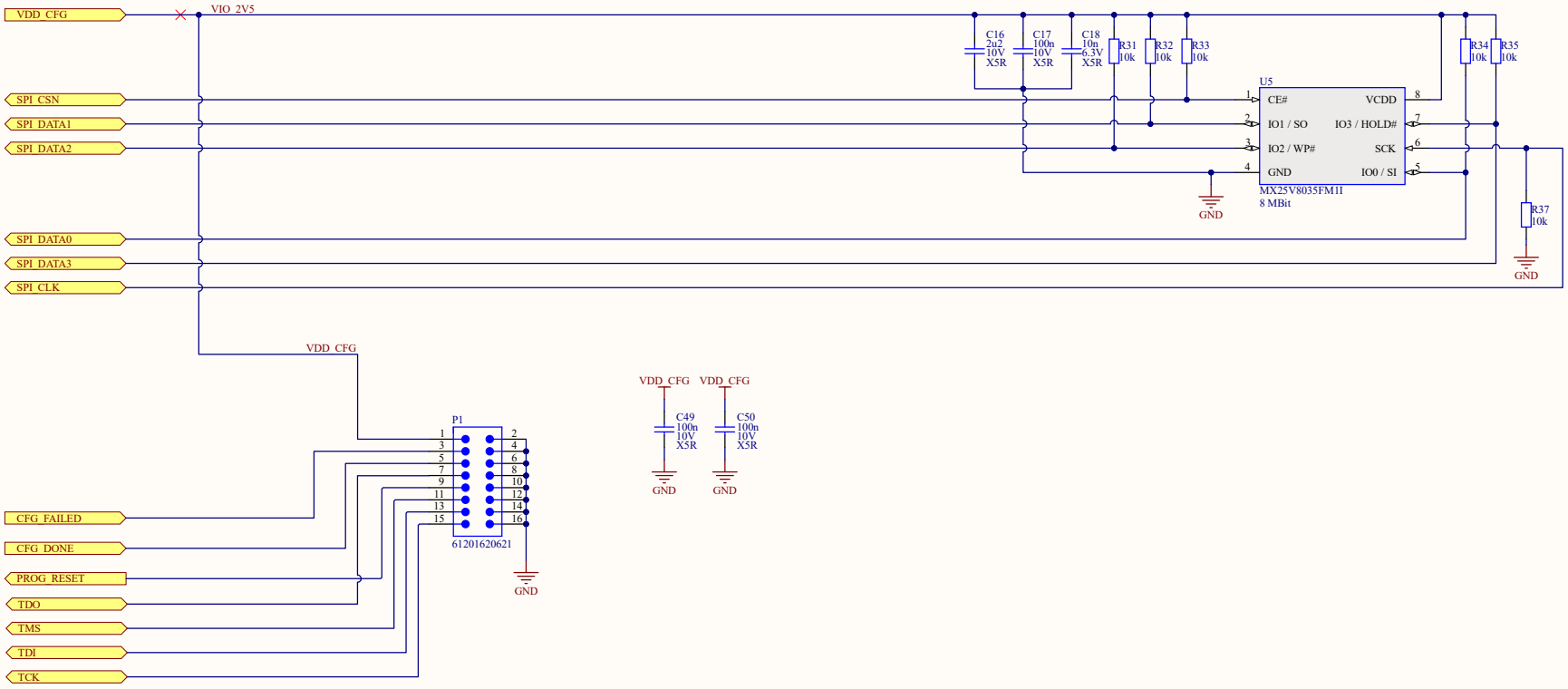

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	SPI/JTAG Interface (FPGA)				
Size:	A3	Author: CCAG	Date: 26.07.2024	Sheet 9	of 21
File:	FPGA_SPI_JTAG.SchDoc				

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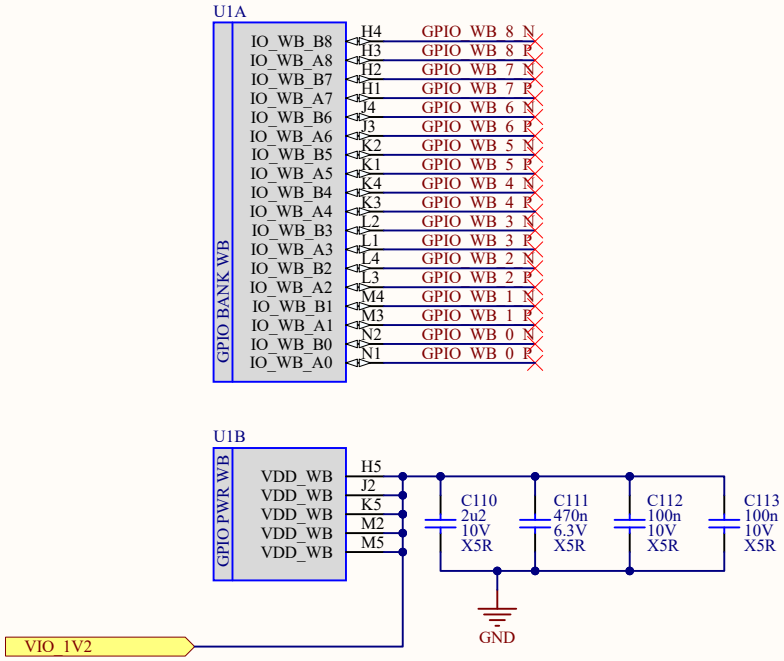

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	WB Bank GPIO Module HyperBus (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet	12 of 21
File:	FPGA_GPIO_WB.SchDoc				

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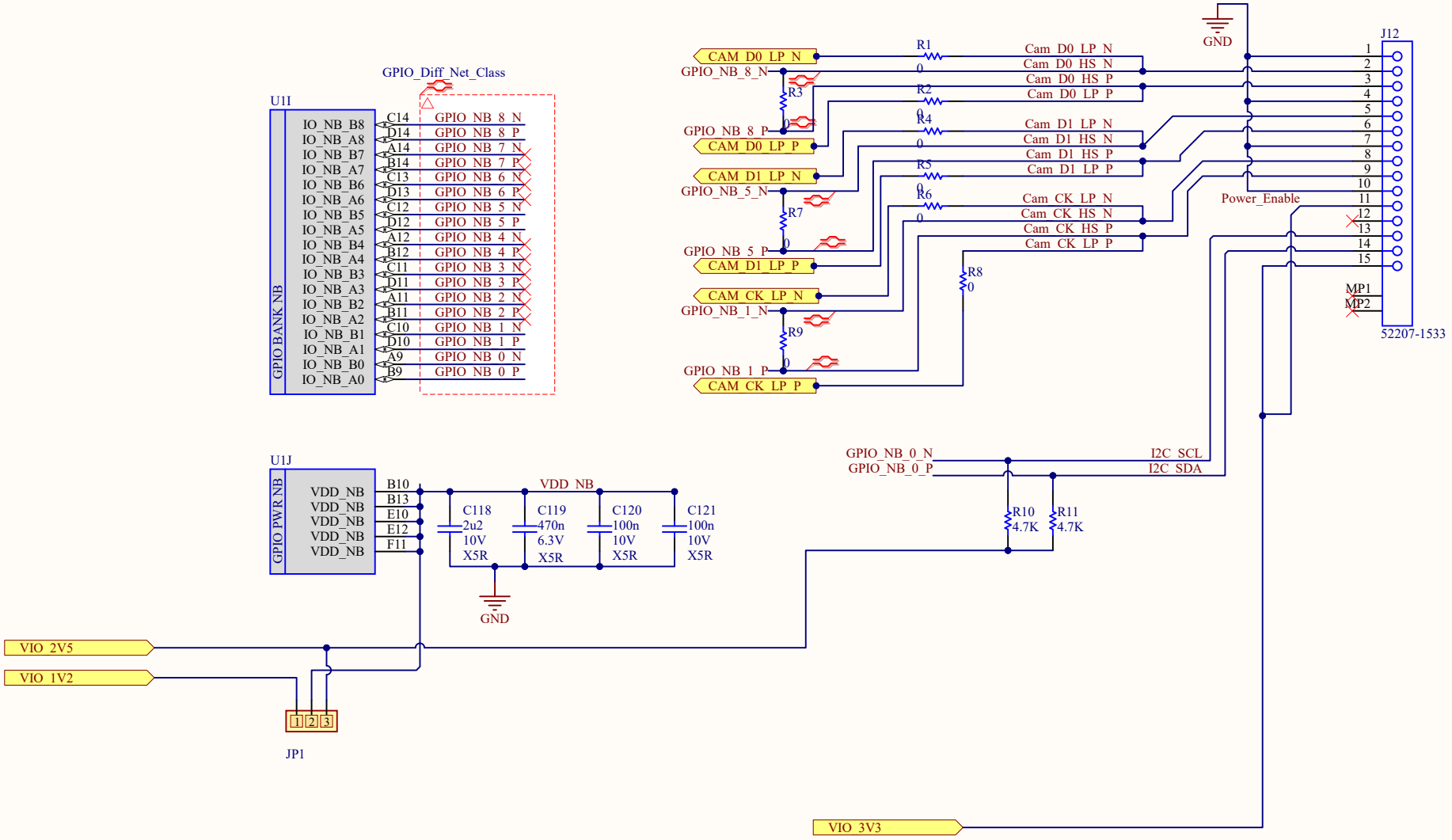

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	NB Bank GPIO Module Pmod (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 13 of 21	
File:	FPGA_GPIO_NB.SchDoc				

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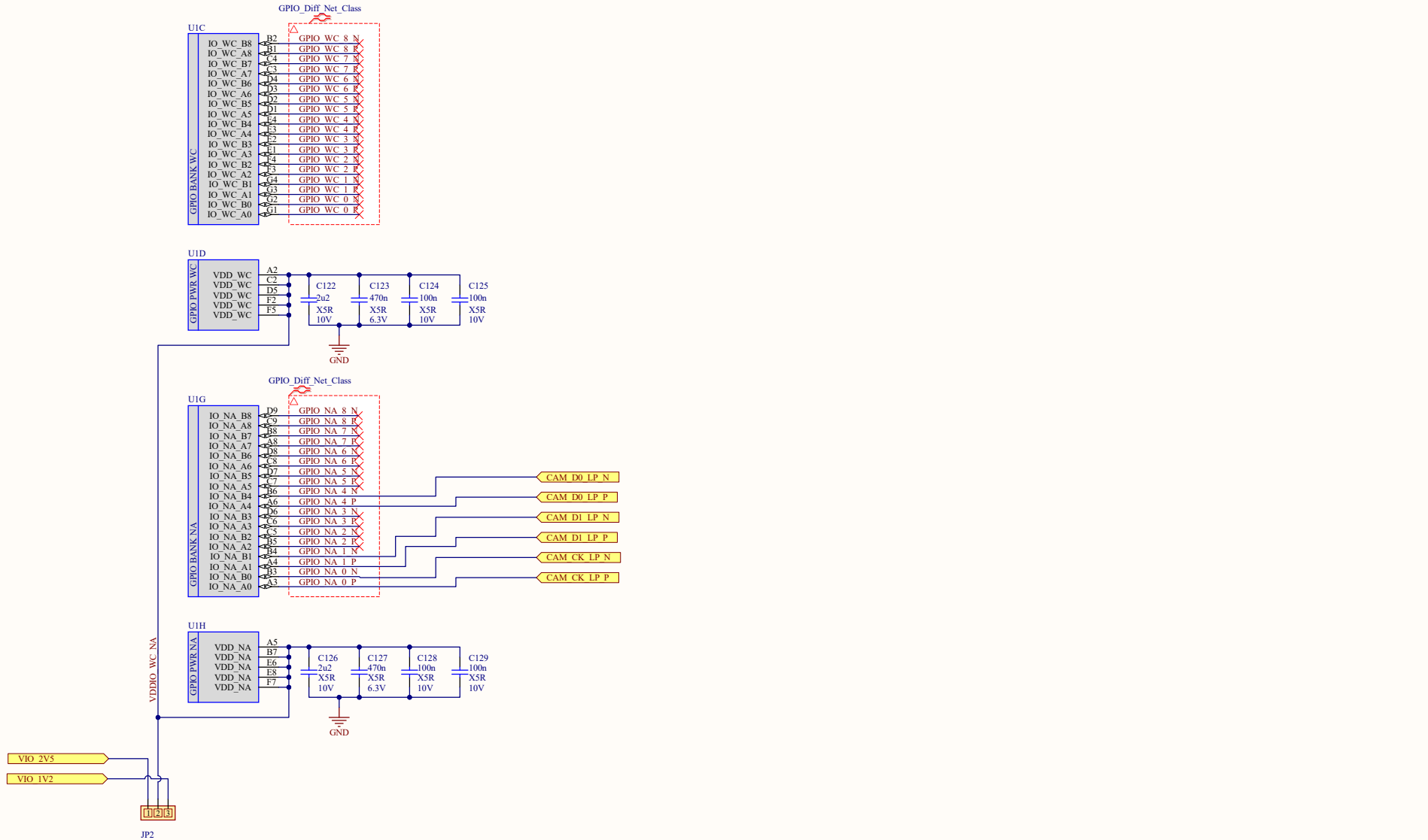

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	WC/NA Banks GPIO Module (FPGA)				
Size:	A3	Author: CCAG	Date: 26.07.2024	Sheet 15 of 21	
File:	FPGA_GPIO_WC_NA.SchDoc				

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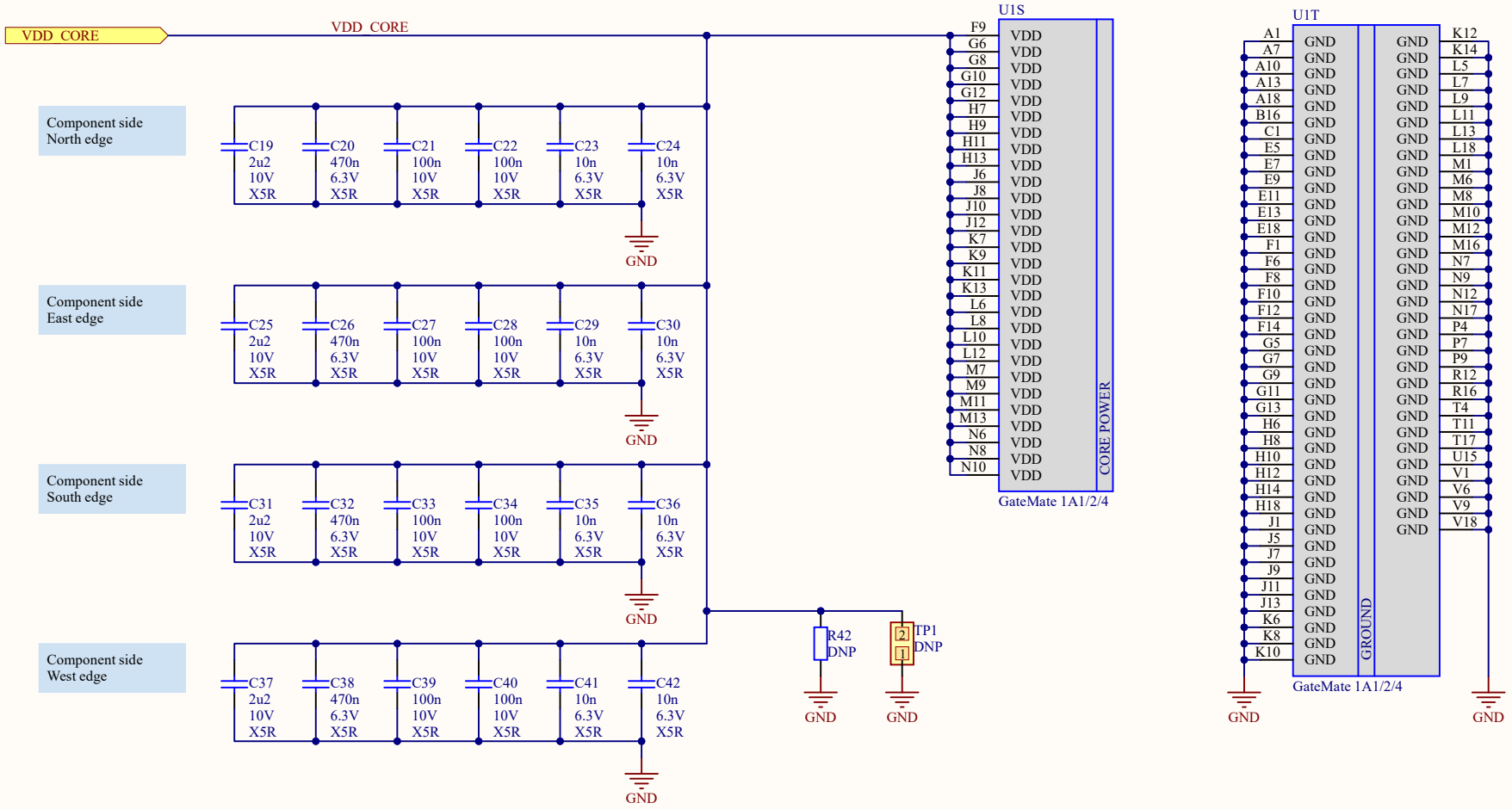

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	Power Supply Core Voltage (FPGA)				
Size:	A4	Author:	CCAG	Date: 26.07.2024	Sheet 16 of 21
File:	FPGA_Power_Supply.SchDoc				

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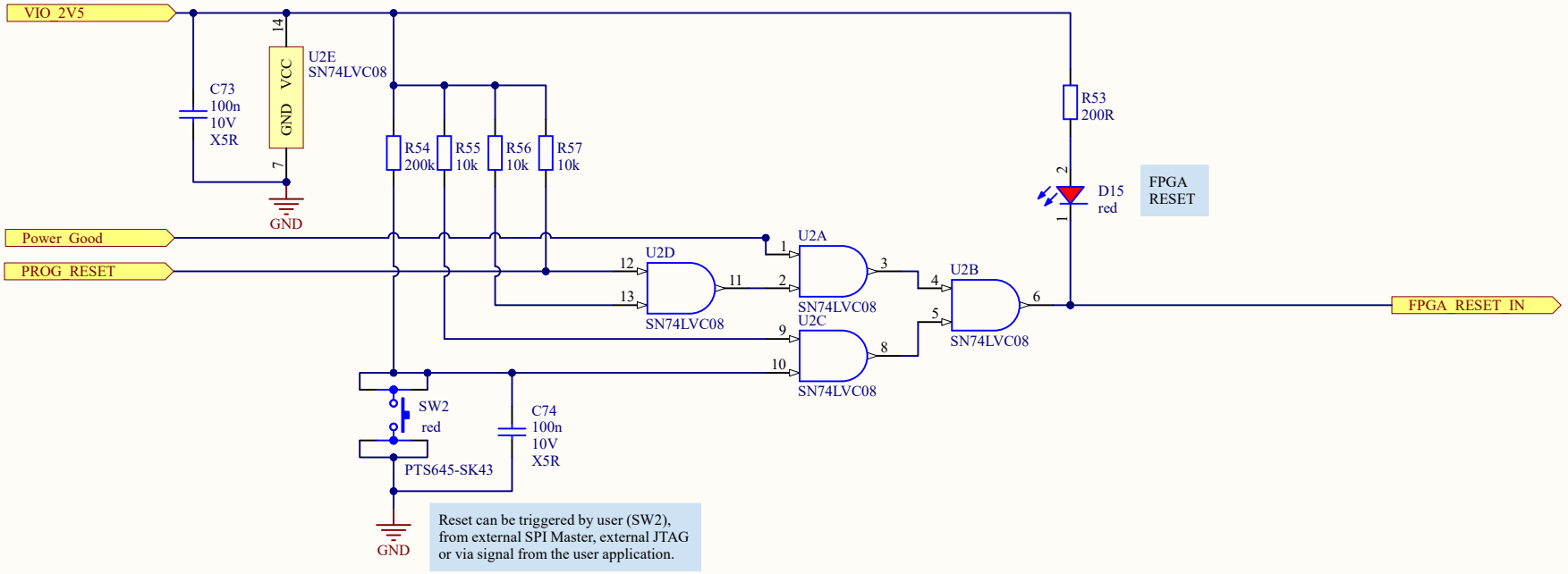

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	Reset (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet	17 of 21
File:	FPGA_RESET.SchDoc				

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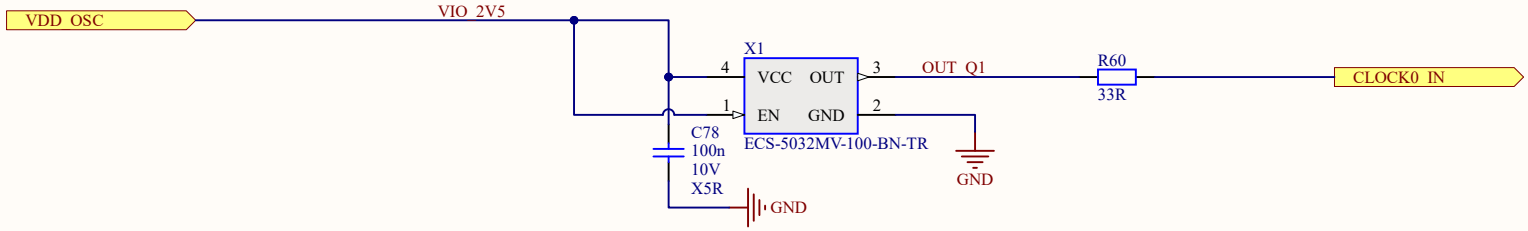

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	Clock (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 18 of 21	
File:	FPGA_Clock.SchDoc				

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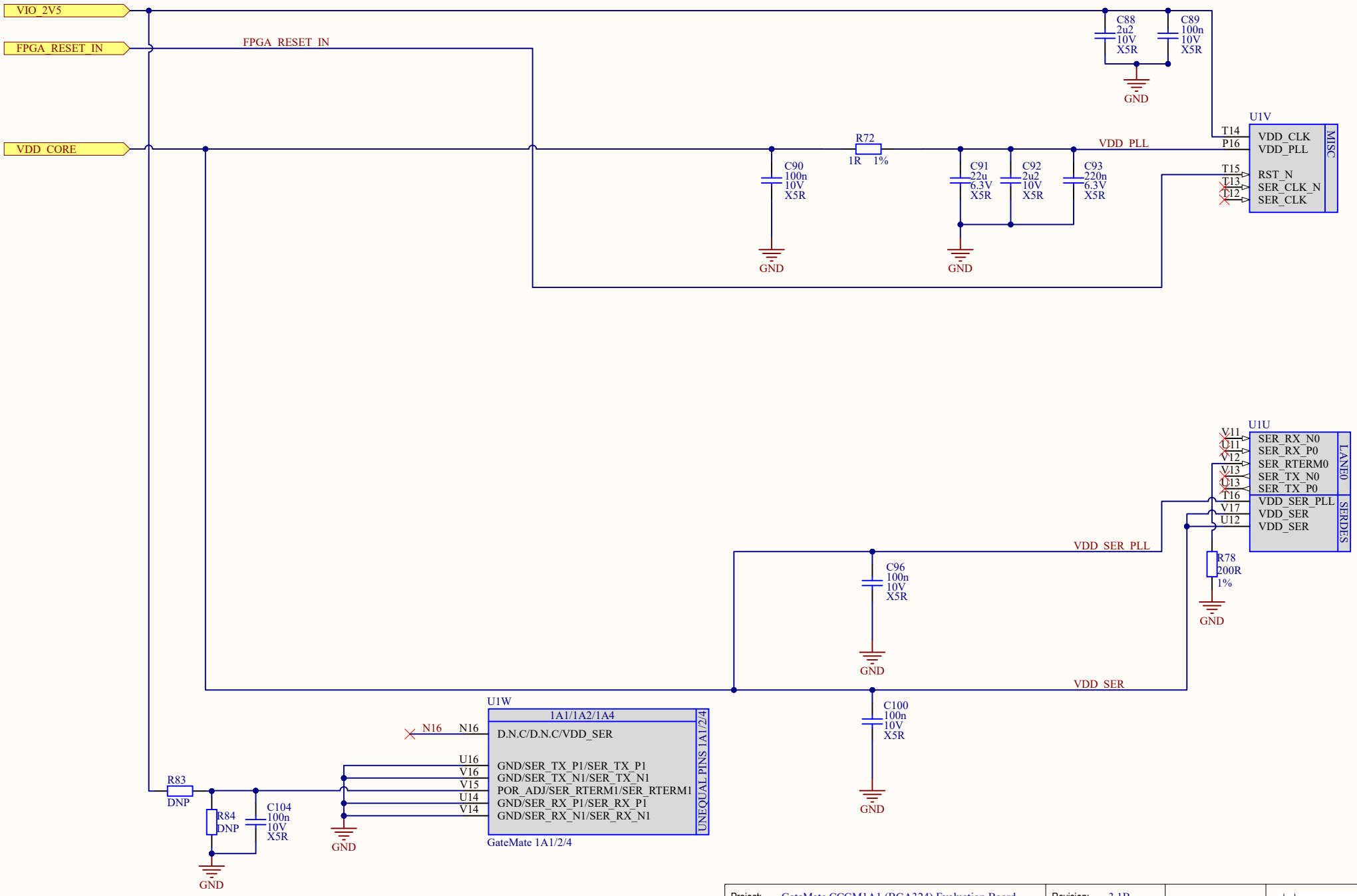

Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	Misc_SerDes (FPGA)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 19 of 21	
File:	FPGA_Misc_Serdes.SchDoc				

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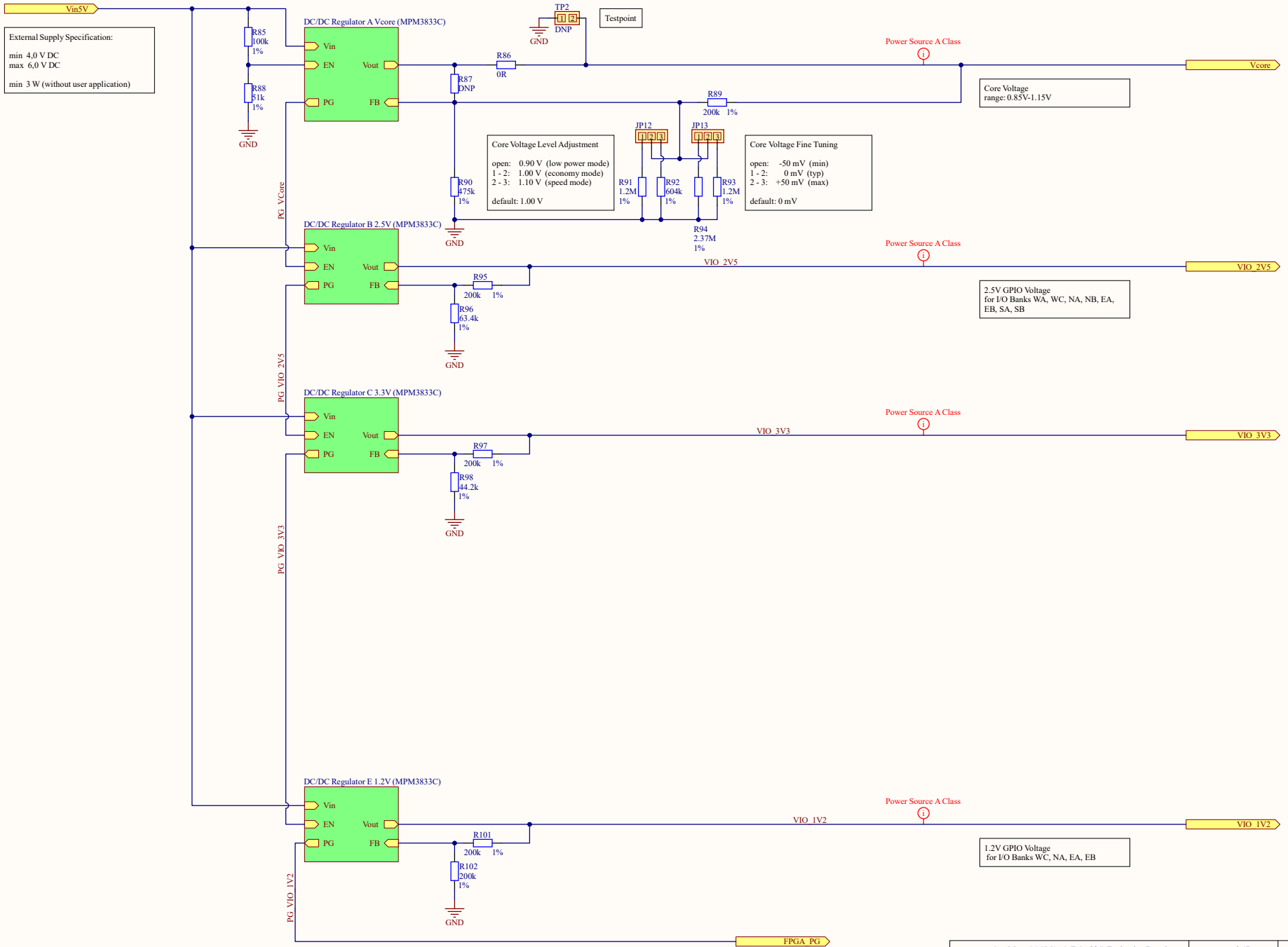
Vin5V
External Supply Specification:
min 4,0 V DC
max 6,0 V DC
min 3 W (without user application)
R85 100k 1%
R88 51k 1%
GND
DC/DC Regulator A Vcore (MPM3833C)
Vin
EN
Vout
PG
FB
TP2
DNP
Testpoint
R86 0R
R87 DNP
R89 200k 1%
Power Source A Class
Vcore
Core Voltage range: 0.85V-1.15V
JP12
JP13
Core Voltage Level Adjustment
open: 0.90 V (low power mode)
1 - 2: 1.00 V (economy mode)
2 - 3: 1.10 V (speed mode)
default: 1.00 V
Core Voltage Fine Tuning
open: -50 mV (min)
1 - 2: 0 mV (typ)
2 - 3: +50 mV (max)
default: 0 mV
R90 475k 1%
R91 1.2M 1%
R92 604k 1%
R93 1.2M 1%
R94 2.37M 1%
PG_VCore
DC/DC Regulator B 2.5V (MPM3833C)
VIO_2V5
R95 200k 1%
R96 63.4k 1%
2.5V GPIO Voltage for I/O Banks WA, WC, NA, NB, EA, EB, SA, SB
PG_VIO_2V5
DC/DC Regulator C 3.3V (MPM3833C)
VIO_3V3
R97 200k 1%
R98 44.2k 1%
PG_VIO_3V3
DC/DC Regulator E 1.2V (MPM3833C)
VIO_1V2
R101 200k 1%
R102 200k 1%
1.2V GPIO Voltage for I/O Banks WC, NA, EA, EB
PG_VIO_1V2
FPGA_PG
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Power Supply Module (MPM 3833C)
Size: A3
Author: CCAG
Date: 26.07.2024
Sheet 20 of 21
File: Eval_Power_MPM.SchDoc
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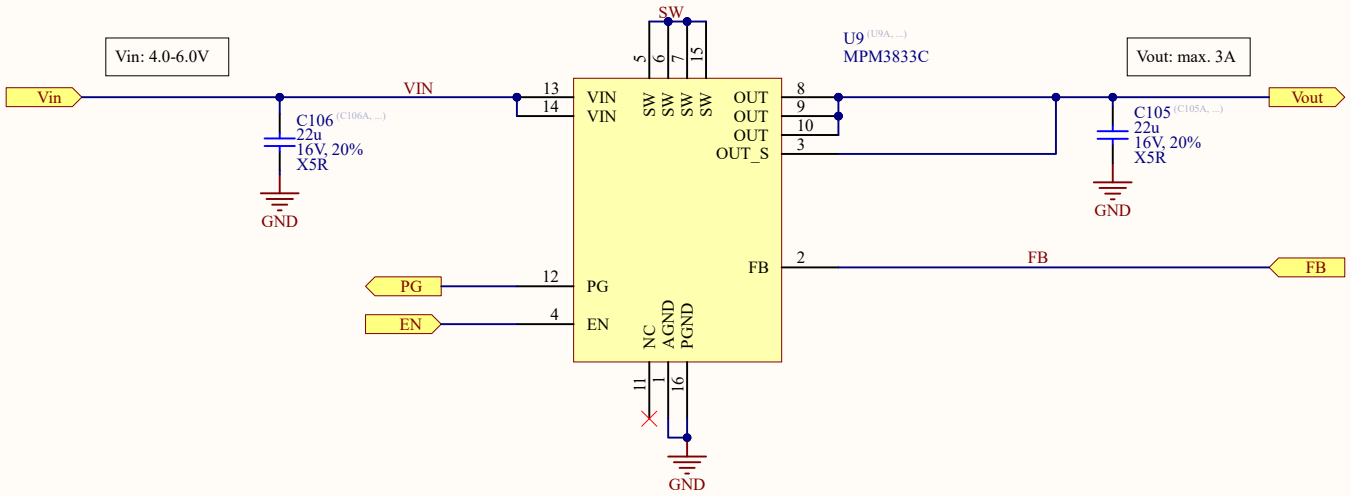
Cologne Chip



Project:	GateMate CCGM1A1 (BGA324) Evaluation Board			Revision:	3.1B
Title:	DC/DC Regulator (MPM3833C)				
Size:	A4	Author: CCAG	Date: 26.07.2024	Sheet 21 of 21	
File:	Eval_dcdc_MPM3833C.SchDoc				

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