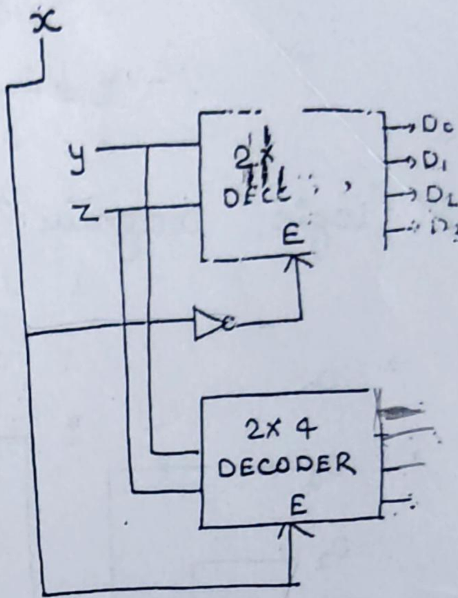
Design 3×8 by using 2×4 Decoder

| x | y z | |
|---|---|---|
| 0 | 0 0 | → $D_0$ |
| 0 | 0 1 | → $D_1$ |
| 0 | 1 0 | → $D_2$ |
| 0 | 1 1 | → $D_3$ |
| 1 | 0 0 | → $D_4$ |
| 1 | 0 1 | → $D_5$ |
| 1 | 1 0 | → $D_6$ |
| 1 | 1 1 | → $D_7$ |




30/08/16

Encoder - $2^n$ input & n output

Decoder - n-input & $2^n$ output

Encoders - An Encoder is a digital circuit that performs the inverse operation of a Decoder.

TRUTH-TABLE

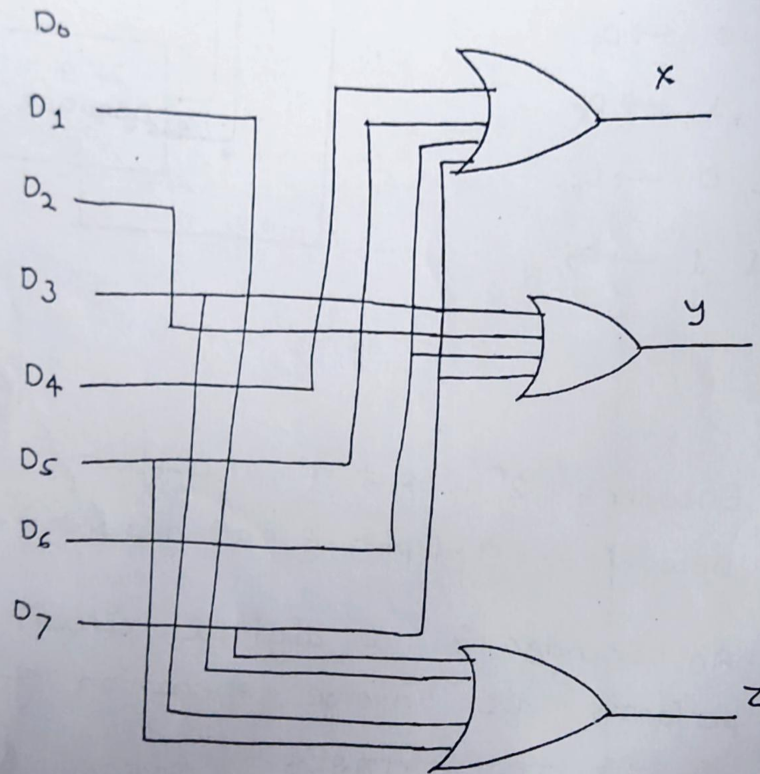
| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | x y z |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 0 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 0 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 1 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 1 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 0 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 0 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 1 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 1 1 |

$$x = D_4 + D_5 + D_6 + D_7$$

$$y = D_2 + D_3 + D_6 + D_7$$

$$z = D_1 + D_3 + D_5 + D_7$$

Logic Diagram for Encoders -




Priority Encoder- A Priority Encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time. The input having the highest priority will take precedence.

$D_0 \rightarrow$ Lowest $\quad D_3 \rightarrow$ Highest $\quad$ Low $\xrightarrow{D_0 D_1 D_2 D_3}$ High Priori.

| Input | | | | Output | | |
|---|---|---|---|---|---|---|
| $D_0$ | $D_1$ | $D_2$ | $D_3$ | A | B | V |
| 0 | 0 | 0 | 0 | x | x | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| x | 1 | 0 | 0 | 0 | 1 | 1 |
| x | x | 1 | 0 | 1 | 0 | 1 |
| x | x | x | 1 | 1 | 1 | 1 |

K-Map for A -

| $D_0D_1 \backslash D_2D_3$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | x | 1 | 1 | 1 |
| 01 | | 1 | 1 | 1 |
| 11 | | 1 | 1 | 1 |
| 10 | | 1 | 1 | 1 |

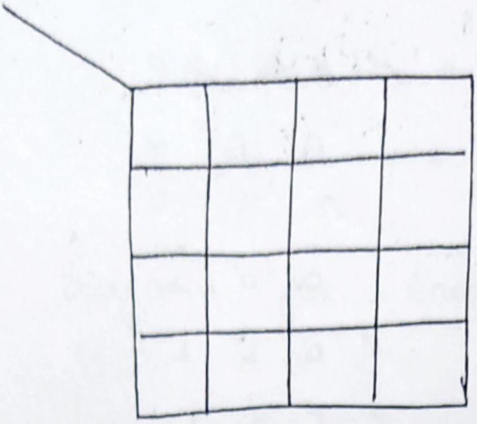
$$A = D_2 + D_3$$

K-MAP for B -

| $D_0D_1 \backslash D_2D_3$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | x | 1 | 1 | |
| 01 | 1 | 1 | 1 | |
| 11 | 1 | 1 | 1 | |
| 10 | | 1 | 1 | |

$B = D_3 + D_1\overline{D_2}$

K- MAP for V -



31/08/16

Q. Design 4-bit priority Encoder. $D_0 \rightarrow$ high
$D_3 \rightarrow$ low

Sol$^n$

| $D_3$ | $D_2$ | $D_1$ | $D_0$ | x | y | V |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| X | 1 | 0 | 0 | 1 | 0 | 1 |
| X | X | 1 | 0 | 0 | 1 | 1 |
| X | X | X | 1 | 0 | 0 | 1 |

K- MAP for X -

| $D_2D_3 \backslash D_0D_1$ | $\overline{D_0}\,\overline{D_1}$ | $\overline{D_0}D_1$ | $D_0D_1$ | $D_0\overline{D_1}$ |
|---|---|---|---|---|
| $\overline{D_2}\,\overline{D_3}$ | X | | | |
| $\overline{D_2}D_3$ | 1 | | | |
| $D_2D_3$ | 1 | | | |
| $D_2\overline{D_3}$ | 1 | | | |

$$X = \overline{D_0}\,\overline{D_1}$$

K-MAP for Y –

| $D_2D_3 \backslash D_0D_1$ | $\overline{D_0}\,\overline{D_1}$ | $\overline{D_0}D_1$ | $D_0D_1$ | $D_0\overline{D_1}$ |
|---|---|---|---|---|
| $\overline{D_2}\,\overline{D_3}$ | X | | | 1 |
| $\overline{D_2}D_3$ | | | | 1 |
| $D_2D_3$ | | | | 1 |
| $D_2\overline{D_3}$ | 1 | | | 1 |

$$Y = D_0\overline{D_1} + \overline{D_1}\,\overline{D_3}$$

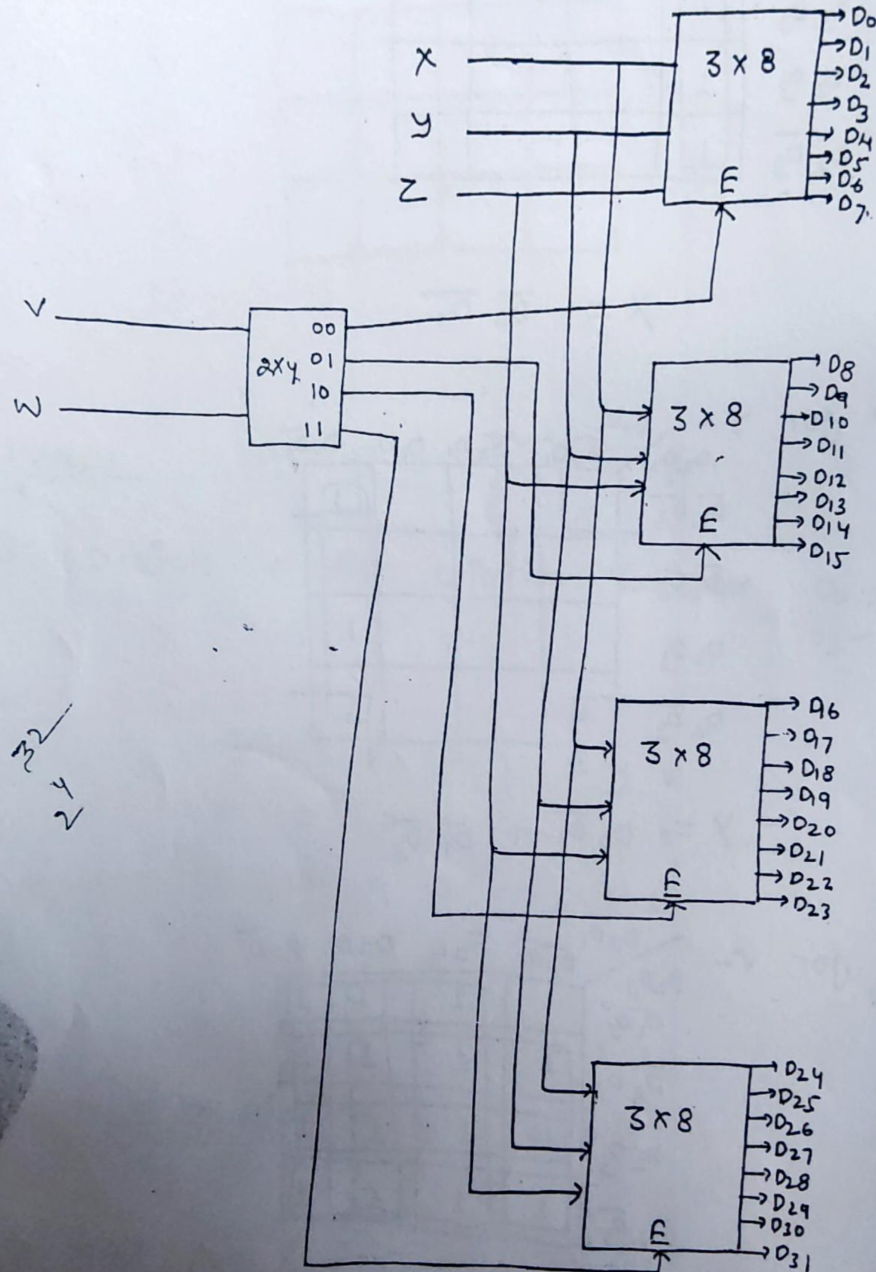
K-MAP for V –

| $D_2D_3 \backslash D_0D_1$ | $\overline{D_0}\,\overline{D_1}$ | $\overline{D_0}D_1$ | $D_0D_1$ | $D_0\overline{D_1}$ |
|---|---|---|---|---|
| $\overline{D_2}\,\overline{D_3}$ | | 1 | 1 | 1 |
| $\overline{D_2}D_3$ | 1 | 1 | 1 | 1 |
| $D_2D_3$ | 1 | 1 | 1 | 1 |
| $D_2\overline{D_3}$ | 1 | 1 | 1 | 1 |

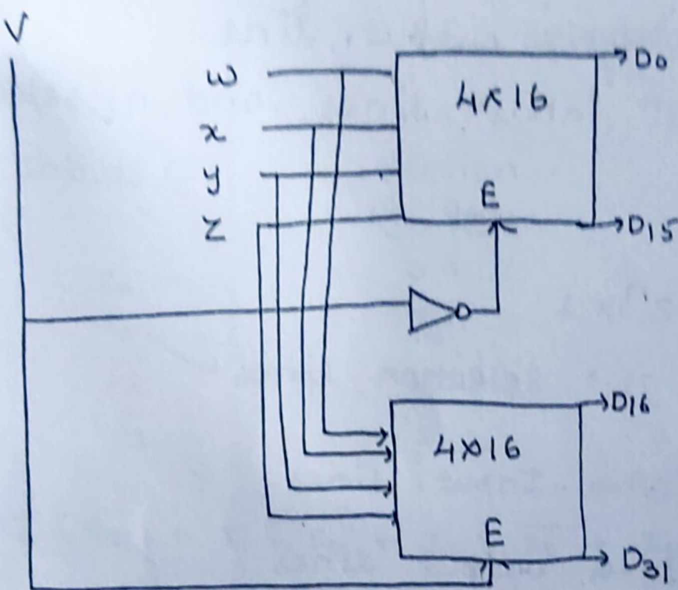
$$V = D_0 + D_1 + D_3 + D_2$$

Q. Construct 5 × 32 decoder with enable and 4 3×8 and one 2×4 Decoder.

<u>Soln</u>



8. Construct 5×32 decoder with enable and 4×16 (two).




| v | w | x | y | z | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | → 0 |
| 0 | 0 | 0 | 0 | 1 | → 1 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| 0 | 0 | 1 | 1 | 1 | → 7 |
| 0 | 1 | 0 | 0 | 0 | |
| 0 | 1 | 0 | 0 | 1 | |
| 0 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | |
| ⋮ | | | | | |
| 0 | 1 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | 1 | |
| 1 | 0 | 0 | 0 | 1 | |

| | | | | |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | 1 | 1 |

05-09-16

MUX- A Multiplexer is a combinational circuit that selects binary informati from one of many input lines and direc it to a single output line.

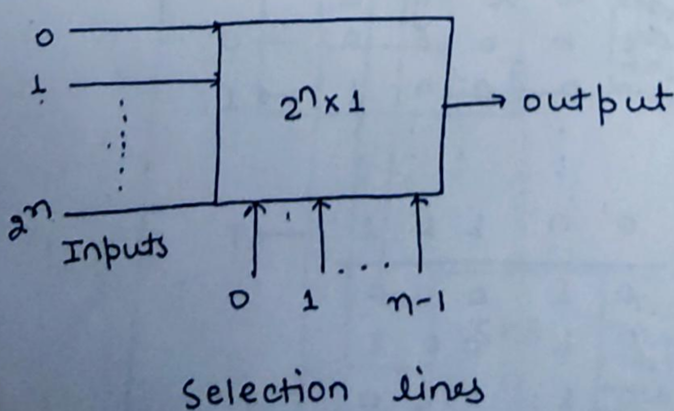
There are $2^n$ input lines and n-selection lines.

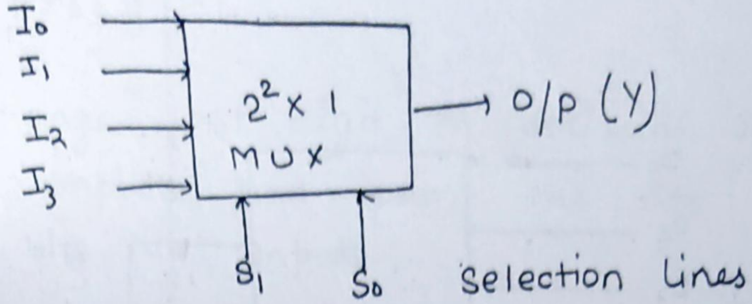
$2^n \times 1$

$n \rightarrow$ Selection lines

$2^n \rightarrow$ Input lines

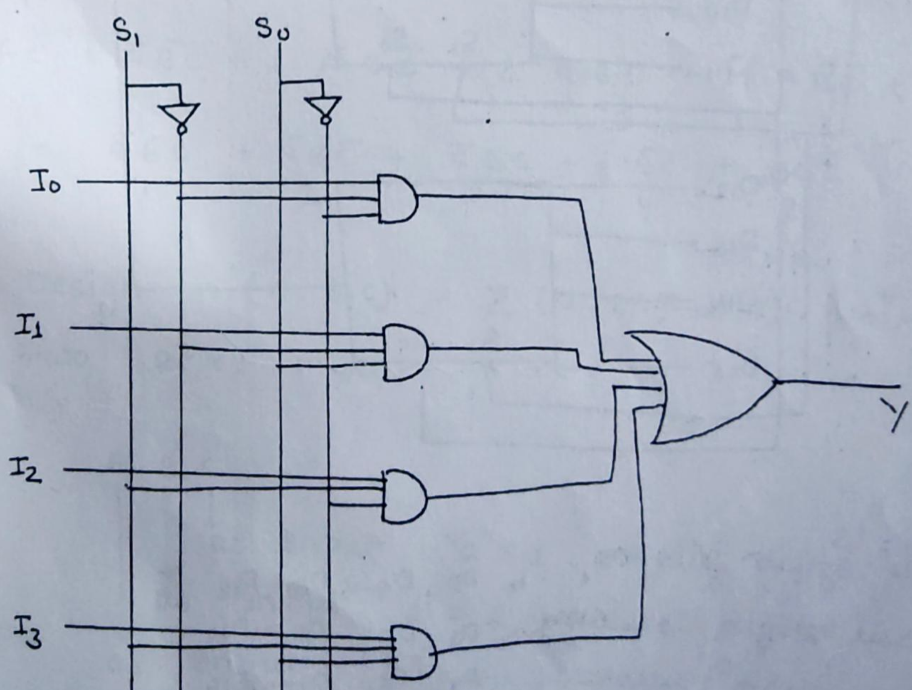
$1 \rightarrow$ output lines



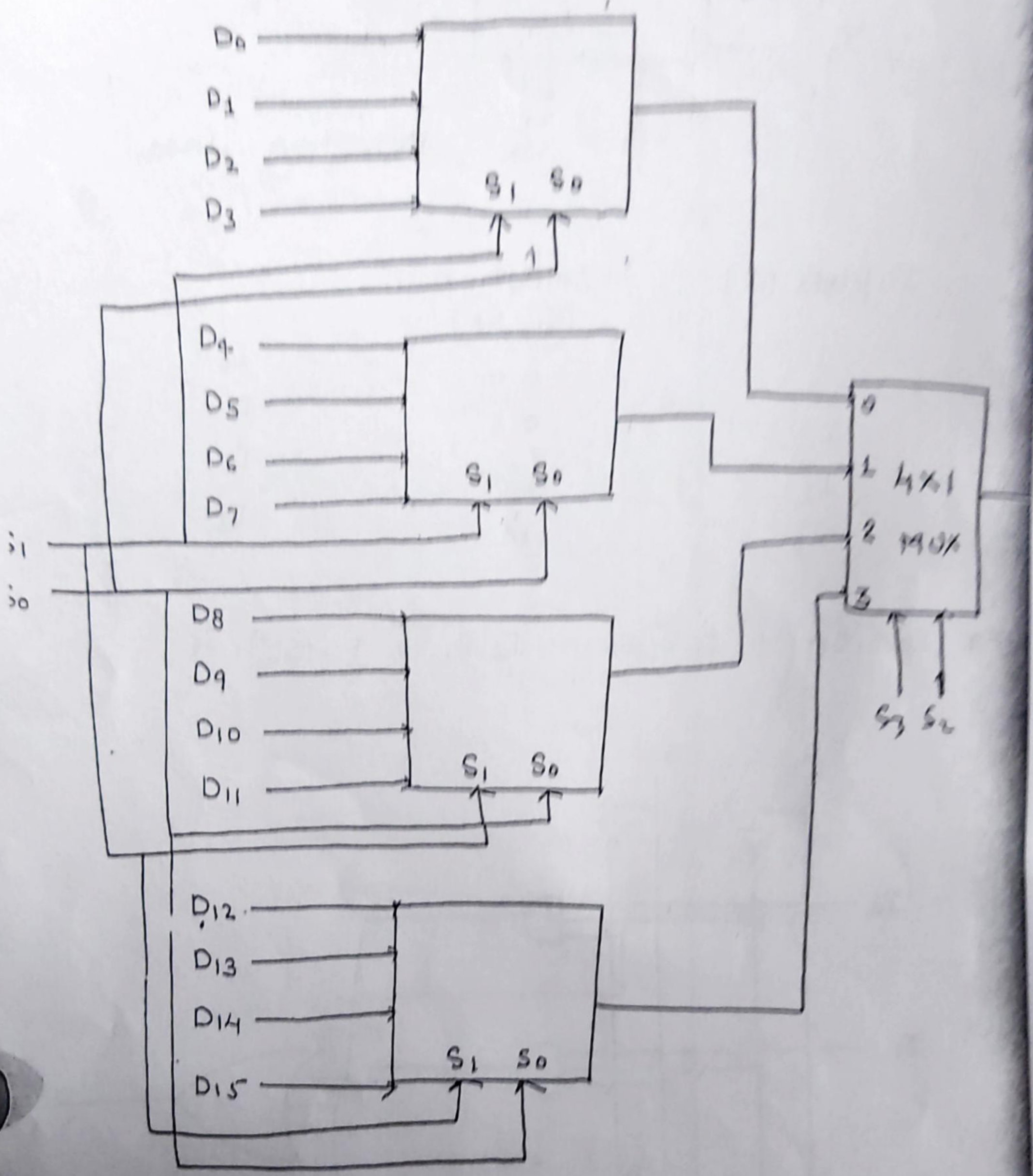



| Inputs (I) | Selection ($S_1$, $S_0$) | O/P |
|---|---|---|
| $I_0$ | 0 0 | $I_0$ |
| $I_1$ | 0 1 | $I_1$ |
| $I_2$ | 1 0 | $I_2$ |
| $I_3$ | 1 1 | $I_3$ |

$$Y = I_0 \overline{S_1}\,\overline{S_0} + I_1 \overline{S_1} S_0 + I_2 S_1 \overline{S_0} + I_3 S_1 S_0$$



Q. Design 16×1 mux using 4 Inputs.

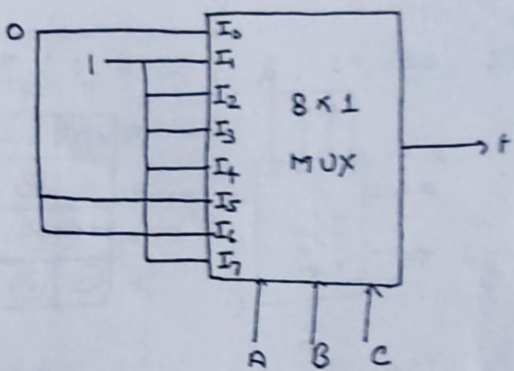



| $S_1$ | $S_0$ | Y | | | |
|---|---|---|---|---|---|
| 0 | 0 | $D_0$ | $D_4$ | $D_8$ | $D_{12}$ |
| 0 | 1 | $D_1$ | $D_5$ | $D_9$ | $D_{13}$ |
| 1 | 0 | $D_2$ | $D_6$ | $D_{10}$ | $D_{14}$ |
| 1 | 1 | - | - | - | - |

Q. Design $F(A, B, C) = \Sigma(1, 2, 3, 4, 7)$ using $8 \times 1$.

change last digit in decimal in absence of inputs and count the bits The no of bits are inputs.

| | 4 | 2 | 1 |
|---|---|---|---|
| | A | B | C |
| 0 = | 0 | 0 | 0 |
| 1. = | 0 | 0 | 1 |
| 2. = | 0 | 1 | 0 |
| 3 = | 0 | 1 | 1 |
| 4 = | 1 | 0 | 0 |
| 7 = | 1 | 1 | 1 |




$$F = 1 \cdot \bar{A}\bar{B}C + 1 \cdot \bar{A} \cdot B \cdot \bar{C} + 1. \ \bar{A} \cdot B \cdot C + 1. \ A\bar{B}\bar{C} + 1 \cdot AB$$

$$= \underset{1}{\bar{A}\bar{B}C} + \underset{2}{\bar{A}B\bar{C}} + \underset{3}{\bar{A}BC} + \underset{4}{A\bar{B}\bar{C}} + \underset{7}{ABC}$$

Q. Design $F(A, B, C) = \Sigma(1, 2, 3, 4, 7)$ using two $2^2 \times 1$ MUX.

A B C

C → as input $2^0 = 1$ parallel digits use

B → as input $2^1 = 2$ parallel digits use

A → as input $2^2 = 4$ parallel digits use.

Implementation Table for A,B,C –

For C –

| | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|---|
| $\bar{C}$ | 0 | 2 | 4 | 6 |
| $C$ | 1 | 3 | 5 | 7 |
| | $C$ | 1 | $\bar{C}$ | $C$ |

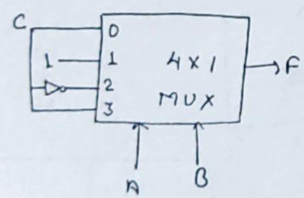
For B –

| | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|---|
| $\bar{B}$ | 0 | 1 | 4 | 5 |
| $B$ | 2 | 3 | 6 | 7 |
| | $B$ | 1 | $\bar{B}$ | $B$ |

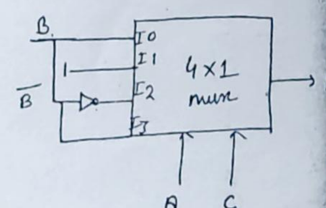
For A –

| | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|---|
| $\bar{A}$ | 0 | 1 | 2 | 3 |
| $A$ | 4 | 5 | 6 | 7 |
| | $A$ | $\bar{A}$ | $\bar{A}$ | 1 |

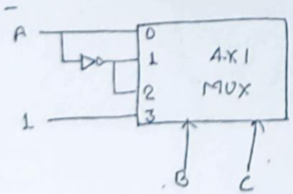
For C –




For B –




For A –



r C - $F = \bar{A}\bar{B}C + \bar{A}B\cdot 1 + A\bar{B}\bar{C} + ABC$

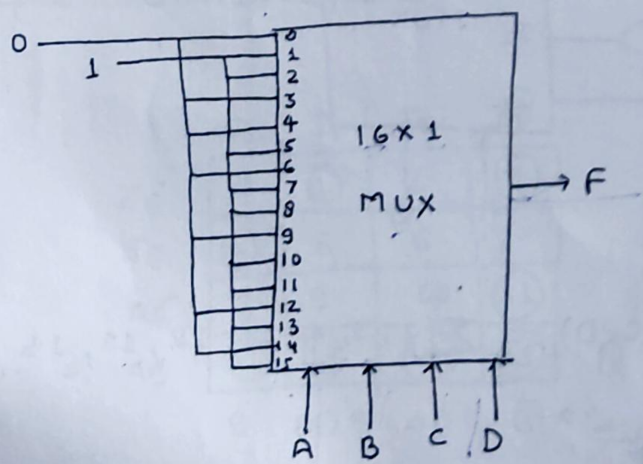
r B - $F = \bar{A}\bar{C}B + \bar{A}C\cdot 1 + A\bar{C}\bar{B} + ACB$

r A - $F = \bar{B}\bar{C}A + \bar{B}C\bar{A} + B\bar{C}\bar{A} + B\cdot C\cdot 1$

06/09/16

$F(A, B, C, D) = \Sigma(1, 2, 5, 7, 8, 10, 11, 13, 15)$

Design with 16×1 MUX.




$\underbrace{AB}_{2}\ \underbrace{CD}_{0}$

CD - As an input

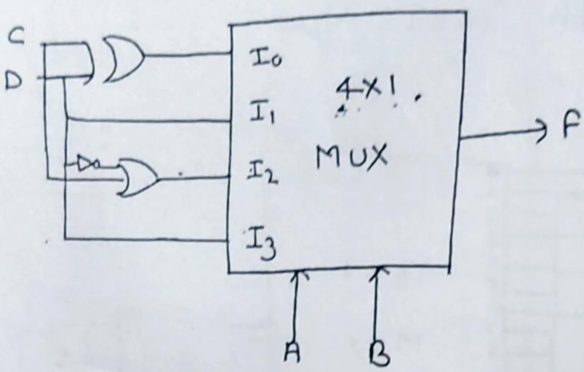
$2^0 = 1$ parallel digits

Implementation Table for CD -

| | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|---|
| 00 $\bar{C}\bar{D}$ | 0 | 4 | 8 | 12 |
| 01 $\bar{C}D$ | 1 | 5 | 9 | 13 |
| 10 $C\bar{D}$ | 2 | 6 | 10 | 14 |
| 11 $CD$ | 3 | 7 | 11 | 15 |
| | $\bar{C}D + C\bar{D}$ | $D$ | $\bar{C}\bar{D} + \bar{C}D + CD$ | $D$ |

$\bar{C}D + C\bar{D} \Downarrow C \oplus D$

$\bar{C}\bar{D} + \bar{C}D + CD \Downarrow \bar{D} + C$

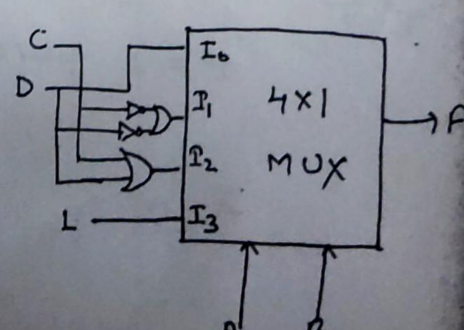


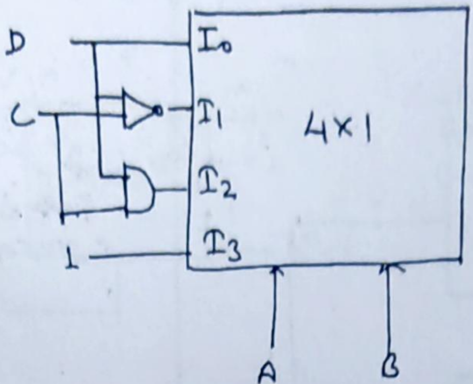

Q. $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$

CD - as input

$2^0 = 1$ parallel line

| | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|---|
| $\bar{C}\bar{D}$ | 0 | 4 | 8 | 12 |
| $\bar{C}D$ | 1 | 5 | 9 | 13 |
| $C\bar{D}$ | 2 | 6 | 10 | 14 |
| $CD$ | 3 | 7 | 11 | 15 |
| | $D$ | $\bar{C}\bar{D}$ | $CD$ | 1 |

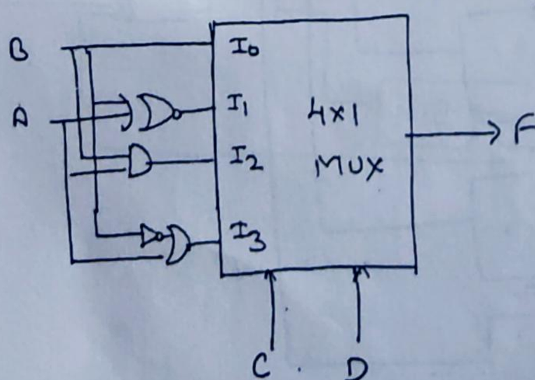




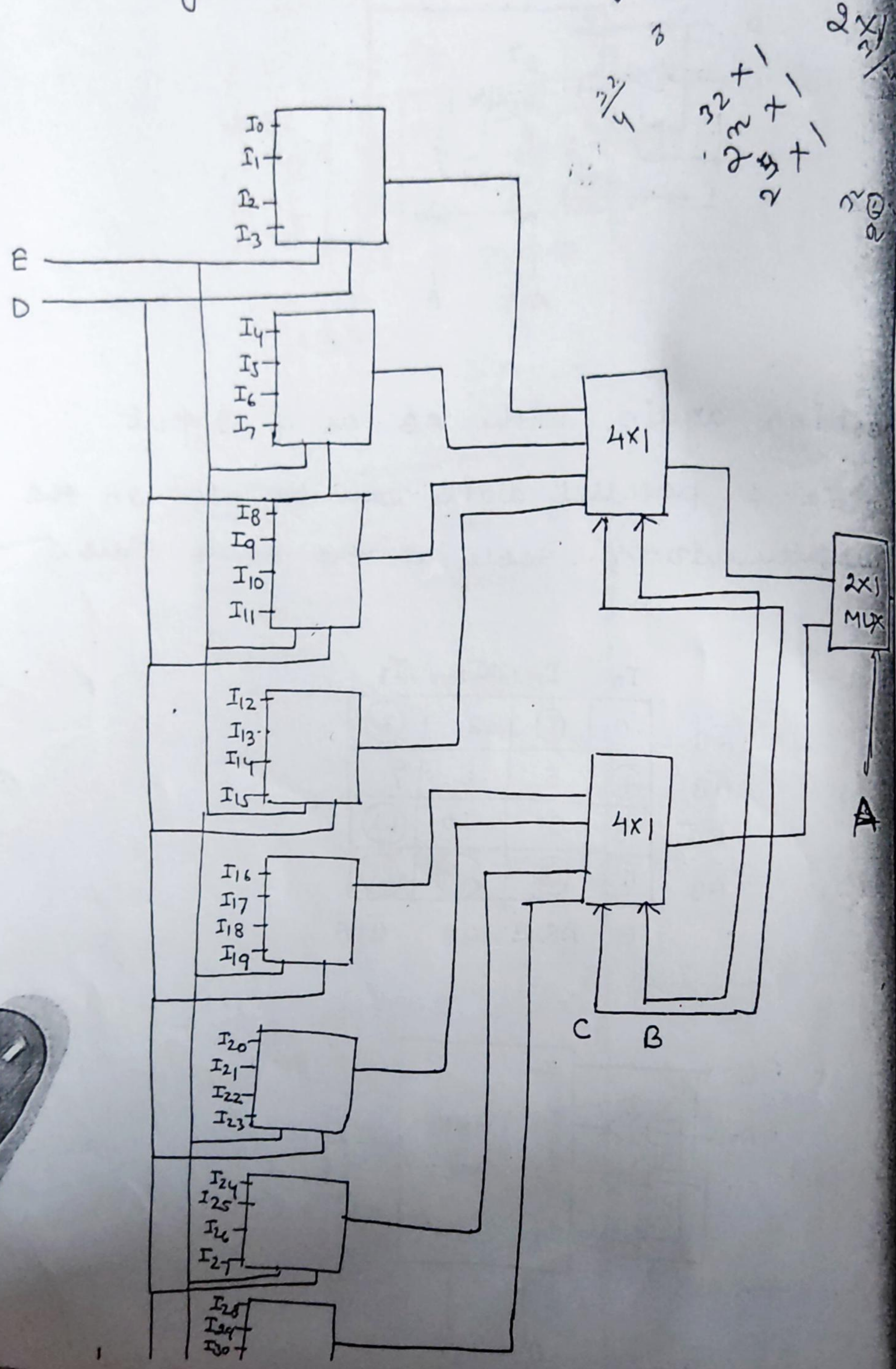

Design again with AB as a input

$2^2 = 4$. parallel digits can be used in the Implementation table at the same time.

| | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|---|
| $\bar{A}\bar{B}$ | 0 | 1 | 2 | 3 |
| $\bar{A}B$ | 4 | 5 | 6 | 7 |
| $A\bar{B}$ | 8 | 9 | 10 | 11 |
| $AB$ | 12 | 13 | 14 | 15 |
| | $B$ | $A \odot B$ | $AB$ | $\bar{B}+A$ |



Q. Design 32x1 MUX using four 4x1 MUX



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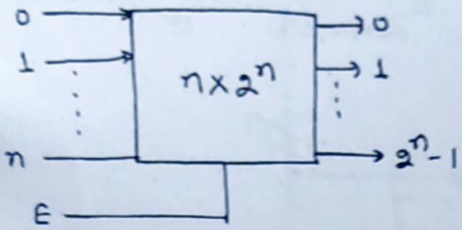
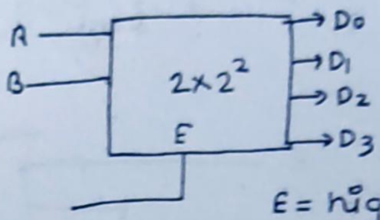
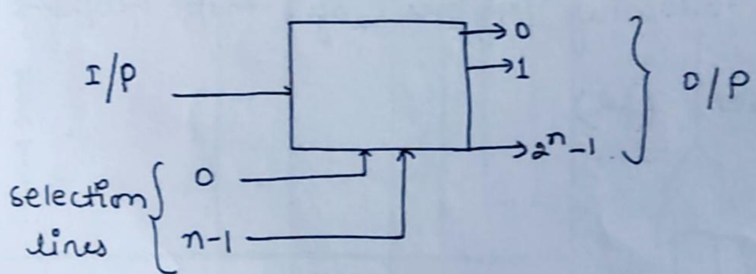


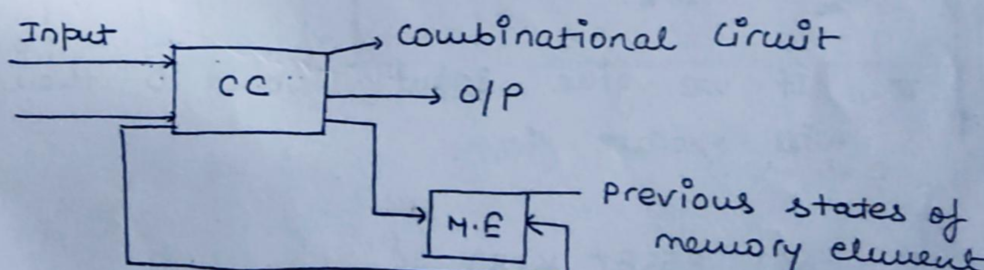




E = high 1
low 0

Decoder – Demux – output – Selection lines
enable – input

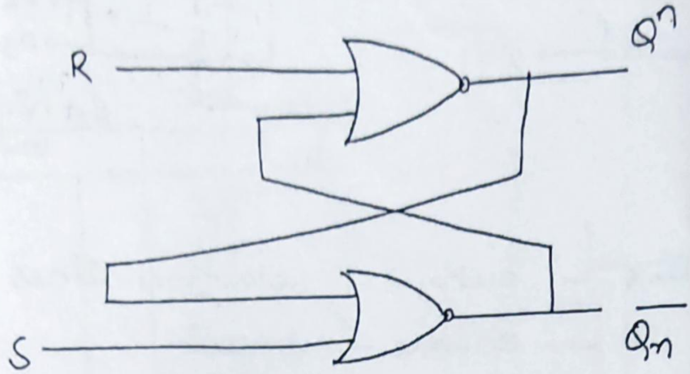



Sequential Circuits –




Scanned by CamScanner

Flip-Flop - Flip flop is a memory element used for storing single bit either 0 or 1. Flip-Flop is a bistable device.




There are following types of flip-flops -

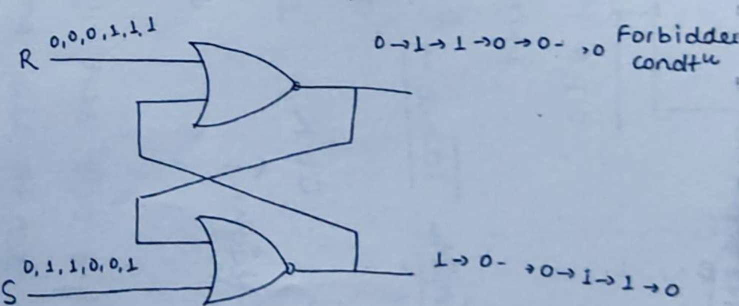
1. Set Reset (SR)
2. D
3. JK
4. T
5. Master Slave

★ If we give Input - 1 and 0 then one will operate first.

1. SET RESET (SR) -

Truth- Table for SR-

| S | R | Present State $Q_n$ | Next State $Q_{n+1}$ | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | - Always zero |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 1 | Always one In case of 1,0 |
| 0 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 0 | Next state will always zero |
| 1 | 1 | 0 | 0 | Forbidden value condition |




✡. If we consider 0 or 1 as a previous state then next state will be 0 or 1.

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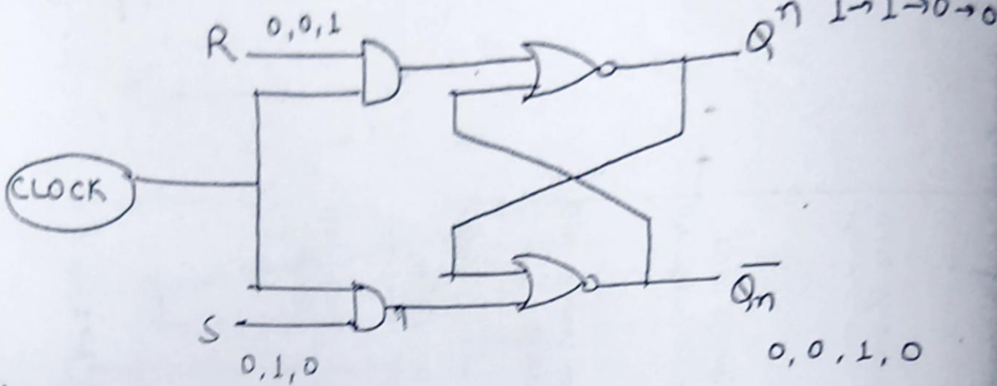
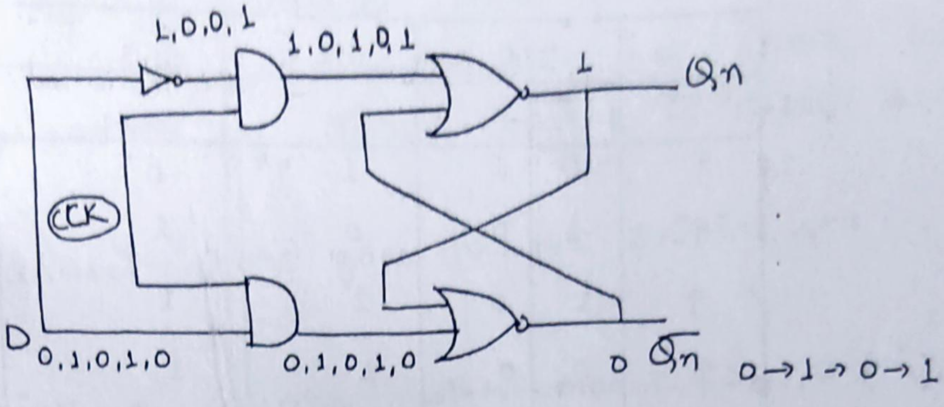
Flip- Flop with clock -




## Truth Table -

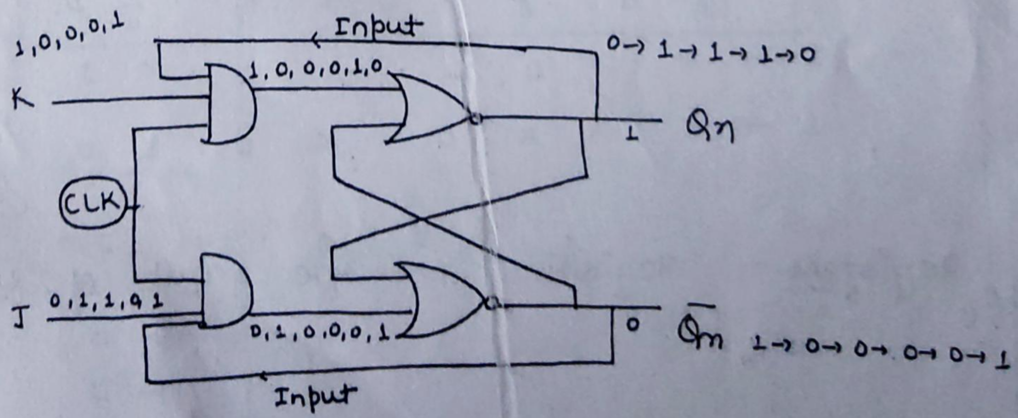
| CLK | S | R | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|---|
| (high) ↑ | 0 | 0 | 1 | 1 |
| ↑ | 0 | 1 | 1 | 1 |
| ↑ | 1 | 0 | 1 | 0 |
| ↑ | 1 | 1 | 0 | ? |

D- Flip Flop -- (Delay) - It is used for transfer the data from one to another. It can be used for one clock delay.




| Input | P.S | N.S |
|---|---|---|
| D | $Q_n$ | $Q_{n+1}$ |
| 1 | 1 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |

J. K Flip-Flop – JK Flip flop has two inputs and performs all three actions.




Toggling – output changes in same clock pulse.

Truth - Table for JK -

| | I/P | | P.S | N.S |
|---|---|---|---|---|
| CLK | J | K | $Q_n$ | $Q_{n+1}$ |
| ↑ | 0 | 1 | 1 | 0 |
| ↑ | 1 | 0 | 0 | 1 |
| ↑ | 1 | 0 | 1 | 1 |
| ↑ | 0 | 0 | 1 | 1 |
| ↑ | 1 | 1 | 1 | 1→0→1→0 |

12/09/16

Excitation Table -

| P.S | N.S | F/F | | | | | |
|---|---|---|---|---|---|---|---|
| $Q_n$ | $Q_{n+1}$ | S | R | J | K | D | T |
| 0 → | 0 | 0 | X | 0 | X | 0 | 0 |
| 0 → | 1 | 1 | 0 | 1 | X | 1 | 1 |
| 1 → | 0 | 0 | 1 | X | 1 | 0 | 1 |
| 1 → | 1 | X | 0 | X | 0 | 1 | 0 |

Registers - Registers are the group of flip-flops.

Counter- A Register that goes through a prescribed sequence of states upon the application of input pulses is called a counter

* unused state goes to the initial state.

Design a counter with mod 7 by D-FF's op.

Initial state - $S_5 \to S_4 \to S_2 \to S_0 \to S_3$ final state

| $Q_2$ | $Q_1$ | $Q_0$ | $D_0$ | $D_1$ | $D_2$ |
|---|---|---|---|---|---|
| | | | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | | | |
| 1 | 1 | 1 | 1 | 0 | 1 |

$S_5 - S_4$

| | P.S | N.S | $D_0$ |
|---|---|---|---|
| $Q_0$ | 1 → 0 | | 0 |
| $Q_1$ | 0 → 0 | | 0 |
| | 1 → 1 | | 1 |
| | 0 → 1 | | 1 |

K-MAP for $D_0$ -

| $Q_2 \backslash Q_1Q_0$ | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | 1 | 1 | 1 | |
| $Q_2$ | | | 1 | 1 |

$$D_0 = \overline{Q_2}\,\overline{Q_1} + \overline{Q_2}Q_0 + Q_2Q_1$$

K-MAP for $D_1$ -

| $Q_2 \backslash Q_1Q_0$ | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | 1 | | | |
| $Q_2$ | 1 | | | |

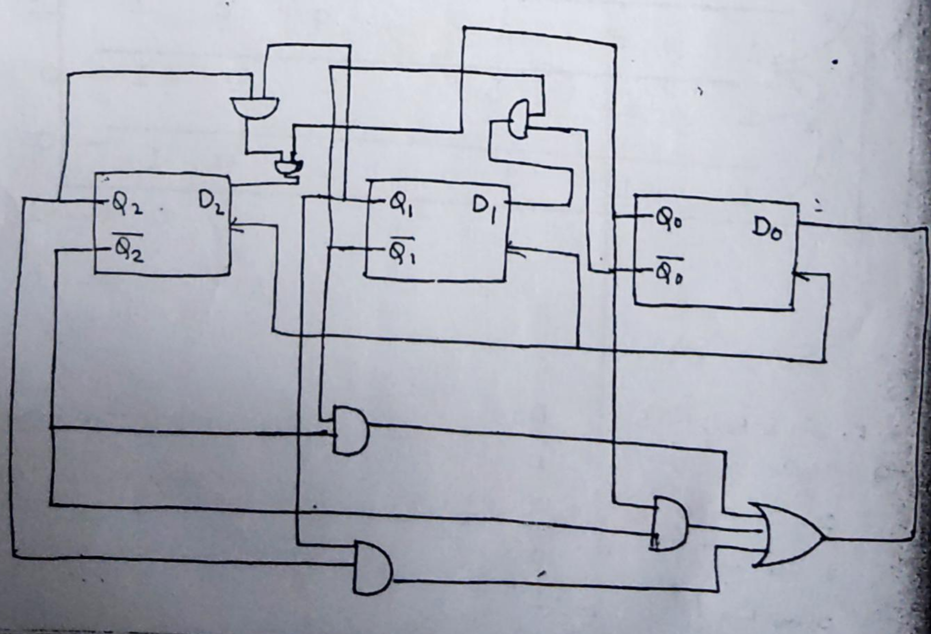
$$D_1 = \overline{Q_1}\,\overline{Q_0}$$

K-MAP for $D_2$ -

| $Q_2 \backslash Q_1Q_0$ | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | | 1 | 1 | |
| $Q_0$ | | 1 | 1 | 1 |

| $Q_n$ | $Q_{n+1}$ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

$$D_2 = Q_0 + Q_2Q_1$$



14/09/16

Q. Design counter with mod 6.

| $Q_2$ | $Q_1$ | $Q_0$ | | $J_0$ | $K_0$ | $J_1$ | $K_1$ | $J_2$ | $K_2$ |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | x | 0 | x | 0 | x |
| 0 | 0 | 1 | 1 | x | 1 | 1 | x | 0 | x |
| 0 | 1 | 0 | 2 | 1 | x | x | 0 | 0 | x |
| 0 | 1 | 1 | 3 | x | 1 | x | 1 | 1 | x |
| 1 | 0 | 0 | 4 | 1 | x | 0 | x | x | 0 |
| 1 | 0 | 1 | 5 | x | 1 | 0 | x | x | 1 |
| 1 | 1 | 0 | 6 | 0 | x | x | 1 | x | 1 |
| 1 | 1 | 1 | 7 | x | 1 | x | 1 | x | 1 |

K-MAP for - $J_0$

| $Q_2 \backslash Q_1Q_0$ | $\bar{Q}_1\bar{Q}_0$ | $\bar{Q}_1Q_0$ | $Q_1Q_0$ | $Q_1\bar{Q}_0$ |
|---|---|---|---|---|
| $\bar{Q}_2$ | 1 | X | X | 1 |
| $Q_2$ | 1 | X | X | 0 |

$J_0 = \bar{Q}_2 + \bar{Q}_1$

K-MAP for - $K_0$

| | $\bar{Q}_1\bar{Q}_0$ | $\bar{Q}_1Q_0$ | $Q_1Q_0$ | $Q_1\bar{Q}_0$ |
|---|---|---|---|---|
| $\bar{Q}_2$ | X | 1 | 1 | X |
| $Q_2$ | X | 1 | 1 | X |

$K_0 = 1$

K-MAP for $K_1$ -

| | $\bar{Q}_1\bar{Q}_0$ | $\bar{Q}_1Q_0$ | $Q_1Q_0$ | $Q_1\bar{Q}_0$ |
|---|---|---|---|---|
| $\bar{Q}_2$ | X | X | 1 | |
| $Q_2$ | X | X | 1 | 1 |

$K_1 = Q_0 + Q_2$

K-MAP for $J_1$ -

| | $\bar{Q}_1\bar{Q}_0$ | $\bar{Q}_1Q_0$ | $Q_1Q_0$ | $Q_1\bar{Q}_0$ |
|---|---|---|---|---|
| $\bar{Q}_2$ | | 1 | X | X |
| $Q_2$ | | | X | X |

$J_1 = \bar{Q}_2Q_0$

K-MAP for $J_2$ -

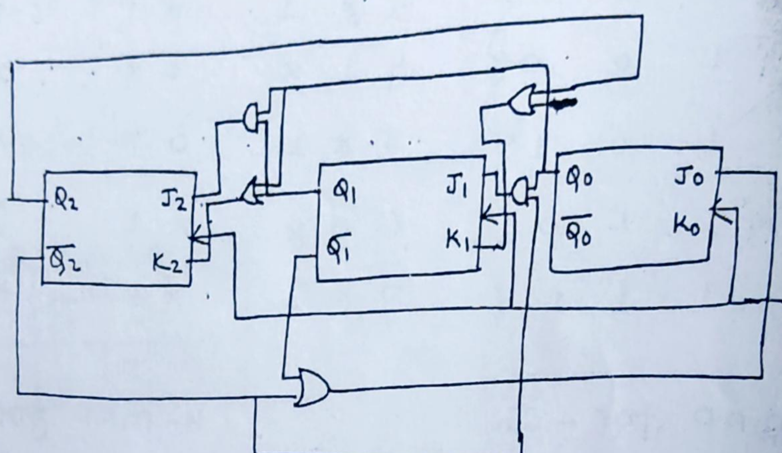
| | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | | | 1 | |
| $Q_2$ | X | X | X | X |

$J_2 = Q_1Q_0$

K-MAP for $K_2$ -

| | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | X | X | X | X |
| $Q_2$ | 0 | 1 | 1 | 1 |

$K_2 = Q_0 + Q_1$




Design the same with D- Flip-Flop -

| $Q_2$ | $Q_1$ | $Q_0$ | $D_0$ | $D_1$ | $D_2$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

K-MAP for D0 -

| | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | 1 | | | 1 |
| $Q_2$ | 1 | | | |

$$D_0 = \overline{Q_1}\,\overline{Q_0} + \overline{Q_2}\,\overline{Q_0}$$

K-MAP for - D1

| | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | | 1 | | 1 |
| $Q_2$ | | | | |

$$D_1 = \overline{Q_2}\,\overline{Q_1}Q_0 + [illegible]\,Q_1\overline{Q_0}$$

$$= \overline{Q_2}\,(\overline{Q_1}Q_0 + Q\ [illegible])$$

$$= \overline{Q_2}\,(Q_1 \oplus Q_0)$$

K-MAP for D3 -

| | $\overline{Q_1}\,\overline{Q_0}$ | $\overline{Q_1}Q_0$ | $Q_1Q_0$ | $Q_1\overline{Q_0}$ |
|---|---|---|---|---|
| $\overline{Q_2}$ | | | 1 | |
| $Q_2$ | 1 | | | |

$$D_2 = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_1}\,\overline{Q_0}$$