<table>
<tr><td>Module</td><td>CPU_Pipelined</td></tr>
<tr><td>Dependencies</td><td>SameBit, MUX2, Flopr_32, Flopenr_32, Flopr, DSwitch, MUX2_5, MUX2_32, Four, SE16_32, SL2_32, RF, Flopenr, DESwitch, MUX4_32, MUX3_32, MUX32_32, MUX32, Decoder_32, MUX4, MUX3, ALU32, IM, DM, SPLICE_PCJ, ALUBit31, ALUBits0To30, OneBitAdder, INC4_32</td></tr>
<tr><td>Inputs</td><td>
<table>
<tr><th>Name</th><th>Size (Bits)</th></tr>
<tr><td>reset</td><td>1</td></tr>
<tr><td>clk</td><td>1</td></tr>
<tr><td>Strategy</td><td>2</td></tr>
</table>
</td></tr>
<tr><td>Outputs</td><td>
<table>
<tr><th>Name</th><th>Size (Bits)</th></tr>
<tr><td>PC</td><td>32</td></tr>
<tr><td>IFIR</td><td>32</td></tr>
<tr><td>IDIR</td><td>32</td></tr>
<tr><td>EXIR</td><td>32</td></tr>
<tr><td>MEMIR</td><td>32</td></tr>
<tr><td>WBIR</td><td>32</td></tr>
</table>
</td></tr>
<tr><td>Description</td><td>MIPS Five-Stage Pipelined CPU
Standard clk and reset inputs; also takes a Branch Prediction Strategy (00=Not Taken, 01=Taken, 10=Delay Slot)
Outputs the following information:
PC: Address of the current instruction
IFIR: Instruction in IF stage
IDIR: Instruction in ID stage
EXIR: Instruction in EX stage
MEMIR: Instruction in MEM stage
WBIR: Instruction in WB stage</td></tr>
</table>