Module	CPU_Pipelined
Dependencies	**SameBit, MUX2, Flopr_32, Flopenr_32, Flopr, DSwitch, MUX2_5, MUX2_32, Four, SE16_32, SL2_32, RF, Flopenr, DESwitch, MUX4_32, MUX3_32, MUX32_32, MUX32, Decoder_32, MUX4, MUX3, ALU32, IM, DM, SPLICE_PCJ, ALUBit31, ALUBits0To30, OneBitAdder, INC4_32, Adder_32**

Inputs	Name	Size (Bits)
	reset	1
	clk	1
	Strategy	2

Outputs	Name	Size (Bits)
	PC	32
	IFIR	32
	IDIR	32
	EXIR	32
	MEMIR	32
	WBIR	32

Description	MIPS Five-Stage Pipelined CPU
	Standard **clk** and **reset** inputs; also takes a Branch Prediction Strategy (00=Not Taken, 01=Taken, 10=Delay Slot)
	Outputs the following information:
	PC: Address of the current instruction
	IFIR: Instruction in IF stage
	IDIR: Instruction in ID stage
	EXIR: Instruction in EX stage
	MEMIR: Instruction in MEM stage
	WBIR: Instruction in WB stage