

Module Fabrication Document

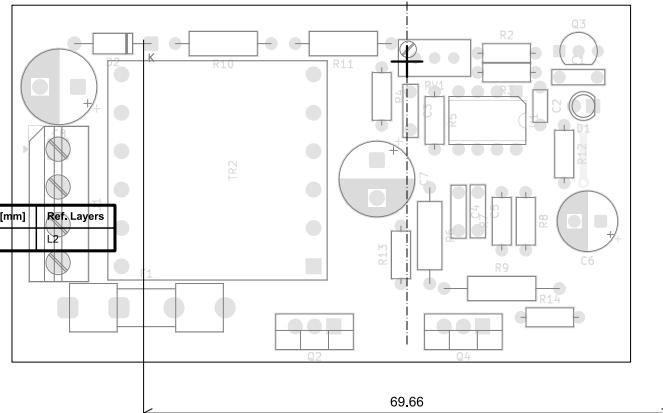
Layer Stack Legend

A

Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste			Paste Mask	
	F.Silkscreen		Direct Printing	Legend	GBR
	F.Mask	0.02mm	Solder Resist	Solder Mask	GBR
Copper	L1 (Sig, PWR)	0.07mm (2.00oz)		Signal	GBR
Core		1.48mm	FR4_7628	Dielectric	
Copper	L6 (Sig, PWR)	0.07mm (2.00oz)		Signal	GBR
	B.Mask	0.02mm	Solder Resist	Solder Mask	GBR
	B.Silkscreen		Direct Printing	Legend	GBR
	B.Paste			Paste Mask	

Total thickness: 1.66mm
Note: external layer thicknesses are specified after plating

Top Fabrication (Scale 1:1)



B

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
Edge-Coupled Coated Microstrip	100	±10 %	L1	0.2032	0.28	L2

C

All dimensions are in millimeters unless otherwise specified.

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.
DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX
SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.
- 4) SURFACE FINISH: IMMERSION GOLD
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR BLACK.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING YELLOW NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:
 - A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
 - B. Tg 170 C OR EQUIVALENT.
 - C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY FR.

10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE	81.800 × 47.200 mm
BOARD THICKNESS	1.660 mm
TRACE WIDTH	1.000 mm
TRACE TO TRACE	0.200 mm
MIN. HOLE (PTH)	0.800 mm
MIN. HOLE (NPTH)	N/A mm
ANNUAL RING	0.320 mm
COPPER TO HOLE	0.254 mm
COPPER TO EDGE	0.250 mm
HOLE TO HOLE	0.254 mm

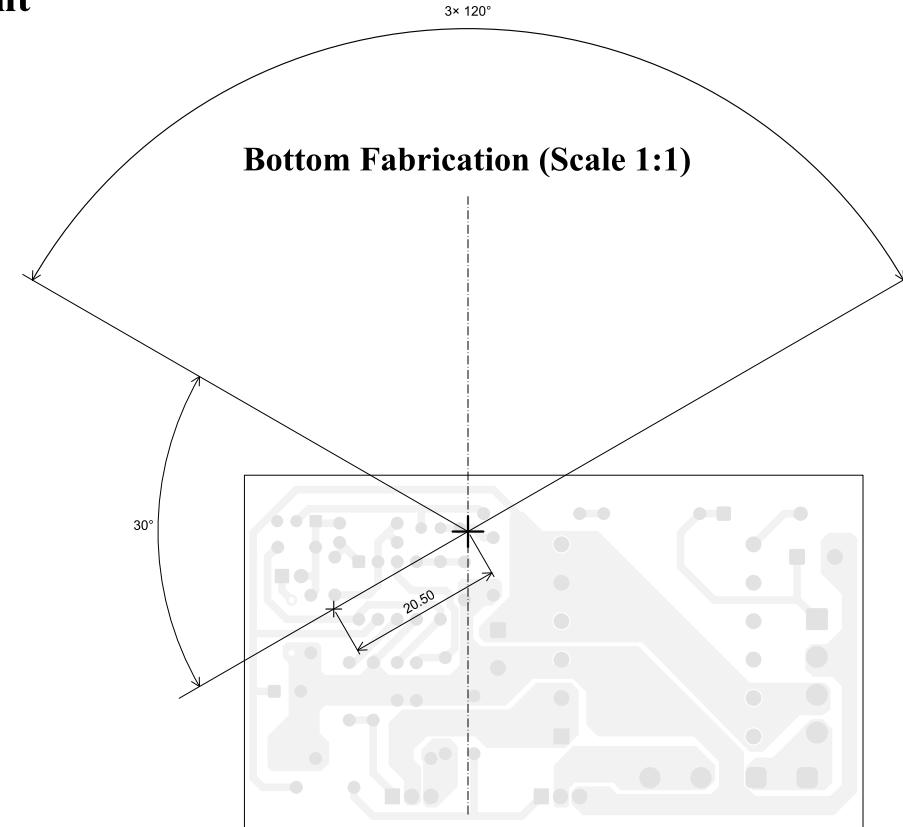
11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.

12) CONFIRM SPACE WIDTHS AND SPACINGS.

D

	Comments:	Company: FR	Variant: PRELIMINARY	Git Hash: 0ceba30
	Board Name: Module	Project Name: Alixp Step up module 12 to 450 V		
	Sheet Title: Top Fabrication (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13 Revision: + (Unreleased)
	Sheet Path:	Reviewer: A4		Size: Sheet: 1 of 7

Module Fabrication Document



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	Sheet Path:		Reviewer:	Size: A4 Sheet: 2 of 7

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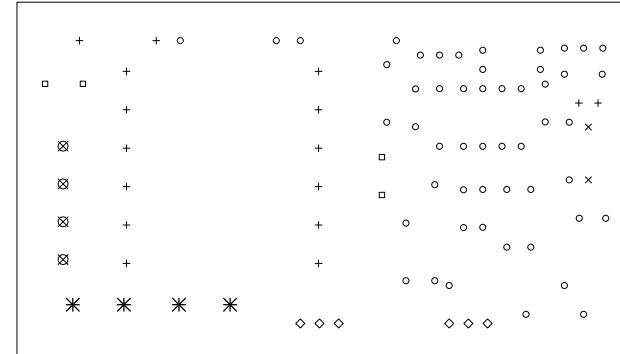
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Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
X	2	0.80mm (31.50mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Via
O	52	0.80mm (31.50mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
+	16	0.90mm (35.43mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
□	4	1.00mm (39.37mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
◊	6	1.20mm (47.24mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
☒	4	1.30mm (51.18mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
*	4	1.70mm (66.93mils)	PTH	Round	L1 (Sig, PWR) - L6 (Sig, PWR)	Pad
Total 88						

Drill Drawing L1 - L2 (Scale 1:1)



B

B

C

C

D

D

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Module Fabrication Document

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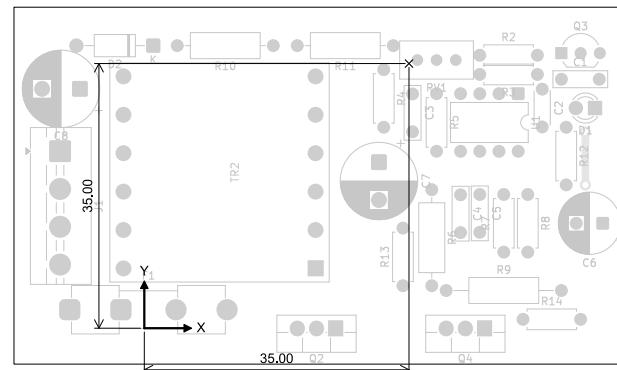
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Top Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]

Ref.	Net	X [mm]	Y [mm]



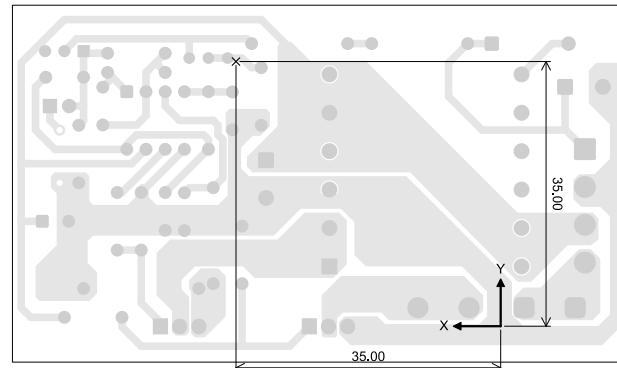
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	Sheet Path:		Reviewer:	Size: A4 Sheet: 4 of 7

Module Fabrication Document

Bottom Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]
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Module Fabrication Document

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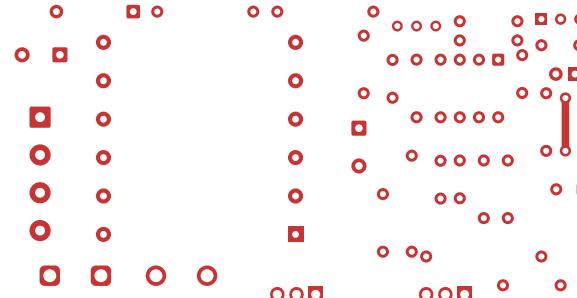
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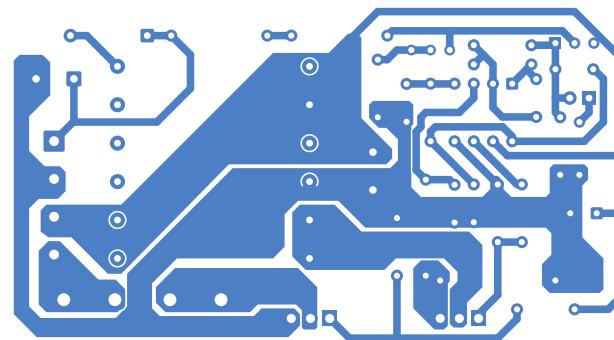
L1 (Sig, PWR) (Scale 1:1)



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L6 (Sig, PWR) (Scale 1:1)



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