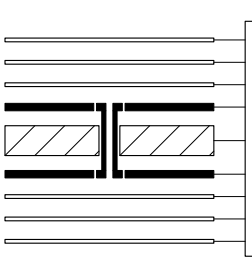
Module Fabrication Document

Layer Stack Legend



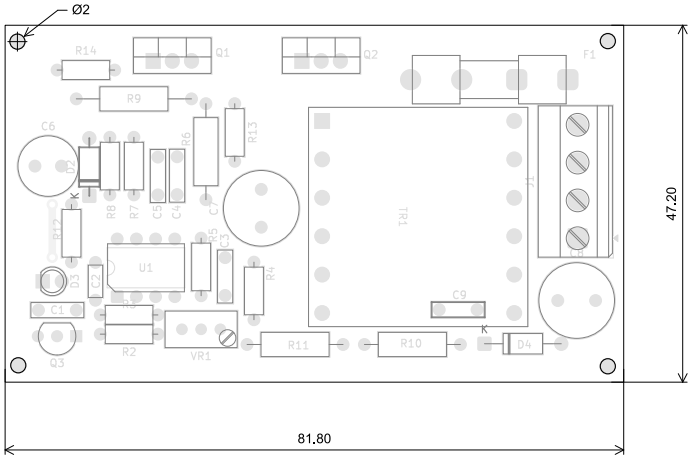
Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste			Paste Mask	
	F.Silkscreen		Direct Printing	Legend	GBR
	F.Mask	0.02mm	Solder Resist	Solder Mask	GBR
Copper	**L1 (Sig, PWR)**	**0.07mm (2.00oz)**		**Signal**	**GBR**
Core		1.48mm	FR4_7628	Dielectric	
Copper	**L2 (Sig, PWR)**	**0.07mm (2.00oz)**		**Signal**	**GBR**
	B.Mask	0.02mm	Solder Resist	Solder Mask	GBR
	B.Silkscreen		Direct Printing	Legend	GBR
	B.Paste			Paste Mask	

Total thickness: 1.66mm
Note: external layer thicknesses are specified after plating

Impedance Table

Transmission Line	Impedance [ohms]	Tolerance [ohms]	Layer	Trace Width [mm]	Gap [mm]	Ref. Layers
Edge-Coupled Coated Microstrip	100	±10 %	L1	0.2032	0.28	L2

Top Fabrication (Scale 1:1)



FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

1) FABRICATE PER IPC-6012A CLASS 2.

2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.

   DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

   SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

4) SURFACE FINISH: IMMERSION GOLD

5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR TOP: #8071501A / BOTTOM: GREEN.

6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.

7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.

8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING

9) PCB MATERIAL REQUIREMENTS:

   A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
   B. Tg 170 C OR EQUIVALENT.
   C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY FR.

10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE	81.800 × 47.200 mm
BOARD THICKNESS	1.660 mm
TRACE WIDTH	1.000 mm
TRACE TO TRACE	0.200 mm
MIN. HOLE (PTH)	0.800 mm
MIN. HOLE (NPTH)	2.100 mm
ANNULAR RING	0.320 mm
COPPER TO HOLE	0.254 mm
COPPER TO EDGE	0.250 mm
HOLE TO HOLE	0.254 mm

11) REFER TO IMPEDANCE TABLE FOR IMPEDANCE CONTROL REQUIREMENTS.

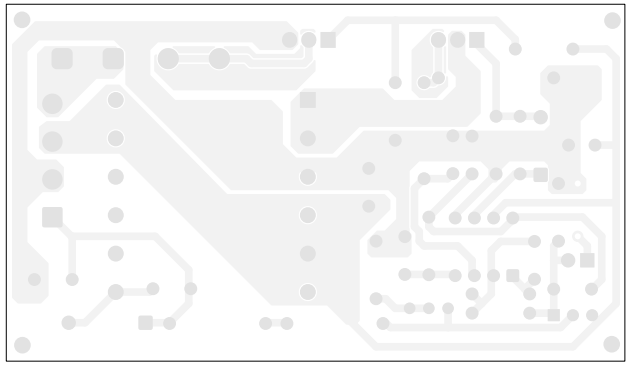
12) CONFIRM SPACE WIDTHS AND SPACINGS.

All dimensions are in millimeters unless otherwise specified.

Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b
	Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
Sheet Title: Top Fabrication (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **1** of **8**

Module Fabrication Document

Bottom Fabrication (Scale 1:1)



All dimensions are in millimeters unless otherwise specified.

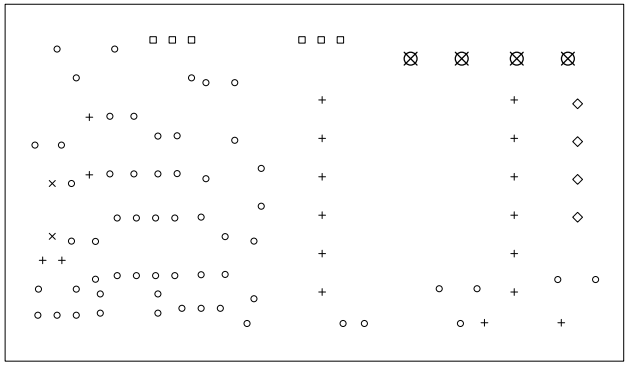
	Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b
		Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
	Sheet Title: Bottom Fabrication (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **2** of **8**

Module Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	2	0.80mm (31.50mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Via
○	58	0.80mm (31.50mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Pad
+	18	0.90mm (35.43mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Pad
□	6	1.20mm (47.24mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Pad
◇	4	1.30mm (51.18mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Pad
⊠	4	1.70mm (66.93mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Pad
	Total 92					

Drill Drawing L1 - L2 (Scale 1:1)



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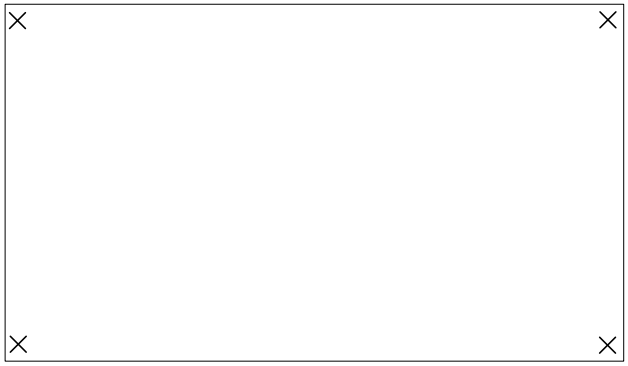
		Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
	Sheet Title: Drill Drawing (L1 - L2)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **3** of **8**

Module Fabrication Document

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	4	2.10mm (82.68mils)	NPTH	Round	L1 (Sig, PWR) - L2 (Sig, PWR)	Mechanical
	Total 4					

Drill Drawing L1 - L2 (Scale 1:1)



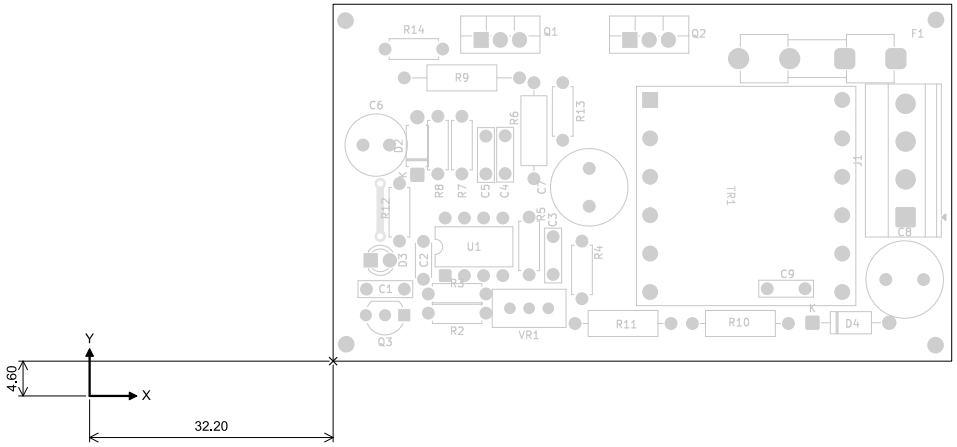
	Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b
		Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
	Sheet Title: Drill Drawing (L1 - L2)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **4** of **8**

Module Fabrication Document

Top Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]

Ref.	Net	X [mm]	Y [mm]



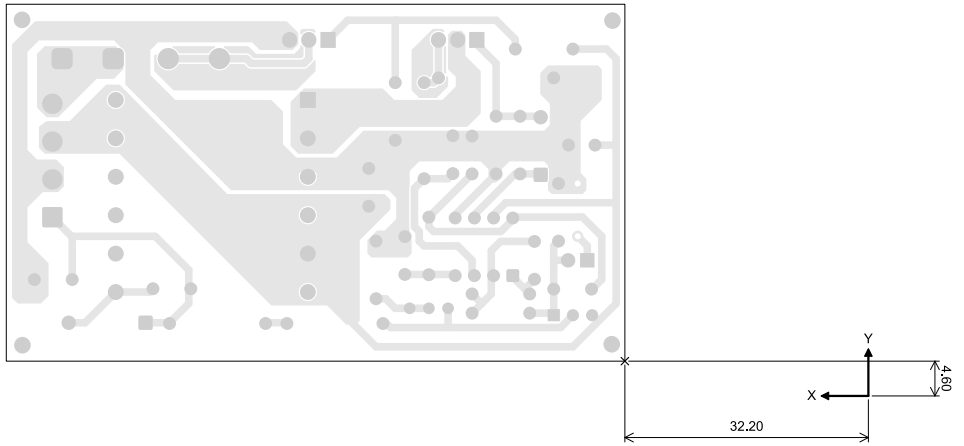
All dimensions are in millimeters unless otherwise specified.

	Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b
		Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
	Sheet Title: Top Test Points (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **5** of **8**

Module Fabrication Document

Bottom Test Points (Scale 1:1)

Ref.	Net	X [mm]	Y [mm]

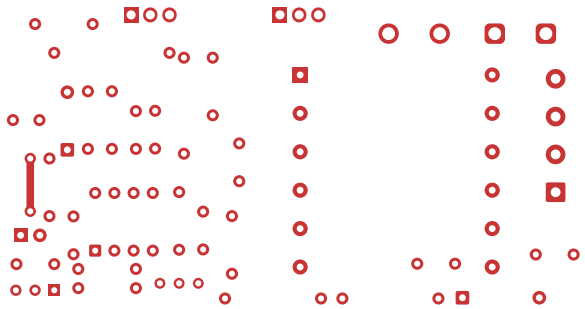


All dimensions are in millimeters unless otherwise specified.

	Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b
		Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
	Sheet Title: Bottom Test Points (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
	Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **6** of **8**

Module Fabrication Document

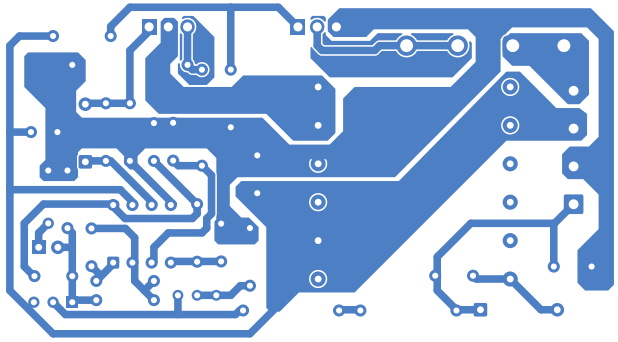
L1 (Sig, PWR) (Scale 1:1)



Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b	
	Board Name: **Module**		Project Name: **Step-up module 12:450 V**		
Sheet Title: L1 (Sig, PWR) (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)	
Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **7** of **8**	

Module Fabrication Document

L2 (Sig, PWR) (Scale 1:1)



Comments: Comment 1 Comment 2 Comment 3 Comment 4	Company: **FR**		Variant: PRELIMINARY	Git Hash: 357a42b
	Board Name: **Module**		Project Name: **Step-up module 12:450 V**	
Sheet Title: L2 (Sig, PWR) (Scale 1:1)	File Name: StepUp_module_12to450V.kicad_pcb	Designer: FR	Date: 2024-04-13	Revision: + (Unreleased)
Sheet Path:		Reviewer: NA	Size: **A4**	Sheet: **8** of **8**