Max Lan

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Education

University of Washington Seattle, WA

Bachelor of Science in Electrical and Computer Engineering, GPA: 3.62 (in major) *Sep. 2022 – Jun. 2026*

- Relevant Coursework: Embedded Systems, Digital Systems Design, Computer Architecture I, Systems Programming, Hardware/Software Interface, Device and Circuits I, Circuit Theory, Data Structures, Algorithm Design

Experience

Firmware Developer Oct. 2022 – Present

Husky Robotics, University of Washington *Seattle, WA*

- Developed PSoC-based CAN bridge firmware enabling seamless integration between PSoC MCU and ODrive microcontroller.
- Implemented firmware for BLDC motor control in robotic applications with real-time command execution.
- Achieved stable 250kbps data transfer through efficient CAN communication protocols between PSoC and ODrive systems.
- Enhanced PCB debugging efficiency by 30% using UART interfaces with PuTTY and oscilloscope signal analysis.
- Optimized servo motor control performance by 25% through developing automated firmware scripts.
- Implemented stepper motor precision control and mechanical assessments for enhanced robotic performance.

Undergraduate Researcher Oct. 2024 – Present

Nanophotonics and Photonics Lab, University of Washington *Seattle, WA*

- Developed FPGA-based AOBS controller using Verilog and Intel Quartus IP blocks for optical beam steering.
- Achieved sub-microsecond latency in optical beam steering applications through optimized FPGA implementation.
- Implemented bidirectional I^2C communication between embedded TI board (Time Digital Converter) and FPGA.
- Utilized OpenCore I^2C controller with wishbone interface for master/slave data transfer protocols.
- Developed efficient RF signal processing and control algorithms for precision beam steering applications.
- Designed comprehensive FPGA testbench and validation framework for embedded systems.
- Ensured reliable serial communication protocols between embedded systems through rigorous testing.

Projects

Five-Stage Pipelined ARM CPU | *SystemVerilog, ModelSim, Intel Quartus*

- Implemented 64-bit RISC-V ARM CPU with five-stage pipeline architecture for enhanced performance.
- Achieved 20% clock frequency improvement over single-cycle design through pipeline optimization.
- Developed data forwarding and hazard detection units in SystemVerilog for pipeline efficiency.
- Enhanced instruction execution efficiency by 40% through advanced pipeline hazard management.
- Utilized ModelSim simulation and Intel Quartus synthesis for comprehensive timing analysis.
- Conducted CPU performance validation through extensive testing and optimization procedures.

CAN_Bridge | *PSoC-Creator, C, PuTTY, Altium365, Odrive*

- Developed PSoC firmware for efficient CAN packet ID translation between ODrive and custom protocols.
- Achieved stable 250kbps communication through optimized CAN protocol implementation and validation.
- Implemented real-time CAN protocol conversion reducing communication latency by 25%.
- Enabled seamless ODrive integration for enhanced robotic system performance and reliability.
- Created custom Python validation scripts to configure and test ODrive CAN communication protocols.
- Reduced CAN communication error rate by 20% through comprehensive testing and optimization.
- Collaborated with hardware team to refine PCB design for robust signal integrity.
- Ensured reliable robotic applications through enhanced PCB design and signal validation.

Technical Skills

Languages: C, Python, SystemVerilog, Verilog, C++, Java, Bash/Shell Scripting, ARM/x86 Assembly, MATLAB, JavaScript, HTML, CSS

Software Tools: PSoC Creator, STM32CubeIDE, CCSTUDIO IDE, ROS2, Intel Quartus, Xilinx Vivado, Git, RTOS, Docker, ModelSim, PuTTY, Linux

Hardware Tools: LTSpice, MultiSim, Picoscope, Oscilloscope, Logic Analyzers, Altium Designer, KiCad