Max Lan

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Education

University of Washington Seattle, WA

B.S. in Electrical and Computer Engineering (June 2026) *Major GPA: 3.68/4.0*

- Relevant Coursework: Intro to Embedded Systems, Computer Architecture, VLSI I, Design of Digital Systems, Systems Programming, Hardware/Software Interface, Devices and Circuits I & II, Signals and Systems I, Data Structures and Algorithms

Experience

Embedded Systems Developer Oct. 2022 – Present

Husky Robotics, University of Washington *Seattle, United States*

- Configured CAN communication between ODrive S1 and PSoC MCU PCB designed by the hardware team, defining custom protocols for reliable data exchange with 500 kbps baud rate.
- Scripted custom Python frameworks with pytest for control model simulations, CAN packet transmission, and camera sensor control, handling up to 100 packets per second.
- Developed firmware on PSoC Infineon ARM Cortex to test servo and stepper motor functionality using PWM, achieving precise control over position, velocity, and torque within 5% error margin.

Undergraduate Researcher Oct. 2024 – Present

Nanophotonics and Photonics Lab, University of Washington *Seattle, United States*

- Executed ROS ecosystem migration of VINS-Fusion SLAM navigation stack from ROS1 to ROS2, resolving package dependencies and refactoring publisher/subscriber architecture.
- Modified Wishbone-compliant I^2C controller IP core with multi-master arbitration, integrated with Intel NIOS II soft processor for FPGA-based sensor fusion applications.
- Designed high-speed communication interfaces (UART, I^2C, SPI) between TI TDC7200 Time-to-Digital Converter and DE2-115 Cyclone IV FPGA for peripheral applications.

Firmware Engineering Intern Jul. 2025 – Sep. 2025

Asia Vital Components Co., Ltd. *Taipei, Taiwan*

- Researched and analyzed FOC, 6-step commutation, and sensorless estimation algorithms for BLDC/PMSM efficiency in ODrive 0.5.6 codebase; presented findings and built/flashed firmware on legacy STM32F4 ODrive v3.6 boards.
- Implemented CAN 2.0B stack with 500 kbps transmission, retry mechanism, and error handling via STM32 bxCAN; configured UART on serial console at 115200 bps to send CAN packets.
- Developed Mongoose HTTP server with WebSocket for 1kHz real-time ADC/PWM/UART data on NUCLEO-H563ZI via Ethernet; utilized REST API for state reflection and firmware upgrades.

Projects

64-bit Five-Stage Pipelined ARM CPU

- Designed and implemented a 64-bit pipelined processor with a five-stage architecture (IF, ID, EX, MEM, WB) using SystemVerilog, supporting LEGv8 instruction set with register file, ALU, and memory operations.
- Implemented data forwarding and hazard detection logic to resolve pipeline dependencies, along with branch prediction state machines to minimize control and data hazards.
- Validated functionality through SystemVerilog testbenches and ModelSim simulation for debugging and verification.

FPGA Taiko No Tatsujin

- Developed FPGA-based rhythm game on DE1-SoC, rendering scrolling red notes from ROM-preloaded frames synchronized to song rhythm via VGA display.
- Implemented algorithmic state machine, key input synchronization with edge detection, and combinatorial collision detection for scoring on 7-segment displays.
- Utilized PLL-generated 25 MHz clock for VGA timing and divided 50 MHz clock to 6 Hz for frame updates; simulated FSM and display logic in ModelSim waveforms.

Technical Skills

Languages: SystemVerilog, C, C++, Python, Java, TypeScript, MATLAB, ARM/x86 Assembly
Software Skills & Tools: STM32CubeIDE, Infineon PSoC Creator, ROS2, Intel Quartus, ModelSim, Xilinx Vivado, Git, PuTTY, Linux, GDB, LTSpice, Cadence Virtuoso, FreeRTOS
Hardware Skills & Tools: Oscilloscope, Logic Analyzer, PCB Design, IC Layout, Soldering