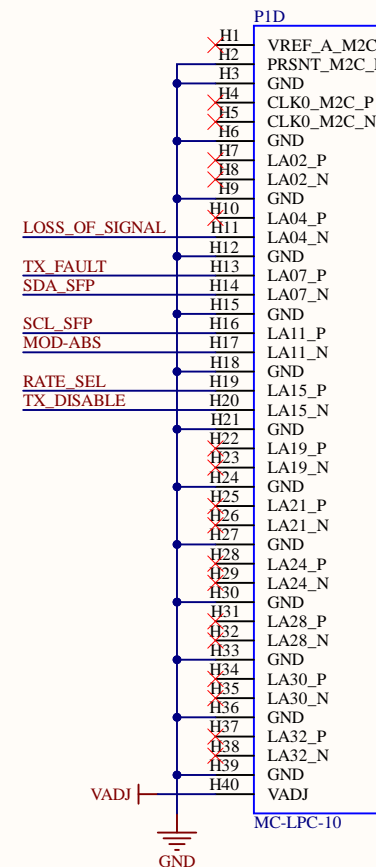
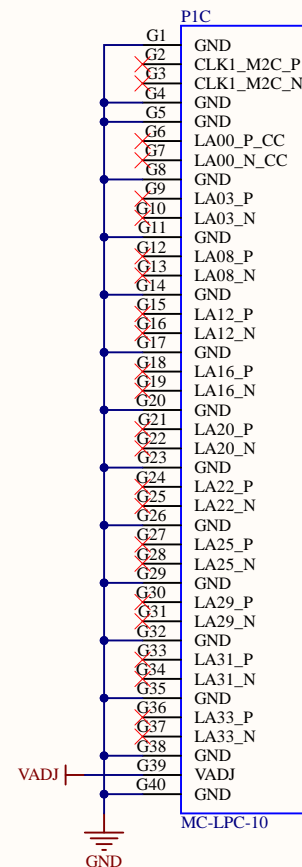
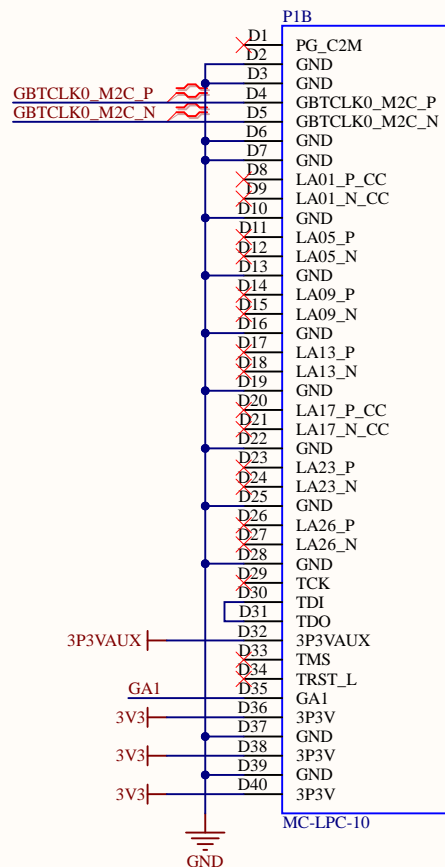
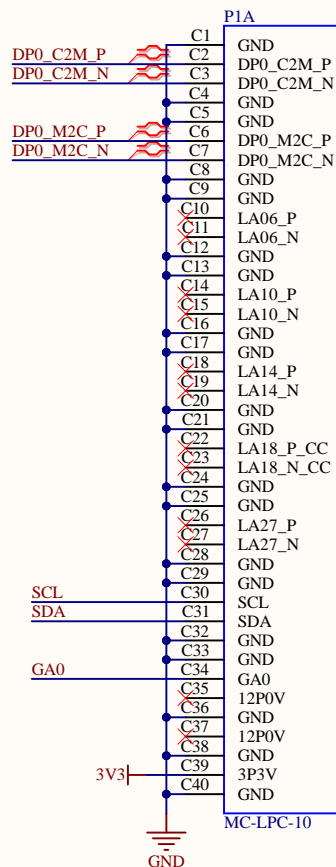
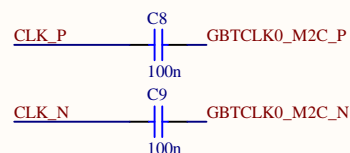


Low-pin count (LPC) connector

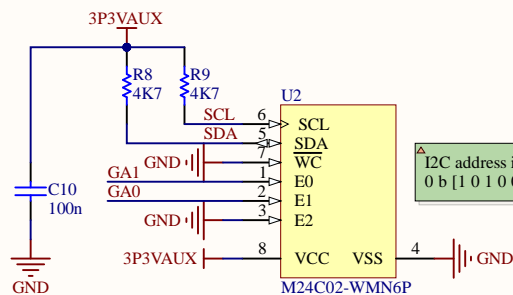


AC coupling for clock signal



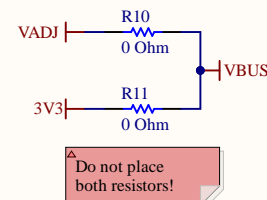
Clock is ac coupled on mezzanine, termination is on FPGA carrier

I2C EEPROM (256 Byte) for FRU information

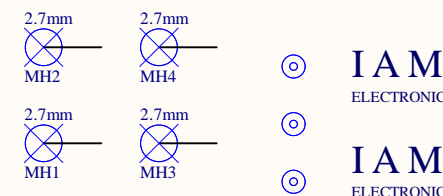


I2C address is:
0 b [1 0 1 0 0] [GA0] [GA1] [RW]

Voltage selection for I2C bus



Mounting holes (commercial grade mounting)



Title: Connector (LPC), Commercial grade mounting, FMC FRU EEPROM

Project: FMC-to-SFP Adapter

Website: www.fmchub.com

Date: 10.03.2021

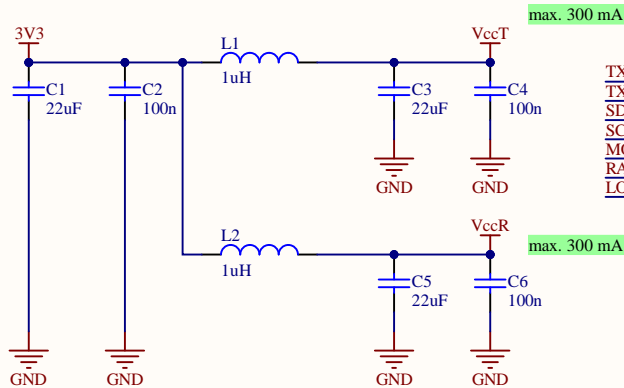
Engineer: PFH

Rev: A

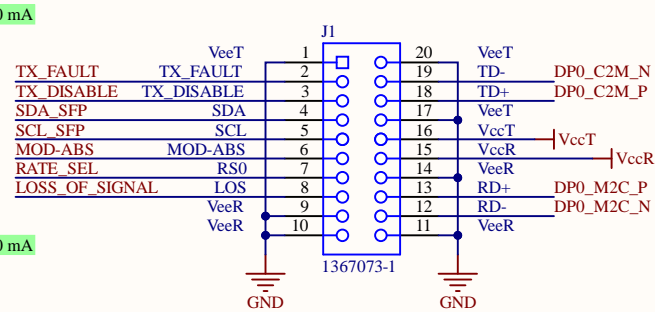
Sheet: 1 / 2

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Host board supply filtering network



SFP board connector



SFP Cage

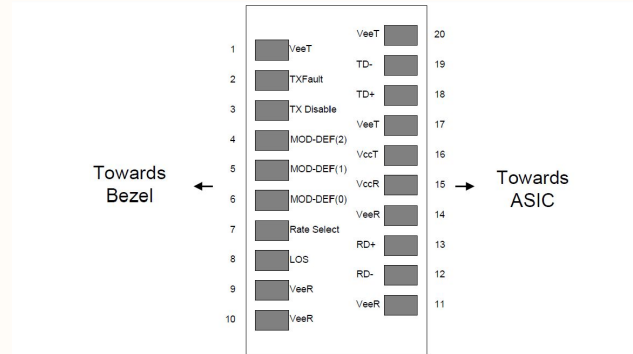
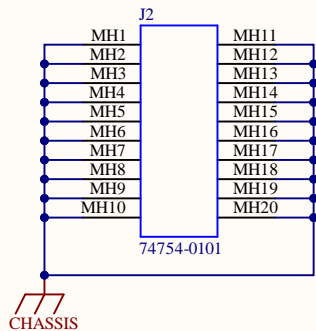
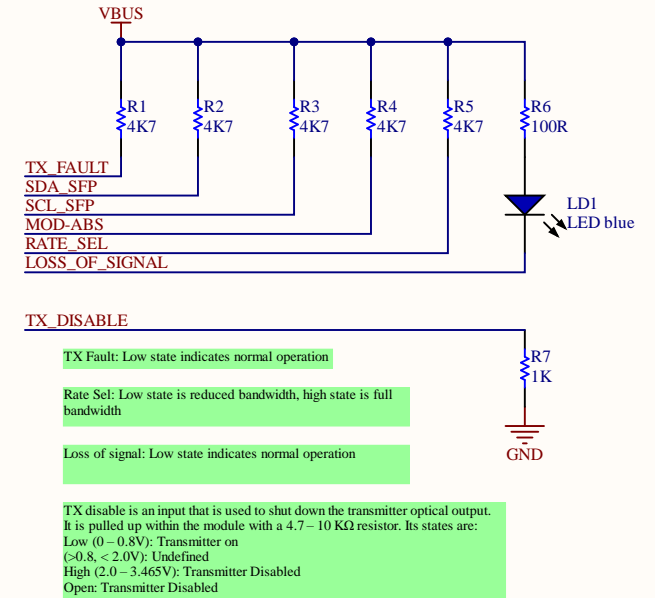
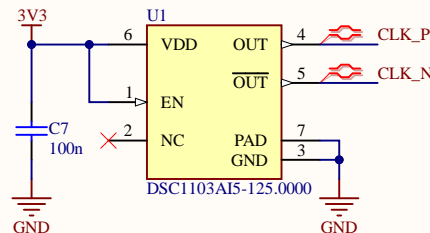
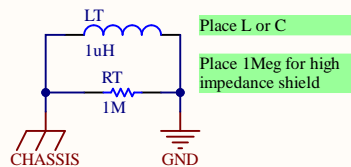


Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names

SFP configuration



Gigabit transceiver clock 125 MHz



Title: SFP Connector and case, power supply filtering and status flags, 125 MHz clock

Project: FMC-to-SFP Adapter

Website: www.fmchub.com

Date: 10.03.2021

Engineer: PFH

Rev: A

Sheet: 2 / 2

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