Title: **Modelling of Open Circuit Fault Analysis of 11 bus system using the Open IPSL**

Name of the Contributor: Aritra Banerjee

Institution/Organization: Meghnad Saha Institute of Technology, Kolkata

Email: aritrabanerjee343@gmail.com

Model Abstract:

The simulation represents Open Circuit Fault Analysis of 11 bus system. Open circuit faults have been simulated on standard IEEE 11 bus system. State of the system before and after the fault has been estimated in terms of bus voltages and line losses by solving load flow. Open circuit conditions have been simulated on the lines one by one and their effect on the bus voltages has been observed and most critical lines are sorted out. An electric power system should ensure the availability of electrical energy without interruption to every load connected to the system. Open Circuit fault occurs if a circuit is interrupted by some failure. The power system model consists of 5 generators, 11 buses, 6 loads, 18 lines. The system is on a 100 MVA base. The model submitted is implemented in Modelica language using Open IPSL package. A fault simulated at Bus 9 for the duration of 0.4 seconds (5 seconds to 5.4 seconds), the simulated voltage profiles of IEEE 11 bus system at various buses. For all analysis of this system, the lower voltage magnitude limits at all buses are 0.98 p.u and upper limits are 1.09 p.u. Simulation obtained shows voltage profiles at various buses.

Conclusion:

The implemented IEEE 11 bus model in Modelica represents the system behavior before and after the fault occurs at the 9 th bus. Bus voltage magnitudes (p.u.) of all 11 buses obtained are found to be between 0.98 p.u and 1.09 p.u. The relation between line impedance and fault severity observed. If there is any fault occurs in a system it can be a open circuit fault and here we observed a open circuit fault in a 11 bus system.