Title: Contingency Analysis of 16 bus test system using OpenModelica and OpenIPSL

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Abstract:

Contingency Analysis refers to the performance of the system when there is any outage of any of the elements in the power system. This project performs N-1 line contingency of one of the line in 16 bus test system. The parameters will be analysed with and without contingency. Simulations will be performed using OpenModelica and OpenIPSL.