```
//example 8.6(b)//
clc
//clears the screen//
clear
//clears all variables//
close
//closes all existing files//
disp('When the ENABLE input is LOW, the upper AND gate is disabled(with
its output going to logic 0) and the lower AND gate is enabled(with its
output becoming the same as the Q output owing to the feedback). The
NOR gate output in this case is Q'', which means that the Q output
holds its state as long as the ENABLE input is LOW')
```