PROJECT PROPOSAL

PROJECT TITLE:

Design of FLIP-FLOP's using MULTIVIBRATOR circuit.

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EXECUTIVE SUMMARY:

This proposal is based on the design of different types of driven filpflop circuits using bistable multivibrator circuit in ESIM software. The bistable multivibrator itself is designed using the NAND gates and is fixed as one of the component. The remaining 4 circuits are designed by altering the basic circuit of a bistable multivibrator that is constructed using 2 NPN transistors. The multivibrator circuit with NAND gates are designed using the Subcircuit option as mentioned earlier. This project proves to be as a connector which connects the ANALOG circuits [bistable multivibrator] with DIGITAL circuits [flipflops].

PROJECT DESCRIPTION:

The project consists of a task of designing 5 different components by using the ESIM- software. The components chosen for designing are listed above in the table.

DESIGN 1: **BISTABLE MULTIVIBRATOR using NAND gates.**

TITLE	DESIGN OF BISTABLE MULTIVIBRATOR
COMPONENTS DETAILS	NAND GATES [SCHMITT]
DESCRIPTION	The circuit consists of 3 Schmitt NAND gates in which 2 of the NAND gates form the circuit of SR flipflop. The remaining 1 NAND gate is used to trigger the SR flipflop. This triggering is achieved by feeding the inputs of the SR flipflop with the SET terminal connected to the External Trigger Pulse that is provided to the shorted inputs of the 1st NAND gate whereas the RESET terminal is connected with the output of the 1st NAND gate. This circuit is built using Sub-circuit Modelling.

DESIGN 2: **Base Driven Flip-Flop Circuits using Separate paths. [SR flipflop]**

TITLE	DESIGN OF SET-RESET FLIPFLOP
COMPONENTS DETAILS	Transistors, Resistors, Diodes, Capacitors
DESCRIPTION	As per the circuit initially the transistor T1 is saturated and T2 is in OFF state. When a driving trigger input [clock signal] is applied to the base of T2 through R2C2 it is differentiated and the output is given to Diode D2 this allows the negative peak thus the transistor T2 is even more blocked by the negative voltage peak. Thus the switching does not take place in this case. This process repeats for T1 in OFF and T2 saturated. By considering the base of T2 and T1 as the input terminals SET-RESET terminals the switching operations of the transistor for the given Trigger inputs resembles the operation performed by the SR filflop for a given clock pulse.

DESIGN 3: **Base Driven Flip-Flop Circuits using Separate paths. [JK flipflop]**

TITLE	DESIGN OF JK FLIPFLOP
COMPONENTS DETAILS	Transistors, Resistors, Diodes, Capacitors
DESCRIPTION	As per the circuit initially the transistor T1 is saturated and T2 is in OFF state. When a driving trigger input [clock signal] is applied to the collector of T2 it passes the signal to the base terminal where it is differentiated by R2C2 and the output is given to Diode D2 this allows the negative peak thus the transistor T2 is even more blocked by the negative voltage peak. Thus the switching does not take place in this case. This process repeats for T1 in OFF and T2 saturated. By considering the collectors of T2 and T1 as the input terminals i.e, J-K terminals the switching operations of the transistor for the given Trigger inputs resembles the operation performed by the JK filflop for a given clock pulse.

DESIGN 4: **Collector Driven Flip-Flop Circuits using Common paths. [T flipflop]**

TITLE	DESIGN OF TOGGLE FLIPFLOP
COMPONENTS DETAILS	Transistors, Resistors, Diodes, Capacitors
DESCRIPTION	As per the circuit initially the transistor T1 is saturated and T2 is in OFF state. In this circuit the R1, R2 resistors of T1, T2 are connected to the collectors C1, C2. The base capacitors of T1, T2 are short circuited through which external trigger input [T- input] is applied. When a driving trigger input [clock signal] is applied it is differentiated by 2 different RC networks at the same time. The differentiated output is passed to Diodes D1, D2 respectively. These diodes conduct onlu negative peaks of the differentiated outputs obtained. Hence conduction occurs only through the transistor present in the saturation state. This condition is maintained throughout the clock cycle and hence alternate switching of transistors T1 and T2 resembles the working of T- flipflop.

DESIGN 5: **Collector Driven Flip-Flop Circuits using Common paths. [D flipflop]**

TITLE	DESIGN OF DELAY FLIPFLOP
COMPONENTS DETAILS	Transistors, Resistors, Diodes, Capacitors
DESCRIPTION	As per the circuit initially the transistor T1 is saturated and T2 is in OFF state. In this circuit the R1, R2 resistors of T1, T2 are connected to the collectors C1, C2. The collecotr capacitors of T1, T2 are short circuited and replaced by a single capacitor through which external trigger input [D- input] is applied. When a driving trigger input [clock signal] is applied at the collector of transistors it is passed to Diodes D1, D2 respectively. These diodes conduct only negative peaks of the differentiated outputs obtained. Hence conduction occurs only through the transistor present in the saturation state. This condition is maintained throughout the clock cycle and hence alternate switching of transistors T1 and T2 resembles the working of D- flipflop.

INFERENCE: **Design of MOD-15 Counter using the above mentioned flipflops**

TITLE	DESIGN OF MOD-15 COUNTER
COMPONENTS DETAILS	Transistors, Resistors, Diodes, Capacitors, flipflops [SR,T, JK, D]
DESCRIPTION	The inference from the above mentioned designs is to design a MOD-15 COUNTER by using all the above mentioned different driven flipfop circuits which were constructed using the ordinary bistable multivibraor circuit. The development of MOD-15 COUNTER by using 4 flipflops which controls the next state output of each bit present in the COUNTER will be the flipflops that are designed by the conventional bistable multivibrator circuit under 2 different driven and path configuration.

CONCLUSION:

In this project we have created the different types of flipflop circuits using the BISTABLE multivibrator that deploys only discrete analog components such as transistors, resistors, capacitor etc. Hence we have tried to interface the ANALOG and DIGITAL circuits by creating flipflop[s using multivibrators and also we have created a multivibrator using the logic gates. At the end of this project we have also tried to establish a MOD-15 counter using the designed 4 different flipflops to govern the next state of 4 bit output for the counter. Hence it is proved that both ANALOG and DIGITAL circuits go hand in hand in the development of different circuits in all the modern inventions.

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