Analysis of Ethernet-Switch Traffic Shapers for In-Vehicle Networking Applications

Sivakumar Thangamuthu, Nicola Concer
Central R&D, CTO Office
NXP Semiconductors
Name.Lastname@NXP.com

Pieter J.L.Cuijpers and Johan J.Lukkien
Department of Mathematics and Computer Science
Technische Universiteit Eindhoven
P.J.L.Cuijpers@TUE.nl and J.J.Lukkien@TUE.nl

***Abstract*—Switched Ethernet has been proposed as network technology for automotive and industrial applications. IEEE AVB is a collection of standards that specifies (among other elements) a set of network traffic shaping mechanisms (i.e., rules to regulate the traffic flow) to have guaranteed Quality of Service for Audio/Video traffic. However, in-vehicle control applications like advanced driver-assistance systems require much lower latencies than provided by this standard. Within the context of IEEE TSN (Time Sensitive Networking), three new traffic shaping mechanisms are considered, named Burst Limiting, Time Aware and Peristaltic shaper respectively. In this paper we explain and compare these shapers, we examine their worst case end-to-end latencies analytically and we investigate their behavior through a simulation of a particular setup. We show that the shapers hardly satisfy the requirements for 100Mbps Ethernet, but can come close under further restrictions. We also show the impact the shapers have on AVB traffic.**

Keywords: Ethernet switching, IEEE 802.1AVB, IEEE 802.1TSN, In Vehicle Networks

I. Introduction

The bandwidth requirements of modern and future automotive applications are quickly reaching the limits of the established In-Vehicle Networking (IVN) technologies such as LIN, CAN and FlexRay. The recent introduction of the *BroadR-Reach* technology enabled the use of a 100Mbps Ethernet link over an unshielded twisted pair copper wire while limiting the electro-magnetic interference emissions below the threshold imposed by automotive application requirements [1], [2]. BroadR-Reach, which is now under standardization in the working group *IEEE P802.3br*, implements a point to point communication technology. More complex network topologies are defined by using ISO Layer 2 (bridges) or Layer 3 (routers) switches.

Switches enable complex network topologies while offering basic services such as relaying of frames from one source node to multiple destinations, as well as more complex ones such as channel bandwidth allocation, network partitioning via Virtual LANs (VLANs) and traffic prioritization [3]. Switched Ethernet networks have been implemented in the automotive market for supporting telemetry (via On-Board Diagnostic, *OBD2* port) and bandwidth-intensive applications such as vehicle surround-view applications. It accomodates recent developments in the entertainment and Advanced Driver Assistance Systems (ADAS) domains that require very flexible networks targeted to support a vast range of traffic patterns with minimal configuration complexity, low implementation cost but with a guaranteed Quality of Service (QoS).

In the entertainment domain the IEEE defined *Audio/Video Bridging* (AVB), a set of standards that allows switches to identify different types of traffic patterns, categorize them into specific traffic classes, and assign a different QoS to each class. An important element of AVB is *IEEE 802.1Qav* "*Forwarding and Queuing for Time-Sensitive Streams*" (FQTSS). Here IEEE defined the *Credit-Based Shaper* (CBS), the main AVB mechanism responsible for selecting the next frame to be transmitted from a network interface of switches or end-nodes. Through the (scheduling) rules defined by this shaper, specific guarantees are given to time-sensitive traffic such as video and audio streams. Timing properties resulting from AVB traffic shaping are not sufficient for automation and control applications. To build upon the success of the AVB standards, automotive and industrial OEMs together with software and electronic-components suppliers joined their efforts in the *AVnu* alliance [4], to further extend the capabilities of the AVB standards [5]. The AVnu alliance participated in the definition of a new set of requirements captured in the revised version of the IEEE AVB standards, recently renamed as IEEE *Time-Sensitive Networking*, IEEE 802.1TSN [6]. A key new feature of TSN is the definition of new traffic shaping mechanisms capable of accommodating hard real-time streams with deterministic end-to-end delays. At the time of writing, TSN is evaluating a set of new traffic shaping mechanisms, respectively called *Time-Aware* (TAS), *Burst-Limiting* (BLS) and *Peristaltic* (PS) shaper.

Contribution. In this work we perform the analysis and comparison of these three traffic shapers with respect to delay performance. We evaluate the worst-case behavior of the traffic shapers through analysis and simulation in a scenario where the controllers are synchronized to avoid intra-control interference. This allows us to focus on the traffic shaping rather than on the access control mechanism. In particular, we evaluate the impact of AVB traffic on control traffic, and vice-versa.

Related Work. The capabilities of switched Ethernet to accommodate real-time data traffic have been investigated extensively. Two main approaches include the synchronized time-triggered based medium access approach and the asynchronous event-triggered approach by over-provisioning and prioritizing. An example of the former technique is TTEthernet (AS6802) [7] and of the latter technique, the IEEE802.1AVB standard with Credit Based traffic shaping (CBS) [3]. Bordoloi *et.al.* investigate the worst-case response time for standard

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Traffic Class	Frame Interval	Max End-to-End Delay
Class A	125μs	2ms over 7 hops
Class B	250μs	50ms over 7 hops
Class BE	n.a.	n.a.

TABLE I. TRAFFIC CLASSES SPECIFICATIONS IN IEEE 802.1AVB. NO RESTRICTION ON FRAME SIZES.

AVB streams targeting applications with hard real-time constraints [8]. The paper proposes a precise model to first analyze the CBS mechanism and then propose a set of updates to improve the performance of the shaper. Boiger *et.al.* [9] provide a comparative study of the *Burst-Limiting* and *Peristaltic* shapers which are also considered in our work. Different from our approach, the authors consider a traffic-overloaded scenario and do not discuss the end-to-end latencies achieved by the control data traffic, which is the main contribution of our analysis. Götz *et.al.* compare the *Burst-Limiting* and the *Time-Aware* shapers, also considered in our work, considering a large industrial network [10]. Here the authors investigate the impact of the frame size on the overall network performance. In our work we target smaller automotive networks which also support AVB streams. Meyer *et al.* present a network scenario to analyze the impact of the Time-Aware shaper on AVB Class A traffic [11]. The authors present a theoretical analysis for the maximum end-to-end latency of an AVB Class A traffic class and compare it with results from simulation. In our work we address such analysis as well but we include the Burst-Limiting and Peristaltic shapers. Cummings describes the performance tradeoffs to achieve a certain end-to-end latency in AVB [12]. In our work, we use the papers of Rahmani and Cummings for defining a static schedule for control data traffic in the TAS. Finally the presentations of D.Pannel, C.Boiger and M.Kießling from various IEEE meetings provide illustrations and theoretical methods to compute the worst case end-to-end latency for a control data frame [13], [14], [15]. These works offer valuable details for identifying the worst case behavior of each of the traffic shapers. In our work we used these details in computing the theoretical maximum values for end-to-end latencies.

II. IEEE AUDIO VIDEO BRIDGING

IEEE802.1AVB defines a collection of standards aimed at optimizing the transmission of audio and video streams over an Ethernet network. AVB Streams are classified according to a set of *Traffic Specifications* composed by two main elements: *i*) *Maximum Frame Size*: indicating how much data is periodically generated by the stream source *ii*) *Minimum Frame Interval*: indicating how often this data is sent at worst. IEEE AVB defines three traffic classes based on these traffic specifications, viz. *Class A, Class B* and *Class BE*. Class A has the highest priority and is indented to transport audio samples. Class B uses the next priority below Class A and it is intended for transporting video streams. Class BE has no restriction on arrival interval as it is classified to include legacy Ethernet traffic. The frame sizes of both Class A"&"B and Class BE traffic depends on the application and can take a maximum Ethernet frame size. Table I lists the traffic class specification and their QoS constraints.

According to the AVB standard, all egress ports of switches and end-nodes belonging to the AVB network (or AVB domain) must be equipped with multiple output queues, each queue representing one or more priority levels. Each time the underlying physical interface becomes available a transmission-selection mechanism selects the next frame to transmit choosing among the queues that are enabled for transmission. A generic queue associated with Class BE traffic is enabled if at least one frame is stored in the corresponding queue. A queue supporting AVB traffic classes A or B is enabled for transmission precisely when the following two conditions hold: *i*), a frame is stored in the queue and *ii*), the CBS associated with that queue is enabling the transmission.

Traffic Class	Max Frame Size	Min Frame Interval	Max End-to-End Delay
Class CDT	128 bytes	500μs	100μs / 5 hops
Class A	256 bytes	125μs	2ms / 7 hops
Class B	256 bytes	250μs	50ms / 7 hops
Class BE	256 bytes	n.a.	n.a.

TABLE II. TRAFFIC SPECIFICATIONS IN IEEE802.1TSN

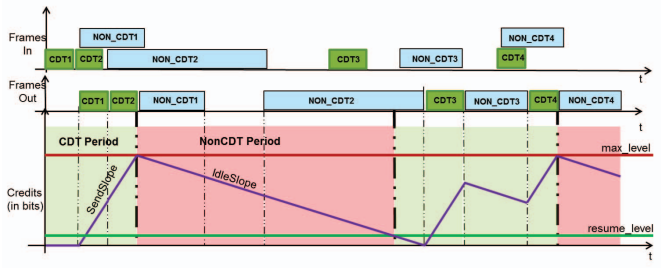


Fig. 1. Operation of a Burst-Limiting shaper.

IEEE AVB also defines a set of standards that provide features specifically designed for audio and video transmission. **IEEE 802.1AS** is a Timing and Synchronization protocol that enables the definition of a common time-reference which is essential for distributed audio and video playback applications. **IEEE 802.1Qat** "*Stream reservation protocol*" is a distributed protocol that allows the sources of audio and video streams, called *talkers*, to *advertise* available streams to potential *listeners*. This protocol also enables listeners to *register* to a stream by reserving and allocating the necessary bandwidth in the switches located on the path between the talker and itself. **IEEE 802.1Qav** specifies the mentioned Credit-Based shaper mechanism that enables the transmission of AVB and non-AVB legacy Ethernet frames. CBS is not explained in detail in this work as the focus is to compare the emerging traffic shaping mechanisms. Finally **IEEE 802.1BA** - Audio Video Bridging Systems defines the AVB profile of configurations and features that all AVB-compliant systems should have.

III. IEEE TIME-SENSITIVE NETWORKING

IEEE 802.1TSN aims to provide the specifications that allow time-synchronized low-latency streaming services for time-critical control applications in automotive and industrial networks. TSN introduces a new Control-Data Traffic (CDT) class, referred to as *Class CDT*. To achieve required guarantees, TSN assigns the highest priority to Class CDT (i.e. higher than Class A/B). Further, TSN imposes maximum frame-size restrictions on all traffic classes. Table II lists the modified traffic specifications with their new constraints, defined for 100 Mbps links [16], [17][1]. There are three techniques to improve

[1]These specifications are based on the general agreement during the plenary meetings of the standardization committee since the standardization is under progress.

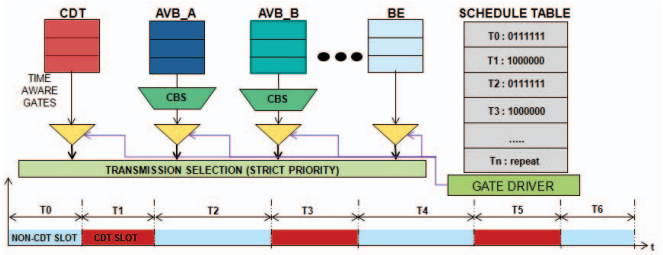


Fig. 2. Operation of a Time-Aware Shaper.

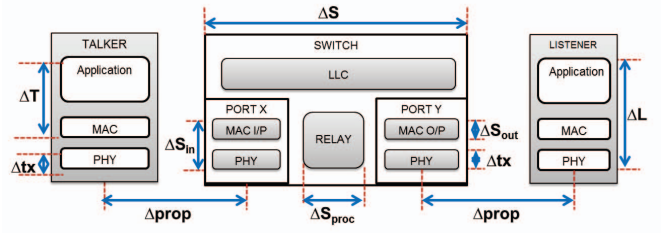


Fig. 3. Delay model used in our worst-case analysis.

the Credit-Based shaping mechanism of IEEE802.1AVB in order to achieve better latencies: *i*) send multiple CDT streams in frame bursts; *ii*) minimize interference from other traffic and *iii*) limit frame residence time. These techniques are used in the three new shapers we discuss below.

A. Burst Limiting Shaper

BLS limits bursts of CDT to remain within well-defined thresholds. BLS enables the queue allocated for supporting CDT traffic by using a *credit-counter* and by introducing a new concept of dynamic queue priority for the CDT queue. A CDT queue is enabled to transmit when *i)* the value of the credit counter associated with the queue is below a threshold max_level and *ii)* the priority of the CDT queue is higher than the priorities of all other existing traffic queues. When a CDT frame is being transmitted the credit counter is incremented at a $sendslope$ rate, while when a frame from a non-CDT queue is selected for transmission or when there is no frame in any of the queues the credit counter is decremented at a rate defined by the $idleslope$ parameter [18]. When the credit counter reaches an upper threshold max_level the priority of the CDT queue changes to the lowest possible value. The priority is finally restored when the counter reaches a pre-defined $resume\_level$. Fig.1 illustrates the operation of BLS in an Ethernet switch. Frames-In represents the arrival of frames in the input ports of the switch targeting the same output port and Frames-Out represents the frames that are being transmitted. Frames are numbered in the order they arrive and named according to their traffic class. Note that the frames are selected for transmission only if they are completely received. The `CDT Period` and `Non-CDT Period` shaded regions represent the regions in the timeline where the priority of the CDT queue is the highest and the lowest respectively.

Given the bandwidth requirement for a CDT class traffic over a link (BW_{CDT} in % of total BW in Mbps), the parameters of the BLS shaper on each network interface are computed as follows:

$$idleslope = BW_{CDT} \times portTxRate \quad (1)$$

$$sendSlope = portTxRate - idleslope \quad (2)$$

$$max\_level = idleSlope \times (\Upsilon + \tau) \quad (3)$$

where $portTxRate$ is the port transmission rate (e.g. 1000Mbps), Υ is the common transmission period of the CDT traffic, i.e., the maximum duration of a burst, which is assumed to be 500 μs by IEEE 802.1TSN [16]. τ is an overload tolerance (overshoot of max_level) within a transmission period. $resume\_level$ is set as a fixed percentage of max_level.

B. Time Aware Shaper

TAS provides latency guarantees by using a pre-defined scheduler that guarantees timely transmission of CDT traffic. Furthermore, the existence of a mechanism is assumed that ensures that non-CDT traffic will not interfere with TAS traffic. TAS defines a fixed and periodic schedule of time intervals which specifies when a traffic queue is enabled (opened) or disabled (closed) for transmission. This schedule is configured offline. Fig.2 shows an example of a schedule with CDT and non-CDT time slots. Opening/closing is implemented by associating each queue of the output port with a time-aware transmission *gate* [19]. These gates are triggered by a *gate driver* which takes a schedule as input and opens or closes the gates accordingly. As shown in the figure, the list of gate configurations is composed of two main fields: *i*) a time indicating the duration of a new configuration, *ii*) a binary gate configuration list representing an open or close event for each queue. The last entry in the schedule is always a repeat event which signifies the end of the present *cycle* and starts the next one. A cycle represents a complete CDT transmission period which is 500μs according to IEEE 802.1TSN [16].

C. Peristaltic Shaper

The Peristaltic shaper is currently at an early drafting stage in the IEEE 802.1TSN working group[2]. PS reduces the end-to-end latency of CDT frames by minimizing their residence time inside the Ethernet switches. PS achieves this by dividing the time line into `odd` and `even` phases of equal widths [20]. Received frames are "tagged" with the phase in which they are received and their residence time in the switch is dependent on the width of the *peristaltic phase* Δps. The value of Δps is determined based on the required maximum end-to-end latency of a CDT stream and the maximum size of the CDT frames. IEEE 802.1TSN specifies the maximum end-to-end latency for CDT frames over 5 hops to be $100\mu s$ therefore imposing[3] $\Delta ps \leq 20\mu s$. A CDT frame received in an odd peristaltic phase is selected for transmission in the successive even peristaltic phase and vice versa. If a CDT frame is forced to wait more than one peristaltic phase due to the interfering traffic, the waiting frame is transmitted as soon as the interference ends, ignoring phase difference. The key internal states for PS are the current transmission phase: *pTphase* and the phase at which a frame was received: *pRphase*. These binary values are computed as follows:

$$pRphase = \lfloor ReceiveTime/\Delta ps \rfloor \bmod 2 \quad (4)$$

$$pTphase = \lfloor CurrentTime/\Delta ps \rfloor \bmod 2 \quad (5)$$

[2]The final standard might differ from the one presented in this work.

[3]Neglecting the propagation delay.

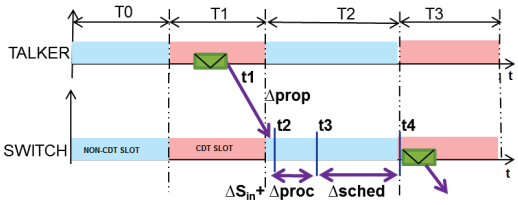


Fig. 4. Worst Case for Time Aware shaper in a two hop scenario.

IV. Analytical Model for Worst Case Analysis

In this section we define a worst-case analytical model that we use throughout the paper. Fig.3 shows the delay components involved in sending a frame from talker T to the listener L over the switch S. From this, we derive a generalized equation governing the end-to-end latency of a frame over n hops. In our model, a frame is created and processed by the IEEE AVB/TSN stack on the talker side with ΔT delay. Once the frame is ready to be transmitted the PHY interface transmits it taking $\Delta tx(bits, tx_{PHY})$ units of time. Δtx is a function of the frame size *bits* including the Ethernet encapsulation fields, and the transmission rate of the port tx_{PHY}. $\Delta prop$ and ΔS_{in} capture the link traversal delay of the first bit and the frame processing delay once this has been fully received in the MAC input port of the switch. The $\Delta proc$ delay captures the frame "filtering" delay where the switch searches its internal tables to select the output ports to be used for forwarding the frame[4]. $\Delta Sout$ captures the time until the out-bound MAC frame is transmitted and is determined by the specific chosen traffic shaper. Finally ΔS captures the overall time that a frame spends in a switch and is defined as:

$$\Delta S = \Delta S_{in} + \Delta proc + \Delta Sout \tag{6}$$

In this model we set $\Delta S_{in} + \Delta proc = 5\mu sec$ based on literature [21]. A generalized equation to express the end-to-end latency of a frame over n hops is now given by:

$$\Delta P(n) = \Delta T + n \times (\Delta tx + \Delta prop) + (n-1) \times \Delta S + \Delta L \tag{7}$$

Below we examine for each considered traffic shaper the value of $\Delta Sout$. Since the CDT traffic can be controlled at the source, in this work we avoid the interference among the CDT traffic by optimal arrangement of CDT traffic generation. So the worst case defined in this work involves only the interference generated by the non-CDT traffic.

Burst Limiting Shaper. The worst case for the BLS occurs due to interfering traffic. When the CDT queue is empty, BLS can select non-CDT frames for transmission. These non-CDT frames can cause delays for CDT frames that need to wait until the end of the transmission. The maximum residence time ΔS is thus determined by an interference term

$$\Delta Sout_{BLS} = \Delta int \tag{8}$$

where Δint is the time needed to transmit the interfering frame. In worst case, this is the Δtx of a non-CDT frame with maximum frame size.

[4]Note that in an actual implementation this operation could be done in parallel with the frame input processing stage.

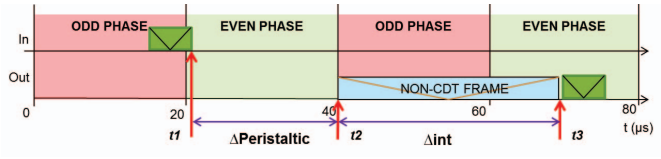


Fig. 5. Worst Case for Peristaltic shaper in a two hop scenario.

Time Aware Shaper. Given the specific characteristics of the TAS, the worst case for this shaper occurs when the schedule of a specific stream is not optimally allocated. The simplest schedule configuration for TAS uses a common schedule in all the nodes of the network. Assuming that all the nodes are perfectly synchronized, the starts and ends of CDT slots are also perfectly synchronized and occur at the same time at all nodes. Fig.4 shows such a synchronized schedule for a two hop network with a Talker sending a CDT frame to a Listener over a switch. The Talker transmits a CDT frame at time *t1*. This frame reaches the switch at time *t2* which happens to be at the beginning of a non-CDT time-slot. Since at this point the CDT gate is closed, the frame has to wait for the next slot starting at *t4*. This fact adds a new delaying effect here called $\Delta sched$. So, the maximum residence time for a CDT frame in a switch using TAS is determined by a maximum scheduling term:

$$\Delta Sout_{TAS} = \Delta sched \tag{9}$$

Here, $\Delta sched$ represents the maximum time between two CDT slots in the schedule.

Peristaltic Shaper. The PS restricts the residence time of a CDT frame inside a switch to a maximum value Δps. Fig.5 shows a worst case scenario at an output port of a switch. At time *t1* a CDT frame is received, which happens to be the beginning of an even peristaltic phase. This frame is to be selected for transmission only at time *t2* which is the beginning of the next peristaltic phase (odd phase). But just before time *t2*, a non-CDT frame is selected for transmission and it occupies the output link at time *t2*. Now, the CDT frame is blocked and can be selected for transmission only at time *t3* when the non-CDT frame releases the link. The maximum residence time of a CDT frame inside a switch using Peristaltic shaper is therefore determined by the combination of interference and peristaltic delay.

$$\Delta Sout_{PS} = \Delta ps + \Delta int \tag{10}$$

V. Evaluation

To evaluate the traffic shapers and their worst-case behaviors we simulate a realistic automotive scenario derived form the work of Meyer *et.al.*[11]. Here we set the traffic configuration according to the most recent Automotive traffic specifications discussed in IEEE TSN [16], [17]. The topology shown in Fig.6 consists of eleven nodes interconnected via three switches. Class BE traffic is broadcast at random intervals following a Poisson distribution by nodes N0 and N10, and is received by all other nodes in the network. AVB Class A traffic generated every 125μs at nodes N1 and N2 is targeted towards N8. Class CDT traffic has two streams from nodes N3 and N4 to N7, and two other streams from nodes N5 and N6 to N9. The CDT transmissions from these nodes are scheduled at 100, 200, 300 and 400μs of every 500μs

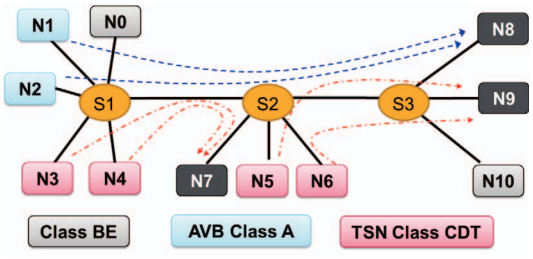


Fig. 6. The considered traffic scenario with AVB-Class A, Class BE and Class CDT traffic.

transmission interval. All streams use a frame size defined in Tab.II. This topology and the traffic configuration provides a high probability of non-CDT interference with Class CDT traffic. The data transmission rate is 100Mbps at all links in the network. Class CDT traffic occupies a total bandwidth of 11Mbps andd Class A traffic occupies 42Mbps. To push the network towards a worst-case scenario we set BE to occupy the remaining bandwidth accepting the fact that some BE frames may be dropped because of excessive load.

General observations. Tab.III shows the results for each of the shapers in detail. All Class CDT streams take three hops to reach their destination. So, the aimed for end-to-end latency requirement for Class CDT in this scenario is 60μs (cf. 100μs over 5 hops). Fig.7(a) shows the cumulative distribution function (CDF) of ΔP latency for Class CDT frames from N6 to N9 with all three traffic shapers. Here TAS provides a constant end-to-end latency for all Class CDT frames (50.598μs) with no noticeable jitter. We have assumed that TAS traffic is generated precisely at the beginning of a TAS time slot, and we have chosen the CDT time slot large enough to fit end-to-end transfer of an entire frame. In addition, nodes are strictly synchronized. This means effectively that $\Delta sched = 0$. The expense is a rather large bandwidth reservation, proportional to the longest path of CDT traffic. Without this synchronization, TAS performs worse than the other two shapers. From the figure we see that both BLS and PS fail to meet the maximum end-to-end latency requirement of 60μs. This is because of the interference from non-CDT frames at S1 and S2 switches. For BLS, ΔP of CDT frames has a jitter of 49.2μs computed as the variation between the maximum and minimum delay. As expressed in Eq.8 the major contributors to this jitter are interfering non-CDT frames. In the simulations the theoretical maximum (106μs) is never reached. The PS shows the worst ΔP among the three shapers. Also PS has the worst minimal ΔP (56.56μs) which is 6μs higher than the theoretical minimum of 50.6μs. According to Eq.10 this minimum is reached when in each switch the interference of other frames is zero and the synchronization is such that the peristaltic delay Δps is not counted. Finally the wide variation in ΔP shows a jitter of 63.16 μs which is the largest among the three shapers.

Proposed Improvement for Peristaltic Shaper. The performance of PS can be improved by implementing a $guardband$ to limit the interference Δint from non-CDT frames (from here on referred as PS^g). As shown in Fig.5, there can be cases in which the switch is aware that a CDT frame is available for transmission (e.g. at time *t1*). Here the switch can avoid the

Shaper	Traffic Class	Max ΔP (μs)	Min ΔP(μs)	Max Jitter(μs)
Burst Limiting	Class CDT	102.35 (106)	53.16 (50.59)	49.20
	Class A	245.68	171.92	73.76
	Class BE	5472.00	290.40	5181.92
Time-Aware	Class CDT	50.59 (326)	50.59 (50.59)	0.00
	Class A	448.32	398.32	50.00
	Class BE	14807.90	393.36	14414.60
Peristaltic	Class CDT	119.72 (146)	56.56 (50.59)	63.16
	Class A	253.88	184.88	69.00
	Class BE	5489.12	341.99	5147.13
Peristaltic with guard band	Class CDT	91.28 (106)	65.28 (50.59)	26.00
	Class A	257.92	181.56	76.36
	Class BE	5511.04	341.99	5169.04

TABLE III. SIMULATION RESULTS GIVING EXTREME END-TO-END DELAY FOR THE STREAMS $N1 \rightarrow N8$ (CLASS A), $N0 \rightarrow N8$ (CLASS BE) AND $N6 \rightarrow N9$ (CLASS CDT). WORST-CASE NETWORK LATENCIES ARE PLACED IN BRACKETS WHERE APPLICABLE. FOR TAS, THE ANALYTICAL RESULT CONSIDERS THE MAXIMUM POSSIBLE $\Delta sched$ FOR THE SCENARIO.

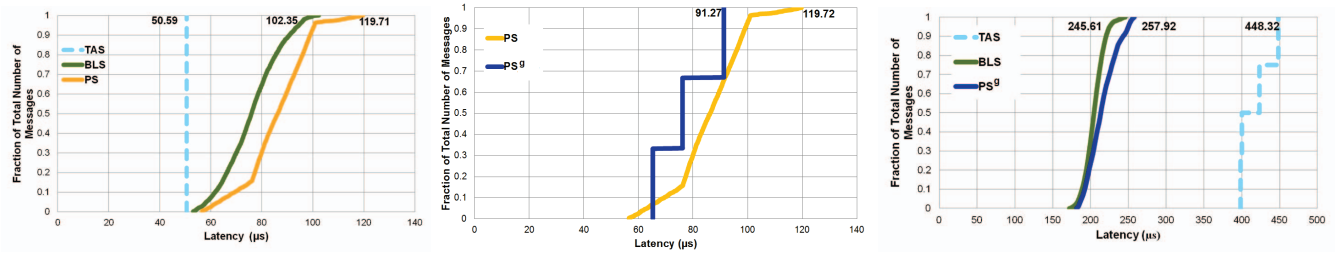
interference of the non-CDT frame by disabling the non-CDT queues when a CDT frame is present in the switch and is waiting for its queue to be enabled (i.e. waiting for the next peristaltic phase). On the other hand, a non-CDT frame could be selected for transmission just before time *t1* when the CDT frame is being received. In this case, the CDT frame has to wait in the queue for either Δps or Δint whichever is maximum. By introducing the guard band Eq.10 changes into:

$$\Delta Sout_{PS} = max(\Delta ps, \Delta int) \quad (11)$$

Fig.7(b) compares the end-to-end delay ΔP of Class CDT considering the guard band. The figure shows an improvement of 28.44μs (i.e. 23%) of the maximum end-to-end latency. Again, the simulation maximum (91.278μs) shows that the-oretical worst case maximum residence time is not reached in any of the switches.

Impact on AVB Traffic. The inclusion of Class CDT as the highest priority traffic and the operation of CDT shapers affects the end-to-end latency ΔP of AVB streams. Fig.7(c) shows the delay ΔP of the AVB Class A stream from node N2 to N8 as affected by the operation of the shapers used for the CDT traffic. Even though the maximum ΔP is well below the maximum allowed by IEEE AVB (2ms over 7 hops), the impact of each traffic shaper on the latency of Class A traffic can be clearly seen. TAS has the maximum impact over the Class A stream since it avoids the interference of other frames by blocking the non-CDT queues during CDT slots. Moreover, Class A traffic is not allowed to transmit if the time for the transmission of the entire frame exceeds the start of the subsequent CDT slot. BLS and PS^g show almost equal impact on the Class A stream. However, PS^g has a slightly higher impact because the guard band blocks the interfering traffic until the waiting CDT frame is selected for transmission. This can be noted from the difference between the maximum end-to-end latencies for Class A traffic among these two shapers. The BLS offers the smallest impact on the AVB Class A data traffic.

Discussion. From the simulation results, it is evident that the IEEE 802.1TSN end-to-end latency requirement of 100μs over 5 hops for Class CDT can be achieved only by TAS with proper scheduling and synchronization (and a large bandwidth reservation). However, as we can see from Eq.8 and Eq.10, the performance of BLS and PS can be improved using a frame pre-emption mechanism. The minimum size of a preempted



(a) Traffic shapers performance for CDT traffic. (b) CDT traffic using PS with and without Guard Band. (c) Effect of CDT traffic shapers on AVB traffic.

Fig. 7. Cumulative distribution function of latencies for Class CDT $N6 \rightarrow N9$ and Class A $N1 \rightarrow N8$ streams.

frame fragment is limited to 64 bytes. This reduces Δint to 5.12μs (for 100 Mbps links). So with Eq.8 and the delay values assumed in the model, the maximum end-to-end delay over 5 hops by a CDT frame using BLS is $\Delta P = 113.23\mu s$. Again, the requirement for end-to-end latency is not met. The requirement can, however, be reached with BLS if the payload size of CDT frames is restricted to 94 bytes rather than 128 bytes.

For the PS, Δint after preemption (5.12μs) is less than Δps. Therefore according to Eq.11, the maximum end-to-end latency of a CDT frame is influenced only by Δps (20μs). Over 5 hops, $\Delta P = 172.75\mu s$, which is much higher than the required 100μs. In this case reducing the CDT frame size or the peristaltic phase cannot bring enough improvements. The only further option to achieve the latency requirement is to increase the link speed from 100 Mbps to 1 Gbps. With a link speed of 1 Gbps, the IEEE 802.1TSN CDT payload-size restriction increases to 256 bytes [16]. Here the theoretical maximum end-to-end latency of a CDT frame over 5 hops is obtained as approximately 25μs which is well below the required 100μs limit.

VI. Conclusion

In this work we analyzed the three traffic shapers that are currently under discussion at the IEEE 802.1TSN working group. These shapers will support control-data traffic while also allowing the use of AVB streams and best-effort legacy traffic. We proposed a analytical worst-case model that allowed us to derive upper bounds to the maximum end-to-end delay of CDT traffic over a path in the network. Additionally we evaluated the analytical model by using an event-based simulation of an automotive-relevant scenario.

According to our results TAS is the shaper that can offer the best low-latency and low jitter performance. This comes at a high cost for the configuration of the switch and the impact that CDT traffic has on the non-CDT streams. BLS can offer a good compromise for low configuration complexity while offering good QoS guarantees. Finally the PS shaper shows a very low configuration complexity at the cost of the achieved performance. From these considerations the choice for the CDT traffic shaper must rely on the requirements of the targeted application.

This work will be further extended in multiple directions by including the analysis of the frame-preemption mechanism, the errors in the distributed synchronization mechanism that governs the TAS and PS shapers and finally by testing more complex CDT patterns with multiple periods and frame sizes.

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