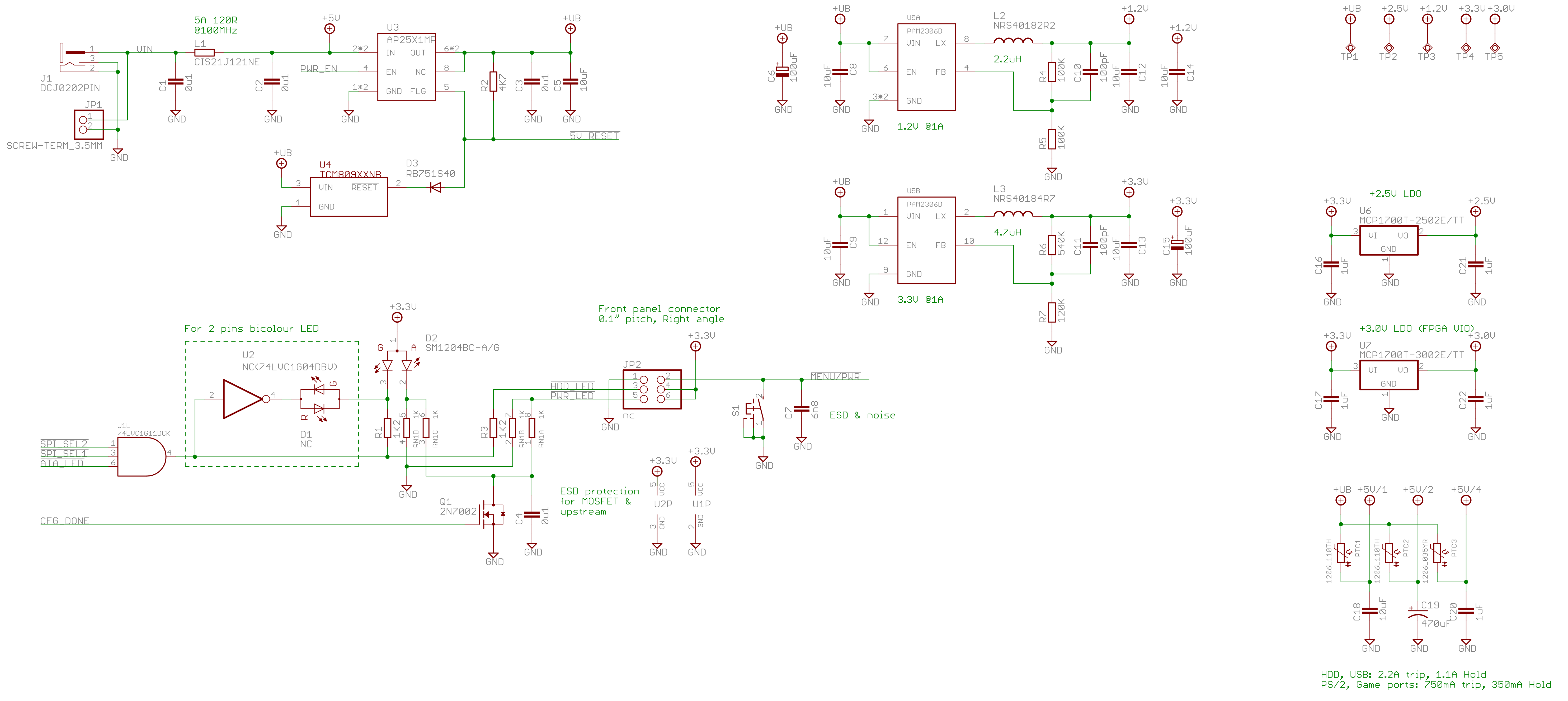
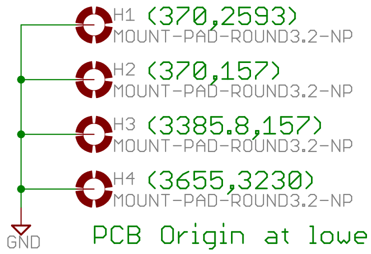


M3 Screws, standoff etc



PCB Origin at lower left corner [mil]

Author: K. C. Lee
"This work" = Schematic and hardware design

http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator/

1 oz copper, 10C Rise, external layer:
8 mil: 0.0631 ohms/in. 0.753A drop: 47.5mV/in
12 mil: 0.0421 ohms/in, 1.010A drop: 42.5mV/in
16 mil: 0.0316 ohms/in, 1.243A drop: 39.3mV/in
20 mil: 0.0252 ohms/in, 1.465A drop: 36.9mV/in
24 mil: 0.0210 ohms/in, 1.670A drop: 35.1mV/in
32 mil: 0.0157 ohms/in, 2.060A drop: 32.4mV/in

Power and Misc

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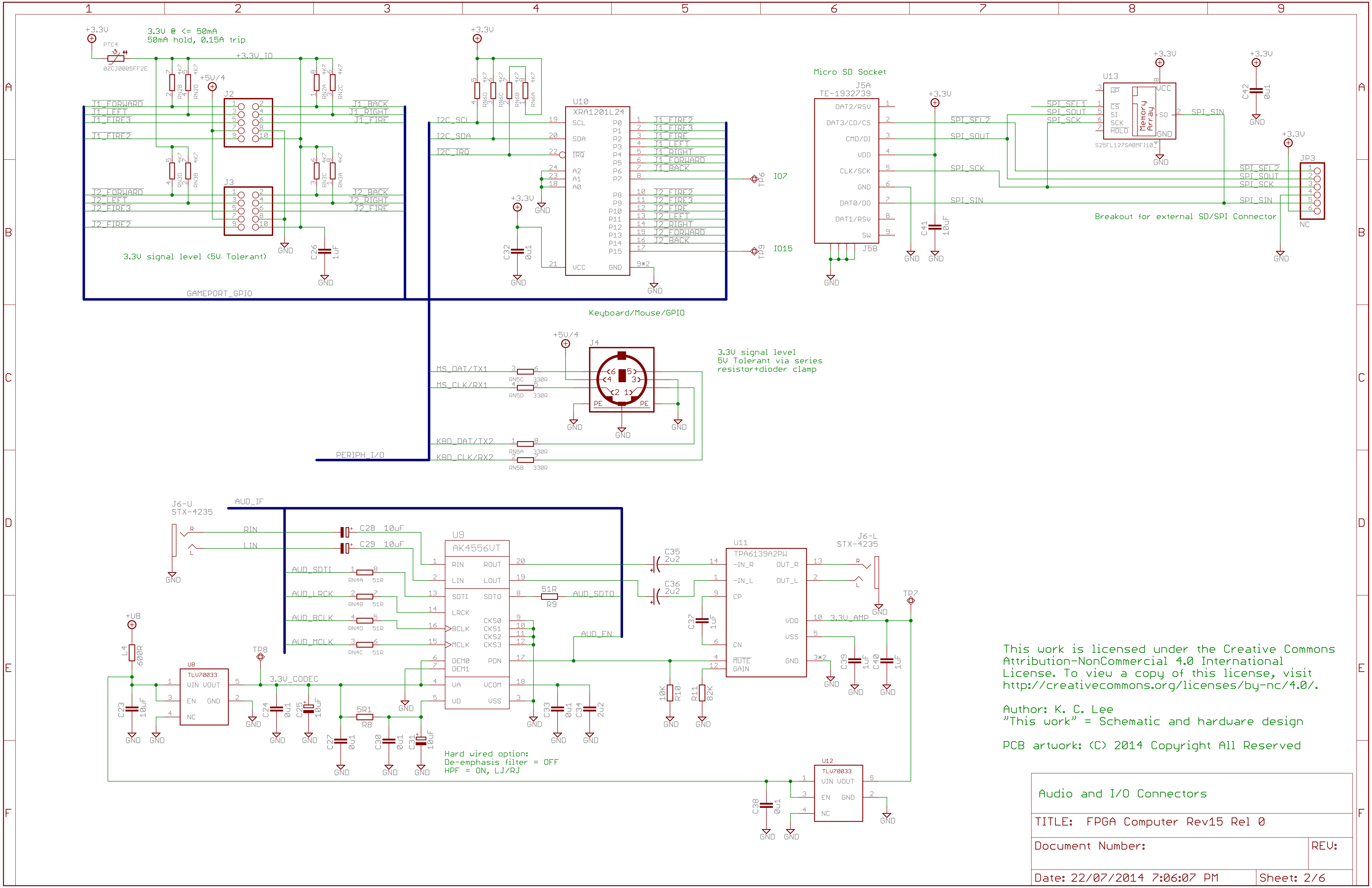

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Author: K. C. Lee
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PCB artwork: (C) 2014 Copyright All Reserved

Audio and I/O Connectors

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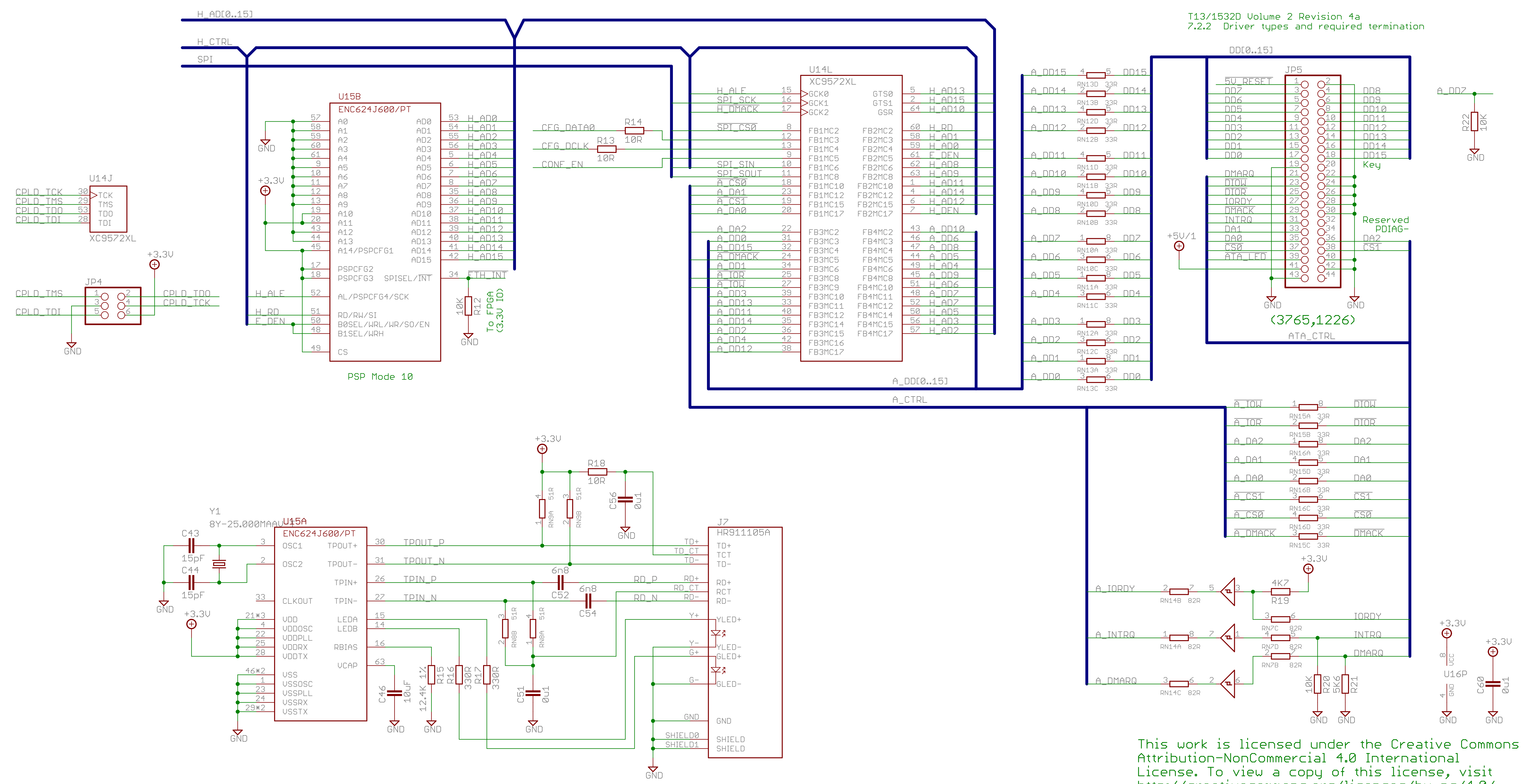

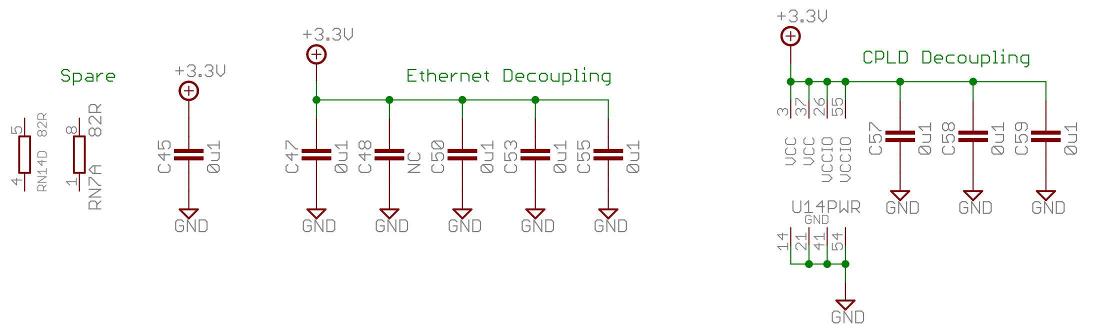

XC9500XL from IBIS models:
3.3V Fast Slew rate: (IO01)
Rising: 1.211V/ns (min) 2.756V/ns (typ) 4.464V/ns (max)
Falling: 1.012V/ns (min) 2.218V/ns (typ) 3.876V/ns (max)
RS ~ 52.4R (pullup) 27.28R (pull down)

3.3V Slow Slew rate: (IO11)
Rising: 0.165V/ns (min) 0.425V/ns (typ) 0.913V/ns (max)
Falling: 0.210V/ns (min) 0.516V/ns (typ) 1.098V/ns (max)
RS ~ 53.13R (pullup) 27.46R (pull down)

UDMA slew rate: 0.4V/ns (min) 1V/ns (max) which can
be met by CPLD using Slow Slew rate for typ/max cases

40 conductor cable: Strobe ~115R

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Local Bus Peripheral: Ethernet, PATA

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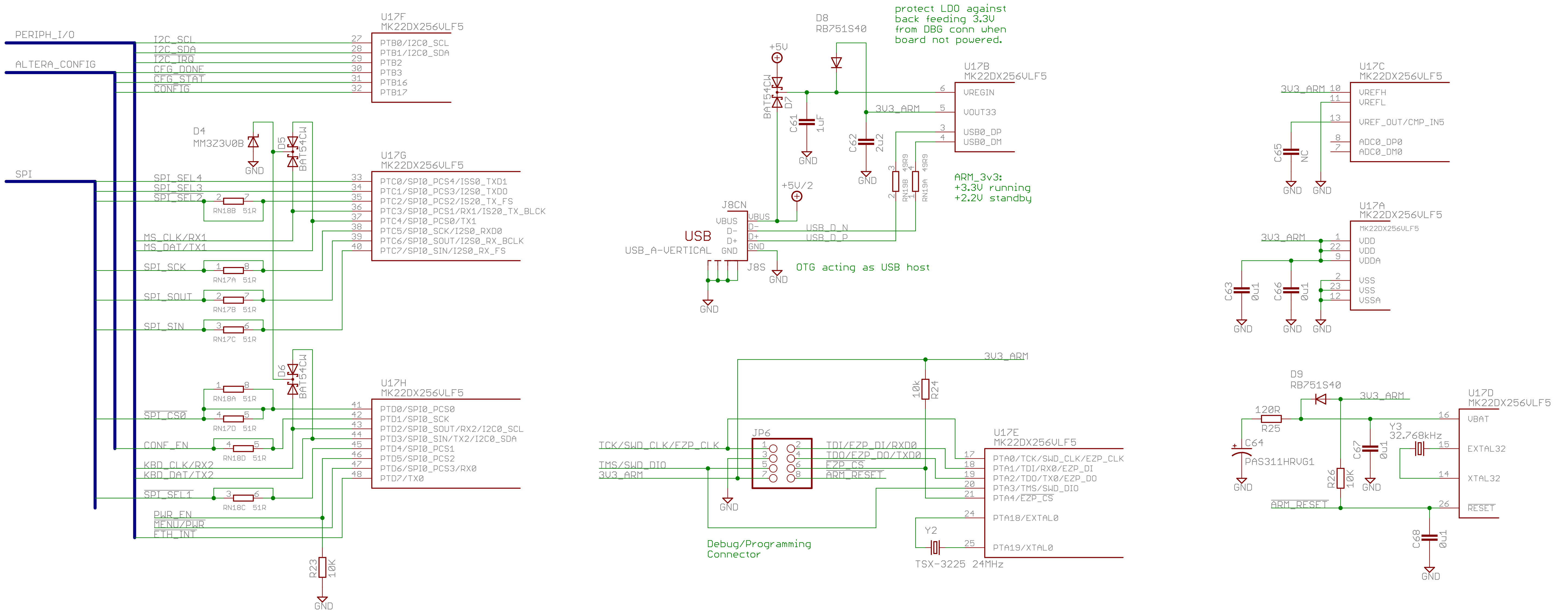

protect LDO against
back feeding 3.3V
from DBG conn when
board not powered.

ARM_3v3:
+3.3V running
+2.2V standby

OTG acting as USB host

Debug/Programming
Connector

Doc K20PB states K22 doesn't have any 5V tolerant I/O.
Clamped signals to 3V zener as 3V3_ARM doesn't have much load.
PWR_EN is active high because chip is not 5V tolerant

Author: K. C. Lee
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ARM Microcontroller	
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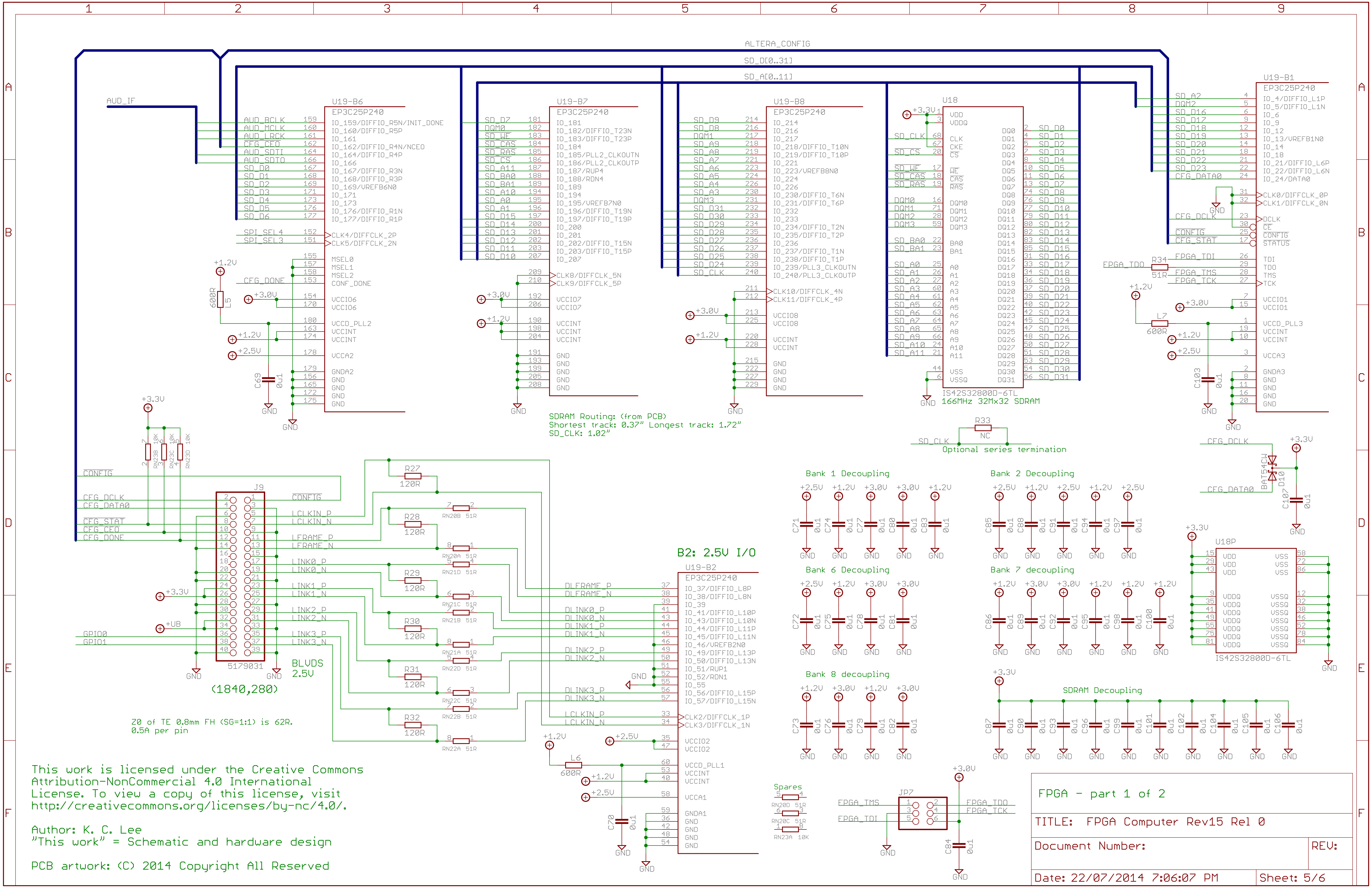

Author: K. C. Lee
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FPGA - part 1 of 2

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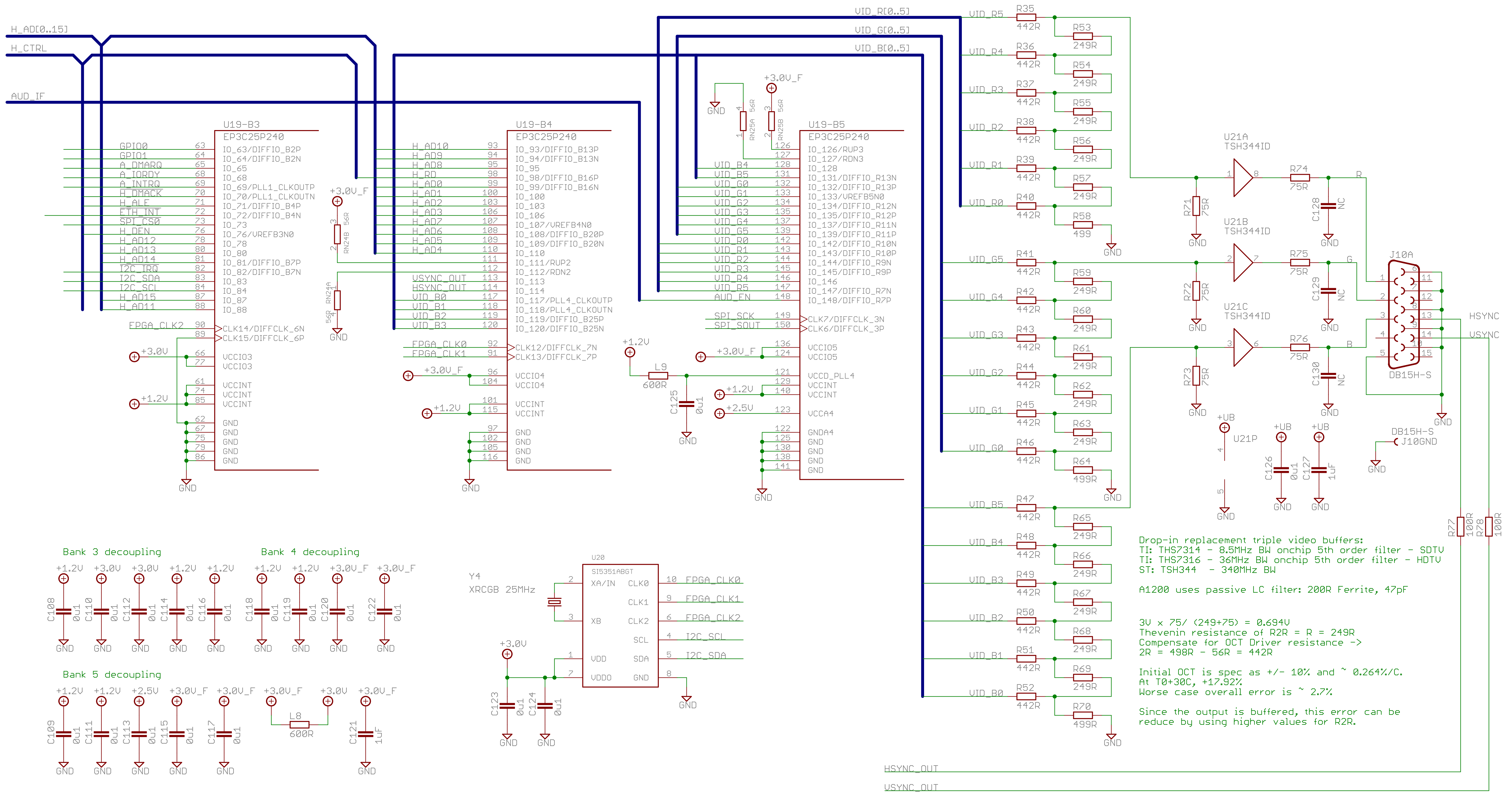

Drop-in replacement triple video buffers:
TI: THS7314 - 8.5MHz BW onchip 5th order filter - SDTV
TI: THS7316 - 36MHz BW onchip 5th order filter - HDTV
ST: TSH344 - 340MHz BW

A1200 uses passive LC filter: 200R Ferrite, 47pF

3V x 75/ (249+75) = 0.694V
Thevenin resistance of R2R = R = 249R
Compensate for OCT Driver resistance ->
2R = 498R - 56R = 442R

Initial OCT is spec as +/- 10% and ~ 0.264%/C.
At T0+30C, +17.92%
Worse case overall error is ~ 2.7%

Since the output is buffered, this error can be
reduce by using higher values for R2R.

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FPGA part 2 of 2

TITLE: FPGA Computer Rev15 Rel 0

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