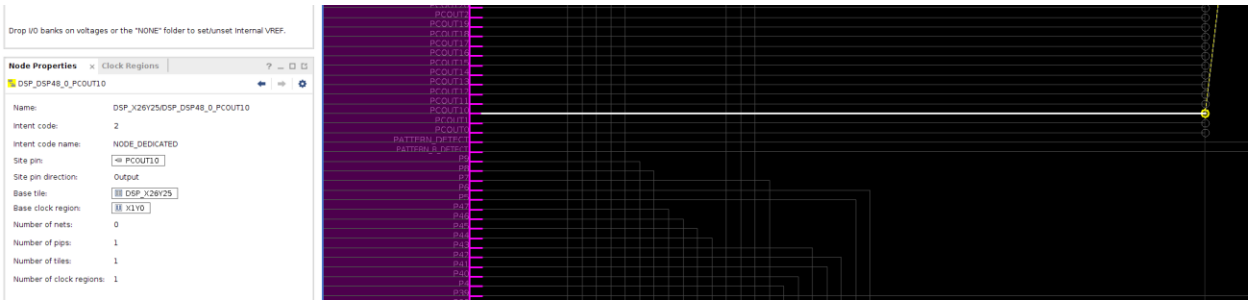
Explanation for false positive of DSP-related designs:

```
1 Output for data/normal_scans/blackscholes_OOC_Synth_partial.json generated at 2020-03-13 14:28:21.426316
2
3 CombinatorialLoopDetector: 1875000.0
```

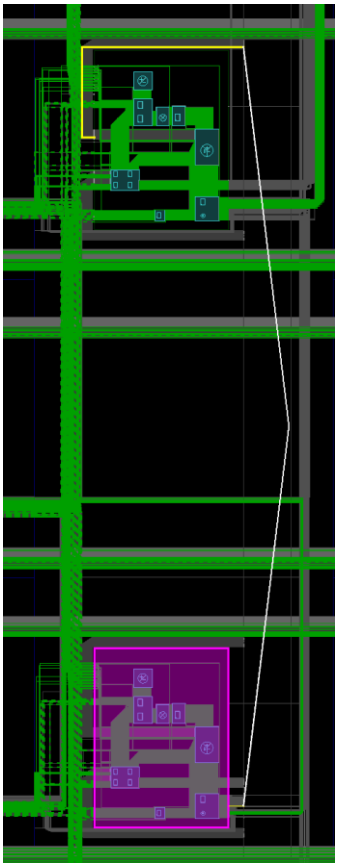
Take one RO for example:

```
DSP_X26Y25 DSP_DSP48_0_PCOUT10 -> DSP_X26Y25 DSP_DSP48_1_PCIN10_PIN -> DSP_X26Y25 DSP_DSP48_1_FAKE_PREG -> DSP_X26Y25 DSP_DSP48_1_PCOUT47 ->
  DSP_X26Y30 DSP_DSP48_0_PCIN47_PIN -> DSP_X26Y30 DSP_DSP48_0_FAKE_PREG -> DSP_X26Y30 DSP_DSP48_0_PCOUT47 ->
    DSP_X26Y30 DSP_DSP48_1_PCIN47_PIN -> DSP_X26Y30 DSP_DSP48_1_FAKE_PREG -> DSP_X26Y30 DSP_DSP48_1_P29 -> INT_INTF_R_X26Y33 LOGIC_OUTS_R25 -> INT_INTF_R_X26Y33 LOGIC_OUTS_L25 -> INT_
      DSP_X26Y25 DSP_DSP48_0_A14 -> DSP_X26Y25 DSP_DSP48_0_FAKE_A-AC -> DSP_X26Y25 DSP_DSP48_0_FAKE_A_PREG_STAGE0 -> DSP_X26Y25 DSP_DSP48_0_FAKE_A_PREG_STAGE1 -> DSP_X26Y25 DSP_DSP48_
```

It starts from PCOUT[10] of DSP0 in DSP_X26Y25 (*DSP_X26Y25 DSP_DSP48_0_PCOUT10*)




Through the daisy chain, it connects to PCIN[10] of DSP1 in DSP_X26Y25 (*DSP_X26Y25 DSP_DSP48_1_PCIN10_PIN*)



PCIN* ports connect straight to PCOUT* ports through FAKE_PREG. Below architecture map and logic view show that we suppose only one configuration bit for connection between internal outputs to DSP ports.  Therefore, if there is no output register, PCIN* will converge at FAKE_PREG and propagate to PCOUT* directly!

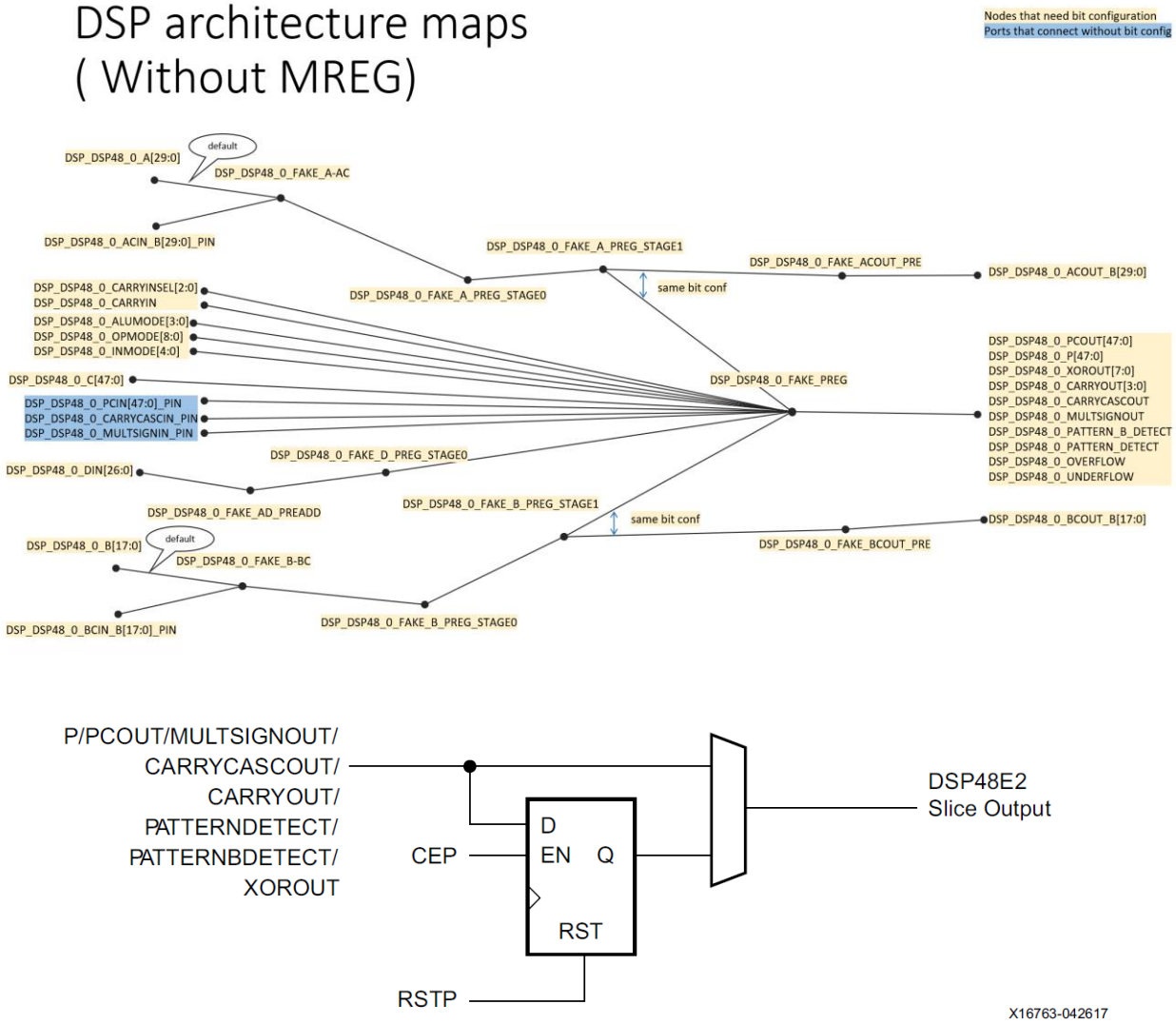




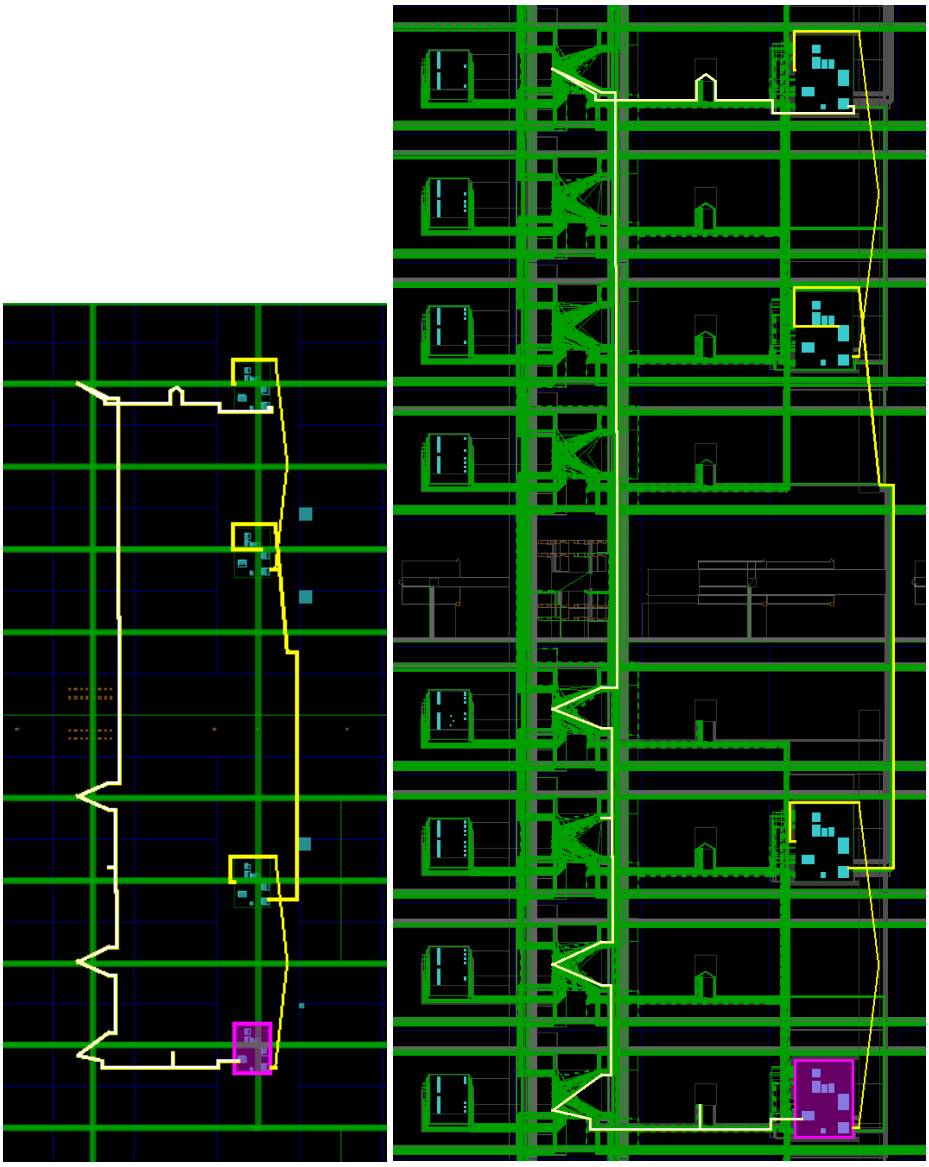


*Figure 2-11:* **Output Port Logic**

*DSP_X26Y25 DSP_DSP48_1_PCOUT47* will then connect to *DSP_X26**Y30** DSP_DSP48_0_PCIN47_PIN* (another tile) through daisy chain.

*DSP_X26Y30 DSP_DSP48_0_PCOUT47* will connect to *DSP_X26Y30 DSP_DSP48_1_PCIN47_PIN*, it get converged at *DSP_X26Y30 DSP_DSP48_1_FAKE_PREG* then propagate to *DSP_X26Y30 DSP_DSP48_1_**P29***.

*DSP_X26Y30 DSP_DSP48_1_**P29*** then connects all the way back to tile *DSP_X26Y25* pin *DSP_DSP48_0_A14*.



At *DSP_X26Y25 DSP_DSP48_0_A14*, it closes a loop to *DSP_X26Y25 DSP_DSP48_0_PCOUT10*