



PUF OVER FPGA

Episode 02: What is a PUF and discussion of the project structure

AGENDA

Part 1 - Course intro

➔ **Part 2 - What is PUF and discussion of the project structure**

Part 3 - HDL Development of PUF

Part 4 - Building a MicroBlaze-based soft processor system

Part 5 - Connect PUF to MicroBlaze and assign FPGA pins

Part 6 – Using pblock for separate PUF and MicroBlaze placement

Part 7 - Introduction to TCL and placing PUF on FPGA

Part 8 - Writing code for the processor system

Part 9 - Debugging and running PUF

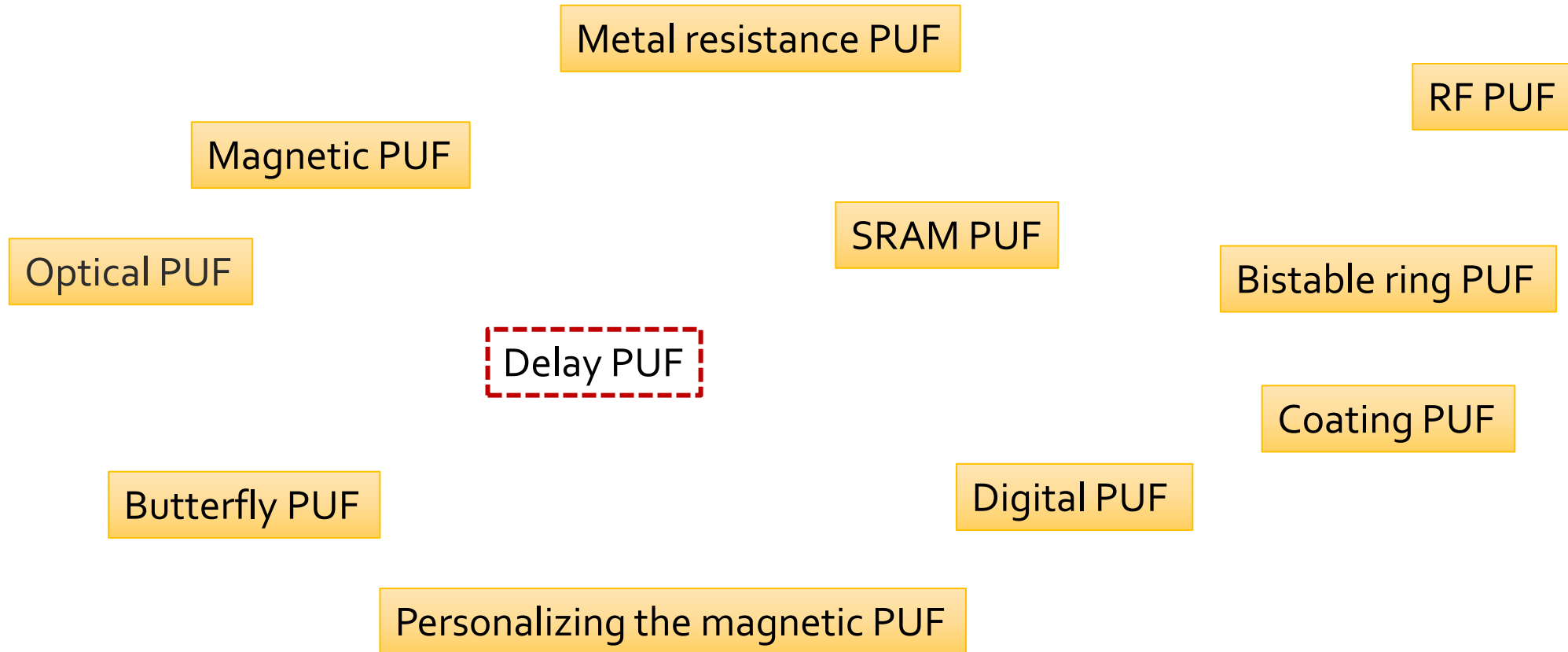
**Number of episodes could be change in future*

WHAT IS A PUF?

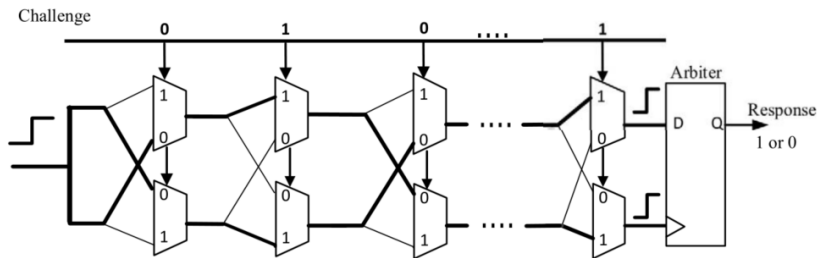
PUF (**P**hysical(**l**y) **U**nclonable **F**unction) is a physical object that for a given input and conditions (challenge), provides a physically defined "digital fingerprint" output (response) that serves as a unique identifier ...PUFs are most often based on unique physical variations which occur naturally during semiconductor manufacturing...

Today, PUFs are usually implemented in integrated circuits and are typically used in applications with high security requirements ([wiki](#))

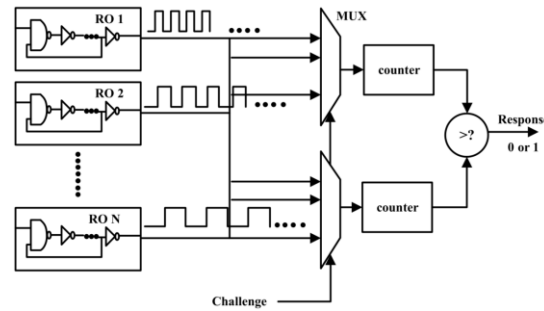
PUFs TYPES



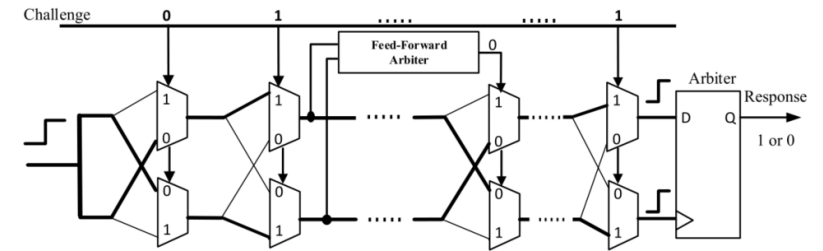
TYPES OF DELAY-BASED PUFs



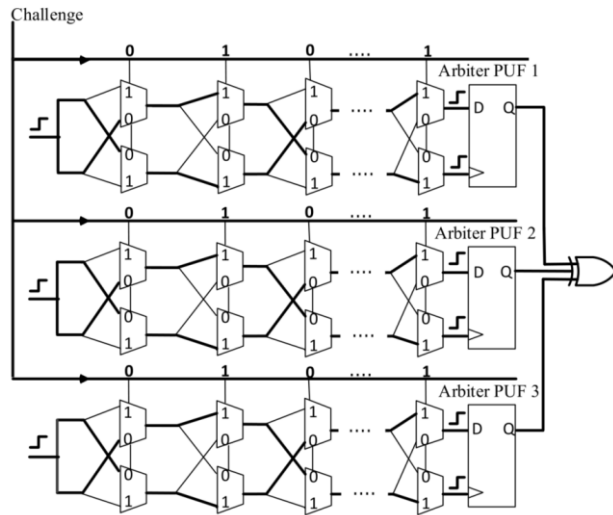
Arbiter PUF



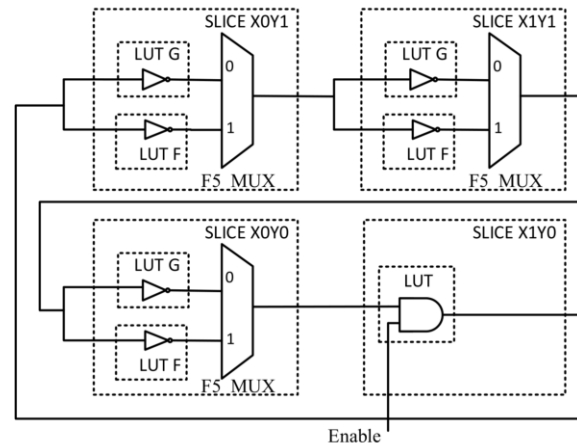
Ring Oscillator PUF



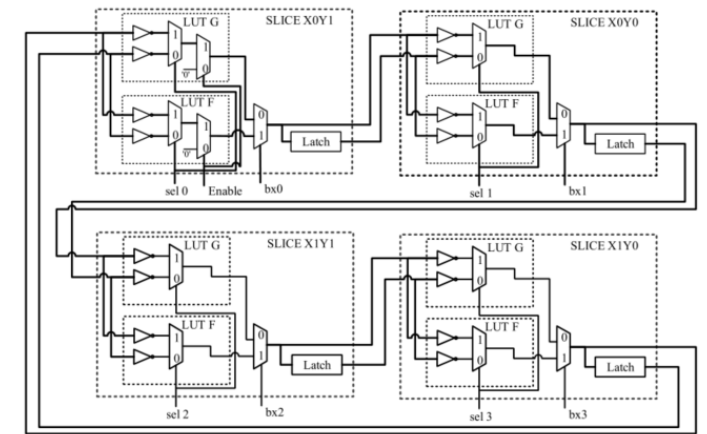
Feed-Forward Arbiter PUF



3-XOR Arbiter PUF



Maiti Configurable Ring Oscillator

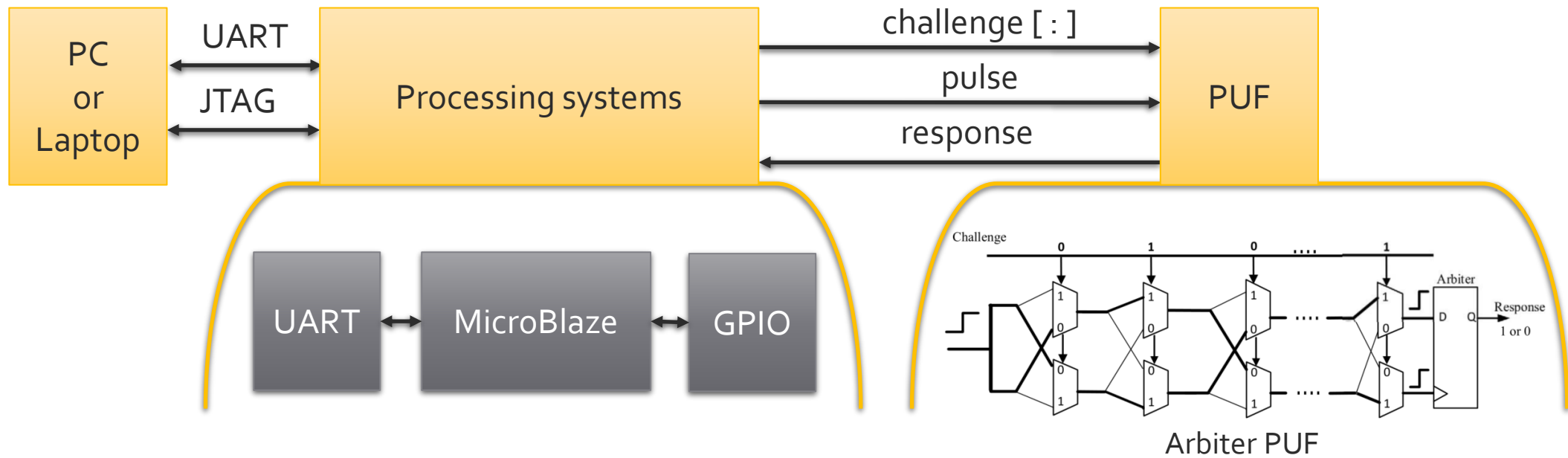


Xin Configurable Ring Oscillator

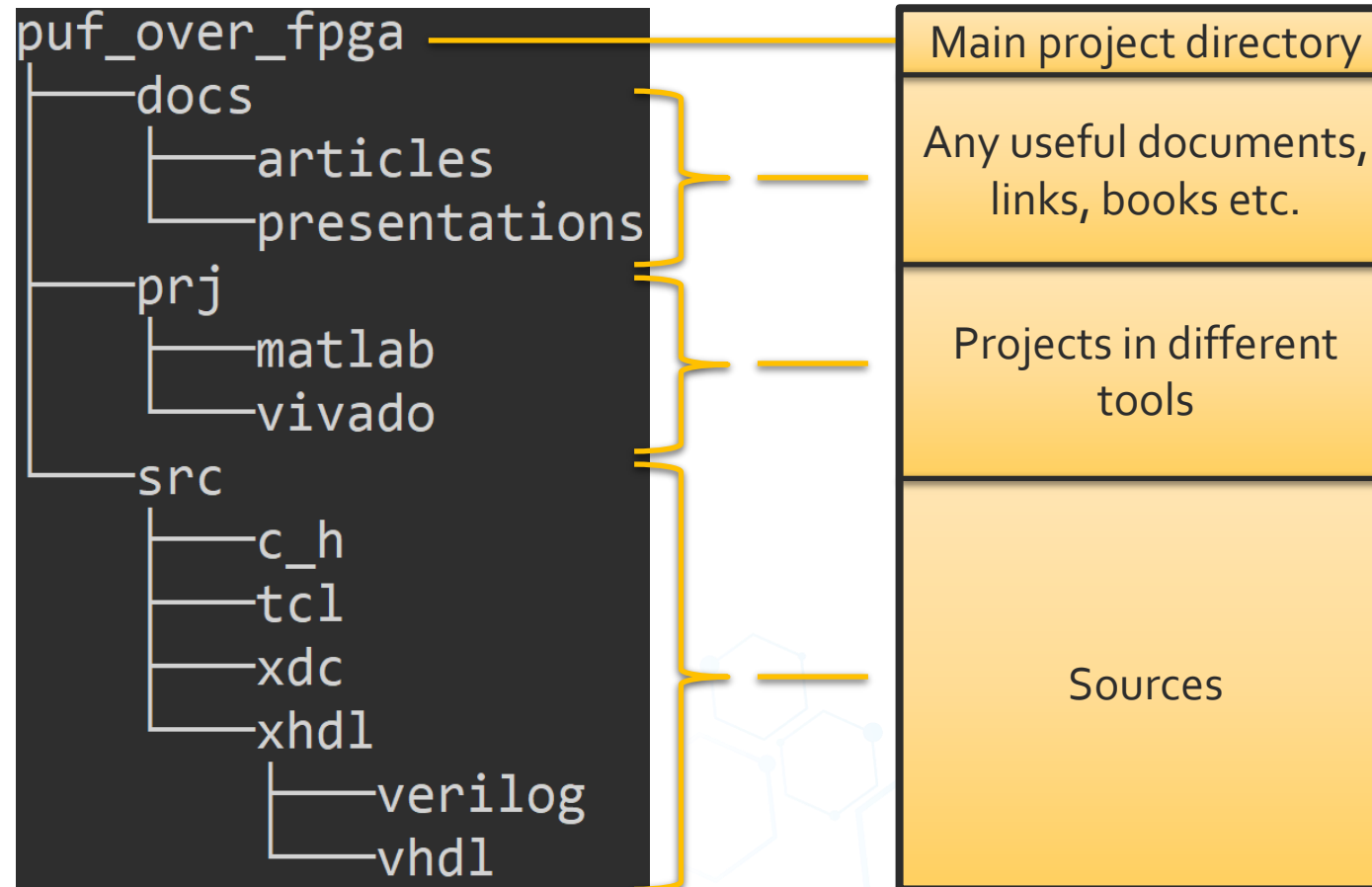
WHAT SHOULD BE DEFINED ?

1. Project structure
2. Communication interface
3. Type of implemented PUF
4. PUF interface
5. How to collect and save statistic from PUF

PROJECT STRUCTURE



PROJECT DIRECTORIES



HAVE A QUESTIONS?



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