

Open FPGA Board

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- The block diagram illustrates the system architecture for the iCE40HX4K FPGA. The central component is the **FPGA iCE40HX4K** (orange box). It is connected to several peripheral components:
- Clock 12Mhz** (yellow box): Connected to the FPGA via a bidirectional arrow.
 - FTDI** (light blue box): Connected to the FPGA via **Serial** and **SPI** interfaces. The FTDI is also connected to a **USB** port (represented by a USB symbol).
 - FLASH 32Mb** (light green box): Connected to the FPGA via a bidirectional arrow.
 - ADC ADS7924** (light green box): Connected to the FPGA via an **I2C** interface.

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- Power
ND
Serial Pin
Analog Pin
Control
Physical Pin
Teststudio name
Pin name
- Data + Power (1.8A max)
- Power Only (3A max)
- PERIPHERALS PWR
- RESET
- 3V3
- 5V_P
- GND
- GND
- NC
- A0 CH0 A0 0_171 114
- A1 CH1 A1 0_172 115
- A2 CH2 A2 0_173 116
- A3 CH3 A3 0_174 117
- SDA DD4 0_177 118
- SCL DD5 0_178 119
- AREF
- GND
- 64 2_104 D13
- 63 2_103 D12
- 21 3_14A D11
- 22 3_14B D10
- 19 3_13A D9
- 20 3_13B D8
- 9 3_5A D7
- 10 3_5B D6
- 7 3_4A D5
- 8 3_4B D4
- 3 3_3A D3
- 4 3_3B D2
- 1 3_2A D1
- 2 3_2B D0
- 45 2_73 LED0
- 44 2_72 LED1
- 43 2_71 LED2
- 42 2_64 LED3
- 41 2_63 LED4
- 39 2_61 LED5
- 38 2_57 LED6
- 37 2_56 LED7
- User Switches
- 34 3_25B SW1
- 33 3_25A SW2
- External Analog Reference: AREF = 3.3V - 5.5V
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|------|----|-------|------|
| SCK | 70 | 2_107 | SCK |
| SDI | 68 | 2_106 | MISO |
| SDO | 67 | 2_105 | MOSI |
| SS | 71 | 2_108 | SS |
| DONE | 65 | CDONE | DONE |
| REST | 66 | CREST | RES |

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|-----|----|-------|-----|
| RX | 61 | 2_96 | RX |
| TX | 62 | 2_102 | TX |
| RTS | 60 | 2_95 | RTS |
| CTS | 56 | 2_94 | CTS |
| DTR | 52 | 2_82 | DTR |
| DSR | 48 | 2_80 | DSR |
| DCD | 47 | 2_79 | DCD |

RESET BUTTON

 Max 4.8A for all 5V_P Pins

CLK Clock 12Mhz 49 2_81

ADC	Interrupt	90	1_138	ADC_INT
I ² C	SDA	83	1_119	ADC_SDA
	SCL	84	1_120	ADC_SCL



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