# Argon CPU bypassing

There are totally 5 bypass ways

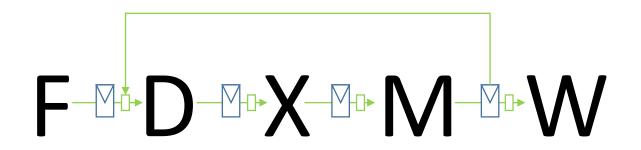
#### 1) After X to D

```
add R3,R2,R1 | F D X M W

nop | F D X M W

add R4,R3,R1 | F D X M W
```

### 2) After M to D



```
add R3,R2,R1 | F D X M W

nop | F D X M W

nop | F D X M W

add R4,R3,R1 | F D X M W
```

## 3) After X to X

```
add R3,R2,R1 | F D X M W add R4,R3,R1 | F D X M W
```

## 4) After M to X

#### 5) After M to M

Don't do this, because memory instructions are of 2 cycles latency