Design and optimization of a low power operational amplifier (OpAmp) in a 130nm technology

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Design and optimization of a low power operational amplifier (OpAmp) in a 130nm CMOS technology

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Task description:

- Design and optimization of the circuits in 130nm CMOS technology.
- Simulation of the circuit over voltage and temperature corners.
- Layout of the circuit (optional).
- Designs which fulfill the industrial standards can be implemented in 130nm technology and tested (optional).

Prof. Dr. Milady

Declaration of Authorship

I, Jingan QIAN, declare that this thesis titled, “Design and optimization of a low power operational amplifier (OpAmp) in a 130nm technology” and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly conducted while in candidature for a degree at Technical University of Applied Sciences Lübeck.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

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Abstract

Department of Electrical Engineering and Computer Science

Bachelor of Science (B.Sc.)

Design and optimization of a low power operational amplifier (OpAmp) in a 130nm technology

by Jingan QIAN

In the history of electronics development , operational amplifies (op-amp) has been thought of as a key factor in the integrated circuit design. The main aim of this study is to investigate the Miller op-amp and folded cascode op-amp.

This thesis is composed of four themed chapters. To begin with, chapter 1 introduces the background of op-amps, PSpice, and the organization of the thesis. Afterward, chapter 2 explores the structure of folded casode op-amp and chapter 3 introduces Miller op-amp with 3 compensation methods, including Miller compensation, voltage buffer, and a nulling resistor. Both of them begin by theoretical dimensioning of the op-amps and put emphasis on how they perform in the PSpice simulation. PSpice is also utilized to obtain the parameter values of two circuits, such as dc gain, slew rate, output swing, ICMR, etc. In addition, the theoretical results are compared with the simulation results. In the end, chapter 4 concludes that the folded cascode op-amp has a better overall performance in 130nm CMOS technology and the future work is then discussed.

Acknowledgements

Acknowledgments by Jingan Qian I would like to express my gratitude to Prof. Dr. Milady, who provided me with a fantastic opportunity to work on this project and served as my advisor for the entire four months. Prof. Dr. Milady led me through the entire project implementation process and provided helpful ideas on both the PSpice implementation and the thesis. I would also like to thank Prof. Dr. Matthies for setting up an online meeting with me to discuss the thesis. I want to express my gratitude to the IHP experienced engineers who advised me on my PSpice simulation. Their advice is very useful for my thesis. My special thanks go to Prof. Razavi and Prof. Allen, this thesis would hardly be fulfilled without their contributions posted on the Internet. In addition, I want to convey my gratitude to my family and friends, who have always been supportive of me.

CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

OpAmp	**Op**erational **Amp**lifier
PM	**P**hase **M**argin
SR	**S**lew **R**ate
CM	**C**ommon **M**ode
GCF	**G**ain **C**rossover **F**requency
ICMR	**I**nput **C**ommon **M**ode **R**ange
DM	**D**ifferential **M**ode

1 INTRODUCTION

1.1 Background and Goals

CMOS operational amplifiers (Op-amp) are indispensable and fundamental components in analog integrated circuit. They can be used to fulfill a variety of functions, including adding, subtracting, averaging, integrating and differentiating. CMOS technology offers an advantage over bipolar technology in terms of circuit configurations and design flexibility; therefore, it is quickly gaining traction as the next generation of linear analog integrated circuits, especially in the telecommunications industry (Ahuja, 1983).

Nowadays, with the penetration of portable products into our daily life, the reduction of power consumption has become increasingly essential. For conserving space, very large scale integrated (VLSI) is employed, which is one of the techniques for putting very large electronic components on a single chip. In such circuits, lowering the power supply voltage is the most effective way to reduce power consumption (Katara et al., 2016) . Hence, there is a growing body of literature that exploring an op-amp with a good performance to meet different requirements.

There are two primary aims of this study:

- 1. To investigate the principles of the two-stage op amps and folded cascode opamps.
- 2. To use PSpice to simulate the circuits and then compare the results in order to find which circuit is the most suitable in 130nm COMS technology.

1.2 Basic Op-amp Concept

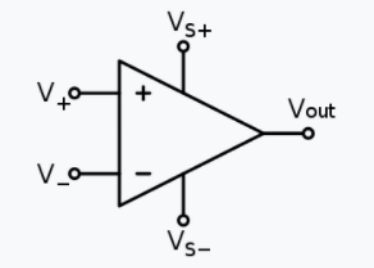


FIGURE 1.1: Operational Amplifier Symbol, Copyright © (Wikipedia, 2021b)

The op-amp symbol is shown in Figure 1.1. The most commonly used op-amp configuration in CMOS has two gain stages. Basically, it has one output and two inputs, one positive input and one negative input. V_{S+} and V_{S-} serve as the voltage supply.

In fact, an op-amp controls the voltage to realize the goal of very large voltage amplification. Due to the narrow linearity region of an op-amp, they are often used with external feedback components. Hence, the stability of the circuit should be guaranteed; otherwise, op-amps will oscillate and become an oscillator instead (Poonam and Saini, 2013).

Stability of the closed loop op-amp circuits can be analysed by investigating the phase and amplitude response of the open-loop (Nyquist stability criterion). In many practiced cases, a simplified version of Nyquist stability criterion can be used where Gain Margin and Phase Margin are used. The reason for the phase shift is the occurrence of the parasitic components. It is widely recognized that a phase margin of 45 degrees or greater will result in "good" stability and reduced overshoot (Gomez, 2019). In conclusion, the circuits require compensation methods to ensure the stability.

1.3 PSpice

This thesis uses the PSpice to simulate various circuits. "PSPICE is a computer-aided simulation program that enables one to design a circuit and then simulate the design on a computer. PSPICE stands for Program Simulation with Integrated Circuit Emphasis" (*Introduction to PSPICE*).

Electronic design engineers utilize it heavily for constructing circuits and then testing how those circuits would simulate, as this is one of its key goals. PSPICE is widely used due to its user-friendly interface, extensions that facilitate digital circuit modeling, and a free base edition (*Introduction to PSPICE*).

"PSPICE is a general purpose program designed for a wide range of circuit simulation including the simulation of nonlinear circuits, transmission lines, noise and distortion, digital circuits, mixed digital and analog circuits. It can perform dc analysis, steady-state sinusoidal (AC) analysis, transient analysis, and Fourier series analysis" (*Introduction to PSPICE*).

1.4 Organization

The rest of the thesis is structured as follows. The structure of folded cascode op amps is explained in Chapter 2, as well as why this topology is used. Chapter 3 explains the Miller Op Amp . Furthermore, the compensation methods are also introduced. Likewise, the PSpice simulation is also included, Chapter 4 discusses the performance of each circuit and come to a conclusion that the folded cascode op amps are one of the most suitable circuit to be implemented in 130nm CMOS technology. Finally, used PSpice transistor models and the temperature simulations (at -40, 0, 25, 135 degrees Celsius) are included in the appendix.

2

FOLDED CASCODE OPERATIONAL AMPLIFIER

2.1 Circuit Introduction

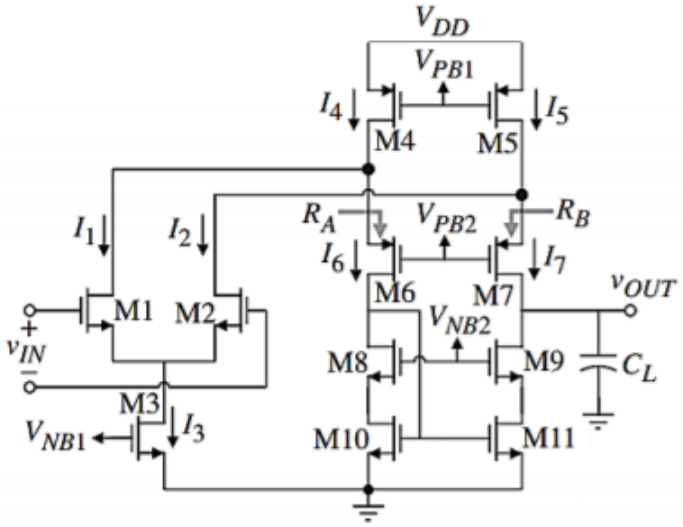


FIGURE 2.1: Basic folded cascode operational amplifier, Copyright © (Sing et al., 2020)

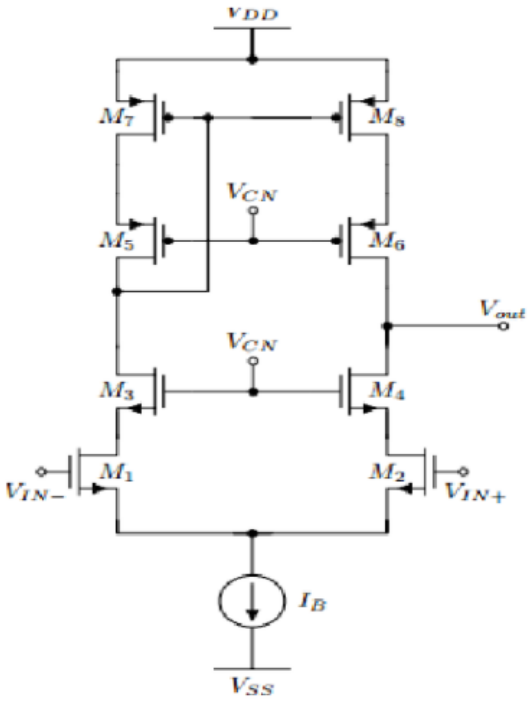


FIGURE 2.2: Telescopic cascode op amp, Copyright © (Silva, Severo, and Girardi, 2014)

Figure 2.1 cited from (Sing et al., 2020) above shows the folded cascode op-amp without the biasing circuitry. The circuit is to be spread over four sections for a detailed explanation.

After comparing the circuit 2.1 with the circuit 2.2 above, folded cascode operational amplifiers(op-amps) are configurations generally developed on the basis of the telescopic amplifiers. The initial p-channel cascode active loads of a differential pair M7, M8 in Figure 2.2 are folded down and then replaced with NMOS M6, M7 in the configuration of the folded cascode op-amps for the purpose of achieving a higher ICMR (input common mode range) and a larger output swing (Sing et al., 2020).

Besides the high ICMR and large output swing, the folded cascode op-amps have two other merits: a single-dominant-pole characteristic and a high voltage gain, as compared to the simple two stage operational amplifiers. To stabilize the simple two stage operational amplifiers, an additional compensation capacitor is added to the circuit. On the other hand, since the folded cascode op-amps have only one dominant pole at the output node and are also self-compensatory,

the stability of the circuit is easier to be maintained. In addition, the large differential gain results from the higher output impedance (Nischal and Kaur, 2019).

These four advantages of the folded cascode op-amps mentioned above are inspiring; however, in comparison to the telescopic structure, they are obtained at the cost of higher power dissipation, reduced gain bandwidth, higher noise, and lower voltage gain.(Sing et al., 2020)

Overall, it is undeniable that the properties of folded cascode op-amps have resulted in a number of advantages, including:

- ICMR can rise approximately up to the supply voltage V_{DD} (Sing et al., 2020).
- The circuit can preferably operate under a low voltage supply (Sing et al., 2020).
- A satisfactory circuit for deep negative feedback due to large small signal gain (Rajni et al., 2011).

2.2 Circuit Description

This section will first introduce different compositions of MOSFETs in the folded cascode operational amplifier and then use PSpice simulation to further verify the original analysis of a particular part of the circuit. Finally, various parameters of the circuit will be discussed.

2.2.1 Cascode Current Mirror

The bottom right of the circuit 2.1 demonstrates a cascode current mirror structure, formed by M8, M9, M10, and M11. The usage of this structure contains mainly 3 functions: reduction in channel-length modulation effect, alternating

the double-ended output into single-ended output, and improving voltage gain to the order of $(g_m r_{ds})^2$ (Sing et al., 2020).

In addition, although M1 and M2 are folded down to function as differential pair inputs as well, M1, M2, M6, M7 also constitute the circuit's second cascode current mirror. The output voltage comes from the drains of M7 and M9; therefore, it is of significance to understand this structure as it determines the output stage's operational characteristics (Song et al., 1999).

Two typical configurations 2.3 and 2.4 cited from (Song et al., 1999) of the current mirror are illustrated above, the configuration 2.4 is employed in the folded circuit design because it offers a wider output voltage swing.

2.2.1.1 Classic Cascode Current Mirror

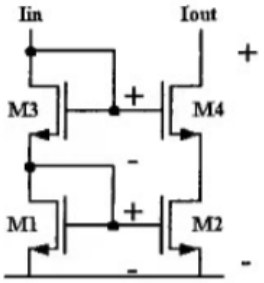


FIGURE 2.3: Classic cascode current mirror, Copyright © (Song et al., 1999)

This circuit shown in Figure 2.3 is a classic cascode current mirror. For simplicity, we assume all MOSFETs are in the same size (same W and L), they will have the same V_{TH} (the threshold voltage). Furthermore, the channel length modulation is neglected. The gate voltage of M4 can be easily calculated as $2V_{GS}$ (V_{GS} denotes the gate-source voltage in the saturation region) from the left part of the circuit. Also, M1, M2, and M3 are considered to be on the edge of the saturation area in order to bias M1 at the minimum drain voltage of M1, which means $V_{DS} = V_{GS} - V_{TH}$. In this circumstance, V_{DS}, the voltage from drain to source, is also called the overdrive voltage, denoted as V_{OD}. Hence, M1's voltage from drain to source equals V_{OD}. As a consequence, $2V_{GS} - V_{TH}$ is the minimum

voltage at the drain of M4 for it to be in the saturation region. The steps are shown as follows:

To ensure that M4 is in the saturation region, its drain voltage should meet the equation

$$V_{GD} \leqslant V_{TH} \tag{2.1}$$

$$V_{G4} - V_{D4} \leqslant V_{TH} \tag{2.2}$$

Substitute the calculation result before, we have

$$2V_{GS} - V_{D4} \leqslant V_{TH} \tag{2.3}$$

$$V_{D4} \geqslant 2V_{GS} - V_{TH} = 2V_{OD} + V_{TH} \tag{2.4}$$

(Letter i denotes MOSFET i)

2.2.1.2 Wide-Swing Cascode Current Mirror

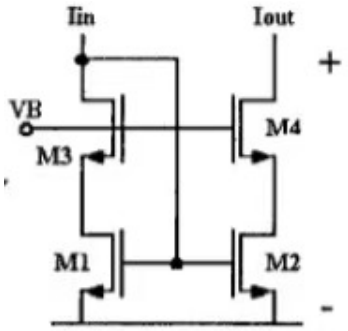


FIGURE 2.4: Wide-Swing cascode current mirror, Copyright © (Song et al., 1999)

Figure 2.4 shows a wide-swing cascode current mirror. The critical point of this structure lies in the value of $V_{G4} = V_B$. There are two main considerations about selecting this voltage V_{G4}. The first is that if the gate voltage of M4 is insufficient, no matter how much the drain voltage of M4 varies, all MOSFETs will never reach saturation simultaneously. The other is that the lowest feasible voltage of M4 is associated with the magnitude of V_B. Only when the value of V_B is set to the lowest possible value, is the minimum drain voltage of M4 able to reach. The following formulas can be used to determine the minimum value:

$$V_B = V_{GS3} + V_{D1} = V_{GS} + V_{D1} \tag{2.5}$$

The minimum value of V_B can be obtained when M1 is on the edge of the saturation region because V_{D1} has a minimum value in this situation.

$$V_{GD} \leqslant V_{TH} \tag{2.6}$$

$$V_{D1} \geqslant V_{G1} - V_{TH} = V_{OD} \tag{2.7}$$

$$V_B \geqslant V_{OD} + V_{GS} \tag{2.8}$$

$$V_B \geqslant 2V_{OD} + V_{TH} \tag{2.9}$$

Then, considering M4 to be in saturation region, the same equation 2.6 as shown above can be used to attain the result:

$$V_D \geqslant 2V_{OD} \tag{2.10}$$

2.2.1.3 PSpice Simulation And Results

In this section simulation results of two different types of current mirrors mentioned above are shown.

Figure 2.5 shows the schematic of a classic current mirror. Figure 2.6 shows the DC simulation of it. A comparatively large voltage of 3V is chosen to make sure M4 is in the saturation region because it is almost close to the voltage supply. As all MOSFETs are in the same scale, we can have the value of V_{TH} and V_{OD} from Figure 2.6, respectively equals 0.503V and 0,299V. Following the calculation steps above, the lowest voltage of M4 is about 1.1V. Figure 2.7 depicts the current through M4 with respect to the DC voltage sweep of the drain voltage of M4. Figure 2.8 presents the rough result when M4 is about to go into the saturation region. The drain voltage of M4 at that specific point is about 1.1V, which is exactly in line with the calculation before.

In the following part, the simulation results of wide-swing cascode current mirrors are discussed. Figure 2.9 shows the schematic of a wide-swing current mirror, M5 and M6 are utilized to give a bias gate voltage of M4. Figure 2.10

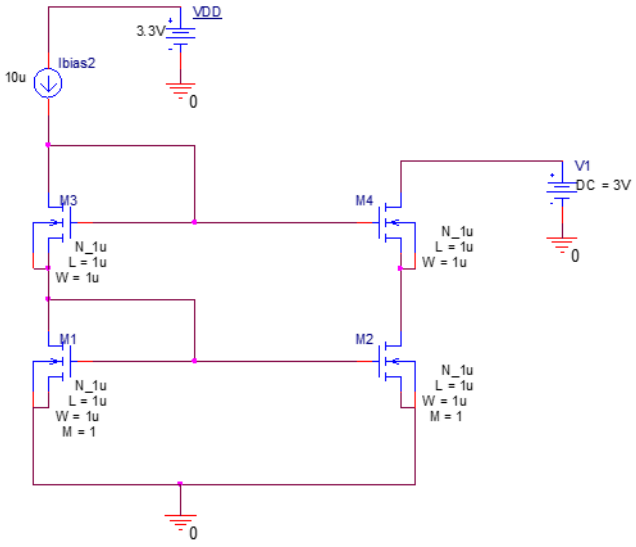


FIGURE 2.5: Classic cascode current mirror schematic

NAME	M_M2	M_M3	M_M4	M_M1
MODEL	N_1u	N_1u	N_1u	N_1u
ID	1.00E-05	1.00E-05	1.00E-05	1.00E-05
VGS	9.29E-01	9.29E-01	9.18E-01	9.29E-01
VDS	9.41E-01	9.29E-01	2.06E+00	9.29E-01
VBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00
VTH	5.03E-01	5.03E-01	5.03E-01	5.03E-01
VDSAT	2.99E-01	2.99E-01	2.93E-01	2.99E-01
Lin0/Sat1	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
if	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
ir	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
TAU	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
GM	3.63E-05	3.63E-05	3.74E-05	3.63E-05
GDS	4.83E-07	4.86E-07	3.14E-07	4.86E-07
GMB	1.86E-05	1.86E-05	1.92E-05	1.86E-05
CBD	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGSOV	2.00E-16	2.00E-16	2.00E-16	2.00E-16
CGDOV	2.00E-16	2.00E-16	2.00E-16	2.00E-16
CGBOV	8.00E-17	8.00E-17	8.00E-17	8.00E-17
CGS	9.21E-16	9.21E-16	9.21E-16	9.21E-16
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00

FIGURE 2.6: Bias condition of MOSFETs

shows the bias condition of all MOSFETs. V_{TH} equals 0.503V and V_{OD} is about 0.3V. Figure 2.11 shows the bias voltage. The gate voltage of M4 equals 1.28V, which meets the requirement of being more than and closer $V_{OD} + V_{TH}$, which is 1.1V. Then, according to equation 2.10, the minimum voltage of M4 is calculated to be 0.6V. Figure 2.12 depicts the current through M4 with respect to the DC voltage sweep of the drain voltage of M4. Figure 2.8 presents the rough result when M4 is about to go into the saturation region. The drain voltage of M4 is 0.583V when it is on the brink of saturation. These results are in agreement with those obtained by theoretical calculation.

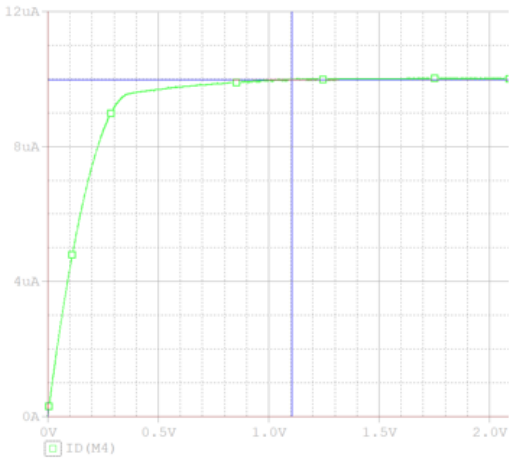


FIGURE 2.7: The current through M4 with respect to the drain voltage of M4(1)

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		9.979u		
	X Values	1.1060	0.000	1.1060		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	ID(M4)	9.979u	0.000	9.979u		0.000	0.000	9.979u	0.000	4.9895u

FIGURE 2.8: Result window of specific point

Furthermore, when the drain voltage of M4 is set to 0.6V, a comparison of two circuits is done in terms of output impedance. As graphed in Figure 2.14, the wide-swing cascode current mirror structure has a larger output impedance, which means that it can achieve a higher gain.

In accordance with the present results, previous studies have demonstrated that the wide-swing cascode current mirror's minimum required output voltage is decreased to $2V_{OD}$. That is its output voltage swing has risen by one V_{TH} as compared to the classic current mirror (Sing et al., 2020).

2.2.2 Differential Input Pair

In Figure 2.1, M1 and M2 compose the differential input pair. Firstly, two identical MOSFETs are employed so that the tail current is equally distributed to two MOSFETs. Secondly, NMOS is more suitable than PMOS in this circuit because of its higher electron mobility and transition frequency. To be more detailed, since the transconductance, g_m, is used to calculate the small-signal gain, NMOS

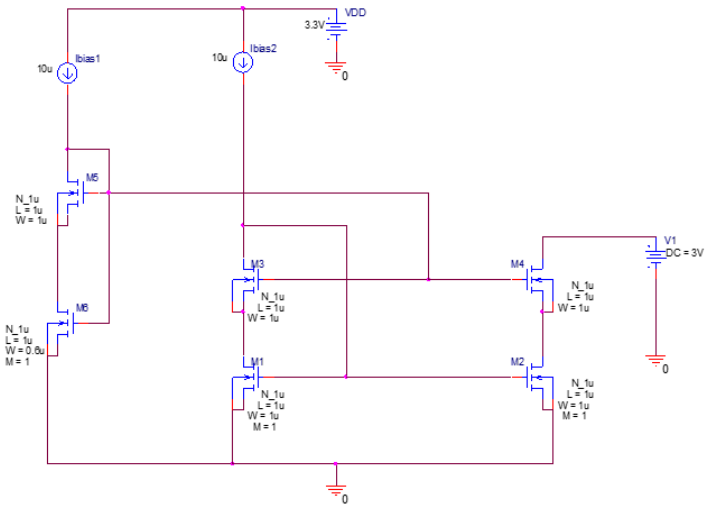


FIGURE 2.9: Wide-swing cascode current mirror schematic

NAME	M_M5	M_M1	M_M3	M_M2	M_M6
MODEL	N_1u	N_1u	N_1u	N_1u	N_1u
ID	1.00E-05	1.00E-05	1.00E-05	1.00E-05	1.00E-05
VGS	9.29E-01	9.40E-01	9.35E-01	9.40E-01	1.28E+00
VDS	9.29E-01	3.50E-01	5.90E-01	3.71E-01	3.55E-01
VBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
VTH	5.03E-01	5.03E-01	5.03E-01	5.03E-01	6.38E-01
VDSAT	2.99E-01	3.05E-01	3.02E-01	3.05E-01	3.71E-01
Lin0/Sat1	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
if	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
ir	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
TAU	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
GM	3.63E-05	3.49E-05	3.57E-05	3.51E-05	2.28E-05
GDS	4.86E-07	1.16E-06	6.67E-07	1.07E-06	3.35E-06
GMB	1.86E-05	1.80E-05	1.84E-05	1.80E-05	1.63E-05
CBD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGSOV	2.00E-16	2.00E-16	2.00E-16	2.00E-16	1.20E-16
CGDOV	2.00E-16	2.00E-16	2.00E-16	2.00E-16	1.20E-16
CGBOV	8.00E-17	8.00E-17	8.00E-17	8.00E-17	8.00E-17
CGS	9.21E-16	7.93E-16	9.21E-16	8.15E-16	4.34E-16
CGD	0.00E+00	3.83E-16	0.00E+00	3.16E-16	3.55E-16
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	M_M4
MODEL	N_1u
ID	1.00E-05
VGS	9.14E-01
VDS	2.63E+00
VBS	0.00E+00
VTH	5.03E-01
VDSAT	2.91E-01
Lin0/Sat1	-1.00E+00
if	-1.00E+00
ir	-1.00E+00
TAU	-1.00E+00
GM	3.79E-05
GDS	2.79E-07
GMB	1.94E-05
CBD	0.00E+00
CBS	0.00E+00
CGSOV	2.00E-16
CGDOV	2.00E-16
CGBOV	8.00E-17
CGS	9.21E-16
CGD	0.00E+00
CGB	0.00E+00

FIGURE 2.10: Bias condition of MOSFETs

with higher g_m is preferred, Moreover, a higher frequency is easier for engineers to maintain the high bandwidth (Sing et al., 2020).

Two factors should be considered when calculating the input common mode range (ICMR): M1 should be in the saturation region and v_i is large enough to support M3 in the saturation region. For M1 in the saturation region, it satisfies:

$$V_{GD1} \leqslant V_{TH} \tag{2.11}$$

$$v_i - V_{D1} \leqslant V_{TH} \tag{2.12}$$

$$v_i \leqslant V_{TH} + V_{D4} \tag{2.13}$$

(v_i denotes the input voltage)

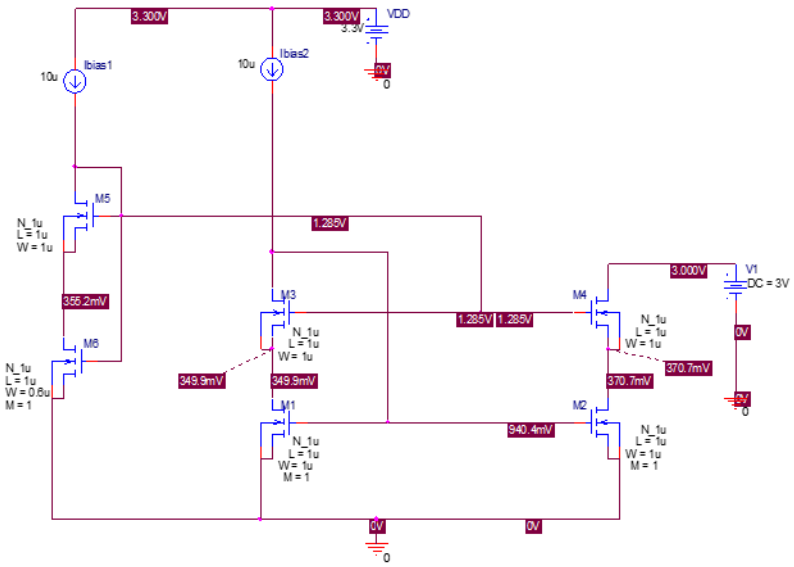


FIGURE 2.11: Bias voltage simulation

The highest V_{D4} can be achieved when M4 is on the edge of the saturation region, which means $V_{D4} = V_{DD} - V_{OD}$. Therefore,

$$v_i \leqslant V_{TH} + V_{DD} - V_{OD} \tag{2.14}$$

For calculating the lowest voltage, v_i satisfy: $v_i = V_{GS1} + V_{D3}$ Likewise, the lowest V_{D3} is achieved when it is on the edge of the saturation region, meaning that $V_{D3} = V_{OD}$ Therefore,

$$v_i \geqslant V_{GS} + V_{OD} \tag{2.15}$$

$$v_i \geqslant 2V_{OD} - V_{TH} \tag{2.16}$$

Consequently, the ICMR is:

$$2V_{OD} - V_{TH} \leqslant v_i \leqslant V_{TH} + V_{DD} - V_{OD} \tag{2.17}$$

2.2.3 Bias Circuit

Figure 2.15 depicts a topology to bias the folded cascode op-amps. Consider for example, the bias circuit of the folded cascode operational amplifier is completed by the combination of M3, M4, M5, M12, M13, M14, M15, and R1, R2. The tail

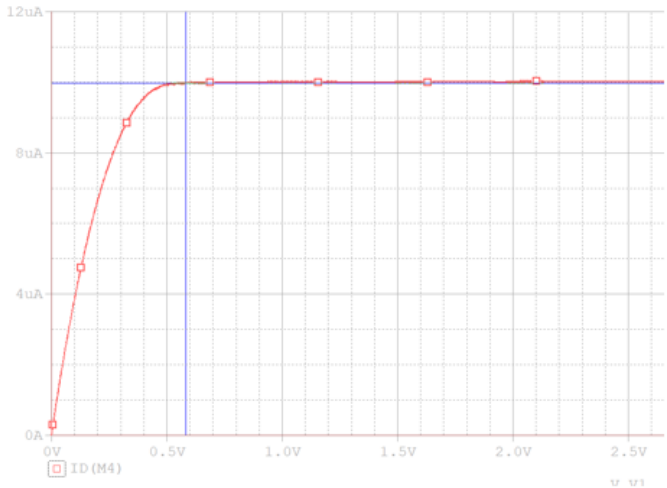


FIGURE 2.12: The current through M4 with respect to the drain voltage of M4(2)

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		9.978u		
	X Values	583.000m	0.000	583.000m		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	ID(M4)	9.978u	0.000	9.978u		0.000	0.000	9.978u	0.000	4.9889u

FIGURE 2.13: Result window of specific point

current flowing through M3 is copied by the usage of M15. M4 and M5 are upper current sources copied from M14. By variation of the width ratio of M4 and M5 to M14, the current I_4 and I_5 can be set to $1.2I_3$, for the purpose of splitting the current respectively to the differential pair and current mirror. Two resistors R1 and R2 are used to enable the circuit to be self-biased (Allen, 2002). Since there is barely any current flowing through the gate of MOSFETs, we can calculate them as $V_{DS13(sat)/I_{13}}$and $V_{DS6(sat)/I_6}$.

This topology largely decreases the number of external MOSFETs so that chip area can be saved. Moreover, it assures the stability of the bias voltages since they do not need to be manually set and are less temperature sensitive as the

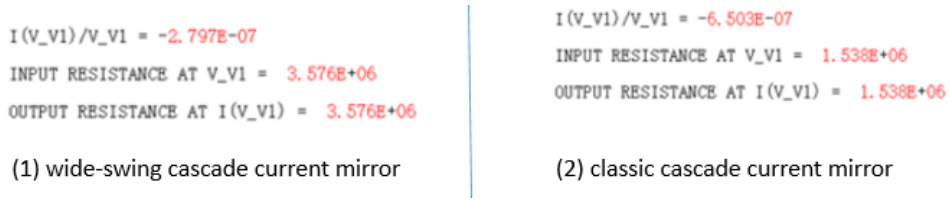


FIGURE 2.14: Output impedance of two current mirrors

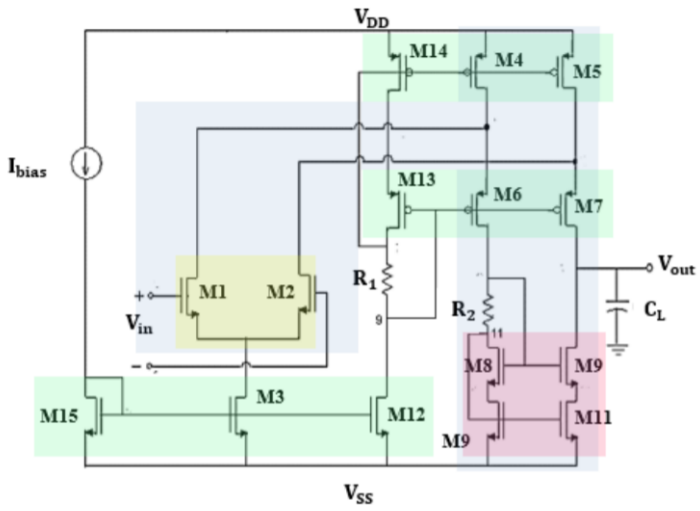


FIGURE 2.15: Biased folded cascode operational amplifier, Copyright © (Sing et al., 2020)

bias point is determined by size ratios only.

2.2.4 Other Parameters

The folded cascode op-amp has a large voltage gain and is extremely stable. It is its single-dominant-pole and high output resistance that has provided these positive attributes. The dominant pole is an important parameter in the small-signal model since it has to do with the stability of a closed-loop circuit. The folded cascode op-amp is actually a single stage operational amplifier; therefore, the dominant pole is determined by the load capacitance. Since the load capacitance is relatively large, the frequency of the dominant pole is correspondingly low because the dominant pole is given by:

$$\omega = -\frac{1}{R_{out}C_L} \tag{2.18}$$

This low frequency also gives a high phase margin, indicating the stability of the circuit. In addition, since there is only one load capacitor in this circuit, the S.R. (slew rate) is given by:

$$S.R = \frac{I_3}{C_L} \tag{2.19}$$

The output resistance can be regarded as two resistors in parallel. As seen from the output node, they are the upper resistor and the down resistor. Consider Figure 2.1 for example, when the channel length modulation is neglected, the output resistance equals $(g_{m7}r_{ds7}r_{ds11})||(g_{m9}r_{ds9}r_{ds11})$ assuming $g_m r_{ds} >> 1$. Also, if these four MOSFETs have same $g_m r_{ds}$, the output resistance becomes

$$\frac{g_m r_{ds}^2}{2} \tag{2.20}$$

which suggests that the voltage gain is in the order of $(g_m r_{ds})^2$

2.3 Circuit Simulation

Circuit performance will be simulated and then examined in this part for different parameters of the circuit. Furthermore, a method to achieve a wider bandwidth is introduced and simulated. In the end, a table 2.38 summarizes all the simulation results, elaborating the performance of the circuit.

The open-loop simulation schematic 2.16, including its simplified model 2.17 and simplified closed-loop simulation model 2.22 analyses are depicted as follows. A special topology is used in open-loop simulation. To ensure that the output does not affect the negative input, a high inductor is used for filtering the AC feedback signal. A big capacitor is also utilized to guarantee that just the small signal is allowed to flow through. In addition, the inductor guarantees that the loop is closed at DC. At high frequencies, however, the impedance of this very large inductor is practically infinite resulting in open loop. The open-loop gain, phase margin, cut-off frequency, and 3dB bandwidth are determined by the former simulation. The latter is in charge of achieving the settling time and S.R.

Slew Rate (SR) is defined as the maximum rate of voltage or current change, or any other electrical quantity, per unit of time (Wikipedia, 2021d). SR is related to the large signal behavior since the op-amp slews and charges the capacitor with a constant current source only when the input signal is high enough; otherwise, the output slope will increase linearly according to the input signal. To

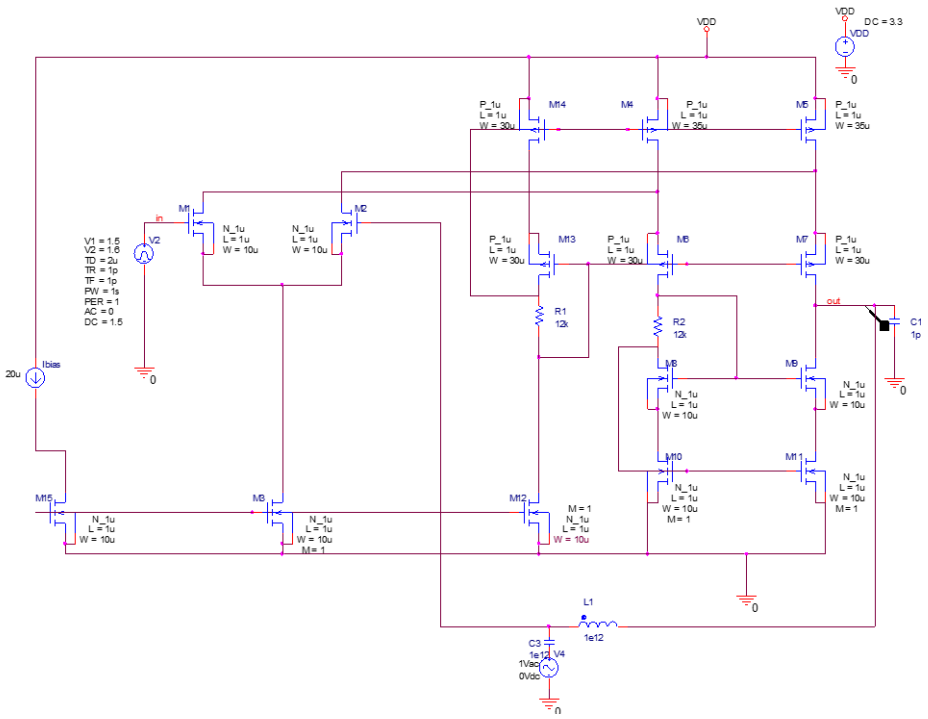


FIGURE 2.16: Open-loop simulation schematic

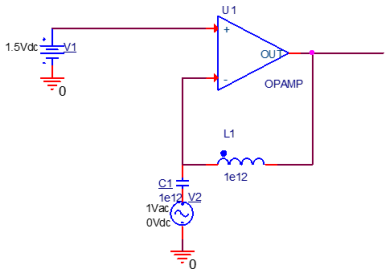


FIGURE 2.17: Simplified open-loop simulation model

account for the ripples, the SR is calculated at two points: when the output voltage reaches 10 percentage and 90 percentage of the ultimate amount of the modified voltage. Therefore, S.R. is 19.76V/us, which is in line with the calculation step 2.19, 20V/us.

Settling time is the time required for the output to reach and remain within a given error band following some input stimulus (Wikipedia, 2021c). Figure 2.25 suggests the specific time where the output voltage fluctuation will remain within a 2 percentage error band in comparison to the final output voltage.

The ICMR simulation 2.26 has a total 1V AC differential input, $V_1 - V_2$. The AC

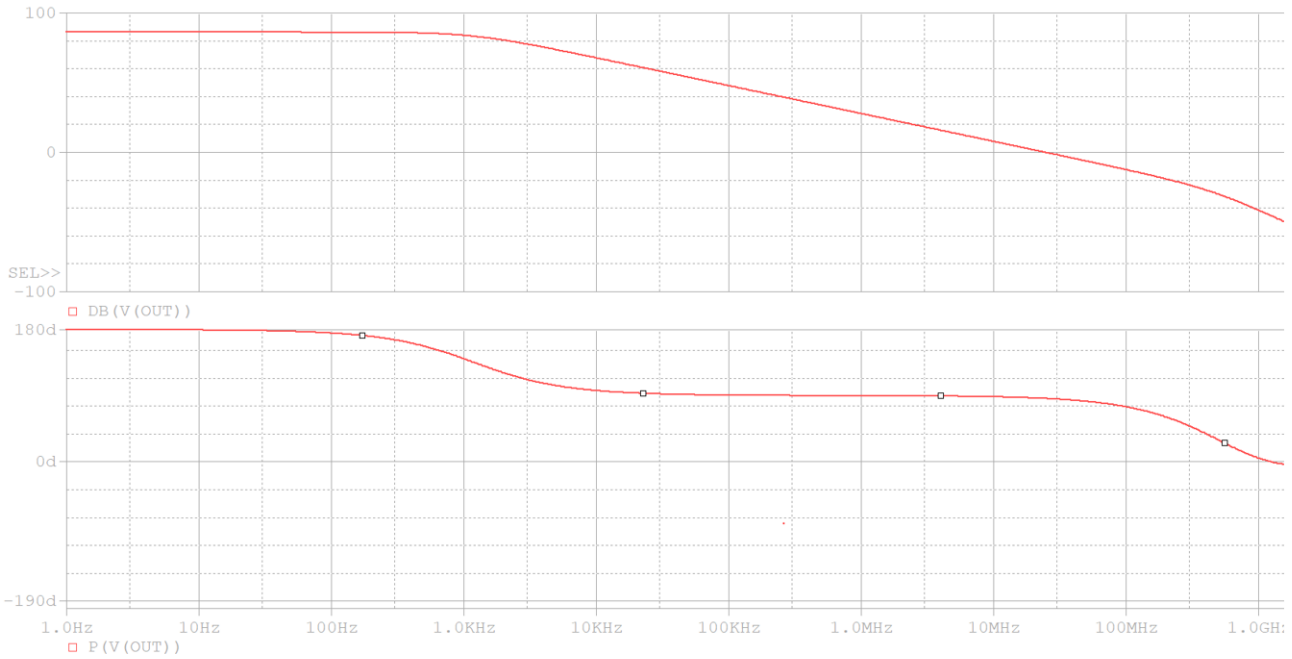


FIGURE 2.18: Open-loop simulation graph

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-1.2207u		
	X Values	1.1877	1.0000	187.716m		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	P(V(OUT))	179.945	179.954	-9.0874m		93.869	93.878	179.954	179.945	179.949
CURSOR 1,2	DB(V(OUT))	86.076	86.076	-1.2207u		0.000	0.000	86.076	86.076	86.076

FIGURE 2.19: Open-loop gain

output is measured when every time V_4 changes. The range of V_1 is set to 0V to 3.3V. The upper graph in Figure 2.27 depicts the maximum voltage value in dB of each line in the lower graph. Then, the range of the input voltage when this op-amp works properly is shown from 2.28. It is approximately 0.53V to 3.27V.

The output swing is also simulated. As shown in Figure 2.31, the usage of two voltage-controlled voltage sources E1 and E2 can simplify the DC sweep simulation because only Vd, the differential input, needs to sweep. The maximum output voltage is calculated as $V_{DD} - 2V_{OD}$ theoretically, which approximately

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-86.072		
	X Values	24.269M	1.000	24.269M		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	P(V(OUT))	86.181	179.9	-93.773		86.176	93.878	179.954	86.181	133.067
CURSOR 1,2	DB(V(OUT))	4.6088m		-86.072		0.000	0.000	86.076	4.6088m	43.040

FIGURE 2.20: Phase margin

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-2.8224		
	X Values	1.1567K	1.0000	1.1557K		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	P(V(OUT))	136.267	179.954	-43.687		53.013	93.878	179.954	136.267	158.110
CURSOR 1,2	DB(V(OUT))	83.254	86.076	-2.8224		0.000	0.000	86.076	83.254	84.665

FIGURE 2.21: 3dB gain bandwidth

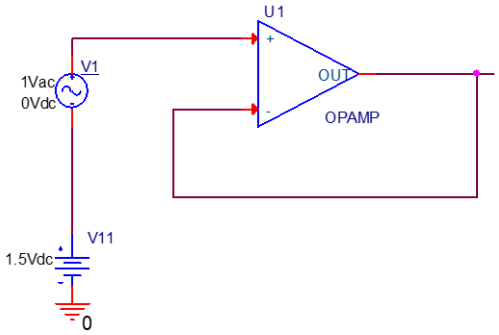
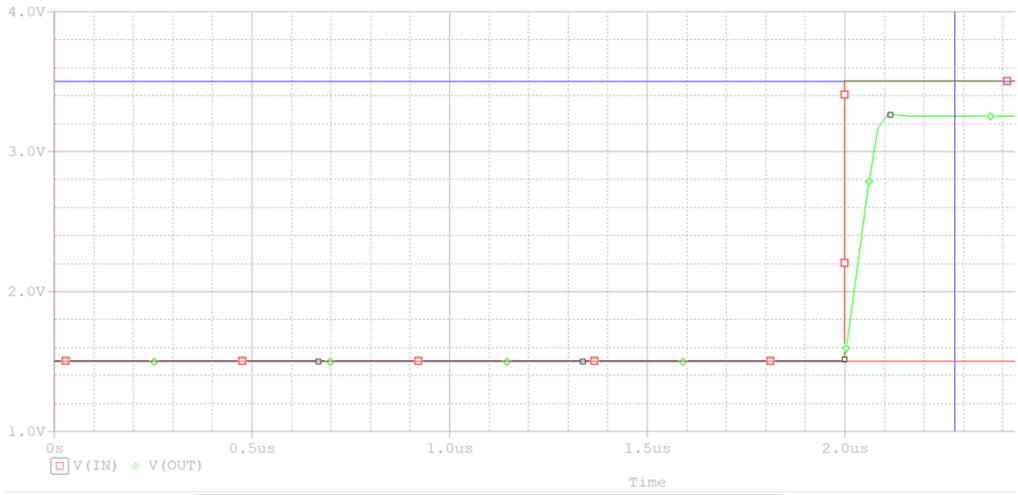


FIGURE 2.22: Simplified closed-loop simulation model

equals 3V. From the open-loop simulation, the gain is known as 86dB. Hence, the maximum value for the Vd is supposed to be 0.15mV. As the minimum value for output voltage is $2V_{OD}$, the range of Vd is chosen from -0.2mV to +0.2mV. Figure 2.30 indicates the output swing, which is from 0.3V to 2.85V. This asymmetry graph is systematic offset caused by the controversy between two currents from the two current mirrors. However, it doesn't play an important role since this circuit is often used with feedback which compensate this systematic offset.

The amplification imparted to signals that appear on both inputs compared to the CM (common mode) is referred to as common-mode voltage gain. In the Common mode simulation schematic 2.31, both input sides have the same 1Vac and DC input. Instead of simply changing the power direction of V_2 in 2.26, a common voltage source is preferred as there will be input noise in reality. The performance analysis of common mode simulation 2.32 is made, and the average value of it is about -55dB.

The CMRR (Common-mode rejection ratio) is defined as the ratio of the differential gain to the common-mode gain. Generally, the result is expressed in dB to indicate the suppression and attenuation of the unwanted common-mode signals passing through the amplifier. To simplify the calculation steps, it can be



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.0000		
	X Values	2.2782u	0.000	2.2782u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(IN)	3.5000	1.5000	2.0000		0.000	0.000	3.5000	1.5000	2.5000
	V(OUT)	3.2507	1.5000	1.7508		-249.267m	-52.649u	3.2507	1.5000	2.3753

FIGURE 2.23: Closed-loop transient simulation

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.0000		
	X Values	2.0068u	0.000	2.0068u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(IN)	3.5000	1.5000	2.0000		0.000	0.000	3.5000	1.5000	2.5000
	V(OUT)	1.6552	1.5000	155.277m		-1.8448	-52.649u	1.6552	1.5000	1.5776

(1) the output voltage reaches 10% of the final amount of the changed voltage

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.0000		
	X Values	2.0785u	0.000	2.0785u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(IN)	3.5000	1.5000	2.0000		0.000	0.000	3.5000	1.5000	2.5000
	V(OUT)	3.0725	1.5000	1.5725		-427.536m	-52.649u	3.0725	1.5000	2.2862

(2) the output voltage reaches 10% of the final amount of the changed voltage

FIGURE 2.24: Two specific points

calculated as differential mode gain (dB) minus common-mode gain (dB). The greater the CMRR is, the better the op-amps suppress the common-mode signals.

The PSRR (power supply ripple rejection ratio) is the ratio of the change in supply voltage (in volts) to the change in output (in volts). When the power supply voltage utilized by the operational amplifier varies, the influence on the output voltage must be limited for high-quality amplifiers.

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.0000		
	X Values	2.0887u	0.000	2.0887u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(IN)	3.5000	1.5000	2.0000		0.000	0.000	3.5000	1.5000	2.5000
	V(OUT)	3.1836	1.5000	1.6836		-316.425m	-52.649u	3.1836	1.5000	2.3418

FIGURE 2.25: Settling time

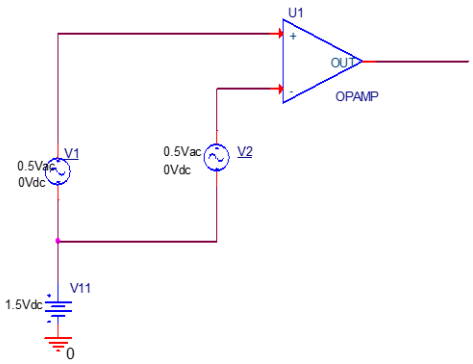


FIGURE 2.26: The simplified ICMR simulation model

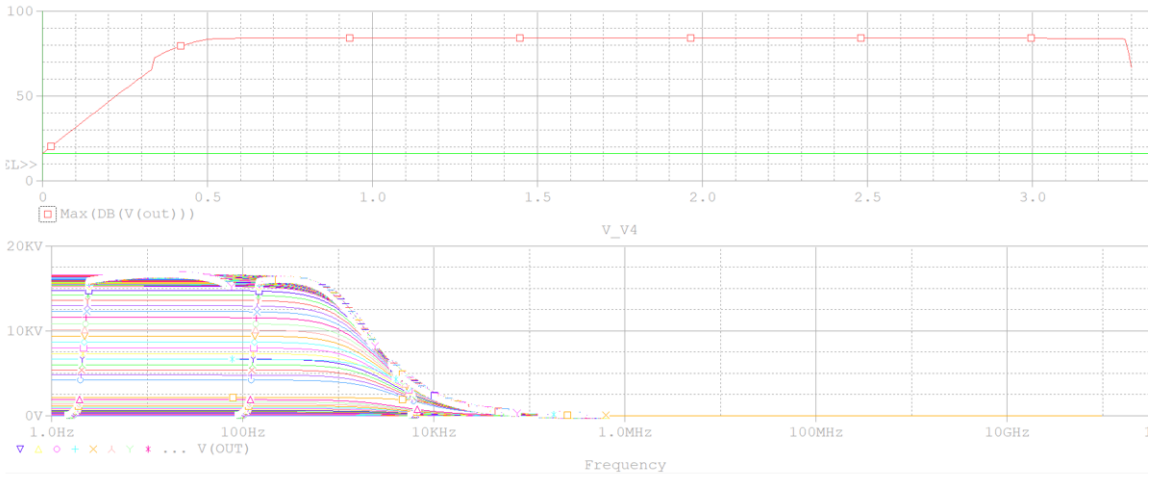


FIGURE 2.27: The performance analysis of ICMR simulation

It is widely recognized that GCF (Gain Crossover Frequency) should be smaller than PCF (Phase Crossover Frequency) for achieving stability. Additionally, the bigger the difference between them is, the better stability the circuit can achieve. In general negative feedback system 2.35, A represents the feedforward system and K represents the feedback ratio. Consequently, by decreasing the feedback ratio K, the whole bode diagram panning down vertically and then causing GCF to move to the left. When the PCF stays the same, the difference between them is bigger. As a result, the circuit is more stable. The simulation above is performed when the feedback ratio K is 1 (unity gain feedback); thus, the bandwidth can be further increased by decreasing the K. Figure 2.36 utilizes two resistors to form the feedback circuit. The ratio K is reduced to $R2/(R1 + R2)$. Due to the fact that the output impedance of the original amplifier is in Meg ohms, which is quite huge, R1 and R2 must be on the scale of Meg ohms; otherwise, the

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		67.755		
	X Values	529.644m	0.000	529.644m		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	Max(DB(V(out)))	83.960	16.205	67.755		0.000	0.000	83.960	16.205	50.083

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		67.472		
	X Values	3.2708	0.000	3.2708		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	Max(DB(V(out)))	83.677	16.205	67.472		0.000	0.000	83.677	16.205	49.941

FIGURE 2.28: The range of ICMR

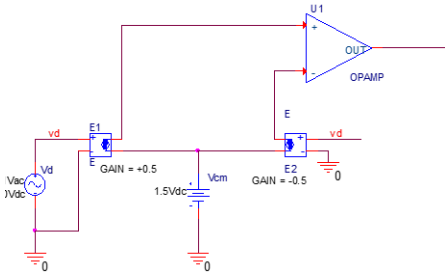


FIGURE 2.29: The simplified output Swing simulation model

output voltage gain will be greatly reduced. If the circuit must drive a heavy load, a source follower stage is recommended since its input impedance is very large (no gate current at DC) and has a low output impedance of $1/g_m$. The new bandwidth from figure 2.37 is almost 30MHz, which is comparatively wider than the previous bandwidth 24.3MHz. If R2 is set to 1 Meg Ohm, bandwidth will further increase as K is further reduced.

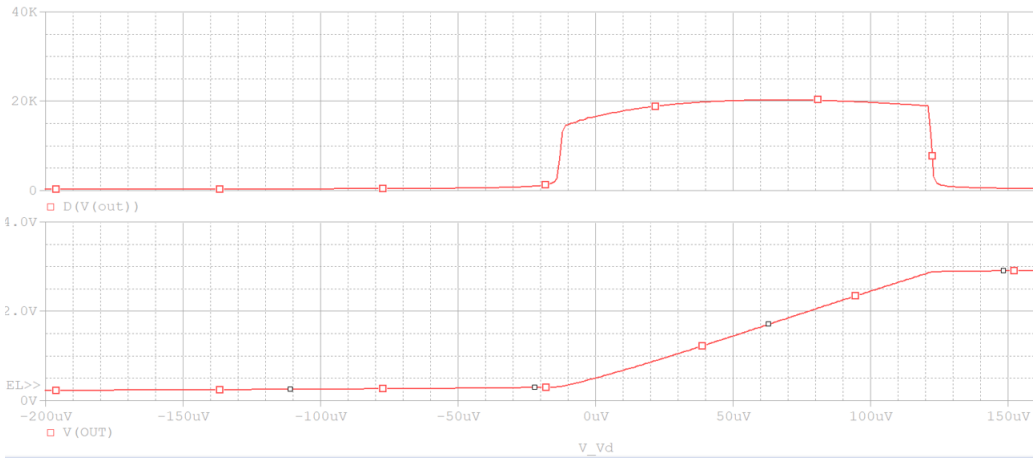


FIGURE 2.30: Output Swing Graph: The lower graph shows the change of output voltage in terms of the input; The top graph shows the derivative of the maximum value of the lower graph

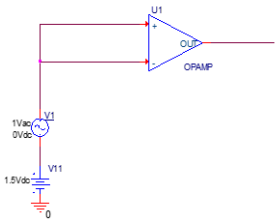


FIGURE 2.31: The simplified CM simulation model

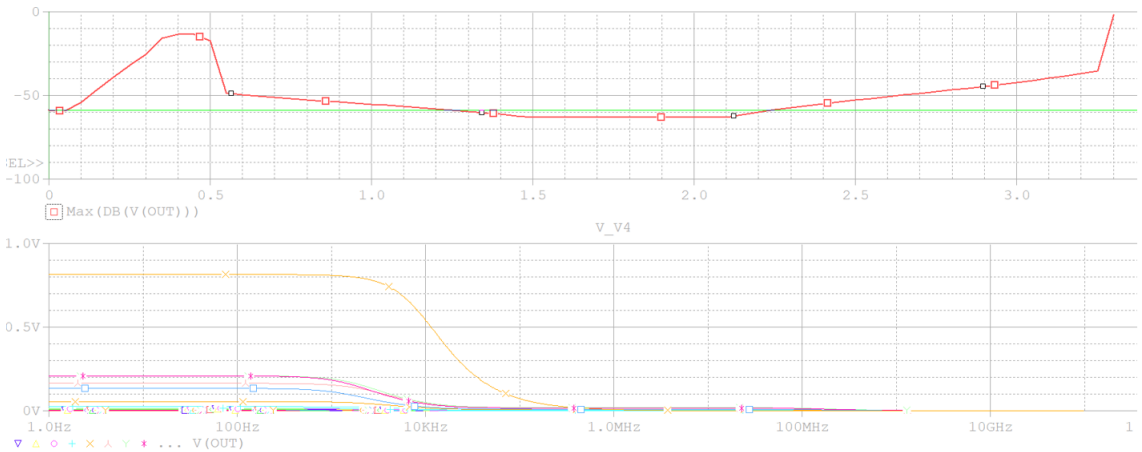


FIGURE 2.32: The performance analysis of CM simulation

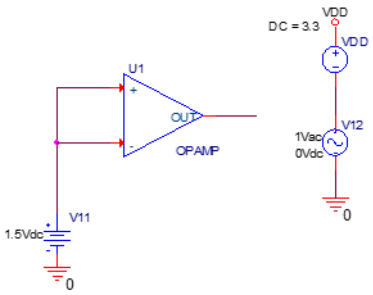
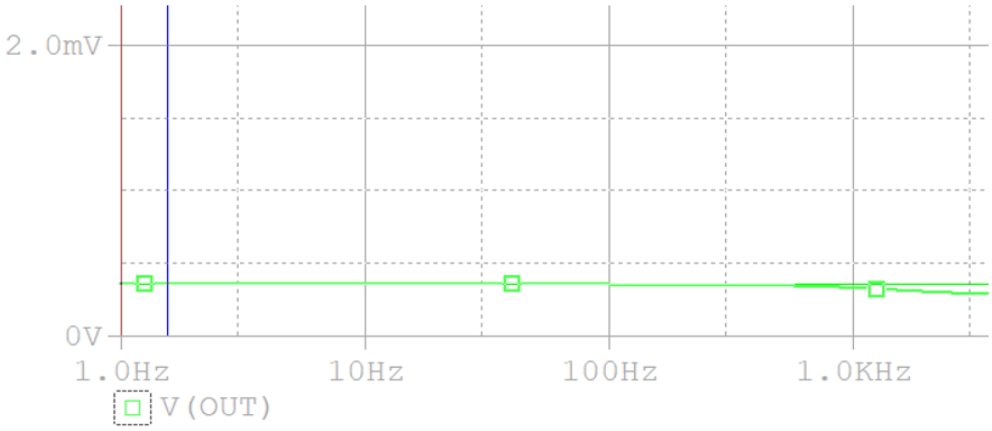


FIGURE 2.33: The simplified PSRR simulation model



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-49.586p		
	X Values	1.5476	1.0000	547.587m		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(OUT)	352.990u	352.990u	-49.586p		0.000	0.000	352.990u	352.990u	352.990u

FIGURE 2.34: The graph of PSRR simulation

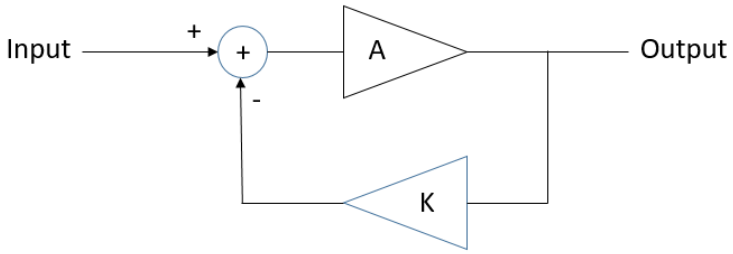


FIGURE 2.35: General negative feedback system

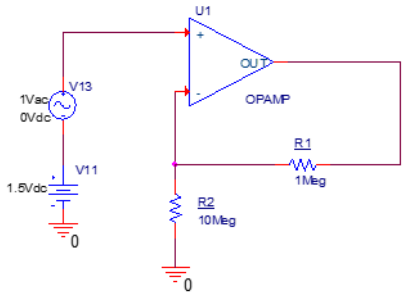


FIGURE 2.36: Simplified decreased feedback model

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	29.992M	1.0000	29.992M
CURSOR 1,2	P(V(OUT))	-112.043	-1.9250u	-112.043
	DB(V(OUT))	-2.9648	821.753m	-3.7866

FIGURE 2.37: New bandwidth

Open-loop gain (DB)	86
Phase margin (degree)	86
Cut-off frequency (MHz)	24.3
3 dB Bandwidth (KHz)	1.16
ICMR (V)	0.53 ~ 3.3
Output Swing (V)	0.3 ~ 2.85
CMRR (DB)	141
PSRR (DB)	69
S.R (V/us)	19.76
Settling time (us)	0.0887

FIGURE 2.38: The summary of simulation results

3

MILLER OPERATIONAL AMPLIFIER

3.1 Circuit Introduction

The most commonly used multiple stage amplifiers in CMOS analog integrated circuits are two-stage transconductance op-amps. Figure 3.1 illustrates the model of them. These op-amps are chosen because they provide good electrical properties, such as high dc gain, linearity, output swing, and CMRR. Moreover, it also has a simple design strategy and is easy to bias (Palmisano and Palumbo, 1995).

Compared to the single-stage amplifiers, the multiple-stage amplifiers have higher dc gain with fewer constraints on the power supply. However, they have drawbacks concerning the stability of the feedback system because they create two poles during each stage, which implies that the circuit has a two-pole transfer function. Therefore, a compensation topology is required to ensure the stability of the circuit (Gomez, 2019).

Generally, a two-stage op-amp uses miller compensation for stability. This method is also referred to as pole splitting because the poles will be shifted. Though the phase margin can be largely increased with pole splitting, this method creates an right-half-plane zero (RHPZ). It leads to a negative phase shift in the open-loop gain at a relatively high frequency, which reduces the

maximum achievable gain bandwidth and finally influences the stability of the circuit (**palmisano1995opmtimized**).

To date, several studies have revealed various techniques to resolve the problems of the RHPZ, such as Nulling Resistor, Voltage Buffer, Current Buffer, and Current/Voltage Buffer (Palmisano and Palumbo, 1995). All of them provide a higher gain bandwidth. Among them, the gain-bandwidth efficiency and PSRR performance of the Current Buffer are likewise impressive. Two other techniques of applying the Nulling Resistor and Voltage Buffer will be further explained in the next section.

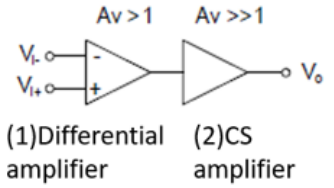


FIGURE 3.1: Two stage op-amp model, Copyright © (*Two-Stage Miller Operational Amplifier*)

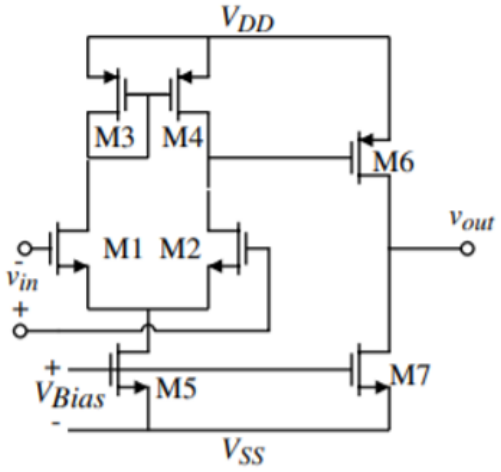


FIGURE 3.2: Miller op-amp, Copyright © (Allen, 2002)

3.2 Circuit Description

First and foremost, the original two-stage op-amp is explained. Then, the following part of this section moves on to describe in greater detail the Miller op-amp.

What's more, compensation methods of Nulling Resistor and Voltage Buffer will be also discussed.

As shown in Figure 3.2, this design is the combination of the simple single-ended differential amplifier and a common source (CS) amplifier with a current source load. The first stage produces an amplified signal of the differential input. The second stage of a CS amplifier is then cascaded to it, which improves the voltage gain and serves as an inverted output stage (**Texas A&M University**). What follows are the analyses of the DC voltage gain and the frequency response.

As previously stated, it has the advantages of high dc gain. If the channel length modulation is neglected and $g_m r_{ds}$ is much larger than 1, then the voltage gain can be calculated as the product of two stages' voltage gain, $A_{v1}A_{v2}$ given by:

$$Av = (G_{mA} r_{ds2} r_{ds4}) * (G_{mB} r_{ds6} r_{ds7}) \tag{3.1}$$

where the former and latter factor respectively stands for the voltage gain of the differential stage and the CS stage (Hamzah, Jambek, and Hashim, 2014).

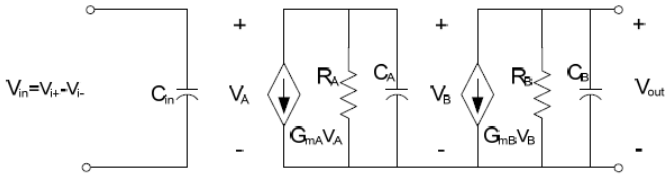


FIGURE 3.3: Operational amplifier small-signal model, Copyright © (*Two-Stage Miller Operational Amplifier*)

The Small-signal model 3.3 of the Miller op-amp is used to analyze the frequency response. The capacitor C_{in} represents the capacitance mostly generated from gate to source in MOSFETs. g_{mA}, g_{mB} respectively represents the transconductance of the first stage and the second stage. Additionally, R_A and R_B respectively model the output impedance of the two stages, The input capacitance of the second stage and the output capacitance of the first stage make up the capacitance C_A. The second step follows the same pattern. It should be noted that in R_B and C_B, the load capacitor and resistor are also incorporated. As the circuit is a two-pole system without zeros, the values for the poles can be expressed as $-\frac{1}{R_A C_A}$ and $-\frac{1}{R_B C_B}$. Hence, the system is unlikely to be stable in unity-gain feedback due to the proximity of the poles and the significant DC gain

(Texas A&M University). The compensation methods will be introduced in the next sections.

3.2.1 Miller Compensation

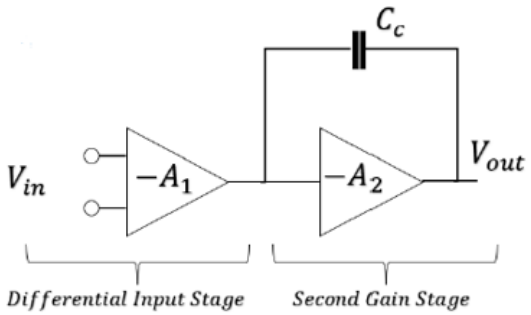


FIGURE 3.4: Block diagram for Miller compensation, Copyright © (Gomez, 2019)

As was mentioned in the previous section, Miller Compensation is pole splitting in disguise. In block diagram 3.4, it illustrates that a capacitor Cc is placed between the output of the second stage and the first stage. It takes advantage of the Miller Effect to compensate the circuit. The original poles will be shifted after the Miller Capacitor is added to the circuit. Therefore, these two-stage op-amps utilizing a Miller capacitor are also named Miller op-amp. Figure 3.3 shows

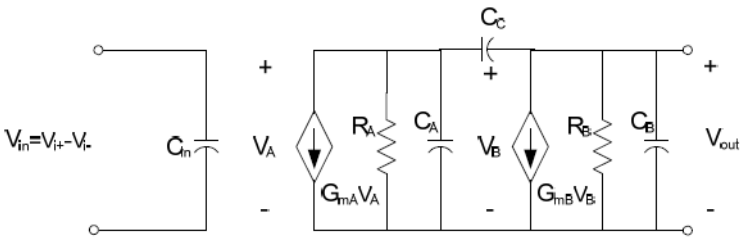


FIGURE 3.5: Operational amplifier small-signal model with Miller compensation, Copyright © (*Two-Stage Miller Operational Amplifier*)

the modified small-signal Model with Miller Capacitor Cc added. By applying Kirchhoff's Current Law at two nodes of the Miller Capacitor Cc, the transfer function can be obtained. Assuming R_A is large and C_A is small, the transfer

function is given by:

$$H(s) = \frac{\frac{g_{mA}}{C_B}(s - \frac{g_{mB}}{C_c})}{(s + \frac{1}{g_{mB}R_AR_BC_C})(s + \frac{g_{mB}}{C_B})} \tag{3.2}$$

Also, the new values for two poles can be expressed as:

$$p_1 = -\frac{1}{g_{mB}R_AR_BC_C} \tag{3.3}$$

$$p_2 = -\frac{g_{mB}}{C_B} \tag{3.4}$$

As the pole-zero plot 3.6 depicts, two poles split apart, one pole moving to a lower frequency and the other moving to a higher frequency by a factor of $g_{mB}R_B$. Consequently, gain crossover frequency (GCF) is reduced, enabling the circuit to achieve a larger phase margin by making the circuit behave like a single-pole amplifier (Gomez, 2019).

This circuit acts as an integrator at low frequencies while the compensation capacitor is shorted at high frequencies. Therefore, the second stage can be seen as a diode-connected transistor at a high frequency, presenting a $1/g_{mB}$ load to the first stage. In addition, the gain of the circuit is decreased to only $\frac{1/g_{mA}}{1/g_{mB}}$ (Gray and Meyer, 1982).

As was pointed out in the previous section, this method creates an RHPZ. Since a zero always arises from the multiple paths from the input to output, it can be speculated that this RHPZ is caused by the forward path through the compensation capacitor to the output. Turning now to two techniques for the compensation of RHPZ, fixing its contribution to a negative phase shift in the open-loop.

3.2.2 Voltage Buffer

In the feedback compensation circuit between the output of the second stage and the Miller Capacitor, a voltage buffer is introduced as shown in Figure 3.7. It is connected in series with the Miller Capacitor to block the path from the compensation capacitor to the output, improving the transient response significantly. Furthermore, the low output impedance of the voltage buffer will add to

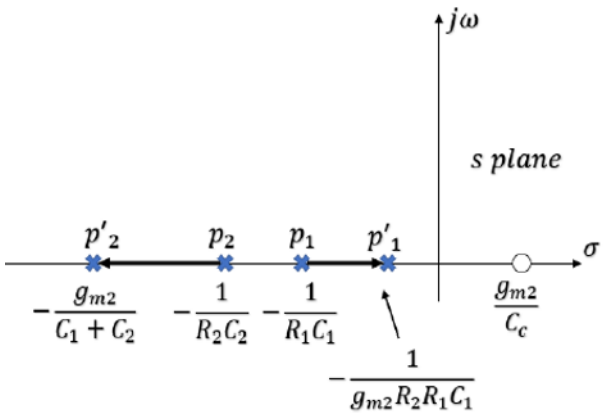


FIGURE 3.6: Pole-zero plot for Miller compensation, Copyright © (Gomez, 2019)

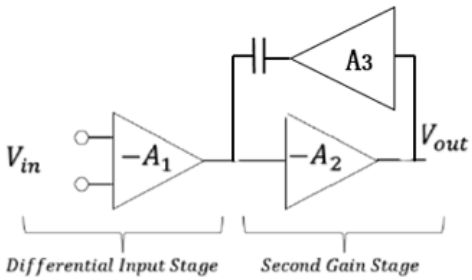


FIGURE 3.7: Block diagram for voltage buffer

the advantage of setting up an effective feedback circuit. Therefore, the voltage buffer which is made up of a common drain stage is preferred (Pakala et al., 2015).

The schematic of the NMOS common drain topology is shown in Figure 3.8. When "the gate terminal of the transistor serves as the input, the source is the output and the drain is common to both (input and output)", the circuit is using a common drain topology. Since the bias current source I and V_{SG9} are fixed, the output will instantly change according to any small-signal change at the input to maintain the constant value of V_{SG9}. Additionally, the output impedance looking into the source of it is $1/g_{m9}$, which is relatively low (Wikipedia, 2021a). It's worth noting that the power supply will increase and the third pole is created when using this method to compensate the RHPZ. The latter factor has not to be considered because it is located in a relatively large frequency. However, due to the existence of the third stage, the circuit will cost extra value to support the

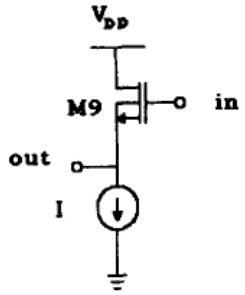


FIGURE 3.8: Common-drain topology, Copyright © (Wikipedia, 2021a)

bias operation.

3.2.3 Nulling Resistor

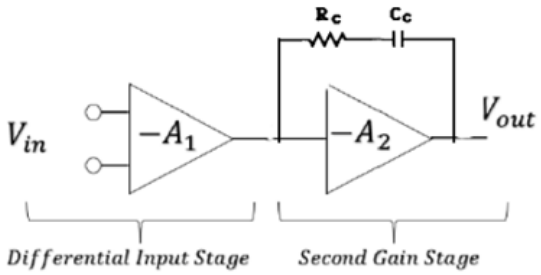


FIGURE 3.9: Block diagram for nulling resistor

Then, the compensation technique with Nulling Resistor will be introduced. A nulling resistor is placed in series with the compensation capacitor as block diagram 3.9 illustrates. This method is the most popular technique because only one MOS transistor biased in the triode region is required to serve as a variable resistance. As compared to the voltage buffer, this technique is easier to achieve because it will not behave in a complex way resulting from the additional poles and zeros (Palmisano and Palumbo, 1995).

After adding a nulling resistor, the drain current in the second stage must be drawn the most current from the output current of the first stage. As a result, voltage change at the second stage's gate is proportional to the small-signal current from the first stage and inversely proportional to the second stage's transconductance (Palmisano and Palumbo, 1995). The influence of RHPZ is

essentially eliminated by setting RHPZ equal to the original second pole, canceling the effect of the zero in the transfer function. Consequently, the circuit increases the maximum achievable gain-bandwidth since this value is dependent on the second-pole frequency. From the small-signal model, the new zero can be analytically given by:

$$\omega_Z = \frac{1}{C_c(\frac{1}{G_{mB}} - R_c)} \tag{3.5}$$

where R_C should be larger than G_{m2} for the zero to stay in the left half-plane.

3.3 Circuit Simulation

Thus far, the former sections have argued all detailed information of the Miller op-amp. In this section, the two techniques mentioned above will be simulated, Miller compensation and Miller compensation with voltage buffer. The technique of applying a nulling resistor is skipped as the voltage buffer has provided a good phase margin. The same models and techniques of evaluating the folded cascode op-amp are also implemented in the simulation. In the end, the performance of the two circuits will be listed as tables.

3.3.1 Miller Compensation

The schematic of Miller op-amp in open-loop simulation is shown in Figure 3.10. In this circuit, M means the multiplication of the MOSFETs, meaning that two same MOSFETs are connected in parallel. In other words, the width of these MOSFETs are multiplied by the ratio M. The same MOSFETs are preferred over different MOSFETs due to the fact that it's hard to control the parameters like the mobility of MOSFETs in reality.

Additionally, the simulation results of the open-loop are also depicted in Figure 3.11. According to the theory, a decline in the phase should occur at a high frequency, which indicates there's an RHPZ. The gain of the second stage is approximately $2g_{m6}$, equal to 8.88 x 10^{-4}. Then the RHPZ frequency can be

calculated according to the equation:

$$\omega_Z = \frac{g_{m6}}{C_c} \tag{3.6}$$

$$f = \frac{\omega_Z}{2\pi} \tag{3.7}$$

which is finally equal to about 141MHz. This simulation result supports the previous finding because the phase margin decreases by 180 degrees from about 1MHz to 141MHz. In addition, the phase margin is observed an increment at a relatively high frequency. This phenomenon may result from the fact that the normal zero produced by the differential stage come to effect at a high frequency.

Some specific points are selected to show the open-loop gain, 3dB bandwidth, the cut-off frequency of the open-loop, and the phase margin in Figure 3.12. They are respectively equal to 85dB, 1.8KHz, 30MHz, and 38 degrees. A circuit should have a phase margin which is larger than 45 degree to achieve good stability; therefore, two other techniques are necessary for the Miller op-amp.

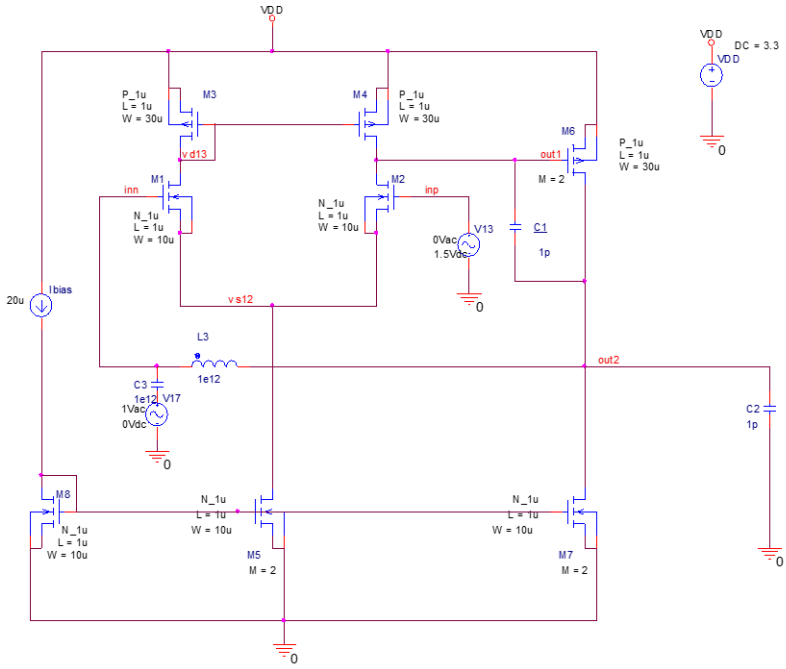


FIGURE 3.10: The schematic Of Miller compensation

From the closed-loop simulation 3.13, the 3db bandwidth of the closed-loop is 71.8MHz and a peaking is observed. This small peaking may result from the

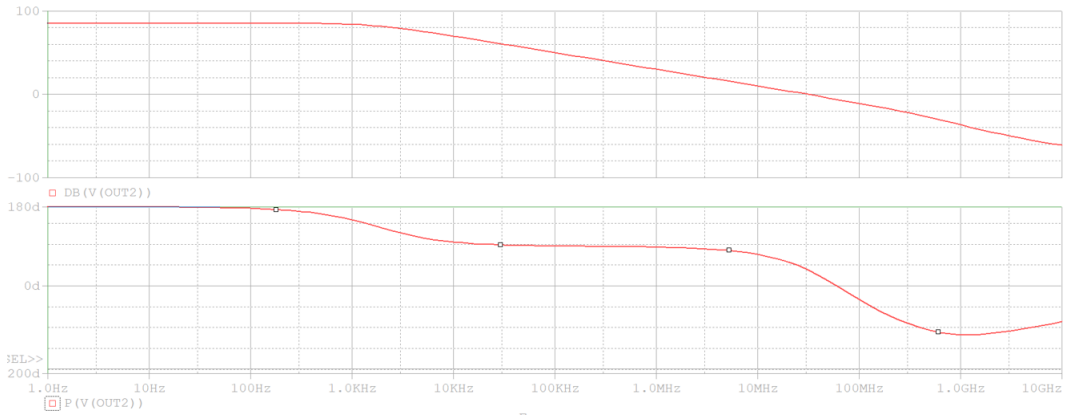


FIGURE 3.11: Open-loop simulation

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-184.820n		
	X Values	1.0544	1.0000	54.359m		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	P(V(OUT2))	179.966	179.968	-1.9189m		94.684	94.686	179.968	179.966	179.967
CURSOR 1,2	DB(V(OUT2))	85.282	85.282	-184.820n		0.000	0.000	85.282	85.282	85.282

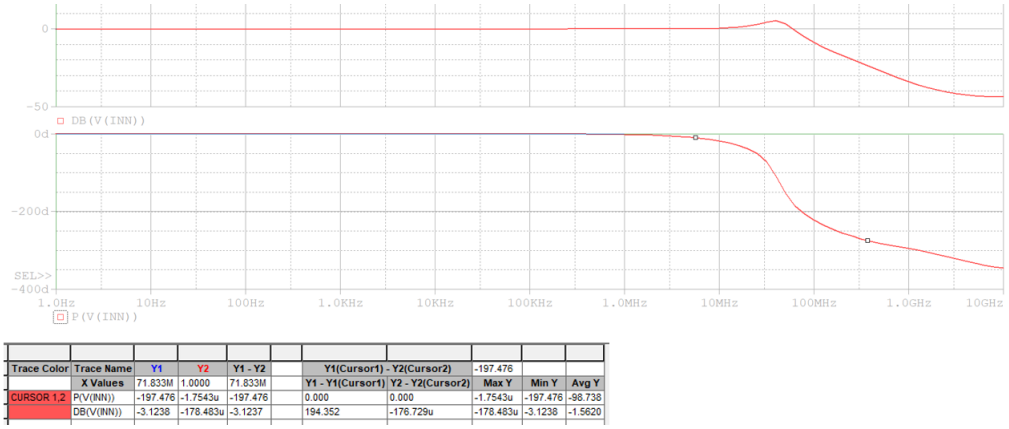
Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-3.0697		
	X Values	1.7901K	1.0000	1.7891K		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	P(V(OUT2))	134.795	179.968	-45.173		52.582	94.686	179.968	134.795	157.381
CURSOR 1,2	DB(V(OUT2))	82.212	85.282	-3.0697		0.000	0.000	85.282	82.212	83.747

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-84.779		
	X Values	29.992M	1.0000	29.992M		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	P(V(OUT2))	38.283	179.968	-141.684		37.781	94.686	179.968	38.283	109.126
CURSOR 1,2	DB(V(OUT2))	502.799m	85.282	-84.779		0.000	0.000	85.282	502.799m	42.892

FIGURE 3.12: Specific points in open-loop simulation

small phase margin of the circuit so we can predict an oscillation appearing in the step response graph, which has been proved in Figure 3.14. Moreover, the transient simulation is also shown in Figure 3.15. By applying a large signal, like what has been done in the folded cascode op-amp, the slew rate and the settling time (2%) can be measured, which respectively equal to 40.8V/us and 0.0439us.

Figure 2.26 is also employed to measure the ICMR of the Miller Op-amp. From the performance analysis graph, ICMR is approximately from 0.6V to 3V. Similarly, we can have the average value of the common-mode gain, which is about -5dB. The PSRR of the Miller Op-amp, on the other hand, is quite low, at only 4.4dB. Finally, the output swing is determined, which ranges between 0.15V to 3.13V. Table 3.20 summarizes the simulation results.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)	-197.476		
	X Values	71.833M	1.0000	71.833M		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	P(V(INN))	-197.476	-1.7543u	-197.476		0.000	0.000	-1.7543u	-197.476	-98.738
	DB(V(INN))	-3.1238	-178.483u	-3.1237		194.352	-176.729u	-178.483u	-3.1238	-1.5620

FIGURE 3.13: Closed-loop simulation

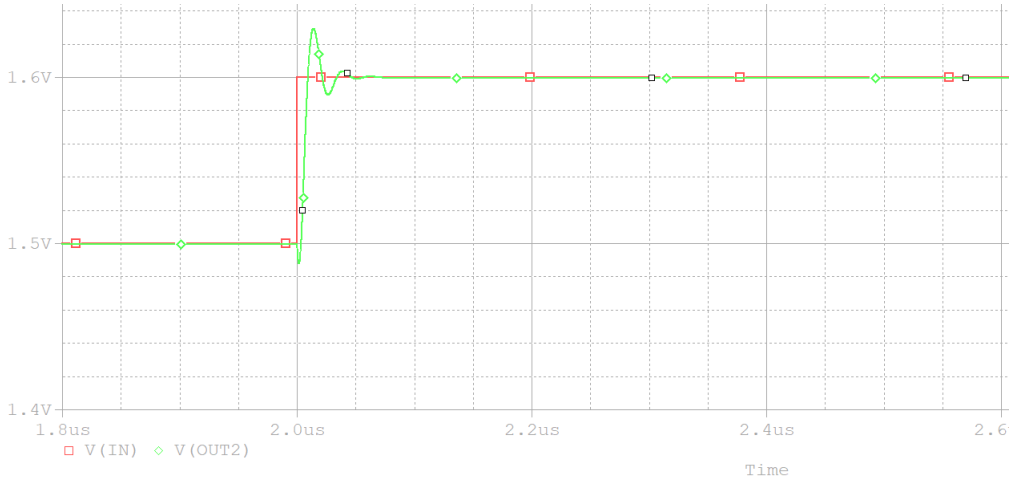


FIGURE 3.14: Step response

3.3.2 Miller Compensation With Voltage Buffer

Figure 3.21 illustrates the schematic of the voltage buffer. The compensation capacitor and the common drain stage in the series have been emphasized in the blue block, which can be compared to the block diagram 3.22. M10 serves as a current source which is copied from I_{bias}. All the same simulations are made and the simulation results are illustrated in the table 3.24. In addition, the bias current is shown in Figure 3.23, indicating that the circuit costs extra current, which is in agreement with the analysis before.

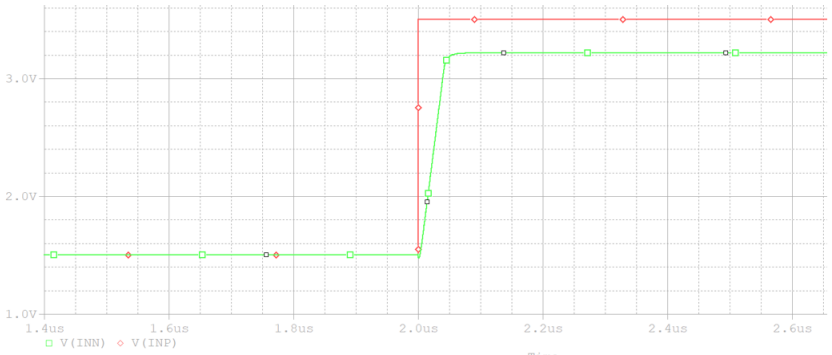


FIGURE 3.15: Transient simulation (SR)

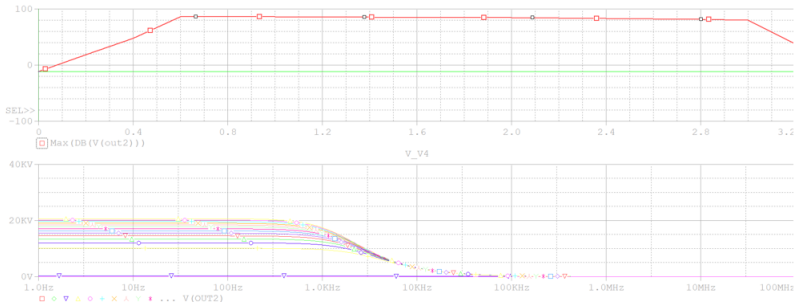


FIGURE 3.16: ICMR simulation

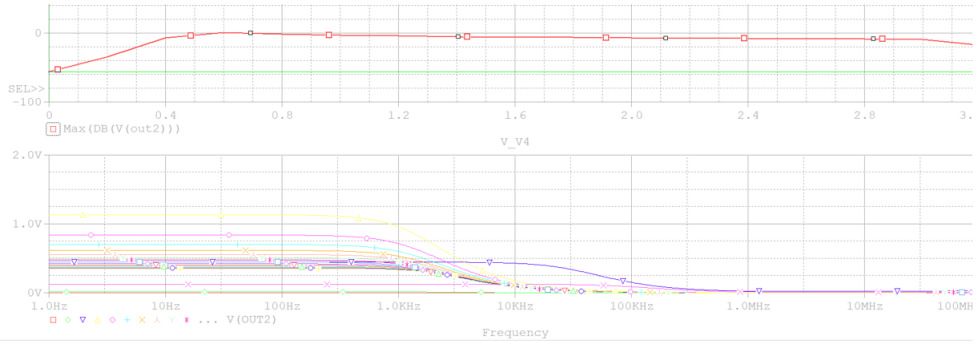
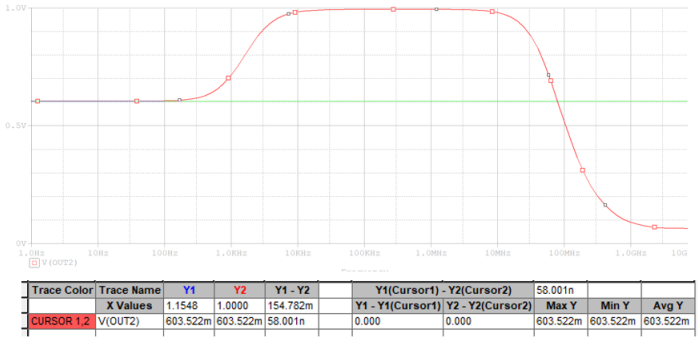
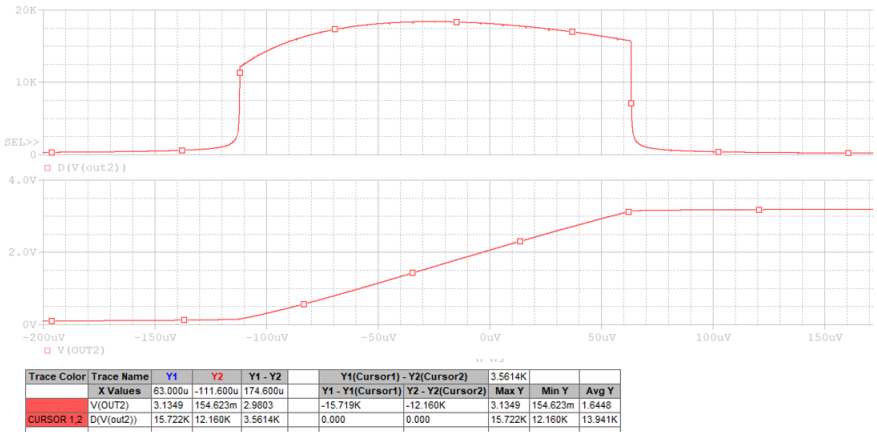


FIGURE 3.17: Common mode gain simulation



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		58.001n		
	X Values	1.1548	1.0000	154.782m		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(OUT2)	603.522m	603.522m	58.001n		0.000	0.000	603.522m	603.522m	603.522m

FIGURE 3.18: PSRR simulation



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		3.5614K		
	X Values	63.000u	-111.600u	174.600u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(OUT2)	3.1349	154.623m	2.9803		-15.719K	-12.160K	3.1349	154.623m	1.6448
CURSOR 1,2	D(V(out2))	15.722K	12.160K	3.5614K		0.000	0.000	15.722K	12.160K	13.941K

FIGURE 3.19: Output Swing Simulation: The lower graph shows the change of output voltage in terms of the input; The top graph shows the derivative of the maximum value of the lower graph

Open-loop gain (DB)	85.2
Phase margin (degree)	38
Cut-off frequency (MHz)	3.73
3 dB Bandwidth (KHz)	0.14
ICMR (V)	0.6 ~ 3
Output Swing (V)	0.15 ~ 3.13
CMRR (DB)	90.2
PSRR (DB)	4.4
S.R (V/us)	40.8
Settling time (us)	0.0439
Current Supply (uA)	100

FIGURE 3.20: Tables for Miller op-amp

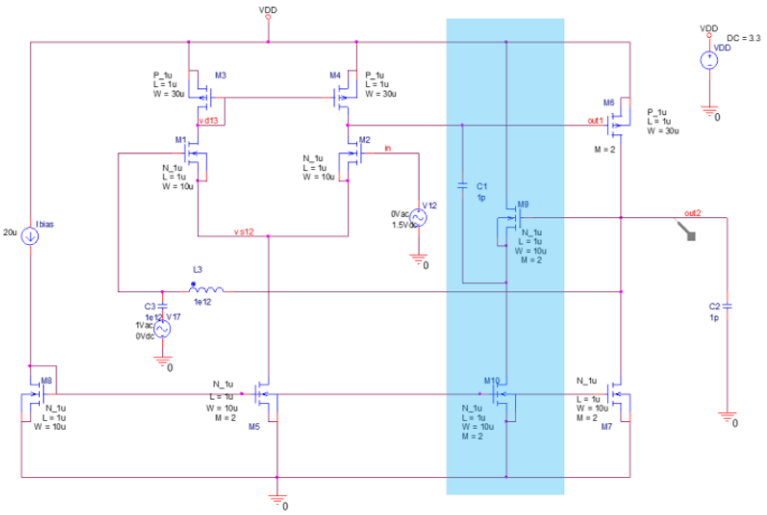


FIGURE 3.21: Second design improving the phase margin

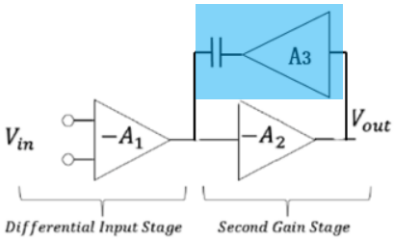


FIGURE 3.22: Block diagram

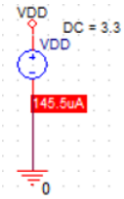


FIGURE 3.23: Power supply of the second Miller Op amp design

Open-loop gain (DB)	85.2
Phase margin (degree)	84.7
Cut-off frequency (MHz)	34.2
3 dB Bandwidth (KHz)	1.4
ICMR (V)	0.6 ~ 3
Output Swing (V)	0.18 ~ 3.15
CMRR (DB)	90.7
PSRR (DB)	4.4
S.R (V/us)	40.2
Settling time (us)	0.041
Current Supply (uA)	145.5

FIGURE 3.24: Tables for the second design

4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

This project was undertaken to investigate and assess the performance of two-stage operational amplifiers and folded cascode amplifiers. The principles implemented in the design were explained in detail. All parameters which indicate the circuit quality, including gain, cut-off frequency, phase margin, ICMR, CMRR, PSRR, output swing, slew rate, and settling time have also been simulated. Some of them are calculated theoretically with the corresponding equation, which turns out they are in line with the simulation results. The following conclusions regarding the three op-amps can be drawn from the present conclusion table 4.1.

- Due to the larger phase margin, Miller Op Amp with voltage buffer is generally better than the original Miller Op Amp except that it will cost more current.
- Compared to two designs of Miller Op-Amps, folded cascode op-amps have increased ICMR by two folded-down P-channel MOSFETs. Moreover, it has a better PSRR and CMRR.
- Miller Op Amp also has advantages over the folded cascode op-amp at the aspect of slew rate, settling time, and cut-off frequency.

Regarding the schematic of the circuit, it also has a simpler bias circuit and smaller size on a chip. Overall, folded cascode op-amps have a better performance on average than the other two op-amps. They are possibly one of the most suitable types of op-amps in 130nm CMOS technology. Nevertheless, to meet different requirements such as a higher slew rate, Miller Op Amps are preferred.

	Miller Op Amp	Miller Op Amp with voltage buffer	Folded cascade op amp
Open-loop gain (DB)	85.2	85.2	86
Phase margin (degree)	38	84.7	86
Cut-off frequency (MHz)	3.73	34.2	24.3
3 dB Bandwidth (KHz)	0.14	1.4	1.16
ICMR (V)	0.6 ~ 3	0.6 ~ 3	0.53 ~ 3.3
Output Swing (V)	0.15 ~ 3.13	0.18 ~ 3.15	0.3 ~ 2.85
CMRR (DB)	90.2	90.7	141
PSRR (DB)	4.4	4.4	69
S.R (V/us)	40.8	40.2	19.76
Settling time (us)	0.0439	0.041	0.0887
Current Supply (uA)	100	145.5	100

FIGURE 4.1: Conclusion table

4.2 Future Work

A natural progression of this work is to design the layout of the circuit to fulfill the industrial requirements. Moreover, the full temperature dependency of the transistors should be further investigated with the official fab models because the models used in this thesis are limited. Besides the temperature dependencies of the model parameters, the process and mismatch variations (Monte Carlo simulation) should be considered in future works. Last but not least, using more realistic transistor models would help establish a greater degree of accuracy on circuit performance analysis.

APPENDIX

A

APPENDIX—USED TRANSISTOR MODEL

```
.MODEL N_1u NMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7            VTO    = 0.3           DELTA  = 3.0
+ UO     = 650            ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6         VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0              NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
```

FIGURE A.1: NMOS PSpice model

```
.MODEL P_1u PMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7            VTO    = -0.4          DELTA  = 0.1
+ UO     = 250            ETA    = 0             THETA  = 0.1
+ KP     = 40E-6          VMAX   = 5E4           KAPPA  = 1
+ RSH    = 0              NFS    = 1E12          TPG    = -1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
```

FIGURE A.2: PMOS PSpice model

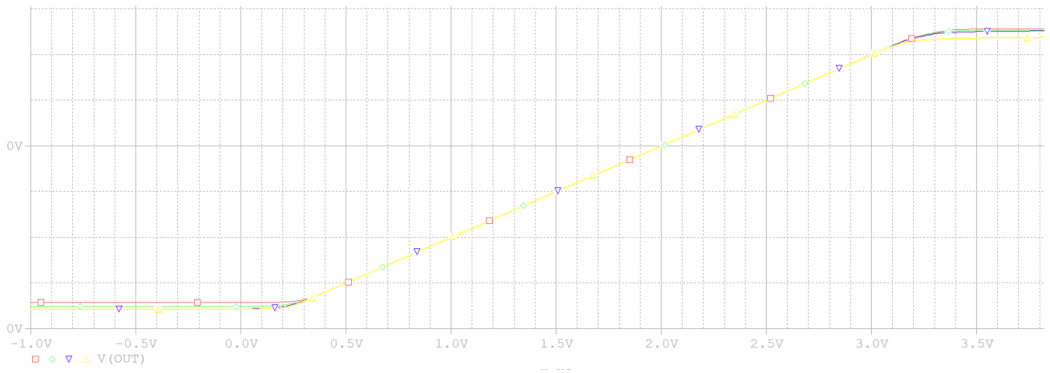


FIGURE A.3: Temperature simulation of folded cascode op amp

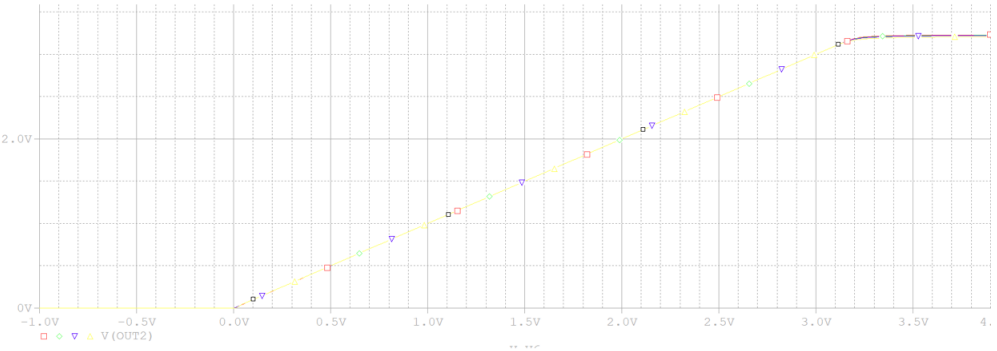


FIGURE A.4: Temperature simulation of Miller op amp

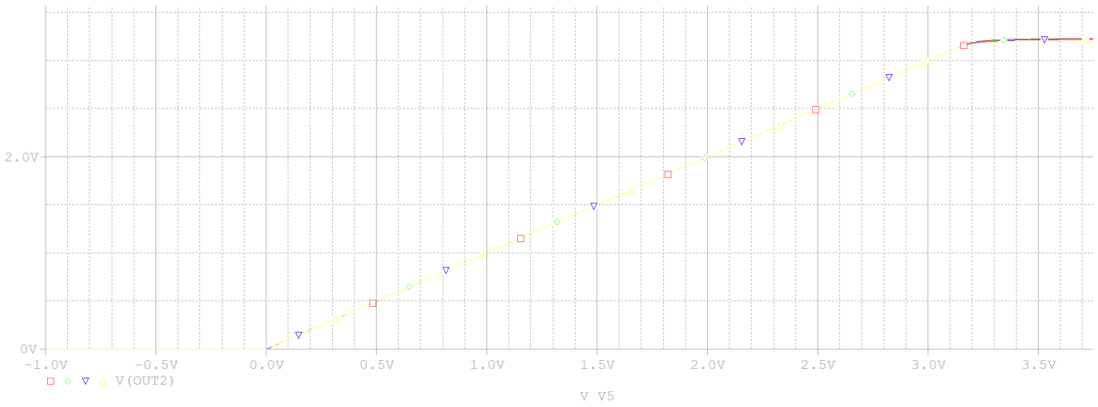


FIGURE A.5: Temperature simulation of Miller op amp with voltage buffer

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