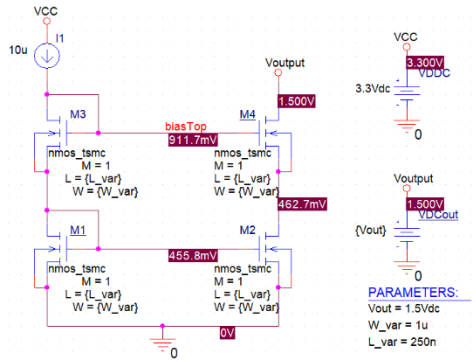
Prelab 3, Analog Integrated Circuits

Ole Jansen, Kaya Runge, Finn Rautenberg, 06.01.2023, Lübeck

1) Simple Cascode

1a) Circuit



1b) DC bias point simulation

NAME	M_M3	M_M1	M_M4	M_M2
MODEL	nmos_tsmc	nmos_tsmc	nmos_tsmc	nmos_tsmc
ID	1.00E-05	1.00E-05	1.00E-05	1.00E-05
VGS	4.56E-01	4.56E-01	4.49E-01	4.56E-01
VDS	4.56E-01	4.56E-01	1.04E+00	4.63E-01
VBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00
VTH	3.28E-01	3.28E-01	3.28E-01	3.28E-01
VDSAT	1.30E-01	1.30E-01	1.25E-01	1.30E-01
Lin0/Sat1	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
if	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
ir	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
TAU	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00
GM	1.07E-04	1.07E-04	1.13E-04	1.07E-04
GDS	1.64E-06	1.64E-06	1.11E-06	1.63E-06
GMB	9.34E-06	9.34E-06	9.88E-06	9.35E-06
CBD	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGSOV	6.05E-16	6.05E-16	6.05E-16	6.05E-16
CGDOV	6.05E-16	6.05E-16	6.05E-16	6.05E-16
CGBOV	2.50E-17	2.50E-17	2.50E-17	2.50E-17
CGS	9.85E-16	9.85E-16	9.85E-16	9.85E-16
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00

All FETs are in saturation due to $V_{GS} > V_{TH}$ and $V_{DS} > V_{DSAT} = V_{OV}$

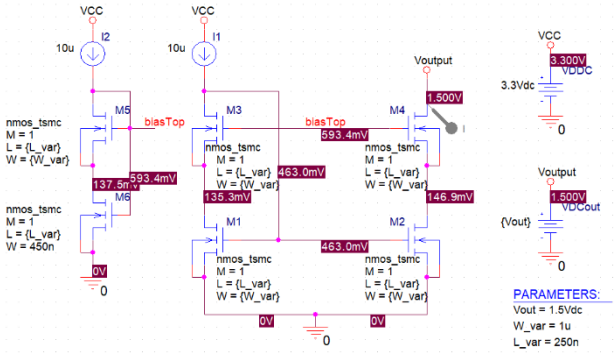
1c) Calculation

$$V_{biasTop} = 2 * V_{GS} = 2 * 456mV = 912mV$$

$$V_{D4,sat,min} \geq 2V_{GS} - V_{TH} = 2 * 456mV - 328mV = 584mV$$

2) Wide-swing Cascode

2a) Circuit



2b) DC bias point simulation

NAME	M_M1	M_M3	M_M2	M_M4	M_M5	NAME	M_M6
MODEL	nmos_tsmc	nmos_tsmc	nmos_tsmc	nmos_tsmc	nmos_tsmc	MODEL	nmos_tsmc
ID	1.00E-05	1.00E-05	1.00E-05	1.00E-05	1.00E-05	ID	1.00E-05
VGS	4.63E-01	4.58E-01	4.63E-01	4.46E-01	4.56E-01	VGS	5.93E-01
VDS	1.35E-01	3.28E-01	1.47E-01	1.35E+00	4.56E-01	VDS	1.38E-01
VBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	VBS	0.00E+00
VTH	3.28E-01	3.28E-01	3.28E-01	3.28E-01	3.28E-01	VTH	3.28E-01
VDSAT	1.35E-01	1.31E-01	1.35E-01	1.24E-01	1.30E-01	VDSAT	2.08E-01
Lin0/Sat1	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	Lin0/Sat1	-1.00E+00
if	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	if	-1.00E+00
ir	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	ir	-1.00E+00
TAU	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	-1.00E+00	TAU	-1.00E+00
GM	9.92E-05	1.05E-04	1.00E-04	1.15E-04	1.07E-04	GM	4.25E-05
GDS	4.19E-06	1.98E-06	3.81E-06	9.95E-07	1.64E-06	GDS	3.36E-05
GMB	8.69E-06	9.17E-06	8.76E-06	1.01E-05	9.34E-06	GMB	3.80E-06
CBD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	CBD	0.00E+00
CBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	CBS	0.00E+00
CGSOV	6.05E-16	6.05E-16	6.05E-16	6.05E-16	6.05E-16	CGSOV	2.64E-16
CGDOV	6.05E-16	6.05E-16	6.05E-16	6.05E-16	6.05E-16	CGDOV	2.64E-16
CGBOV	2.50E-17	2.50E-17	2.50E-17	2.50E-17	2.50E-17	CGBOV	2.50E-17
CGS	9.85E-16	9.85E-16	9.85E-16	9.85E-16	9.85E-16	CGS	3.35E-16
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	CGD	2.83E-16
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	CGB	0.00E+00

All FETs are in saturation due to $V_{GS} > V_{TH}$ and $V_{DS} > V_{DSAT} = V_{OV}$, except M6 which is tuned to result in $V_{BiasTop,min} = 593mV$

2c) Calculation

$$V_{BiasTop,min} \geq 2V_{OD} + V_{TH} = 2 * 124mV + 328mV = 576mV$$

$$V_{D4,sat,min} \geq 2V_{OD} = 2 * 124mV = 248mV$$

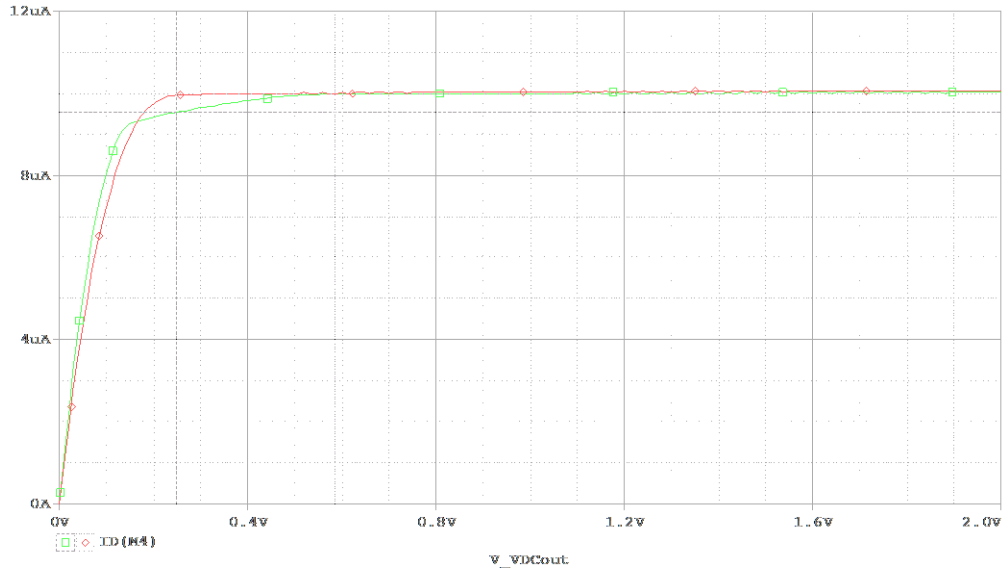


Figure 1: I_D4 in relation to V_D4 at DC Sweep (green: simple Cascode, red: wide-swing Cascode)

3) Comparison simple and wide-swing Cascode

Design	L	W	W_{M6}	V_{Bias}	$V_{BiasTop,min}$	$I_{D4,sat}$ simulation	$V_{D4,sat,min}$ theory
Simple	250 nm	1 µm	-	911 mV	912 mV	9,988 µA (@584 mV)	584 mV
Wide-swing	250 nm	1 µm	450 nm	593 mV	576 mV	9,959 µA (@284 mV)	284 mV

The wide-swing Cascode is able to operate at 284 mV less then the simple Cascode at 584 mV, which is a 300mV improvement. If the saturation voltage $V_{BiasTop}$= $V_{BiasTop,min}$ this difference should even increase. M6 has been modified to 450 nm, which is a none modulo 250 nm width, which is forbidden. The bias voltage is reached but M6 isn't in saturation which may cause changes at other environmental parameters.