① 16 bit ALFA e BETA

- 1 bit x SEGNO
- e bit ESPO ecc 2^{e-1} → ALFA e = 6 m = 9 / BETA e = 9 m = 6
- m bit MANT

D37C ALFA IN BETA

D 3 7 C

1101 0011 0111 1100

↳

101001 -

100000 =

001001 = 9

- SEGNO: 1
- ESPO: 100001001
- MANT: 101111

} 1100001001101111

1001 +

100000000 =

100001001

② $E_A = 2^2 = 4$

③ C1D2 BETA IN ALFA

④ $E_A = 0$

C 1 D 2

1100 0001 1101 0010

- SEGNO: 1
- ESPO: 100111
- MANT: 010010000

100000111 -

100000000 =

000000111 = 7

000000111 +

100000 =

100111

⑤ ERR CORR TOTERR = $(h-1)/2 \rightarrow 2-1/2 = 0$

$$\left[2\left[\left[\begin{matrix}0001\\0100\end{matrix}\right]_2 \left[\begin{matrix}1000\\0010\end{matrix}\right]_2\right]_2\right]_2$$

⑥ 1101 NON POSSO NE RILEVARE NE CORREGGERE

⑦ 1 bit

⑧ FALSO ⑨ B ⑩ B

⑪

A	B	C	U1: A AND B	U2: NOT B OR C	U1 AND U2
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	1	1	1

A AND B AND C

⑫

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(NOT A AND NOT B AND NOT C) OR (A AND B AND C)

$(\overline{A} \cdot \overline{B} \cdot \overline{C}) + (A \cdot B \cdot C)$

⑬ (NOT A AND B) OR A

ESERCIZI IN VIRGOLA MOBILE

① 16 bit ALFA e BETA

- 1 bit x segno
- e per esponente ecc 2^{e-1}
- m bit mantissa

	ALFA	BETA
e	e = 6	e = 9
m	m = 9	m = 6

D37C ALFA im BETA

1101 0011 0111 1100

- SEGNO: 1
- ESPO: 10000100 1
- MANT: 101111

} 1100001001101111

101001 -
100000 =
00100 1 +
10000000 0 =
10000100 1

② $E_A = 6$

③ C1D2 BETA IN ALFA

C	1	D	2
1100	0001	1101	0010

- SEGNO: 1
- ESP: 100000111 − 100000000 = 000000111 + 100000 = 000100111 } 100111
- MANT: 0100010000

} 1100111010010000

④ EA = 0

⑤ $2\left[\begin{matrix}0001\\0100\\1000\\0010\end{matrix}\right]_2$ $h=2$ $m.e=(h-1)/2=0$

⑥ 1101 $h=2$ $m.e=(h-1)/2=0$

b, la sequenza può essere rilevata ma non corretta

⑦ 1

⑧ VERO

⑨ SONO REALIZZATI CON DEI TRANSISTOR

⑩ b

⑪

A	B	C	U1: A AND B	U2: $\bar{B}$ OR C	U1 AND U2
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	1	1	1

A AND B AND C

(12)

A	B	C	y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(NOT A AND NOT B AND NOT C) OR (A AND B AND C)

(13) (A XOR B) (NOT A AND B) OR A

0 1

NOT (A XOR B)

1 0 = 1

U1

A	B	C	(NOT A AND B)	U1 OR A
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

A	B	C	A XOR B	$\bar{y}$
0	0	0	0	1
0	0	1	0	1 ←
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1 ←
1	1	1	0	1

A	B	C	A XOR B
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(16) CACHE MAPP DIRETTA 8 MB $\rightarrow 2^{20}$ bit $\cdot 2^3 = 2^{23}$

BLOCCHI 32 B $\rightarrow 2^5$ bit

SPAZIO PROC 150 KB

DIM MINIMA COLL < 128 BLOCCHI

INDIR DIM = $33 \cdot 2^{11} = 33 \cdot 2^{10} \cdot 2 = 66$ KB

TAG	LINE	32 BLOCCHI
7	11	5

SLOT DIM = 33 B

V	TAG	32 B
1b	76	32 B

(12) TAG = 6
LINE = 12

V	TAG	32 B
1b	66	32 B

DIM :
32+ ≈ 86 ≈ 33 B

DIM INDIR: $33 \cdot 2^{12} = 33 \cdot 2 \cdot 2 \cdot 2^{10} = 132$ KB