

① 1A3 CP2 7A1 ECC 2"

1A3

0001 | 1010 0011

- SEGNO: 0, 1 bit
- ESPO: 7 → 0111, 4 bit →  $2^{m-1}$  → 5 bit
- MANT: 8 bit

X:Y:Z

1:5:8

7A1

7 A 1

0111 1010 0001

1000 0101 1111

- SEGNO: 1, 1 bit
- ESPO: 5, 5 bit
- MANT: 6 bit

④  $E_A = 2^0 + 2^1 = 3$

⑤ CISC IO STATI PIPELINE

CLOCK 2 GHz

MULTITHREADING

$T = 1000 / 2000 = 0,5 \text{ msec}$

$1000 / T = 2000 \text{ MIPS}$

⑥

TEXEC sistema ista

$m \times T = 0,5 \times 10 = 5 \text{ msec}$

$TEXEC = 5 \cdot 2 + 0,5 \cdot 7$

⑦  $1000 / T = 2000 \text{ MIPS}$

⑪

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(NOT(A) AND NOT(B) AND C) OR (A AND D AND NOT(C)) OR (A AND B AND C)

$(\bar{A} \cdot \bar{B} \cdot C) + (A \cdot B \cdot \bar{C}) + (A \cdot B \cdot C)$

⑬

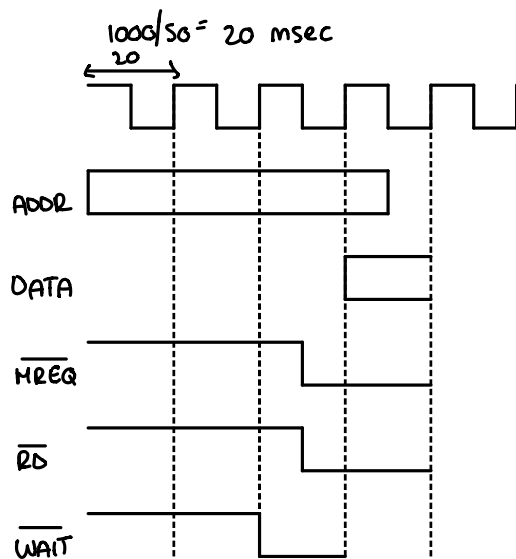
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

X <sub>1</sub>	X <sub>2</sub>	U <sub>1</sub>
0	0	0
0	1	1
1	0	1
1	1	0

X <sub>0</sub>	U <sub>1</sub>	U <sub>2</sub>
0	0	0
0	1	1
1	1	0
1	0	1

TESTA SE C'E' UN SOLO 1

- 14) BUS SINCRONO 50 MHz LINEE SEPARATE  
TRISP 60 msec INDIR STABILI



14) 60 msec

15) 70 msec

16) 80 msec

17) FALSO

1) 1A3 CP2 7A1 ECC 2"

1 A 3  
0001 1010 0011

7A1  
0111 1010 0001 -  
1000 0000 0000 =  
1111 1010 0001

0000 0101 1110 + 1 = 0000 0101 1111

0001 1010 0011

- 1 bit SEGNO  $2^{n-1}$
- $8 = 2^3 = 1000 = 4 \text{ bit} + 1 = 5 \text{ bit espo}$
- 8 bit mantissa

- 1 bit x SEGNO
- $6 = 0110 \rightarrow 5 \text{ bit} \times \text{SEGNO}$
- 6 bit mantissa

2) A 1m ALFA

3) B 1m ALFA

4)  $E_A = 2^0 + 2^1 = 3$

1 A 3  
0001 1010 0011

- SEGNO: 0
- ESPO
- $8 = 01000$
- MANT: 1010 0011

1111 1010 0001

- 1 bit x SEGNO
- $10 = 0110 = 00110$
- 11101000

PIPELINE 10 STADI  $\mu = 2 \text{ GHz}$

5)  $T = 1000/2000 = 0,5 \text{ msec}$   $F(\text{MIPS}) = 2000 \text{ MIPS}$

6) TEXEC 5 istn e 4 istn  $m \times T = 5 \text{ msec}$

$$T_{EXEC} = 5 + 0,5 \cdot 8 = 9 \text{ msec}$$

⑦ F(MIPS) com 5 stadi

2000 MIPS

⑧ FALSE

⑨ C

⑩ LRU  $\rightarrow$  C

⑪

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(NOT A AND NOT B AND C) OR (A AND B AND NOT C) OR (A AND B AND C)

⑫ (NOT A AND B AND NOT C) = 0

$\begin{matrix} 0 & & 1 & & 0 \end{matrix}$

• (NOT A AND NOT B AND C) OR (A AND B) | B

$\begin{matrix} 0 & & 0 & & 1 & & 1 & & 1 \\ & & 0 & & & & 1 & & \\ & & & & & & & & 1 \end{matrix}$

⑬

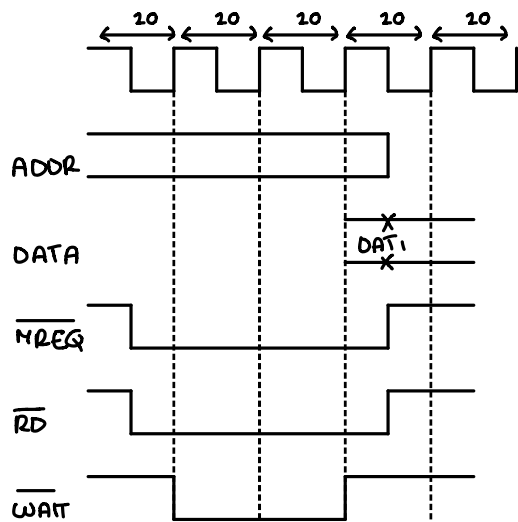
$x_2$	$x_1$	$x_0$	$\overset{v_1}{x_2 \text{ XOR } x_1}$	$\overset{v_2}{v_1 \text{ XOR } x_1}$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1

⑬

$\overset{v_1}{A}$	$\overset{v_1}{B}$	$\overset{v_1}{C}$	$\overset{v_1}{\bar{A}}$	$\overset{v_1}{\bar{B}}$	$\overset{v_1}{\bar{C}}$	$(\bar{A} \text{ AND } \bar{B})$	$\overset{v_2}{v_1 \text{ AND } C}$	$\overset{v_3}{A \text{ AND } B}$	$v_2 \text{ OR } v_3$
0	0	0	1	1	1	1	0	0	0
0	0	1	1	1	0	1	1	0	1
0	1	0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0
1	0	1	0	1	0	0	0	0	0
1	1	0	0	0	1	0	0	1	1
1	1	1	0	0	0	0	0	1	1

16) BUS SINCRONO 50 MHz TRISP 60 msec da IND STABILI

$$1000/50 = 20 \text{ msec}$$



DATA { da lettura inizia sempre sul fronte di discesa successivo

MREQ e RD partono sul fronte di

14) 60 msec

15) 70 msec

16) 80 msec

17) FALSO