# Sequential Logic

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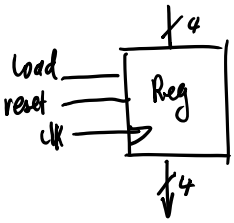
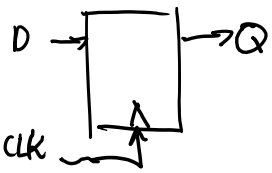
**Sequential Blocks**

An example is a flip flop: The following is a 4-bit register




Positive D-Flip-Flop:

```
1   module DFF(D, CLK, Q);
2       input D, CLK;
3       output reg Q;
4
5       always @(posedge CLK)
6           Q <= D;
7   endmodule
```




In SystemVeriolog, the **always** keyword can be replaced with **always_ff**, which is safer.

## Blocking vs. Non-blocking Assignments

**Blocking**

X = Y;

This will cause the assignment to happen immediately. So any succeeding assignments will use the new values

**Non blocking**

X <= Y;

This just says that X takes the value of Y at the end of the clock cycle. Thus any succeeding assignments will use the values at the beginning of the clock cycle. Thus ordering doesn't matter