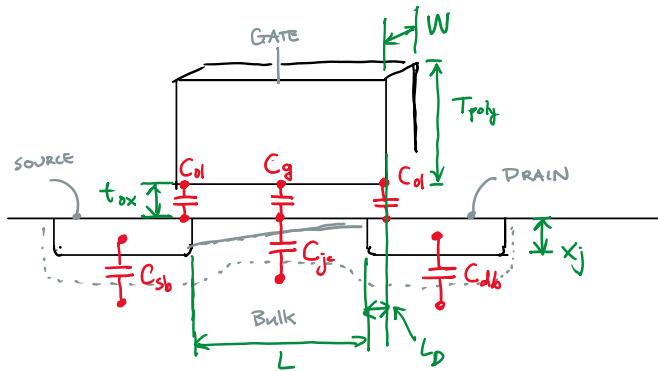


# MOS Capacitances

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Typical MOS:



Capacitances:

$C_g$  - Gate capacitance

$C_{jb}$  - Junction capacitance

$C_{sb}, C_{db}$  - Source/Drain to Bulk capacitance

$C_{ov}$  - Overlap & Fringe Parasitic capacitances

Measurements:

$W$  - Device width

$t_{poly}$  - Gate polyoxide layer thickness

$t_{ox}$  - Thickness between gate & diffusion

$L$  - Device length

$L_D$  - Gate & source/drain overlapping length

$x_j$  - Thickness of sidewall

## Gate Capacitances

Simple Model:  $C_g = C_{ox} \cdot WL$

By regions of operation:

$$C_g = C_{gb} + C_{gs} + C_{gd}$$

(TOTAL) (to BULK) (to SOURCE) (to DRAIN)

$V_{gs} \leq V_T$  - CUTOFF:  $C_{ox} \cdot WL + 0 + 0$

$V_T < V_{gs} \leq V_{gs} + V_T$  - SATURATION:  $0 + \frac{2}{3}C_{ox} \cdot WL + 0$  ← Pinched off

$V_{gs} > V_{gs} + V_T$  - LINEAR:  $0 + \frac{1}{2}C_{ox} \cdot WL + \frac{1}{2}C_{ox} \cdot WL$