MOS Basics

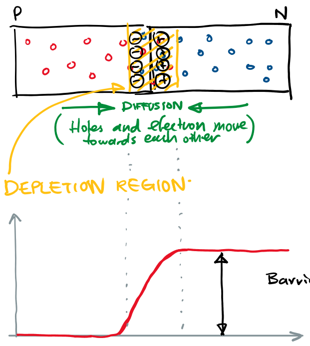
October 3, 2019 18:56

Devices are made of N-type and P-type semi-conductors

Heavily doped with acceptor atoms

Heavily doped with donor atoms

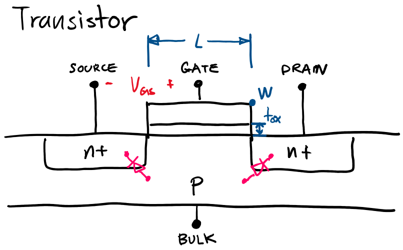
PN JUNCTION:



Barrier Potential / Contact

V_0

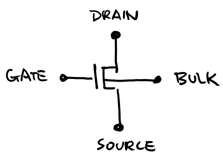
MOS Transistor



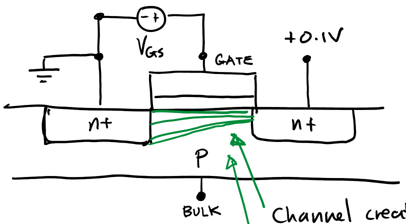
← this is like two diodes back-to-back

so external stimulous is required for conduction

This ↑ configuration is N-P-N (NMOS) and is represented on an schematic as:



We need to apply voltage to the gate to create a channel for electrons to travel

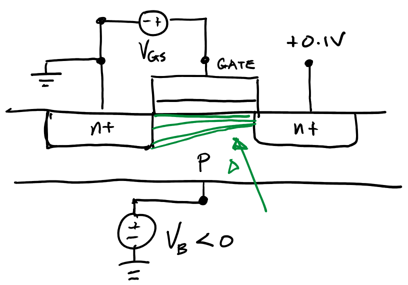


Channel created when $V_{GS} \geq V_{TH}$

THRESHOLD VOLTAGE

Channel gets larger as we increase V_{GS}

We can change threshold voltage by applying negative voltage to BULK



$$V_{T0} = V_{T0} + \gamma\left(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_F|}\right)$$

Body-effect coefficient

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_A}$$

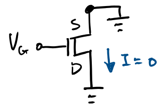
Current Calculation

Recall definition of current: charge moving over time

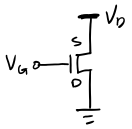
Charge is a function of where in the depletion region (y) we're at.

Recall definition of current: <u>charge moving over time</u>

① When $V_{GS} > V_{TH}$: channel formed, but no current



② when $V_{DS} > 0$: carrier flows from $S \rightarrow D$



Charge is a function of where in the depletion region (y) we're at.

$$\underbrace{Q_n(y)}_{\text{charge / unit area}} = C_{ox} \cdot (V_{GS} - V(y) - V_T) \qquad [C/m^2]$$

$$\underbrace{Q_d}_{\text{charge / length along direction of current}} = \underbrace{W}_{\text{width (design parameter)}} \cdot Q_n(y) \qquad [C/m]$$

Using def. of current: $I = Q_d \cdot v$ $\qquad [C/s]$

speed: $v = \mu E$

field: $E = \frac{dV(y)}{dy}$

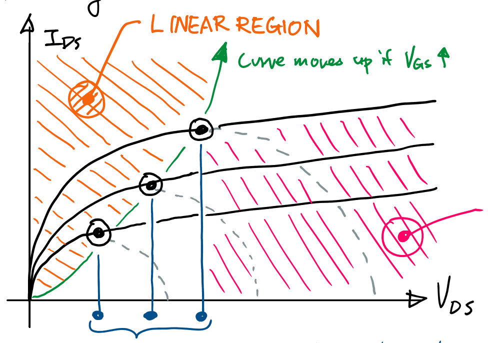
combining all: $I_{DS} = W \cdot C_{ox} \cdot (V_{GS} - V(y) - V_T) \cdot \mu_n \cdot \frac{dV(y)}{dy}$

M A G I C

I_{DS} has quadratic characteristics with respect to V_{DS}

$$I_{DS} = \underbrace{\mu_n \underbrace{\frac{\varepsilon_{ox}}{t_{ox}}}_{C_{ox}}}_{k'} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Plotting I_{DS} vs. V_{DS}



I_{DS} at peak when $V_{DS} = V_{GS} - V_{TH}$

I_{DS} has linear relationship to V_{GS}

$$I_{DS} = \frac{k}{2} (V_{GS} - V_T)^2 \cdot (1 - \lambda V_{DS})$$

I_{DS} doesn't fall back down when $V_{DS} > V_{GS} - V_{TH}$
Because we've reached <u>PINCH-OFF</u>

So MOS is SATURATED. and I_{DS} is mostly flat w.r.t V_{DS}
(which makes a good current source)