JAKE PETERSON

Los Angeles, California |fsharp4.github.io | 612-468-0597 | jacobape@usc.edu | linkedin.com/in/fsharp4

OBJECTIVE

Apply prior industry experience, hone fresh VLSI skills gained at USC, and leverage my enthusiasm for creativity in engineering towards exciting Hardware Engineering opportunities through and outside the Viterbi network.

EDUCATION

University of Southern California — Los Angeles, California
Master of Science, Electrical Engineering (VLSI Design) — August 2024-May 2026

- Coursework in Digital MOS (EE 477, EE 577A), Algorithms (CSCI 570), and Computer Systems Organization (EE 457) (CGPA: 4.00/4.00)

McGill University — Montreal, Quebec
Bachelor of Engineering, Honours Electrical — September 2018-December 2022

- Coursework specialization in Computer Architecture, Microprocessors, and Digital Signal Processing (CGPA: 3.69/4.00)

ACADEMIC PROJECTS

Automated SRAM Design — University of Southern California
VLSI System Design (EE 577A) — March 2025-April 2025

- Programmed SKILL scripts for variable-size SRAM circuits with automatic placement of cell banks and peripherals in layout using GPDK045
- Performed functional verification and timing closure for a 128-Bit SRAM circuit operating at 1 GT/s

Systolic Array Matrix Multiplication — University of Southern California
MOS VLSI Design (EE 477) — September 2024-December 2024

- Leading a 3-person Systolic Array design project to implement 4x4 INT8 matrix multiplication, coordinating division of work and integration
- Designing master-slave D flip flops, utilizing full custom layout techniques, crosstalk minimization, and transmission gate logic to reduce area and increase Multiply-Accumulate (MAC) performance

MIPS CPU Development — University of Southern California
Computer Systems Organization (EE 457) — September 2024-November 2024

- Constructed proof-of-concept pipelined MIPS CPUs using Questa and Verilog in tandem with another Viterbi M.S. student
- Customized TCL test benches for design validation on comprehensive sets of test cases for each supported instruction

A Triangular Lattice Framework for Massive MIMO Pilot Decontamination Schemes — McGill University
Statistical Signal Processing Lab | IEEE VTC 2024 Fall — September 2022-October 2024

- Published a novel method for reducing Pilot Contamination (inter-cell interference during channel estimation) in large cellular MIMO networks with dozens of cells and hundreds of users. (Tools: Python, MATLAB, Gurobi)

EXPERIENCE

Emerson Electric Company — Shakopee, MN
Electrical Design Engineer — April 2023-August 2024

- Conducted component substitutions, design reviews, and I.S. analyses on terminal blocks for high-volume pressure & temperature transmitter products
- Designed test fixtures and other improvements using Cadence Allegro System Capture & PCB Layout
- Developed efficient multiprocessing Python frameworks to enable advanced simultaneous test automation programs (HART, IVI-VISA)

ACTIVITIES

Music — Minneapolis, MN
Piano accompanist, soloist, and production band member — February 2004-Present

- 20 years of experience, classically trained (with 4 years jazz experience leading ensembles of 4-8)
- Auditioned for placement in concert ensembles with the McGill Classical Musicians' Club (2022), performing in two piano duets

Language Learning (French, Mandarin)
Lifelong Student — July 2019-Present

- Received a grant from McGill International Student Services to take immersive French Language courses at the University of Quebec at Chicoutimi; passed with proficiency equivalent to the ECRL A2 level

Student Accessibility & Achievement — McGill University
Volunteer Student Notes-Taker — September 2019-April 2022

- Crafted course lecture notes for nine university courses over six semesters for a student accessibility program at McGill