JAKE PETERSON

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OBJECTIVE

Pursue VLSI and Electrical Engineering Internship and Job opportunities through and outside the USC network. Apply prior industry experience and communication skillsets towards exciting ventures.

EDUCATION

University of Southern California — Los Angeles, California
Master of Science, Electrical Engineering (VLSI Design) — August 2024-May 2026

McGill University — Montreal, Quebec
Bachelor of Engineering, Honours Electrical — September 2018-December 2022

- Coursework specialization in Computer Architecture, Microprocessors, and Digital Signal Processing

ACADEMIC PROJECTS

MIPS ALU Development — University of Southern California
Computer Systems Organization (EE 457) — September 2024-December 2024

- Constructed an ALU for future inclusion in a pipelined MIPS CPU project using Questa and Verilog
- Constructed test benches for design validation on comprehensive sets of test cases for each supported instruction

A Triangular Lattice Framework for Massive MIMO Pilot Decontamination Schemes — McGill University
Statistical Signal Processing Lab | IEEE VTC 2024 Fall — September 2022-October 2024

- Published a novel method for reducing Pilot Contamination (inter-cell interference during channel estimation) in large cellular MIMO networks with dozens of cells and hundreds of users

Full Custom ASIC Labs - RCA Design — University of Southern California
MOS VLSI Design (EE 477) — September 2024-October 2024

- Created a full set of CMOS logic gates (transistor schematics, physical layout) using Cadence Virtuoso
- Verified designs against DRC/LVS rulesets and performed post-layout simulations (including parasitic extraction) for functional verification
- Constructed and verified a 4-bit Ripple Carry Adder using optimized Full Adders from this set of CMOS logic gates; work will be reused in larger projects as semester continues

Biclustering Methodology & Automating Dendrogram Cuts — McGill University
Undergraduate Thesis | Honor's Thesis Poster Session — January 2022-December 2022

- Devised techniques (based on the Bayesian Information Criterion) to automatically determine a desired # of clusters in datasets with several hidden clusters and thousands of data points

EXPERIENCE

Emerson Electric Company — Shakopee, MN
Electrical Design Engineer — April 2023-August 2024

- Conducted component substitutions, design reviews, and I.S. analyses on terminal blocks for high-volume pressure & temperature transmitter products
- Developed efficient multiprocessing Python frameworks to enable advanced test automations (HART, IVI-VISA)

ACTIVITIES

Pianist — February 2004-Present

- 20 years of experience, classically trained (with a sidequest in small combo jazz)
- Auditioned for placement in concert ensembles with the McGill Classical Musicians' Club (2022), performing in two piano duets

Volunteer Course Note-taker — September 2019-April 2022

- Crafted course lecture notes for nine university courses over six semesters for a student accessibility program at McGill

Language Learning (French, Chinese) — July 2019-Present

- Received a grant from McGill International Student Services to take immersive French Language courses at the University of Quebec at Chicoutimi; passed with proficiency equivalent to the ECRL A2 level (Current Duolingo streak: 140 days)