A novel methodology for robustness analysis of QCA circuits

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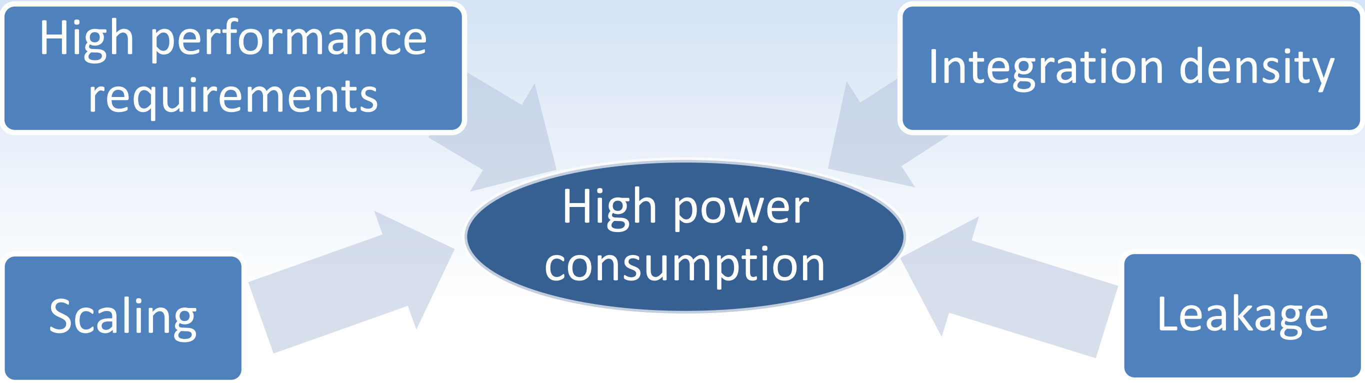
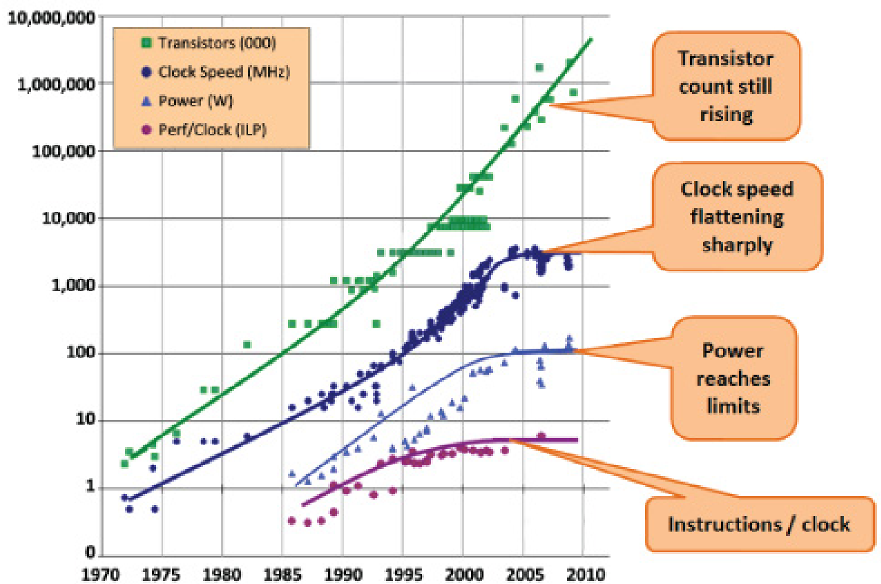
Agenda

- Motivation
- Background
- Methodology
- Simulations and results
- Conclusions

Motivation - CMOS Limits about to be reached





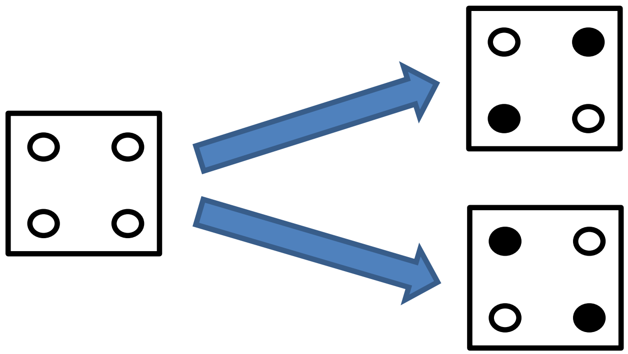
- Nano technologies as QCA have been emerging as possible CMOS successors.

Source: Intel, 2005 (Last updated August 2009)

Background – Quantum-dot Cellular Automata (QCA)

- QCA: A new computation paradigm.

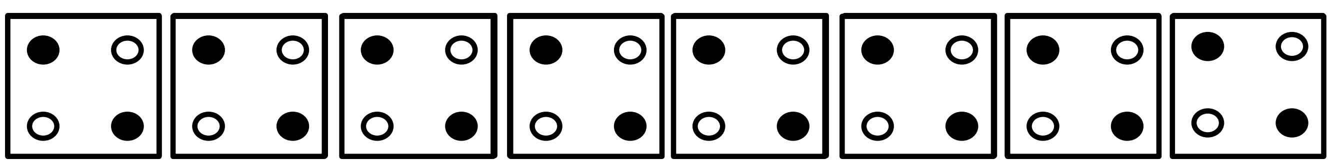
QCA cell (basic unit)



Polarization +1
Logic state 1

Polarization -1
Logic state 0

QCA wire



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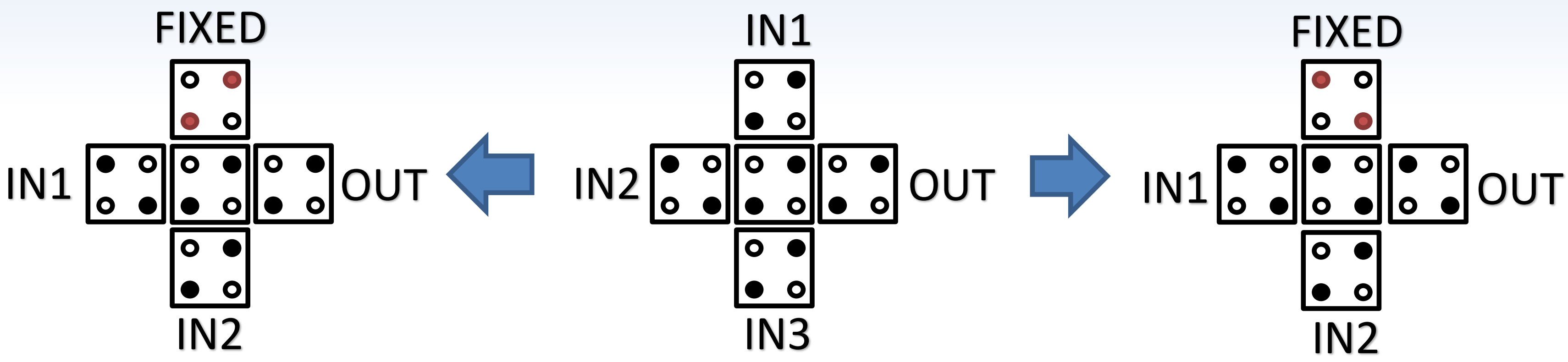
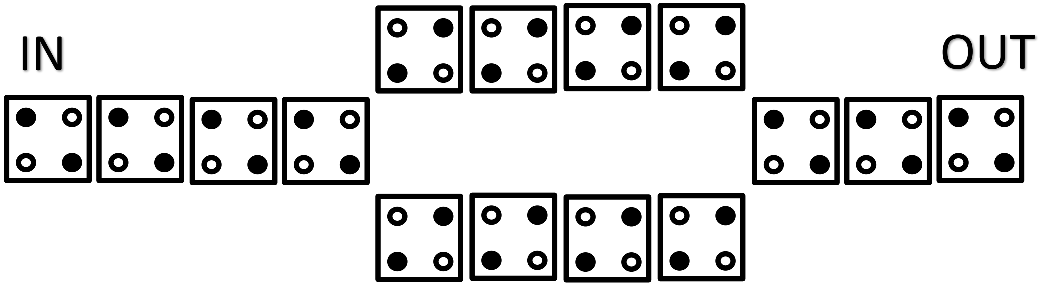
Background – Quantum-dot Cellular Automata (QCA)

OR | Majority gate | AND



Inverter



- Any logic can be created.
- More complex circuits feasible.

Background – Quantum-dot Cellular Automata (QCA)

QCA Pros

- Very high theoretical speeds achieved (within THz range);
- Low power consumption (information is transported with no electric current flow);
- Small dimensions (a molecular QCA cell should be 2x2 nm).

QCA Cons

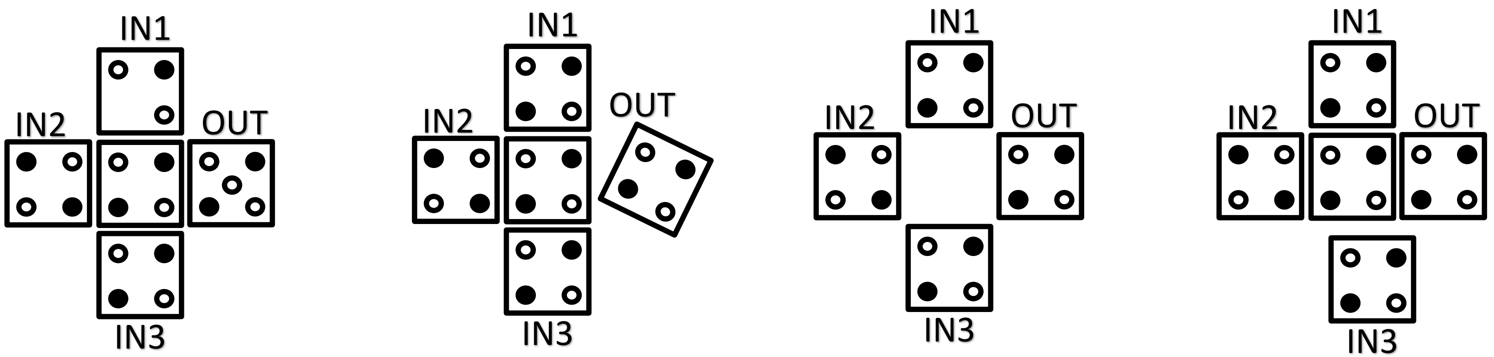
- Extremely difficult physical implementation.

Background – Defects and Errors in QCA circuits

- Defects: flaws of the cells of a circuit.
- Fabrication process issues: Dimensions Susceptible to Variability
- Affect directly the interaction between cells.

QCA Defects Modeling

Dopant Dislocation Vacancy Interstitial



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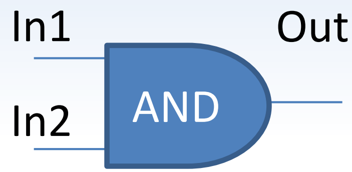
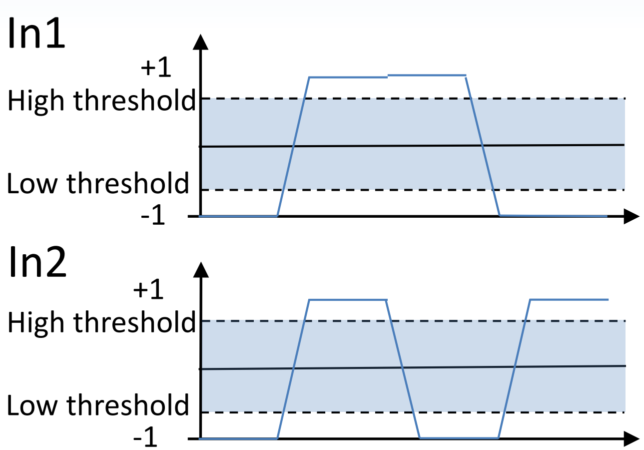
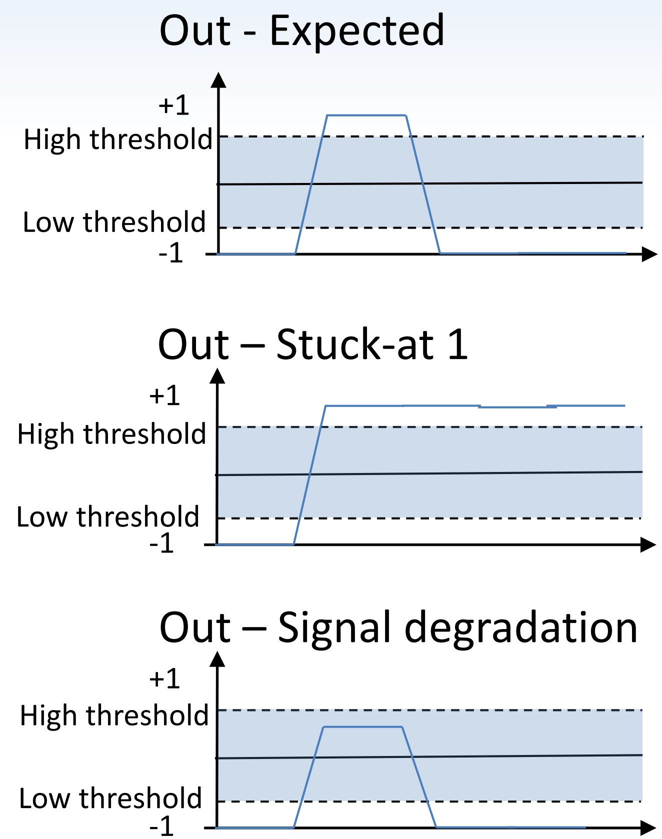
Background – Defects and Errors in QCA circuits

- Errors: unexpected deviations in the behavior of a system.

Example







- Likely to occur due to defects.
- Major consequence: Reliability decreased.

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Methodology – Fault Simulation Flow

A new methodology for error exploration in QCA circuits which aims to be:

Extensive

Four classes of defects + Three probability models

Flexible

Parameter-based approach → Operation under different conditions can be verified;

Innovative

Easy to interpret and visualize the results

→ Error-free simulations calculation (%)

→ Heat map

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Methodology – Fault Simulation Flow

Cycle repeat for all iterations

After all iterations

Initial procedures

- Circuit selection
- Parameters choice

Intermediate procedures

- Error-free reference simulation
- Defect insertion
- Fault simulation
- Comparison (Error-free x defective)

Final procedures

- Result analysis
- Error-free simulations percent calculation
- Design heat map

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Methodology – Fault Simulation Flow

Parameters list

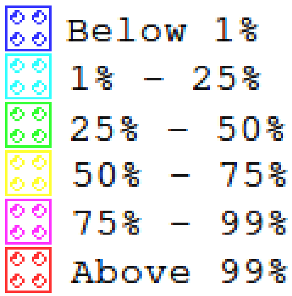
- Sample interval;
- HIGH/LOW thresholds;
- Defect classes (As defect modeling previously exposed);
- Number of iterations;
- Probability model
  - **Sequential:** P=1 for each cell of the design at sequential moments
  - **Assignable:** Any value between 0 and 1 may be assigned as defect probability for each design cell
  - **Uniform:** P=1/(Total of cells) for each cell of the design

Methodology – Heat map

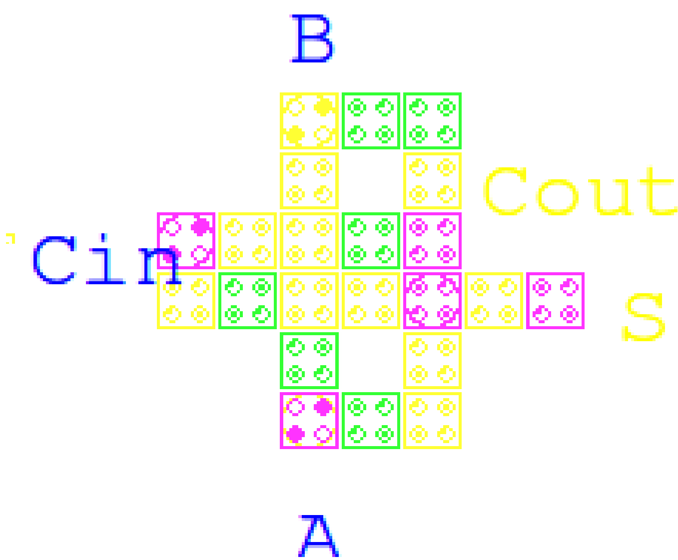
- Map the defective cells leading the outputs to an error.

A visual resource for results analysis

Colors used



Example



- Given a error event, these cells have _________ of probability to be defective.

Methodology – Pros and Cons

Methodology Pros

- Extensive defect modeling applied;
- Allows flexibility for defects insertion by means of probability models;
- Parameters are totally user-set;
- Presents the results by a heat map of the circuit;
- Provides the error-free simulations percent along all iterations.

Methodology Cons

- Simulation-based: May be a computational costly approach depending on the circuit size/ complexity.

Simulations and results

Error-Free Simulations (%)

	INVERTER		3-INPUT MAJORITY		FULL ADDER	
	INV1	INV2	MJ1	MJ2	FA1	FA2
Vacancy	74.6	**86.1**	**60.6**	30.3	2.8	**16.2**
Interstit.	97.4	**99.9**	**94.3**	87.9	54.9	**76.0**
Dopant	83.7	**88.6**	**75.8**	31.1	3.7	**26.2**
Dislocat.	88.6	**93.9**	**78.5**	67.2	25.9	**51.0**

Probability model = Assignable;

Number of iterations = 1.000;

Probability value for individual defect classes = 5%;

Sample Interval = 10% and LOW/HIGH Threshold = 80%.

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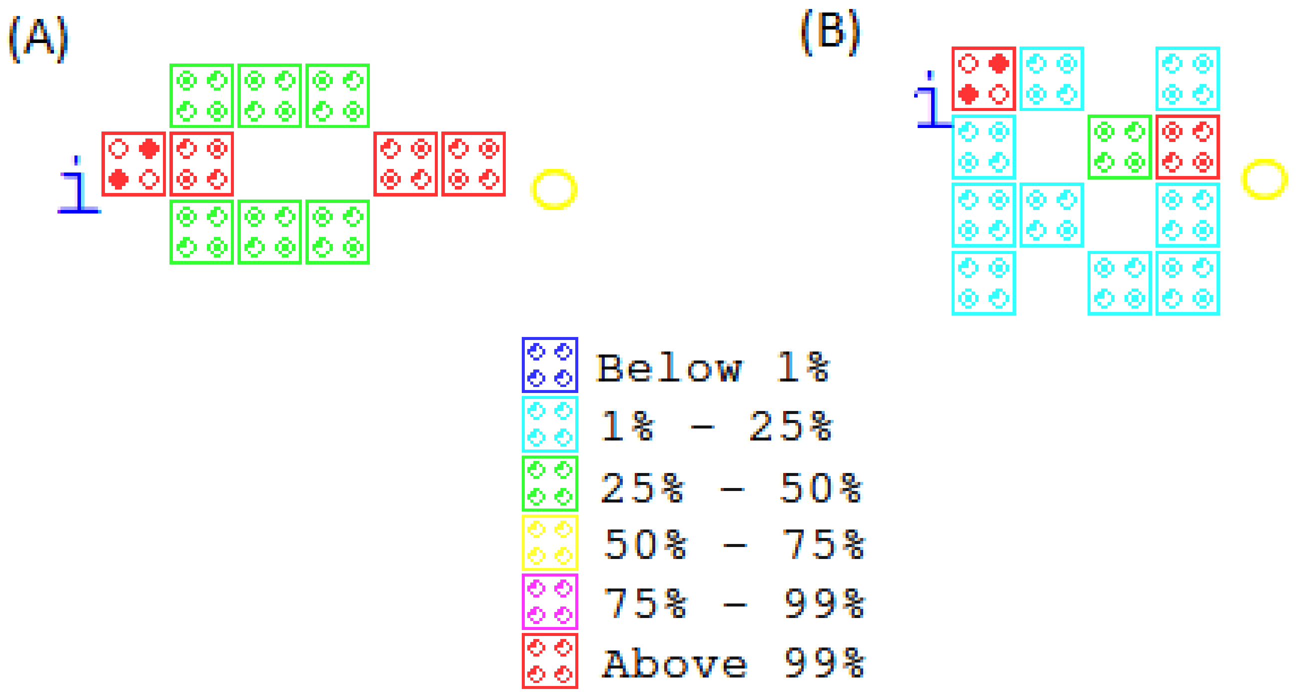
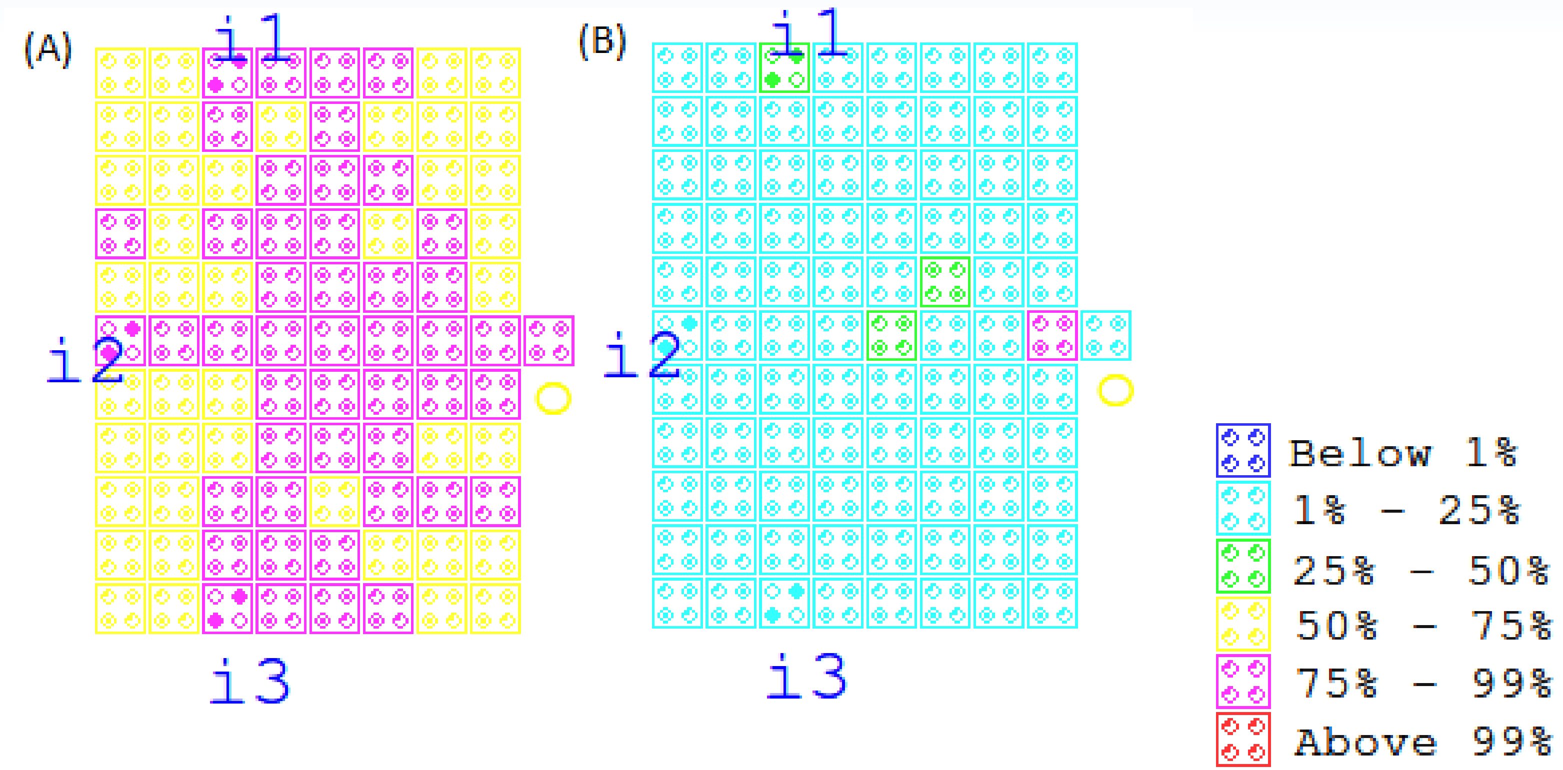
Simulations and results

Two inverter (A) and (B) for 1.000 tests under vacancy defects.
Probability model “Assignable”.



Simulations and results

Reliable majority cell for 1.000 tests under dopant defects (A) and interstitial defects (B). Probability model “Assignable”.



Conclusions

- The new methodology presented is useful to:
  - Design more reliable QCA circuits/ structures;
  - Compare QCA circuits in terms of robustness;
  - Verify the reliability of a QCA circuit undo different test conditions;
- Simulation results proved the feasibility of the methodology.

Thank you! Questions?

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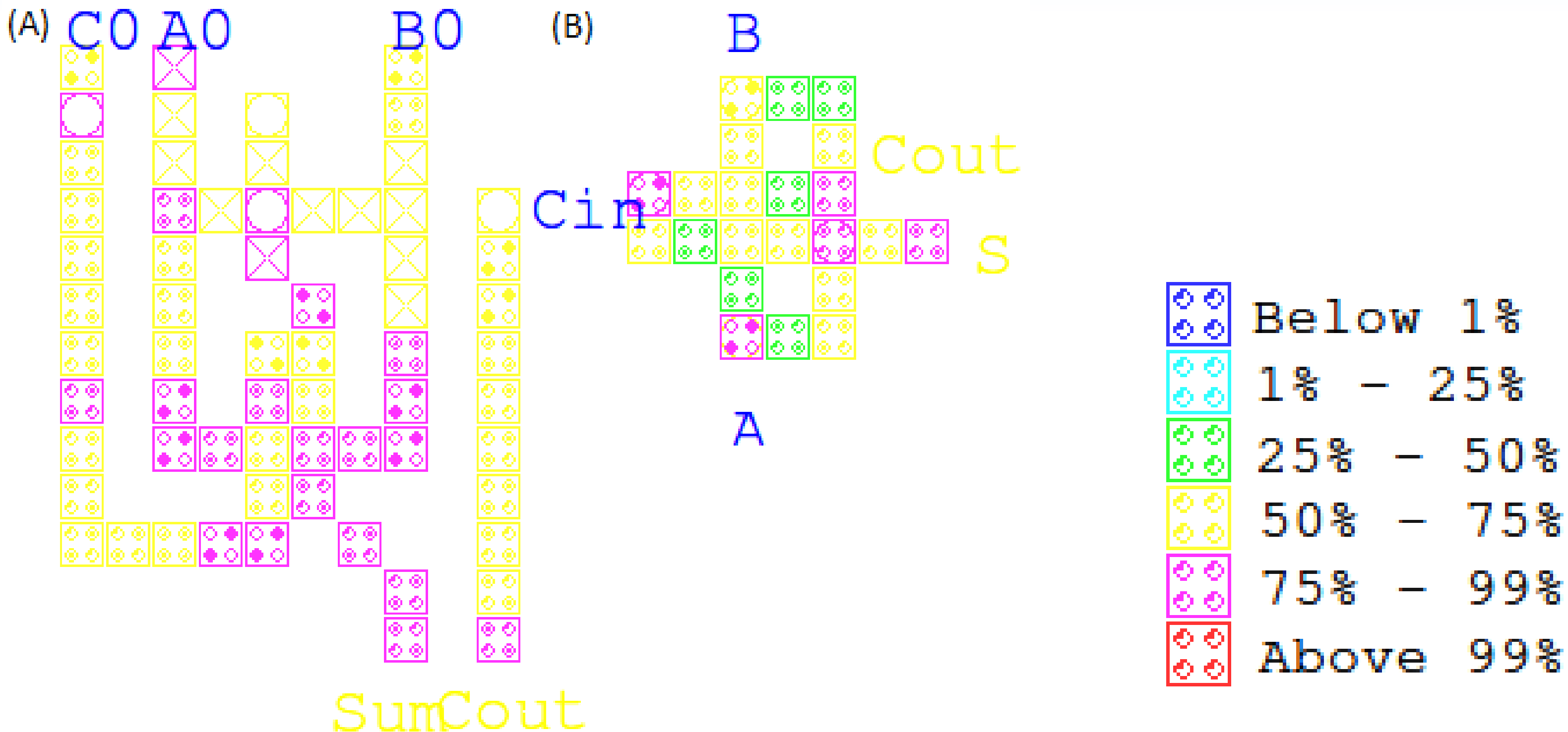
EXTRA

Simulations and results

Two full adder (A) and (B) for 1.000 tests under dislocation defects. Probability model “Assignable”.



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Simulations and results

Tables 1 and 2 - Error-Free Simulations (%)*

	INVERTER		3-INPUT MAJORITY		FULL ADDER	
	INV1	INV2	MJ1	MJ2	FA1	FA2
Vacancy	74.6	**86.1**	**60.6**	30.3	2.8	**16.2**
Interstit.	97.4	**99.9**	**94.3**	87.9	54.9	**76.0**
Dopant	83.7	**88.6**	**75.8**	31.1	3.7	**26.2**
Dislocat.	88.6	**93.9**	**78.5**	67.2	25.9	**51.0**

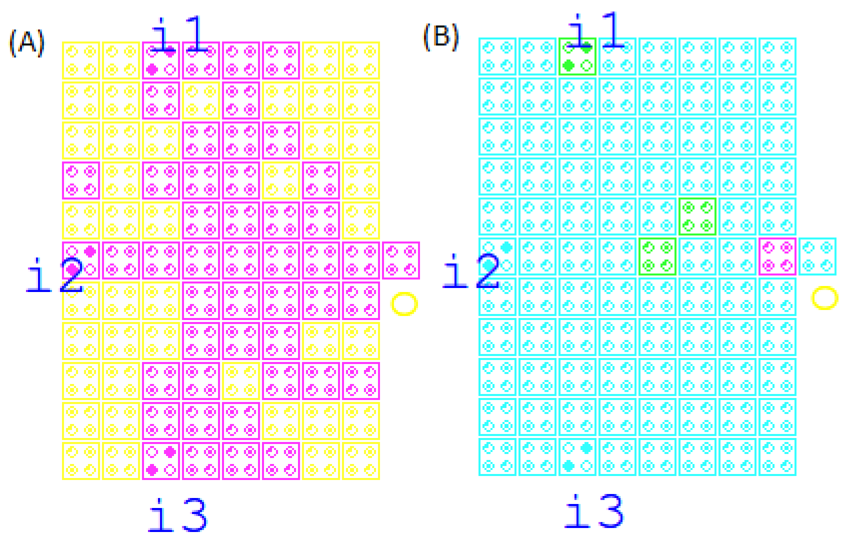
*Probability model=Assignable; Number of iterations=1000; Probability value for individual defect classes=5%; Sample Interval=10% and LOW/HIGH Threshold=80%.

	INVERTER		3-INPUT MAJORITY		FULL ADDER	
	INV1	INV2	MJ1	MJ2	FA1	FA2
Vacancy	60.0	**83.3**	11.1	**89.9**	**26.6**	0.0
Interstit.	96.0	**100**	87.8	**98.9**	50.9	**83.9**
Dopant	69.0	**80.8**	42.2	**85.2**	0.0	**37.4**
Dislocat.	88.0	**90.8**	61.1	**95.2**	**77.2**	39.0

*Probability model=Sequential; Number of iterations=10 for interstitial, dopant and dislocation defect classes. 1 for vacancy defect class. Sample Interval=10% and LOW/HIGH Threshold=80%.

Simulations and results

MJ2 for 1.000 tests under dopant defects (A) and interstitial defects (B). Probability model "Assignable".



INV1 (A) and INV2 (B) for 1000 tests under vacancy defects. Probability model "Assignable".