Robustness Analysis and Enhancement Strategies for Quantum-dot Cellular Automata Structures

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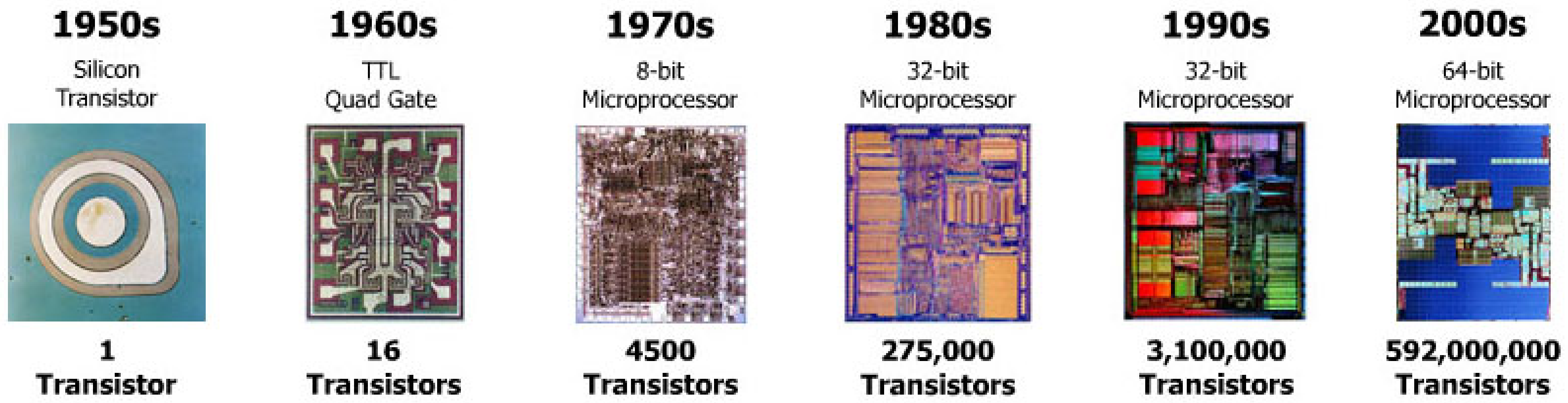
Agenda

- Introduction
- Background
- QCA Defects Simulator
- Robustness Enhancement Strategies
- Results
- Conclusions

Introduction

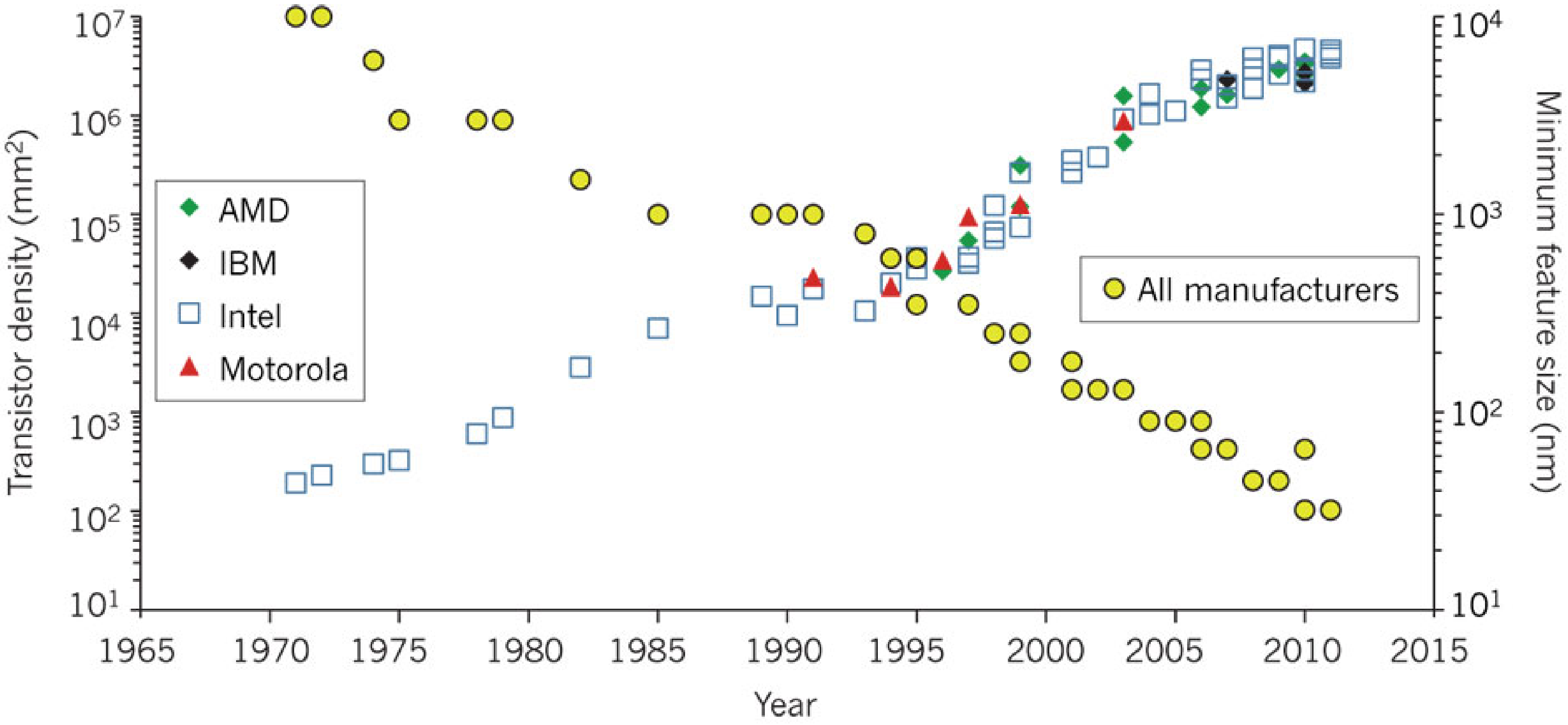
The current technology for computer design

- CMOS – Complementary Metal-Oxide Semiconductor
  - ✓ Silicon transistors
  - ✓ Widely used since the late 1960s
  - ✓ Highly mature manufacturing process
  - ✓ Reliable



Moore's Law and CMOS devices scaling

- 2x number of transistors every twenty four months.



Source: Ferain et al, 2011.

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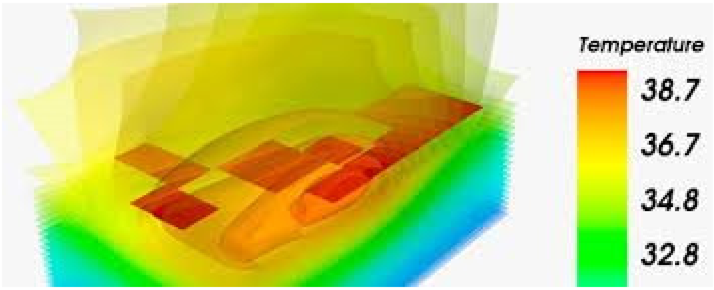
Consequences of CMOS devices scaling

- Transistor count still rising
  - ✓ Moore's Law still sustains
- Clock speed flattening sharply
  - ✓ Multi-core processors
- Power reaches limits

✓ High efforts for cooling

✓ Increasing operational costs

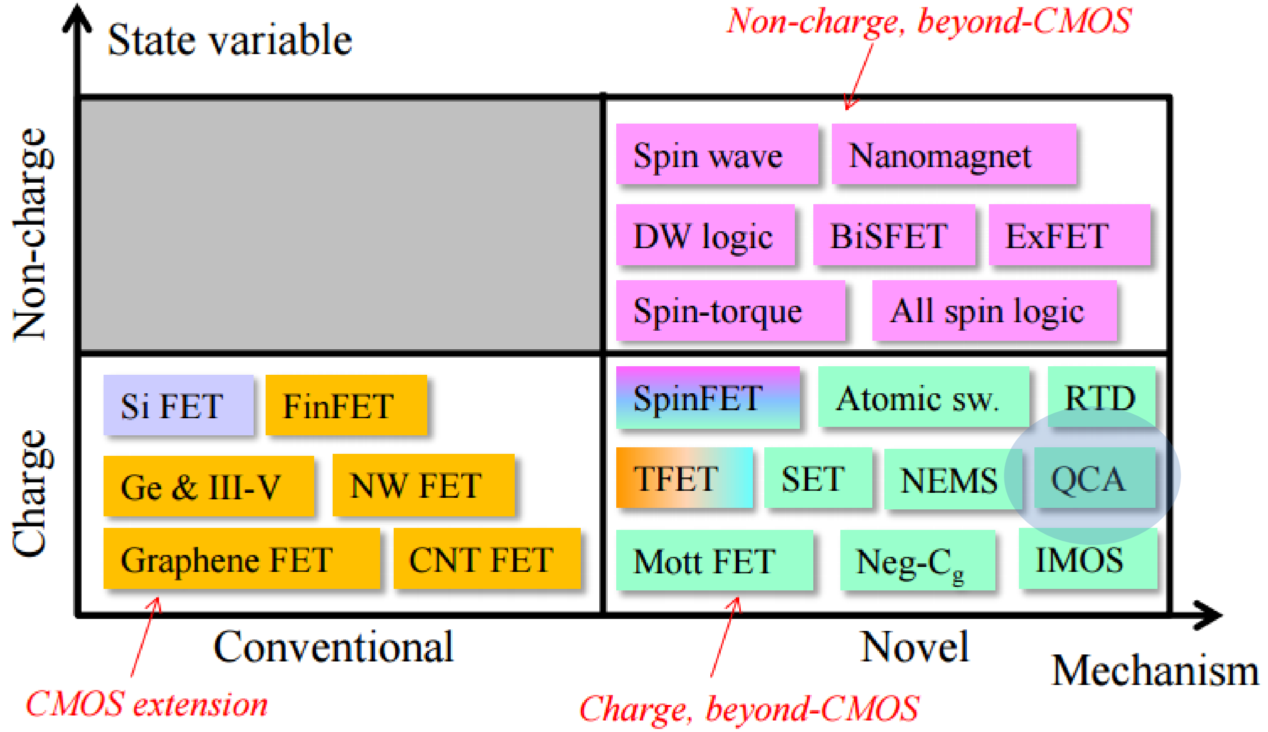


✓ Reduced reliability

What's next?

- Nanoelectronics: The use of nanotechnology in electronic components.

- Nanotechnology exploits:
  - ✓ Material quantum mechanical properties;
  - ✓ Inter-atomic level interactions.

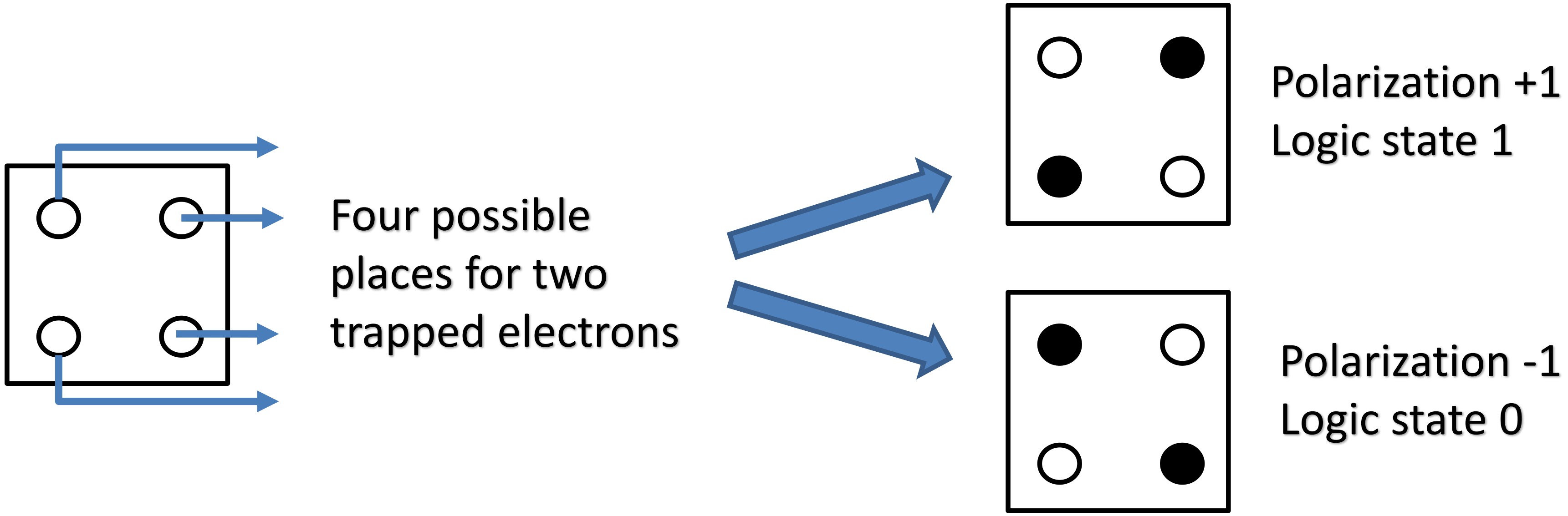


Background

QCA - Quantum-dot Cellular Automata

- A new computation paradigm based on electrostatic interactions.

QCA cell (basic unit)



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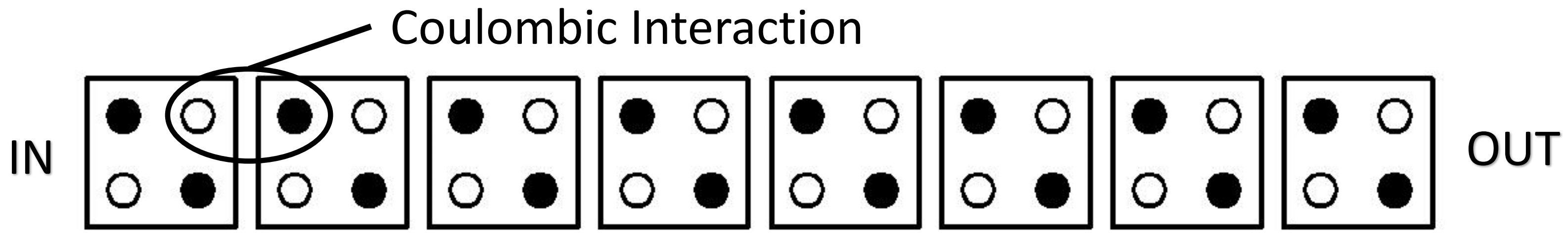
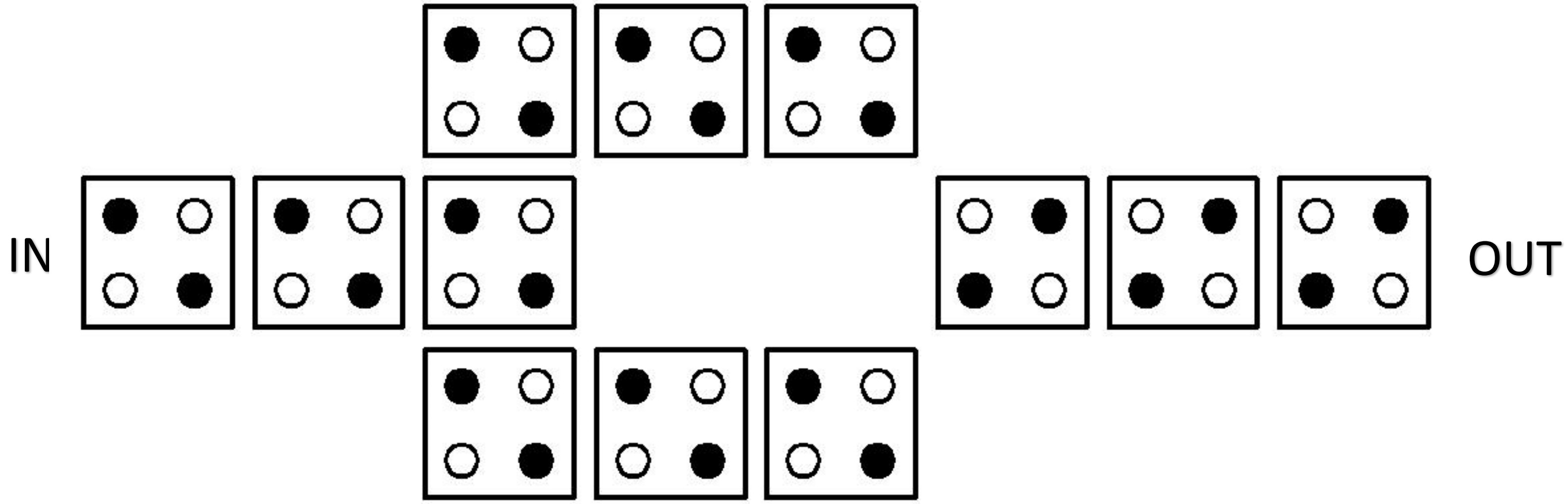
QCA Components

QCA wire



Inverter



- Any logic can be created.
- More complex circuits are feasible.

QCA Pros and Cons

QCA Pros

- Very high theoretical speeds achieved (within THz range);
- Low power consumption (information is transported with no electric current flow);
- Small dimensions (a molecular QCA cell should be 2x2 nm).

QCA Cons

- Extremely difficult physical implementation.

Defects and Errors in QCA circuits

- This work considers as:

Defects

- Flaws of the cells of a structure;
- Phase shifts of the clock signals.

Errors

- Consequences of defects to the output signals.
- Manifest themselves as:
    - ✓ Excessive delay;
    - ✓ Wrong logic state (signal inversion).

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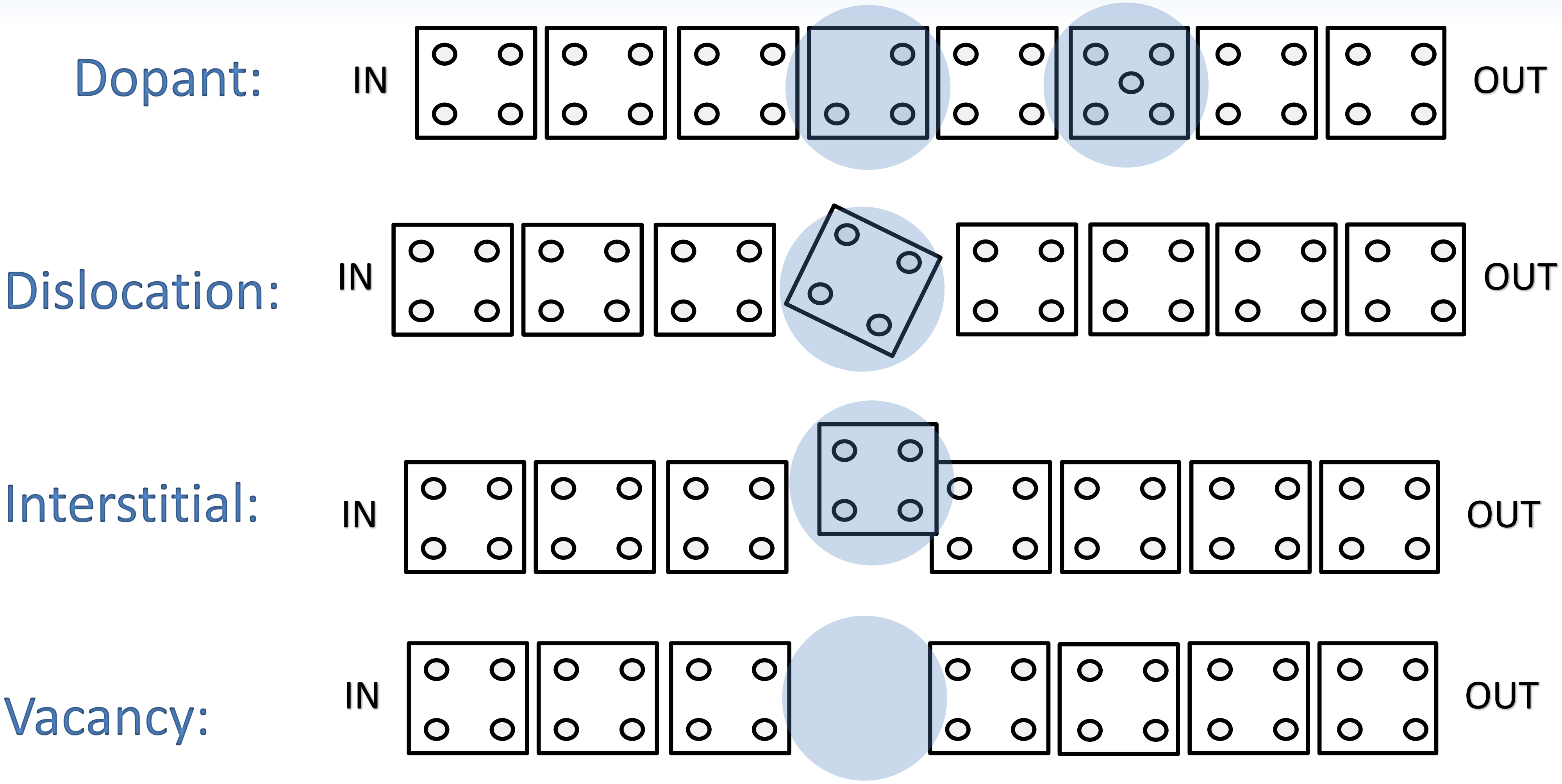
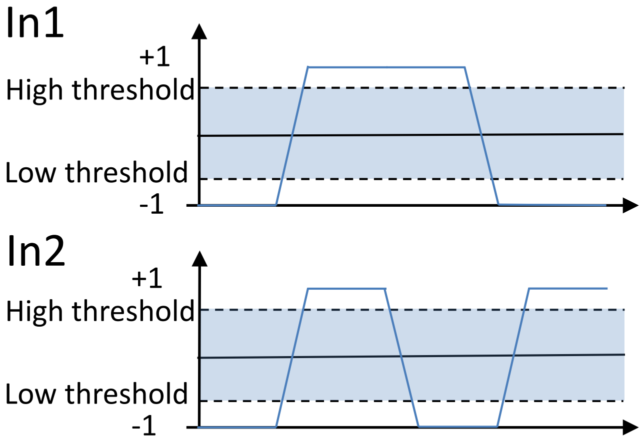
Structural defects modeling

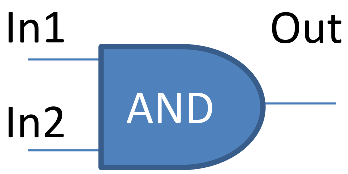


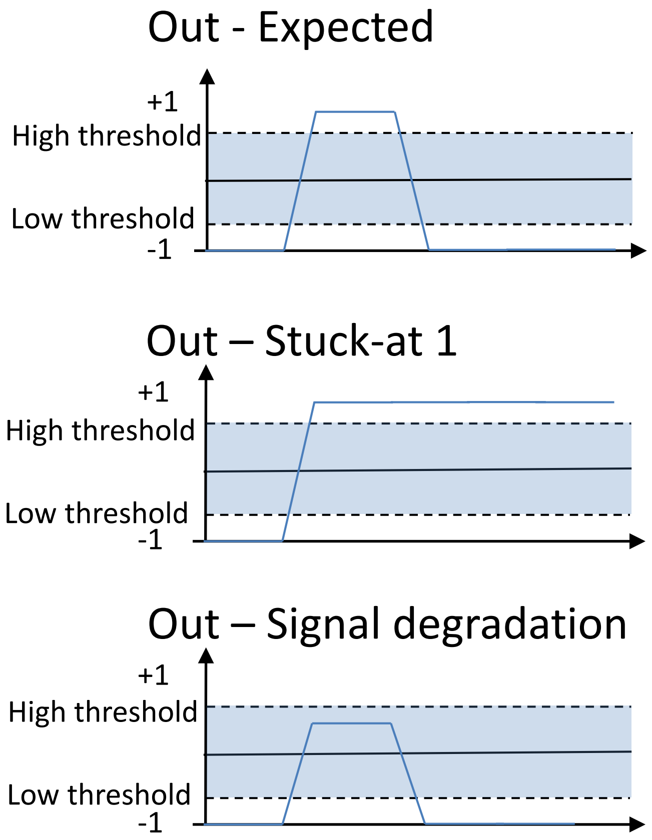
Errors in QCA circuits

- Unexpected deviations in the behavior of a system.

Example







- Likely to occur due to defects.
- Major consequence: Reliability decreased.

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Motivation

Introducing a methodology for QCA robustness analysis

Extensive

Four classes of defects + Three probability models

Flexible

Parameter-based approach → Operates under different conditions

Innovative

Easy to interpret and visualize the results
→ Error-free simulations calculation (%)
→ Heat map

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Methodology Characterization Round

Repeat for all iterations

After all iterations

- Circuit selection
- Parameters setting

Step I

Step II

- Error-free reference simulation
- Defect insertion
- Fault simulation
- Comparison (Error-free x defective)
- Error-free simulations percent calculation

- Result analysis
- Design heat map

Step III

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Step I

Parameters to be set - basics

- Number of iterations;
- Round stop criteria:
  - ✓ Number of stable iterations required.
  - ✓ Maximum error-free simulation rate variation allowed
- Sample interval;
- HIGH/LOW thresholds.

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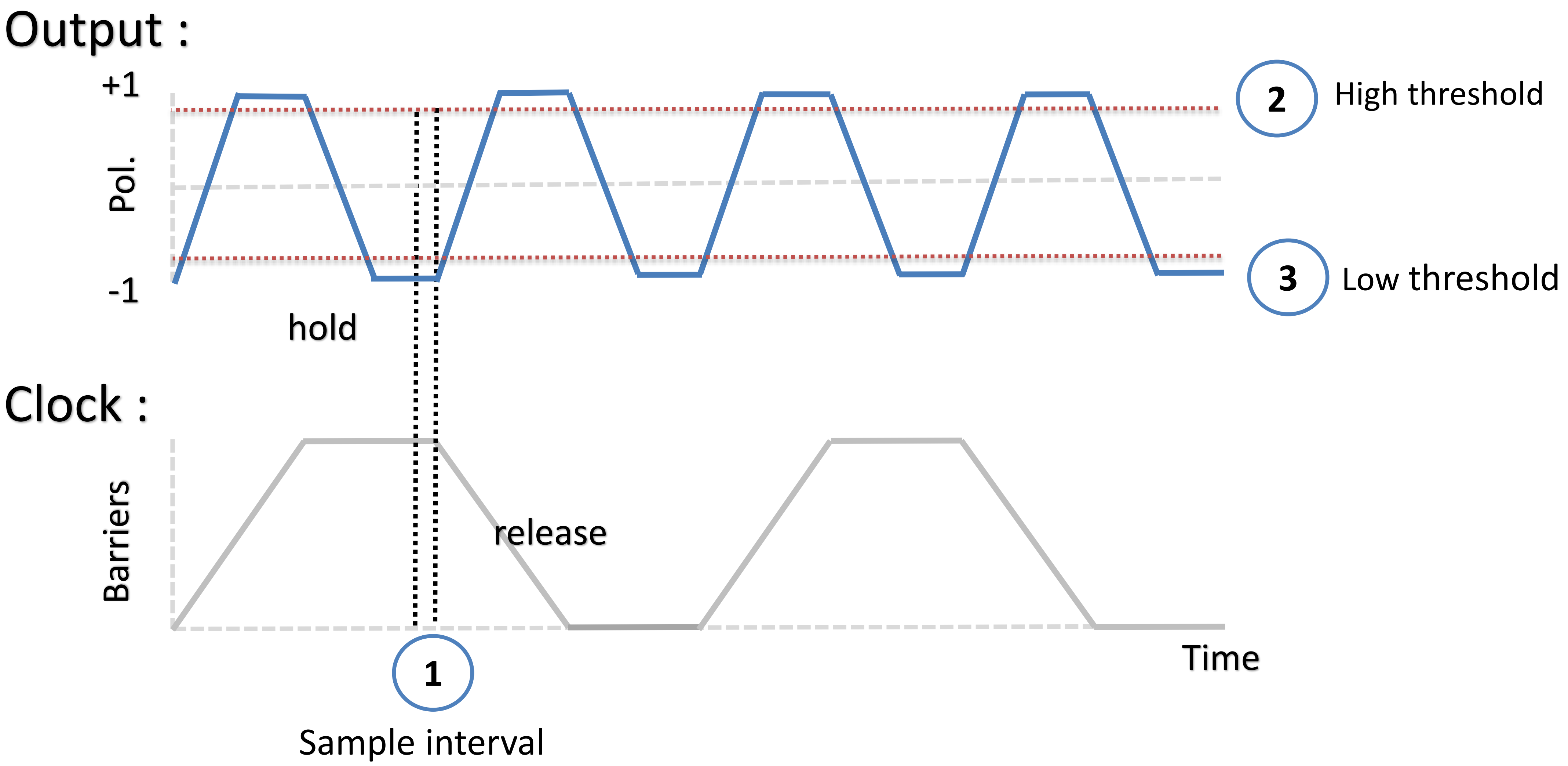
Output :
+1
Pol.
-1
hold
2
High threshold
3
Low threshold
Clock :
Barriers
release
Time
1
Sample interval

Parameters to be set – defect classes and probabilities

- Test framework: structural defects/ clock phase shifts

- Define the defect classes:
  - ✓ Dislocation
  - ✓ Dopant
  - ✓ Interstitial
  - ✓ Vacancy

- Probability model
  - ✓ Sequential
  - ✓ Assignable
  - ✓ Uniform

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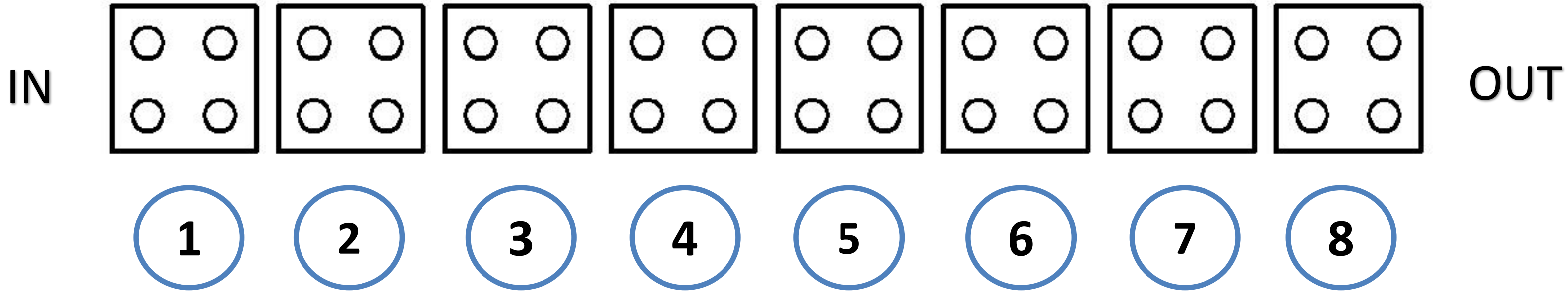
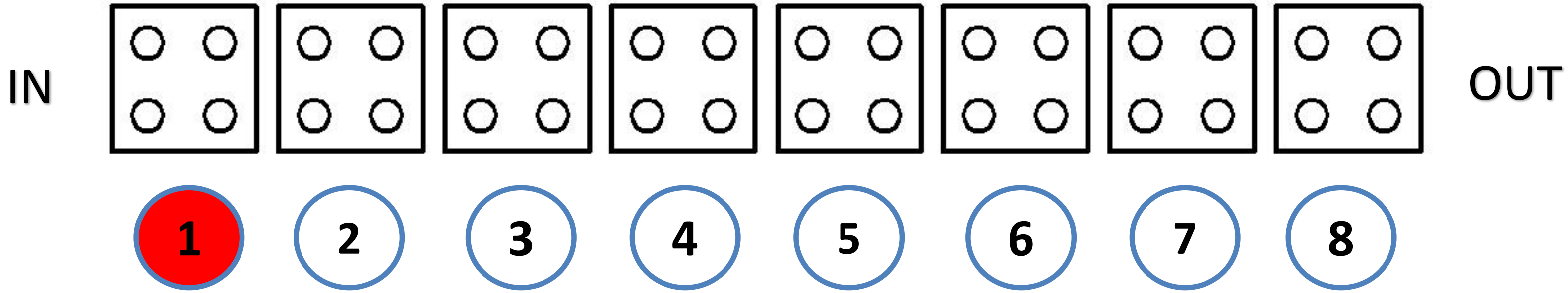
Sequential Probability



Sequential Probability



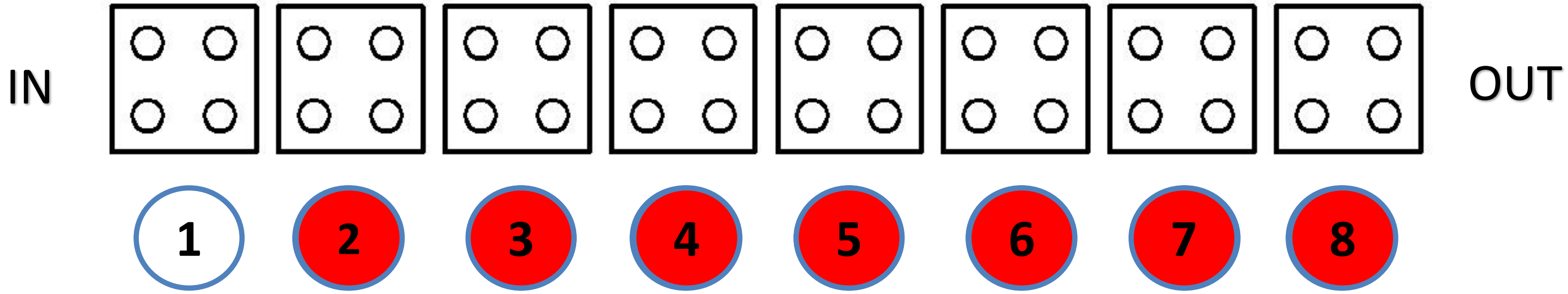
- Cell 1 shall be defective!

- Which defect should be inserted?

It is randomly chosen among the defined (checked) classes.

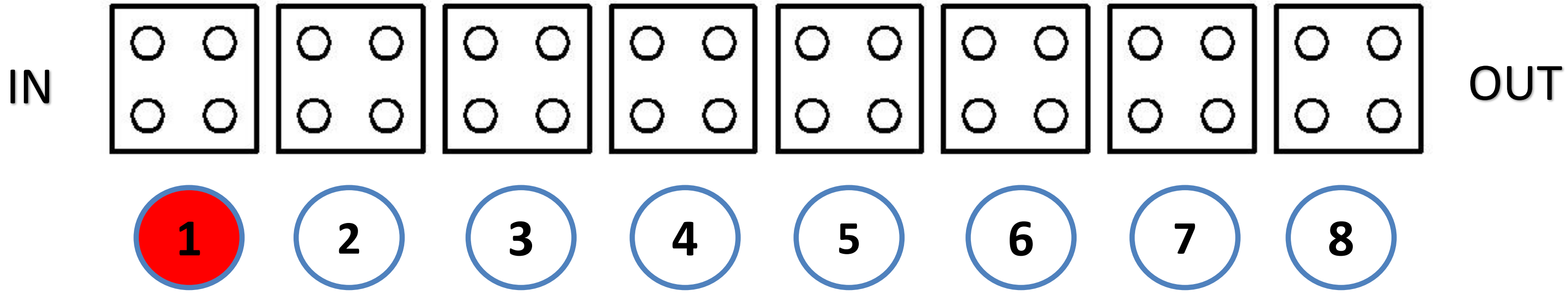
- ✓ Dislocation
- ✓ Dopant
- ✓ Interstitial
- ✓ Vacancy

Sequential Probability



- The defect insertion process is repeated until it reaches the last cell…

Assignable Probability



- Cell 1 may or may not be defective.
  - ✓ It depends on an user-set probability parameter (between 0 and 1)

- Which defect should be inserted?

It is randomly chosen among the defined (checked) classes.

- ✓ Dislocation
- ✓ Dopant
- ✓ Interstitial
- ✓ Vacancy

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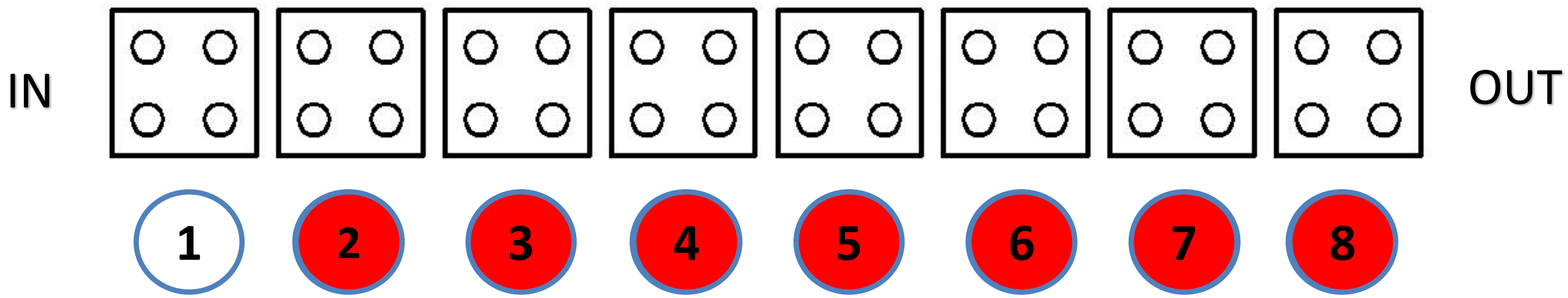
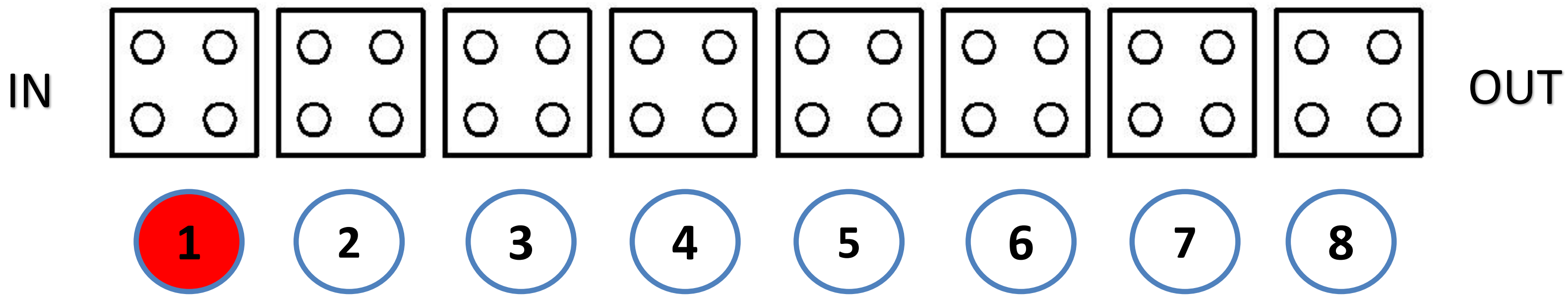
Assignable Probability



- The defect insertion process is repeated until it reaches the last cell…

Uniform Probability



- Cell 1 may or may not be defective.
  - ✓ It depends on the fixed probability value P=1/N.

  N= number of cells

- Which defect should be inserted?

It is randomly chosen among the defined (checked) classes.

- ✓ Dislocation
- ✓ Dopant
- ✓ Interstitial
- ✓ Vacancy

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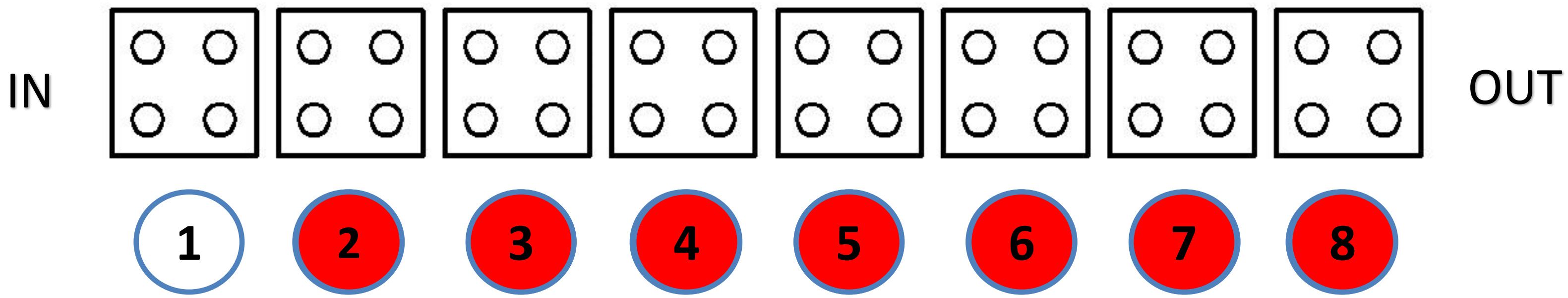
Uniform Probability



- The defect insertion process is repeated until it reaches the last cell…

Step II

Simulations and defect insertion

Repeat until the round stop criteria achievement

- Error-free reference simulation;
  - ✓ Results stored
- Defect insertion;
  - ✓ According to the probabilities
- Simulation of the defective structure;
- Comparison (Error-free x defective);
  - ✓ Error detection
- Error-free simulations rate updated;
- Results file are saved.

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Step III

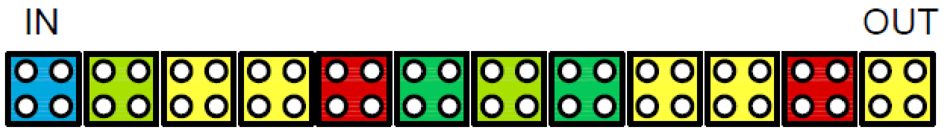
Results analysis

- Design heat map creation (structural defects testing);
- Final update of the results file.

Heat map

- Mapping criticality of defective cells.
  - ✓ How often it provokes an error?

A visual resource for results analysis



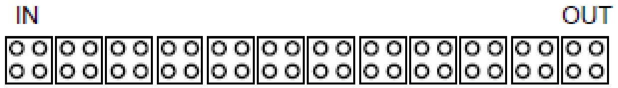
Colors used

- <1%
- 1%-25%
- 25%-50%
- 50%-75%
- 75%-99%
- >99%

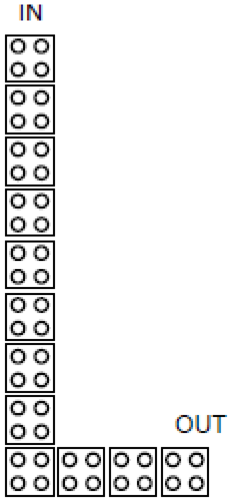
- Yellow cells are majorly related to defects.
- Given an error event, these cells have __50-75%__ of probability to be defective.

Robustness Enhancement Strategies

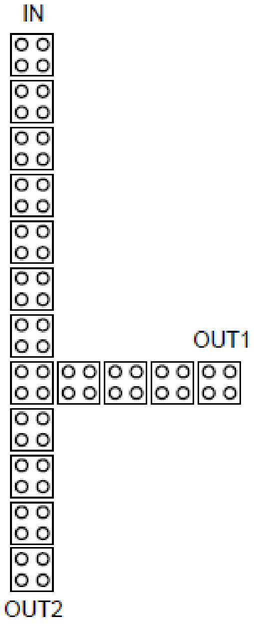
Fundamental components tests set up



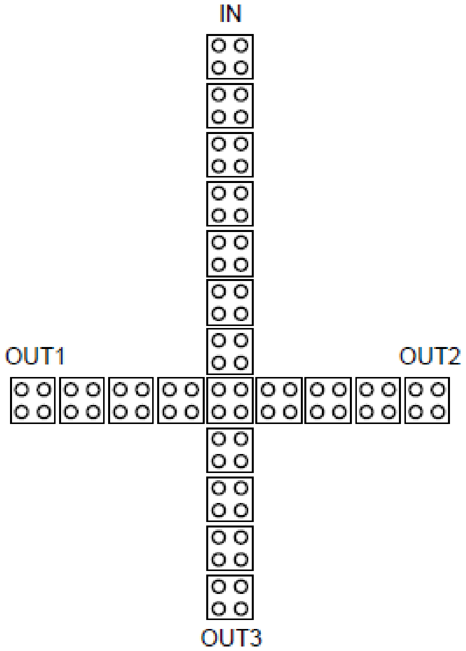
Wire



Bend Wire



Fanout of 2



Fanout of 3

- Sequential probability;
- 16 defect insertion per cell in each component;
- All the four defect classes defined separately.

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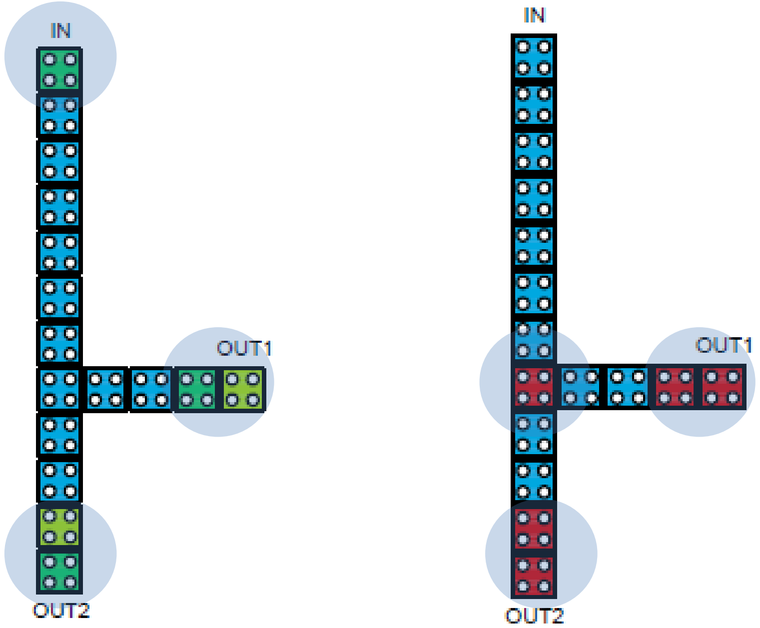
Proposal of Robust Components

The robust components were proposed based on:

- Analysis of the heat maps:
  - ✓ Considers all the defect classes;
  - ✓ Identifies possible polarization weaknesses;
  - ✓ Inputs, Outputs and Turnings are vulnerable.

- The robustness enhancement strategy consists of:
  - ✓ Applying redundancy within the structures;
  - ✓ Perform strategic structural modifications.

Examples:

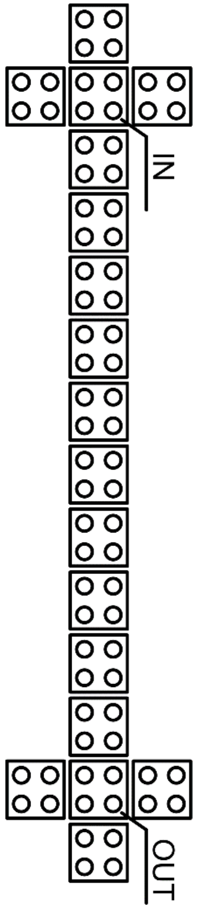


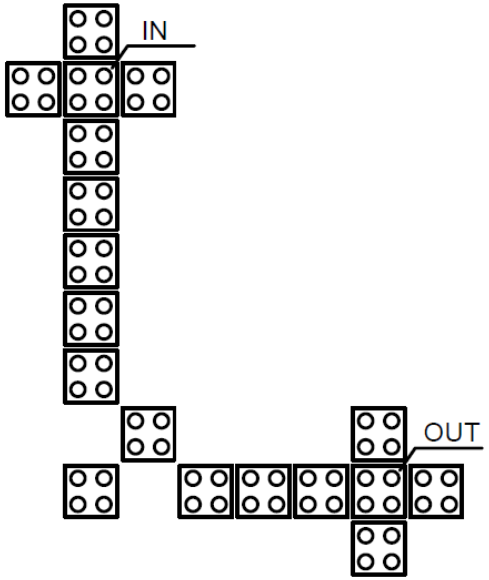
(a) Fanout of 2 under dislocation defects

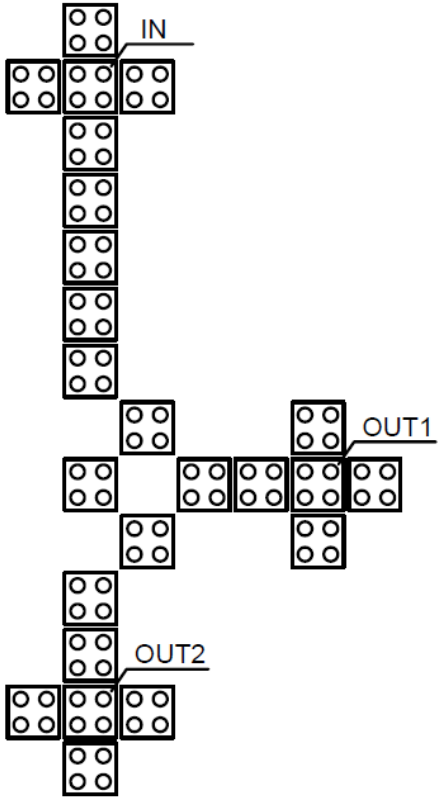
(b) Fanout of 2 under vacancy defects

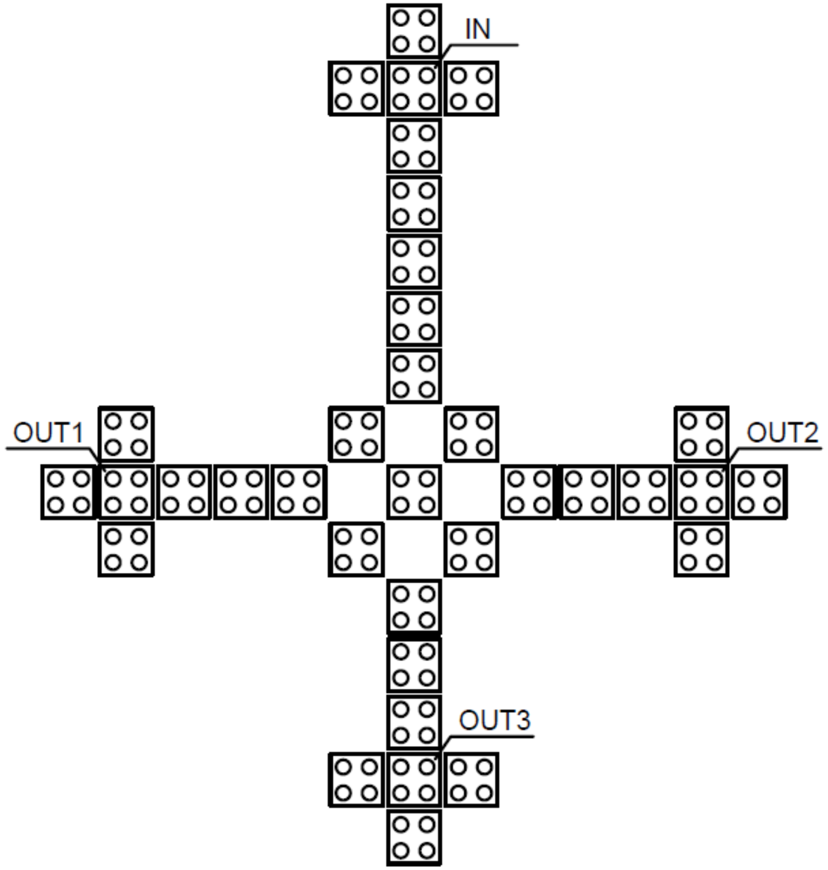
Components Proposed

Modified Wire	Modified Bend Wire	Modified Fanout of 2	Modified Fanout of 3









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Regular x Modified Robustness Verification

- Sequential probability;
- 4 defect insertion per cell in each component;
- All the four defect classes simultaneously defined.

	Error-free simulations rate (%)		
	Regular Component	**Modified Component**	**Rate Variation**
Wire	72.40 %	86.46 %	+14.06 %
Bend Wire	70.83 %	87.85 %	+17.02 %
Fanout of 2	72.27 %	85.16 %	+12.89 %
Fanout of 3	64.38 %	88.75 %	+24.37 %

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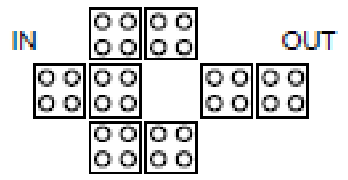
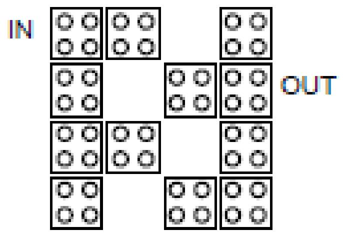
Proposed circuits

- Comparison between:
  - ✓ Regular structure
  - ✓ A robust structure already reported in the literature
  - ✓ The proposed structure (built with the modified fundamental components)

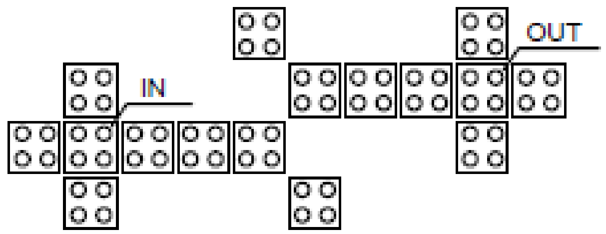
Inverters



(a) INV1 - Regular inverter



(b) INV2 - Robust Inverter (Beard, 2006)



(c) INV3 - The proposed inverter

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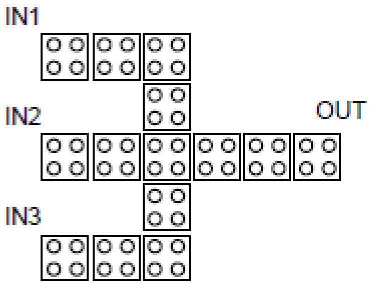
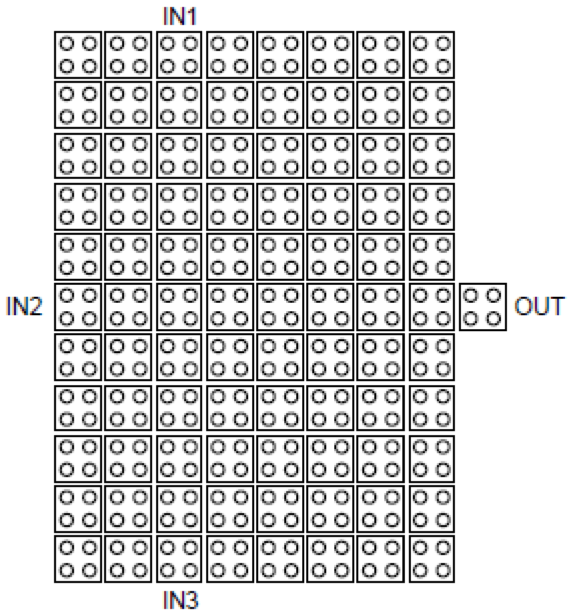
Proposed circuits

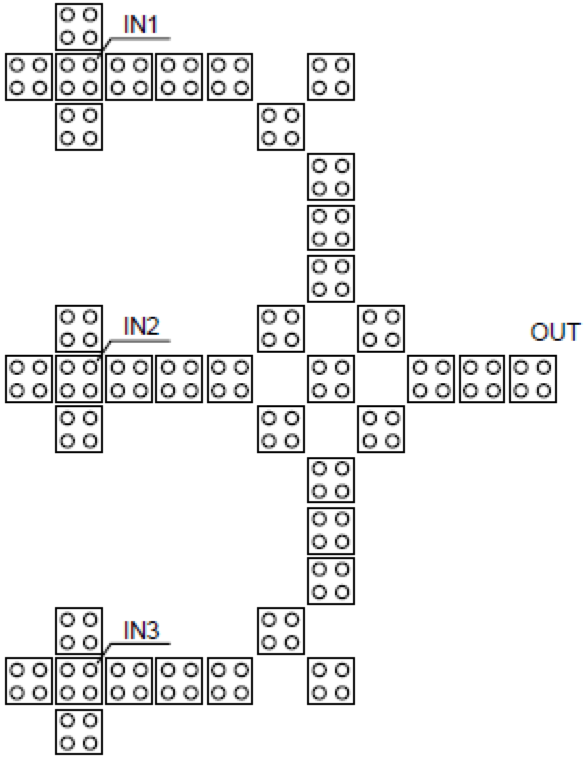
3-input majority gates



(a) MAJ1 - Regular majority gate



(b) MAJ2 - Robust majority gate (Fijany et al, 2001)



(c) MAJ3 - The proposed majority gate

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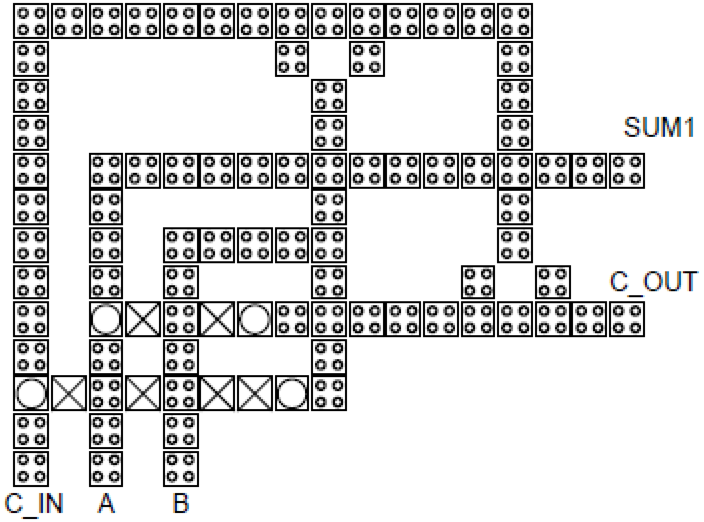
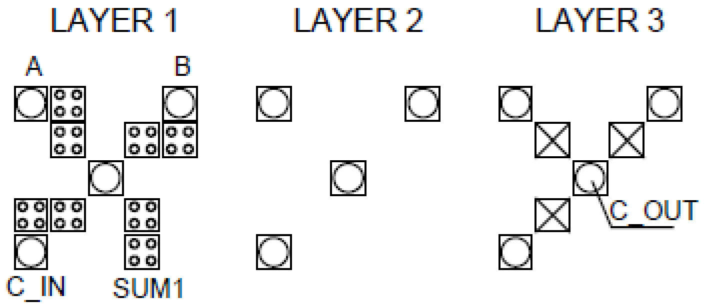
Proposed circuits

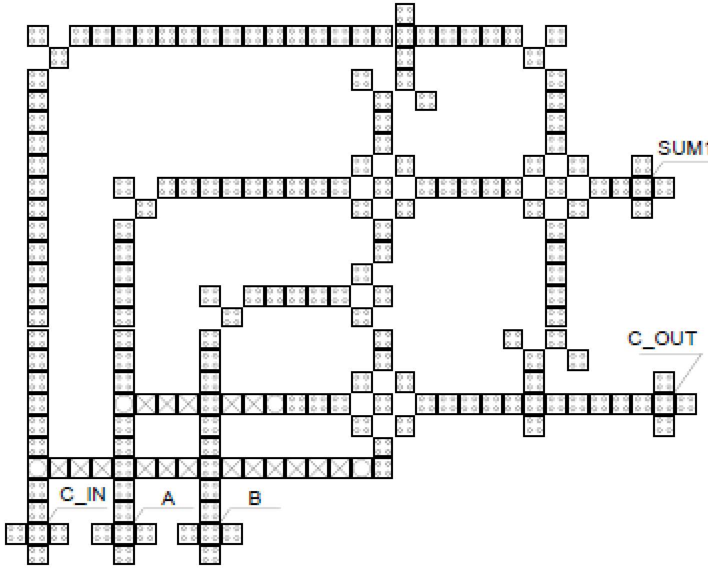
Full adders



(a) ADD1 - Regular full adder (Bruschi et al, 2001)



(b) ADD2 – Compact and robust full adder (Roohi et al, 2015)



(c) ADD3 - The proposed full adder

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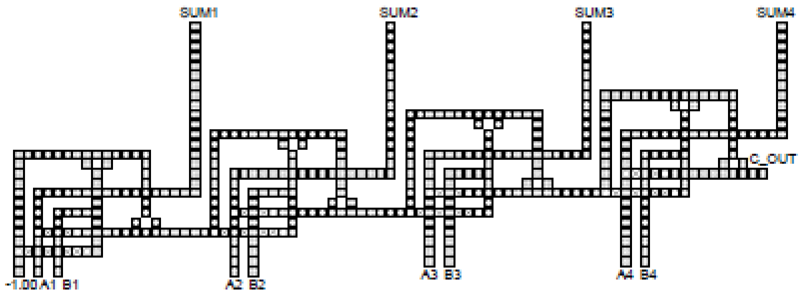
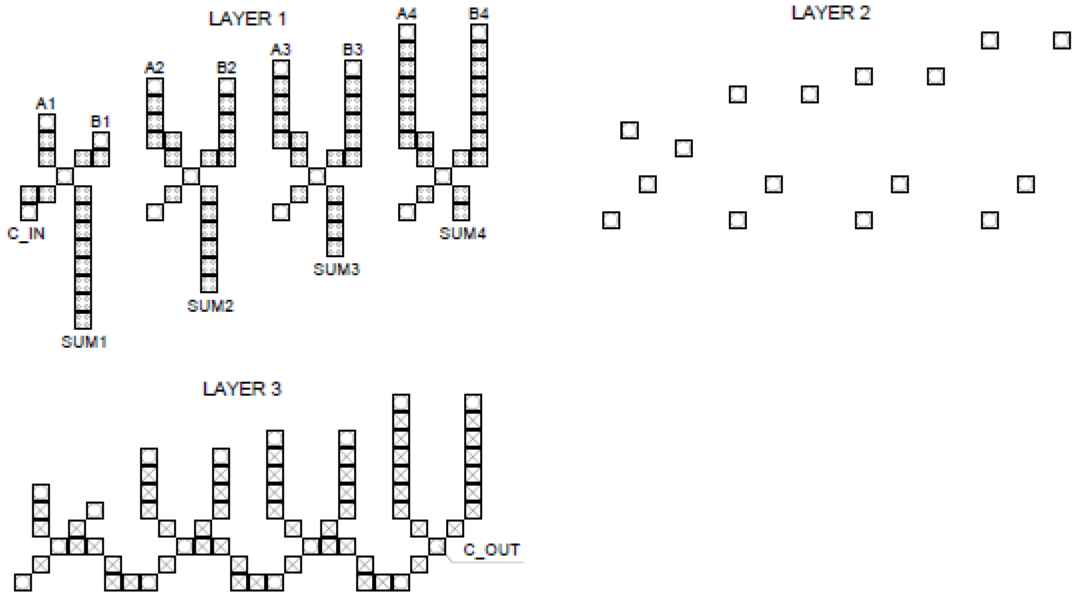
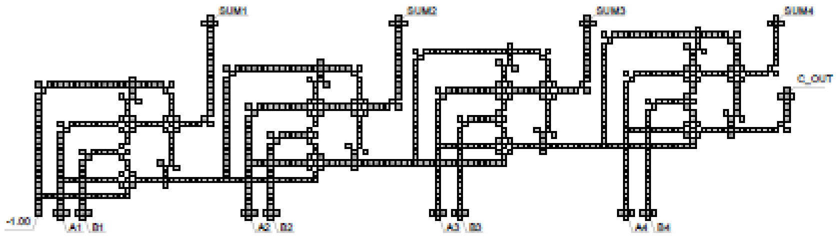
Proposed circuits

4-bit RCAs



(a) RCA1 - Regular RCA
(Bruschi et al, 2001)



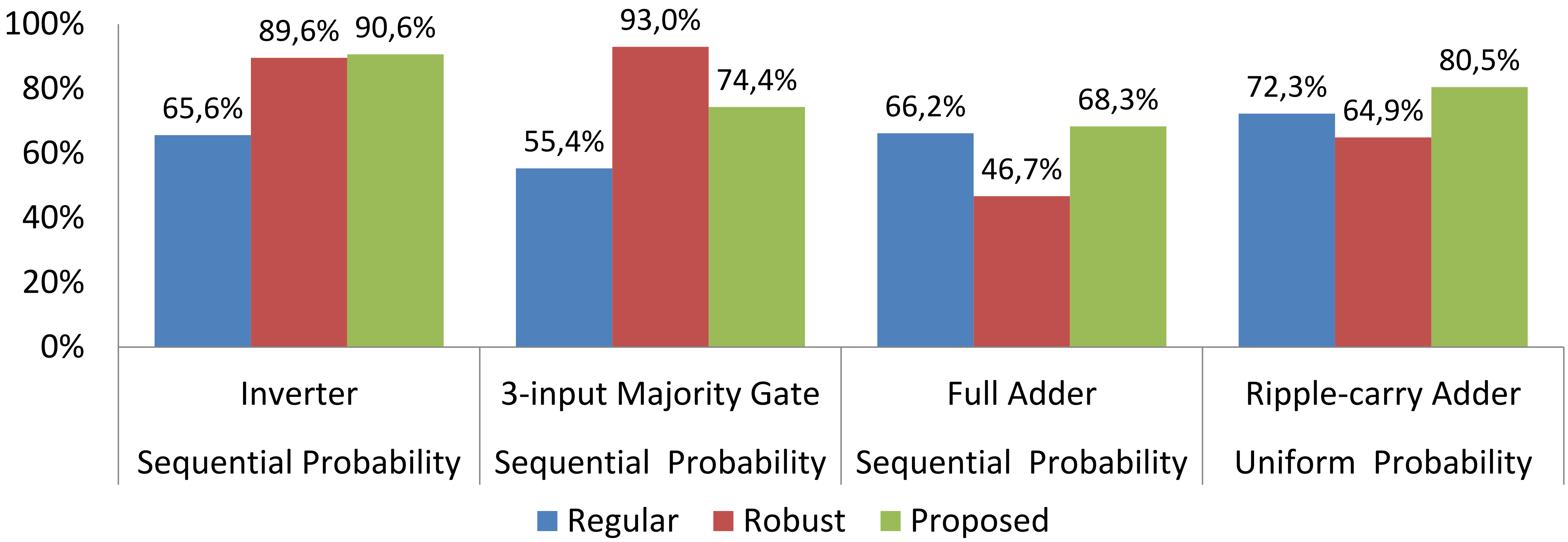


(c) RCA3 - The proposed full adder

(c) RCA2 – Compact and robust RCA
(Roohi et al, 2015)

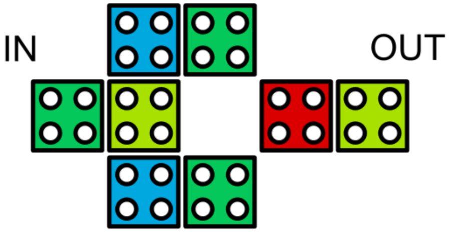
Results - Error-free simulations rates

- 4 defect insertion per cell in each component;
- All the four defect classes simultaneously defined.

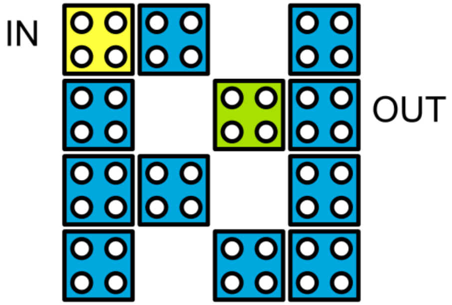


Heat maps

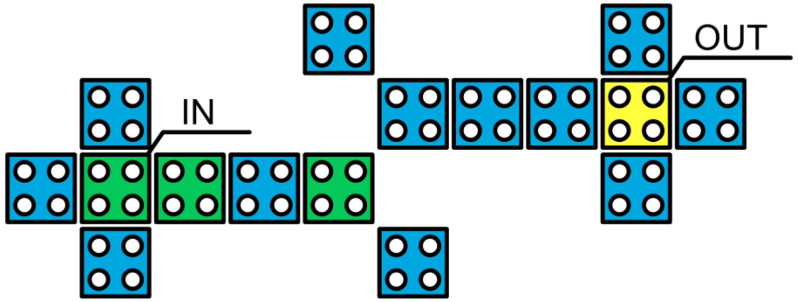
Inverters



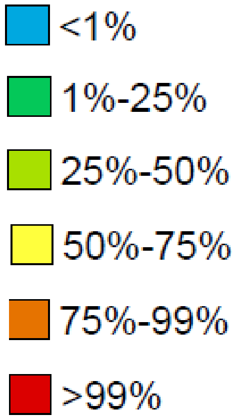
(a) INV1 under combined defects



(b) INV2 under combined defects



(c) INV3 under combined defects



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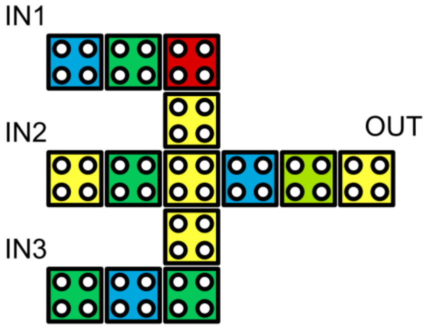
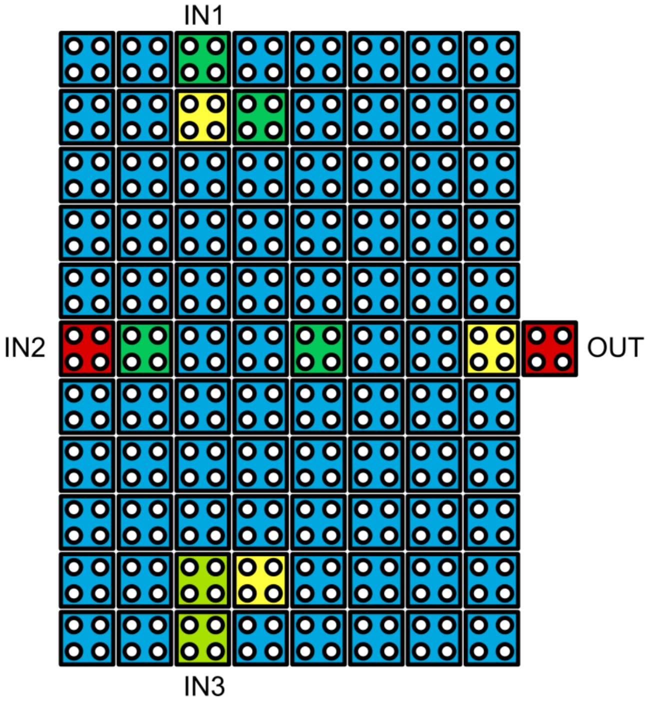
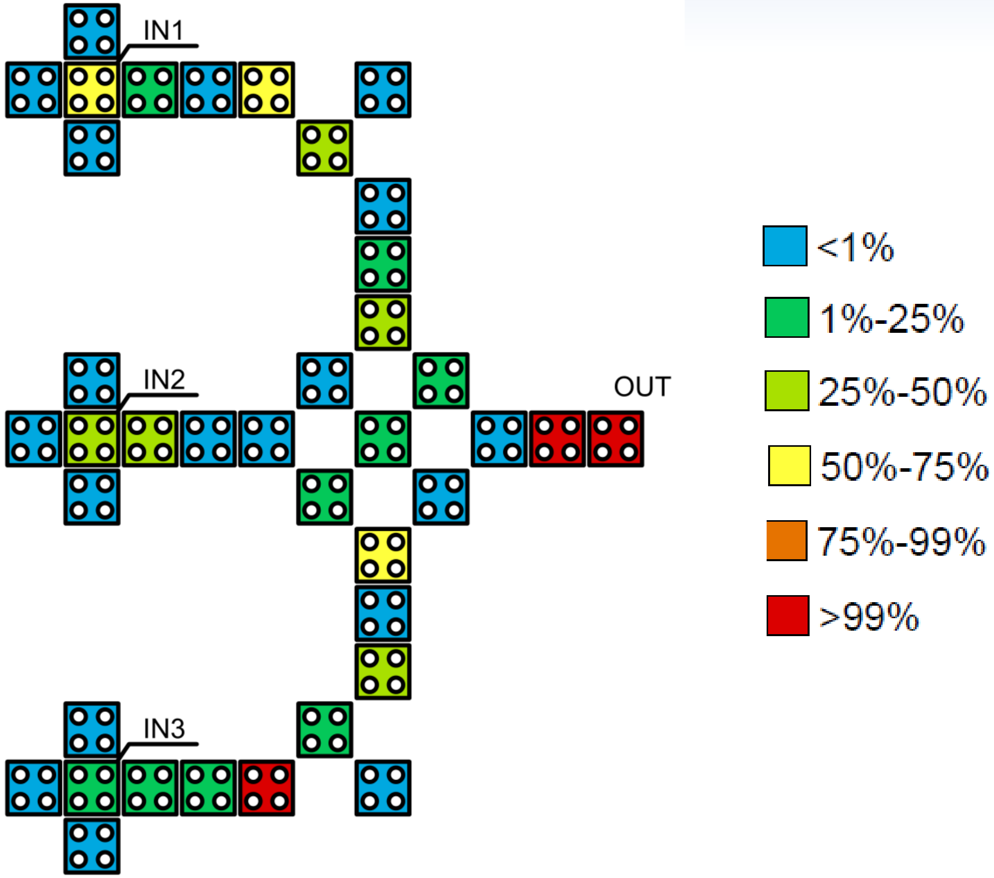
3-input majority gates



(a) MAJ1 under combined defects



(b) MAJ2 under combined defects



(c) MAJ3 under combined defects

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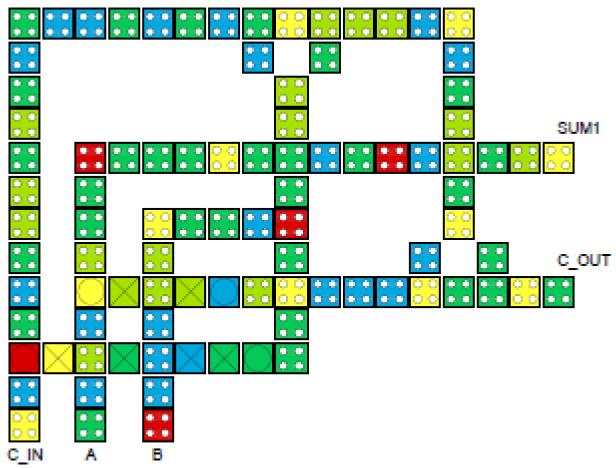
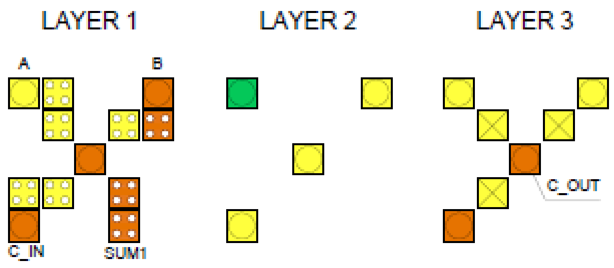
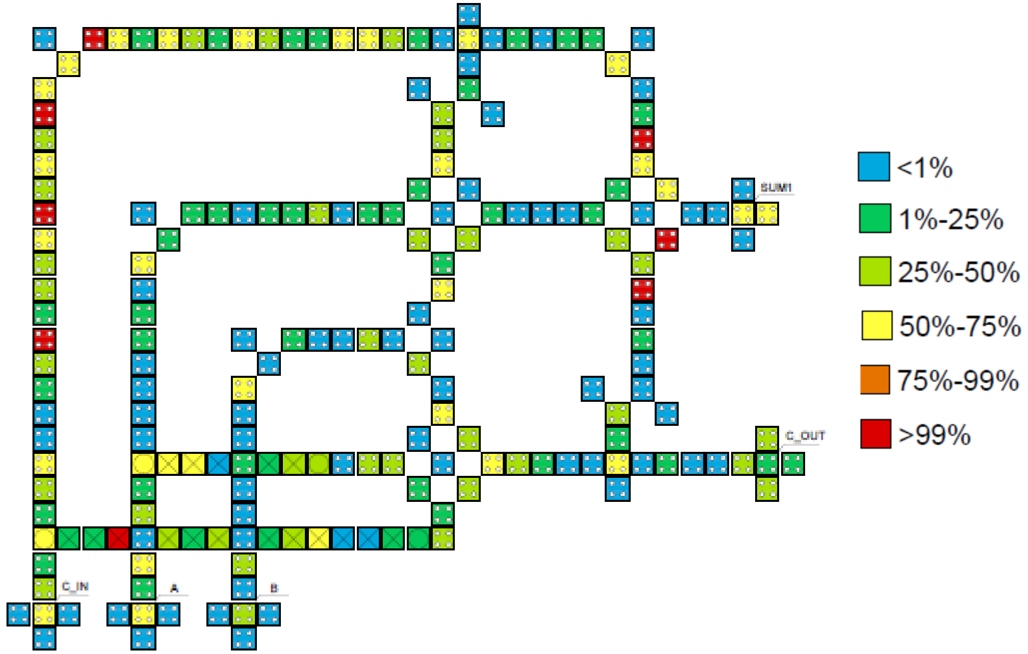
Full adders



(a) ADD1 under combined defects



(b) ADD2 under combined defects



(c) ADD3 under combined defects

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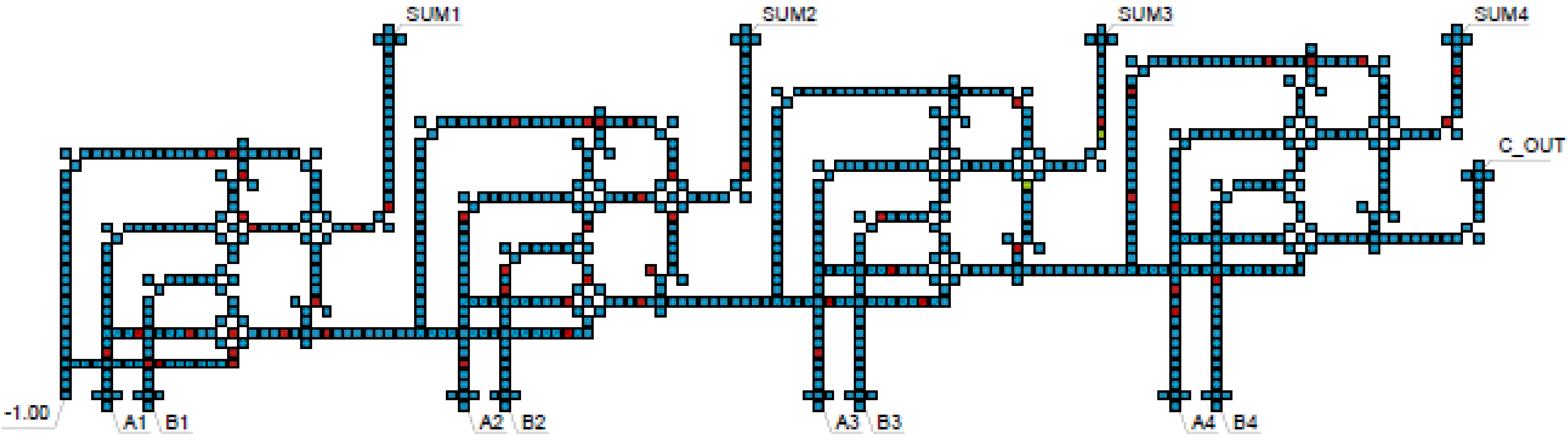
RCA



RCA3 under combined defects

Remaining results

Phase-shifted clocking circuits

	Shifts Range (Synchronous Clock)			Shifts Range (Asynchronous Clock)		
Component	**0 to 45º**	**45 to 90º**	**0 to 90º**	**0 to 45º**	**45 to 90º**	**0 to 90º**
Wire	92.4%	72.3%	84.4%	<u>99.9%</u>	71.7%	85.8%
Bend Wire	96.8%	50.2%	73.5%	<u>99.9%</u>	44.8%	72.3%
Fanout of 2	<u>96.1%</u>	50.0%	73.0%	94.9%	48.7%	72.0%
Fanout of 3	<u>95.6%</u>	50.5%	73.1%	93.9%	50.6%	72.2%

Publications

Journal paper (under review)

Reis, D. A., Sill Torres, F. **Robustness analysis of structures and clocking for QCA devices**. – under review in JICS (Journal of Integrated Circuits and Systems)

Conference papers

Reis, D. A., Sill Torres, F. **A novel methodology for robustness analysis of QCA circuits.** In Proceedings of the 28th Symposium on Integrated Circuits and Systems Design (SBCCI '15). 2015. ACM, New York, NY, USA. DOI=http://dx.doi.org/10.1145/2800986.2800995

Reis, D. A., Sill Torres, F. **O uso do clock assíncrono para aumento da confiabilidade de circuitos QCA.** In Proceedings of the 2nd NaCoWo – Nanocomputing Workshop. Belo Horizonte, Brazil, 2015.
ISSN 2447-9101

Conference paper (accepted)

Reis, D. A., Campos, C. A., Soares, T. R., Vilela Neto, O. P., Sill Torres, F. **A Methodology for Standard Cell Design for QCA**. – under review at IEEE Symposium on Circuits and Systems (ISCAS), Montreal, Canada, 2016

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Conclusions

- The QCA Defects Simulator presented allows to:
    - Design more robust QCA circuits/ structures;
    - Compare QCA circuits in terms of robustness;
    - Verify the reliability of a QCA circuit undo different test conditions;
- The tests performed allow to:
    - Identify polarization weak regions within the structures;
    - Prove the robustness of the proposed components/ circuits.

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Thank you!

Questions?

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