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Introduction

The purpose of this document is to investigate and evaluate different circuit topologies for reliably switching the reference voltage (VREF) of the SKY65383 RF front-end module. Ensuring a clean and stable reference voltage is critical for the proper operation of this device. This report presents a series of simulations and practical design considerations aimed at identifying the most effective method to control VREF using limited GPIO resources on the main MCU

Problem Definition

The SKY65383-11 is a high-performance 2.4 GHz transmit/receive (T/R) front-end module designed for ISM band wireless applications. It integrates a power amplifier (PA), low-noise amplifier (LNA), transmit/receive switch, and digital control logic into a compact 28-pin MCM package. Its operation relies on multiple regulated supply voltages and a stable reference voltage (VREF) to ensure reliable power amplification during transmission. Of particular importance is the accurate switching and timing of the VREF1 and VREF2 pins, which directly affect the PA's enablement and the transition between operational modes.

Table 4. SKY65383-11 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Transmit frequency range	f	2400		2483	MHz
PA supply voltage	V_{CC1}, V_{CC4}	3.0	3.3	4.0	V
PA reference voltage	V_{REF1}, V_{REF2}	2.75	2.85	2.95	V
Receive supply	V_{CC4}	2.7	3.3	3.6	V
Control logic voltage: High Low	 V_{IH} V_{IL}	 1.65 0		 V_{CC1} 0.30	 V V
Control logic current: High Low	 I_{IH} I_{IL}		 9 0.1		 µA µA

Figure 1 SKY65383-11 Recommended Operating Conditions (Source: SKY65383-11 Data Sheet, Table 4)

This table defines the nominal and allowable operating ranges for all key voltage domains. Of particular interest, **VREF1** and **VREF2** are specified to operate within a narrow tolerance band of **2.75 V** to **2.95 V**, with a typical value of **2.85 V**. This tight window implies the use of a precision LDO or regulator, and any switching mechanism must guarantee a stable and noise-free transition into this voltage level.

Table 5. SKY65383-11 DC Electrical Specifications[1]
(VCC1 = VCC2 = VCC4 = 3.3 V, VREF1 = VREF2 = 2.85 V, TA = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
VCC2 current, receive mode	ICC2	VREF1 = VREF2 = 0 V		5		mA
Quiescent current, transmit mode	ICQ	Current through VCC1 + VCC4		240		mA
Operating current, transmit mode	IOP	POUT = +30 dBm, current through VCC1 + VCC4		820		mA
PA reference current 1, transmit mode	IREF1			11	12	mA
PA reference current 2, transmit mode	IREF2			1	2	mA
All VCC current shutdown mode	IOFF	VREF1 = VREF2 = 0 V			1	µA

1 Performance is guaranteed only under the conditions listed in this table.

Figure 2 SKY65383-11 DC Electrical Specifications(Source: SKY65383-11 Data Sheet, Table 5)

Figure 2 illustrates the current consumption characteristics as a function of VREF state. When VREF is active (2.85 V), the PA reference stages draw a combined current of up to **14 mA**. Conversely, in shutdown or receive modes where VREF is explicitly required to be **0 V**, the total supply current drops to the µA range. This reinforces the need for accurate VREF control not only for functional behavior but also for power efficiency and thermal management.

Table 6. SKY65383-11 Electrical Specifications: Receive Mode[1]
(VCC1 = VCC2 = VCC4 = 3.3 V, VREF1 = VREF2 = 0 V, TA = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
ANT to Receive Output						
Small signal gain	G			12		dB
Noise figure	NF			2.5		dB
1 dB input compression point	IP1dB	1 dB gain compression		-12		dBm
Third order input intercept point	IIP3	PIN = -30 dBm/tone, 200 kHz spacing		-3		dBm
Input return loss	S11	@ ANT port		-10		dB
Output return loss	S22	@ TR port		-10		dB
Power-on time[3]	TPUP			5		µs
Transmit to receive switching time[2,3]				4		µs

1 Performance is guaranteed only under the conditions listed in this table.
2 This assumes that the TX and RX signal transitions are within 100 ns of each other.
3 Not production tested. Guaranteed by characterization.

Figure 3 SKY65383-11 Electrical Specifications: Receive Mode (Source: SKY65383-11 Data Sheet, Table 6)

Receive mode is defined under the condition that **VREF1 = VREF2 = 0 V**, effectively disabling the PA circuitry while maintaining full LNA performance. Ensuring the absence of any residual voltage on the VREF pins in this state is essential to prevent unintended current leakage or partial PA activation, which could degrade receive path sensitivity or violate isolation requirements.

Table 7. SKY65383-11 Electrical Specifications: Transmit Mode[1]
(VCC1 = VCC2 = VCC4 = 3.3 V, VREF1 = VREF2 = 2.85 V, T_A = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Transmit to ANT Path						
Output power	P_{OUT}			+30		dBm
Small signal gain	|S21|	P_{IN} = -20 dBm		34		dB
Power-added efficiency	PAE	Measured at ANT port		36		%
2nd harmonic[3]	2fo				-42	dBm/MHz
3rd to 10th harmonics[3]	3fo to 10fo				-42	dBm/MHz
Input return loss	S11	@ TR port		-7.5		dB
Output return loss	S22	@ ANT port		-10		dB
Non-harmonic spurious[3]	P_{SPUR}	VSWR 6:1, all phases			-40	dBm
Power-on time[3]	T_{PUP}			5		µs
Receive to transmit switching time[2,3]				800		ns
ANT to Receive Path						
Isolation	S21	Isolation between ANT and TR ports when in transmit mode	25	30		dB

1 Performance is guaranteed only under the conditions listed in this table.
2 This assumes that the TX and RX signal transitions are within 100 ns of each other.
3 Not production tested. Guaranteed by characterization.

Figure 4 SKY65383-11 Electrical Specifications: Transmit Mode (Source: SKY65383-11 Data Sheet, Table 7)

Transmit mode operation mandates the full activation of both VREF1 and VREF2 at 2.85 V. This activation enables the PA input and output stages, allowing the device to achieve its specified output power and efficiency metrics. Notably, the timing metrics, such as 800 ns switching delay between RX and TX, imply that the VREF application mechanism must be capable of fast, deterministic, and stable transitions, with minimal voltage overshoot or delay.

Considering the above specifications and operational constraints, it becomes evident that the controlled switching of the VREF voltage is not merely a design preference but a functional necessity. In systems where both RX and TX modes are dynamically utilized, the ability to enable and disable the PA stages through precise VREF control plays a critical role in maintaining signal integrity, minimizing power consumption, and ensuring proper mode transitions. Any residual voltage, noise, or timing misalignment on the VREF rails may lead to performance degradation or unintended behavior.

Therefore, identifying a reliable, efficient, and synchronized VREF switching topology is essential for robust system design.

Switching Topology Analysis

Topology A – MOSFET with Gate Driver and Boost Converter

In this topology, a dedicated gate driver and boost converter are used to ensure reliable switching of the reference voltage (VREF) through a MOSFET. The MOSFET plays a central role in selectively connecting the regulated 2.85 V rail to the VREF input of the front-end module. While logic-level N-channel MOSFETs such as the IRLML6344 can theoretically turn on at gate voltages around 2 V, directly driving them from a 3.3 V GPIO pin can lead to several limitations. Variations in gate threshold voltage across production batches may result in incomplete turn-on. Additionally, parasitic effects and noise on the gate line can further degrade switching reliability. Under such

conditions, the MOSFET may operate in a partially conducting region, causing increased power dissipation, slower edge transitions, or insufficient drive for the connected load. These risks are especially critical in timing-sensitive or RF-sensitive systems where VREF control must be precise and stable.

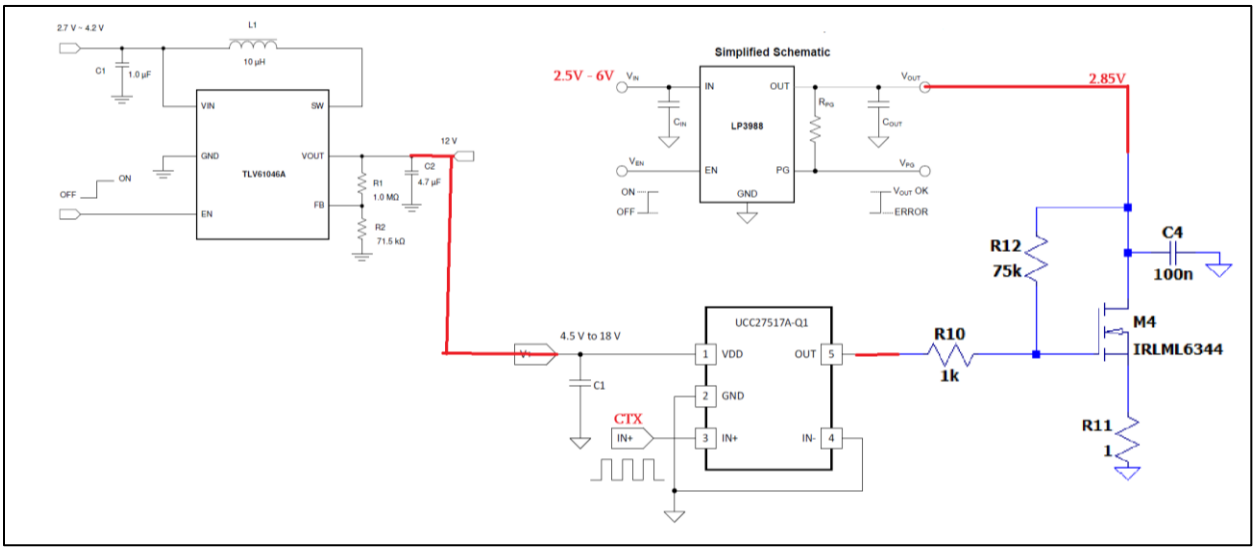

Figure 5 Topology A – MOSFET with Gate Driver and Boost Converter basic schematic

In light of these evaluations, the topology illustrated in Figure 5 adopts a structured architecture composed of a boost regulator, a dedicated gate driver, and a switching MOSFET. For the IRLML6344 MOSFET to generate the 2.85 V reference voltage required by the SKY65383 IC's VREF1 and VREF2 pins, the typical gate-source voltage (V_{GS}) specified in the datasheet must be approximately 4.5 V. Therefore, to ensure proper switching of the MOSFET, a minimum gate voltage of 7.35 V is required. This necessitates the use of a gate driver capable of delivering higher gate voltages.

As shown in the simplified schematic diagram, the UCC27517A, a single-channel, high-speed, low-side gate driver by Texas Instruments, is employed for this purpose. The driver exhibits rail-to-rail output characteristics, meaning the applied VDD voltage at the input is transferred nearly in full to the output (OUT pin). Considering the MOSFET's minimum gate drive requirements, the gate driver must be supplied with a voltage in the range of 8–12 V.

The IN+ input of the gate driver can be directly controlled via a microcontroller GPIO pin configured in push-pull modeDuring firmware implementation, when switching the SKY65383 IC into transmit mode, the ctx_vref GPIO pin must be driven HIGH in push-pull mode to enable the VREF supply.

Notably, the SKY65383 requires synchronized control signals within 100 ns during RX–TX mode transitions. As a result, the VREF voltage must be pre-established when transmit mode is initiated, which significantly emphasizes the importance of the switching performance of the MOSFET and gate driver.

Accordingly, the key switching characteristics of the MOSFET and gate driver are summarized in the table below.

Table 1 switching characteristics of the MOSFET and gate driver

	t_{on}	t_{off}
IRLML6344	~ 9.8 ns	~31.1 ns
UCC27517AQ1	~35 ns	~34 ns

Based on the results summarized in Table 1, the switching operation executed through the GPIO exhibits a T_{on} time of approximately 45 ns and T_{off} a time of around 46 ns.

Under 3.3 V input and 12 V output conditions, the TLV61046A boost regulator can supply a continuous output current of up to 70–80 mA. In our case, the total system load operating alongside the UCC27517A is approximately 66–70 mA. Accordingly, the regulator operates within an efficiency range of 75% to 78%.

$$I_{in} = \frac{I_{out} * V_{out}}{V_{in} * \eta} = \frac{70 * 12}{3.3 * 0.75} = \sim 380\text{mA}$$

Based on these values, the input current drawn by the boost regulator is estimated to be around 380 mA.

Test Plan for Topology A

To verify the functional integrity of the VREF switching mechanism implemented in Topology A, a system-level test plan was prepared based on key electrical checkpoints within the PCB.

Test Step	Test Point	Measurement/Method	Expected Value	Purpose/Justification
1	TP1: Boost Regulator Output	Measure VOUT with a multimeter at the 12 V rail	11.8 V – 12.2 V	Verifies if the gate driver receives a stable supply voltage
2	TP2: Gate Driver Output (OUT)	Measure output level using a DMM or oscilloscope during GPIO HIGH transition	V_G ≥ 7.5 V	Ensures MOSFET is driven into full saturation
3	TP3: Gate Driver Input (IN+)	Verify GPIO PWM or logic HIGH input level	Logic HIGH = 3.3 V	Confirms that the control signal reaches the driver properly
4	TP4: MOSFET Gate-Source Voltage V_{GS}	Measure $V_G - V_S$ with a DMM	≥ 4.5 V	Verifies gate drive amplitude for proper MOSFET conduction
5	TP5: VREF Output (Drain side)	Probe output side of MOSFET during ON/OFF switching	V_{ref} = 2.85 V ± 3%	Confirms that VREF is properly delivered to the front-end IC

Topology B – GPIO-Controlled LDO Enable Pin

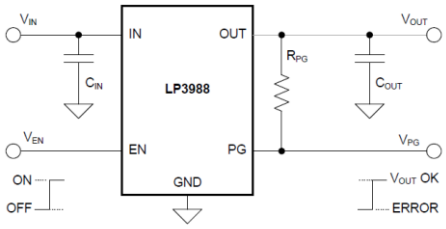

Figure 6 LP3988 simplified schematic

In Topology B, a fixed-output low-dropout (LDO) regulator is employed to provide the 2.85 V reference voltage required by the front-end module. The selected device, Texas Instruments' LP3988, offers a compact and efficient solution with ultra-low quiescent current, fast startup characteristics, and high supply rejection. Designed to operate with minimal external components and ceramic capacitors, the LP3988 ensures a clean and stable VREF rail while minimizing power consumption. Its enable pin allows software-controlled switching of the output, simplifying the architecture by eliminating the need for external switching elements.

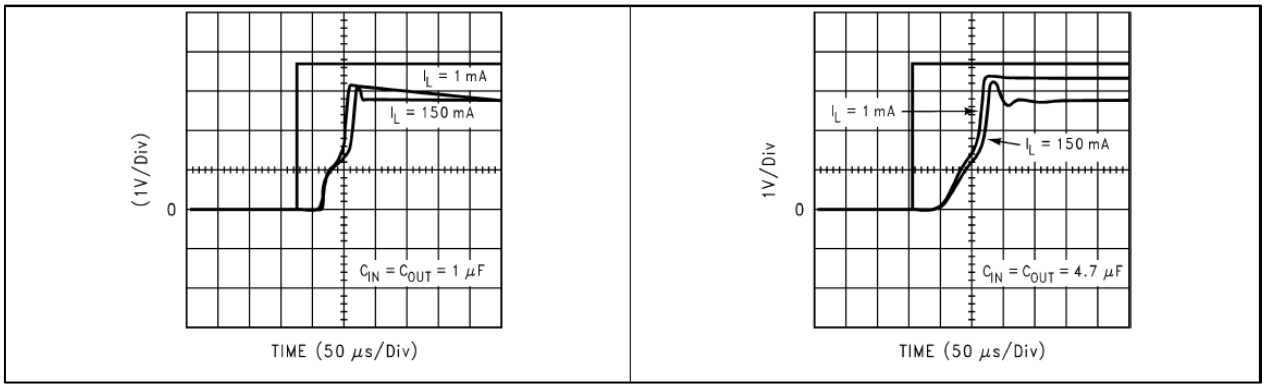

Figure 7 LP3988 Enable Response (Source: LP3988 Data Sheet)

According to the LP3988 datasheet, unless otherwise specified, the standard test conditions are: $C_{in} = C_{out} = 1uF \ \& \ 4.7uF \ ceramic \ cap, V_{in} = V_{out} + 0{,}2V$, $T_A = 25$ °C . Under these conditions, as shown in Figure 7 ("Enable Response"), the time required for the output voltage to reach 95% of its nominal value after the EN pin is asserted is approximately **80–100 µs**. This activation delay defines the effective VREF readiness time, which is critical in applications where synchronized enabling of RF front-end blocks is required. In addition, the turn-off time has been measured at approximately 30 µs, allowing for predictable deactivation of the voltage rail.

During full-load transmission (TX) mode, the SKY65383 module draws approximately 14 mA through its VREF pins. This reference voltage is supplied by the LP3988 LDO regulator from a 3.3 V source. Due to its linear architecture, the input current of the LP3988 closely matches its output current—approximately 14 mA in this case. With a 3.3 V input, this corresponds to an input power of around 46.2 mW, while the output delivers 2.85 V at 14 mA, totaling 39.9 mW. The resulting 6.3 mW power loss is dissipated as heat across the LDO. Given the relatively small magnitude of this

thermal loss, the LP3988 is not expected to experience significant temperature rise, ensuring stable and long-term operation of the system.

Test Plan for Topology B

Since the enable turn-on time of the LDO is sufficiently fast for the system requirements, it is sufficient to ensure that the output voltage remains within the range of 2.75 V to 2.90 V, with a typical value of 2.85 V.

Conclusion

Both proposed topologies were designed to ensure precise and reliable delivery of the 2.85 V reference voltage required by the SKY65383-11 front-end module.

The first topology, which consists of a boost converter, gate driver, and MOSFET, offers precise gate control, strong drive capability, and fast switching performance. This makes it suitable for systems where voltage margins are tight or where external noise immunity is critical.

The second topology, based on a fixed-output LDO regulator with a GPIO-controlled enable pin, significantly reduces design complexity and component count. It provides sufficient current capacity for the front-end module, maintains stable output voltage within the required tolerance, and minimizes switching delays thanks to its fast turn-on characteristics.

While both approaches are technically viable, unless ultra-fast switching is a critical requirement, the second topology provides a simpler, more compact, and power-efficient solution. For RF applications where board space, simplicity, and reliability are key concerns, the second topology is considered the more effective implementation.