EE3235 Analog Integrated Circuit Analysis and Design I
Homework 6
2-Stage Opamp with CMFB

Due date: 2023.12.27 (Wed.) 23:59 (upload to eeclass system)

Suppose V_{DD}=1.8V, temperature=25°C in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

In this homework, you are asked to build the circuit shown in Fig. 1, and the specifications you need to meet are listed in Table. 1. Please make sure your circuit meets all specs in TT, FF, and SS corners.

Please note that, there's no restriction on how to design the **CM SENSE** and **CMFB** blocks, if only the common-mode feedback loops are stable; however, you are welcomed to refer to Fig. 5. for a basic implementation.

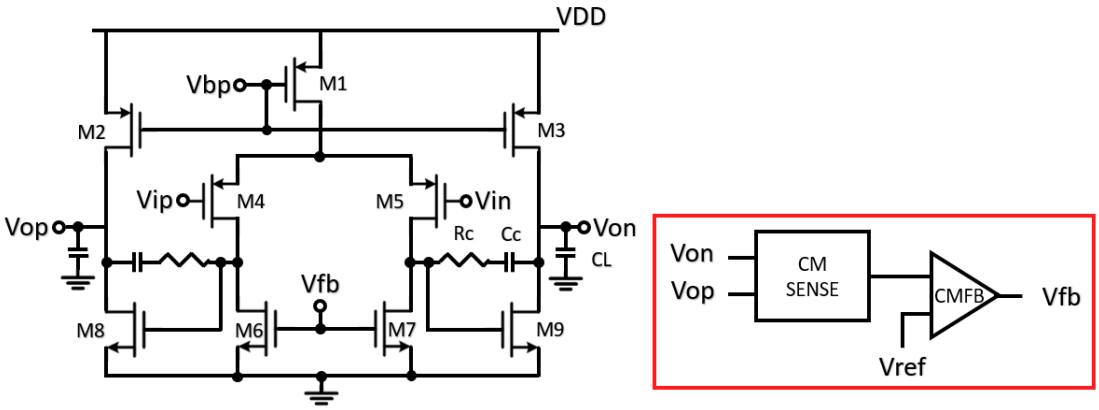

Fig. 1. 2-Stage Opamp with Common Mode Feedback.

Parameters	Specification	This Work		
		TT	FF	SS
Supply Voltage (V)	1.8			
Temp. (°C)	27			
Loading Cap. (pF)	1			
Output CM Voltage @ Vin,cm=0.8V (V)	0.9±20mV			
Open Loop Gain (dB)	> 70			
GBW (MHz)	> 5			
Phase Margin (degree)	> 60			
Input Common Mode Range (V)	≥ 1			
Power Consumption (uW)	< 50			

Table. 1. Specification and Performance

1. Elaborate on your design strategy, including how you intend to meet each specification and how you determine the size of the transistors. Please note that, every design strategy must come from certain reasonable inferences or calculations, no SPICE monkeys are allowed in the class!

2. From fig. 1, we can observe a common-mode feedback loop in this circuit. Please analyze the loop by hand, the content must include the breakdown of the entire loop gain and also the distribution of poles.

3. Compare the SPICE simulation result with the hand analysis you do in question number 1, and explain what causes the error between the simulation and your calculation (at least include open loop gain, GBW, and Power Consumption).

4. Run the **ac** simulation to make sure your common-mode feedback loop is stable. Please note that the content must include the graph of gain and phase margin. Hints are provided in Fig. 4.

5. Run the transient simulation. Insert an input signal with an amplitude of 0.1mVpp and set the initial value of both output nodes to 0V. Observe whether, after a period of time, the output common mode stabilizes back to 0.9V±20mV.

6. Sweep input common-mode voltage to make sure your input CM range meet the spec.

7. Neatly list the sizes of all transistors, capacitance of the compensation capacitors and resistance of the compensation resistors.

How to measure the ac response of a CMFB loop

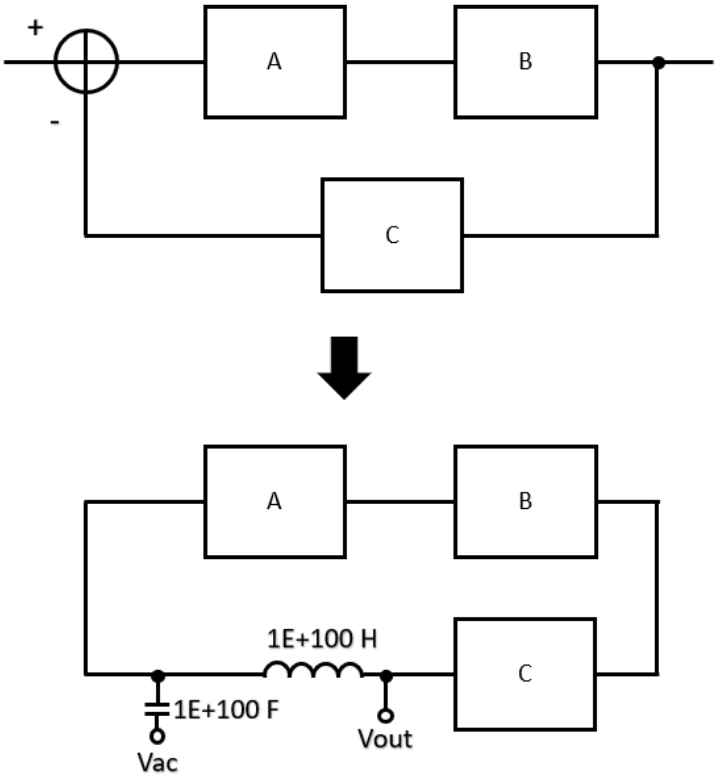

Fig. 4. Frequency Analysis of a Feedback Loop

R-Sense CMFB loop

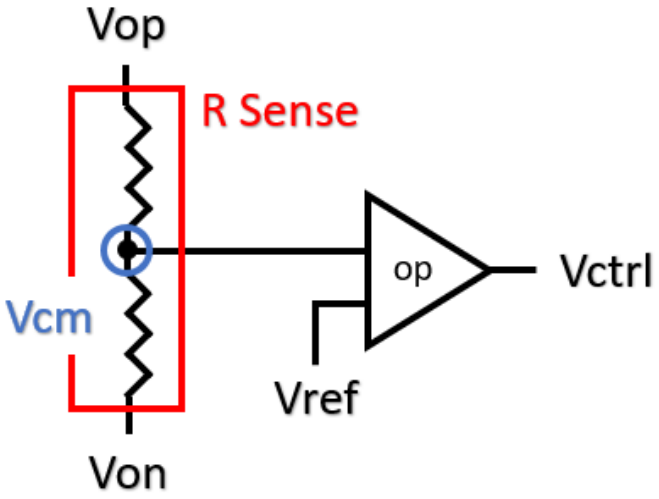

Fig. 5. R-Sense Common-Mode Feedback Loop