112 Fall EE3235 Analog Integrated Circuit Analysis and Design I

Homework 5 Operational amplifier with resistive feedback

Due date:2023.12.13(Wed.) 23:59 (upload to eeclass System)

In the last homework, you have simulated the performance of closed-loop ideal operational amplifier(opamp). This homework is to design an opamp with resistive feedback as shown in Fig.1, which the amplifier here is a real opamp. The architecture of opamp is shown in Fig.2, which is a low-voltage telescopic cascode amplifier. The problem sets include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.

Finally, we want to have the closed-loop gain $10 \pm 0.2(V/V)$ in Fig. 1. In this homework, please use V_{DD}=1.8V, temperature=25^{o}C.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report in **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include the output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

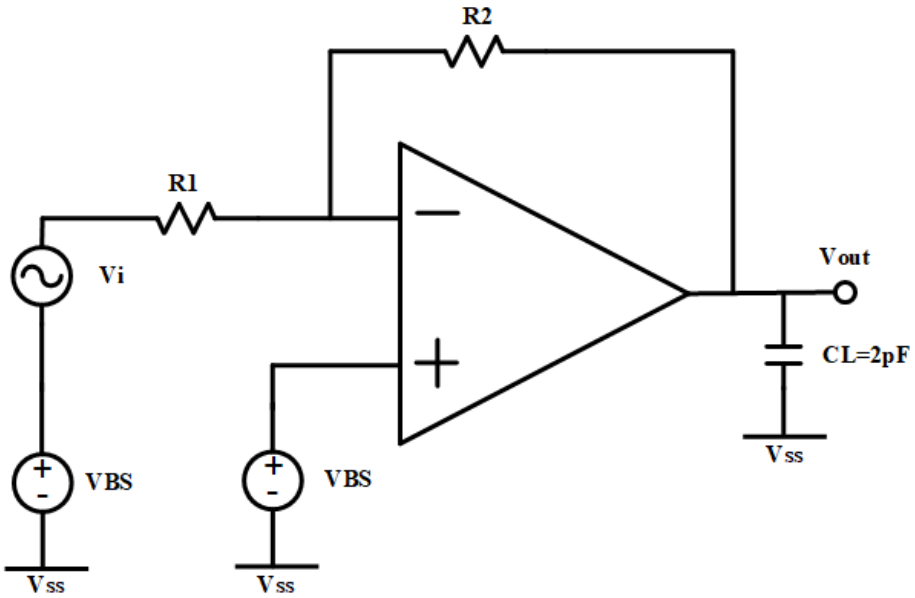

Fig. 1. operational amplifier with resistive feedback

We divide the design procedure into two parts. PART1 is to design the operational amplifier. PART2 is to add the feedback resistors R_1、R_2 as in Fig. 1. and the ratio of $R_1$and R_2 (that is $\frac{R_2}{R_1}$) should be 10. When doing simulation in each part, the loading capacitance in output is CL=2pF.

(Suggest: pmos body connect to VDD；nmos body connect to VSS)

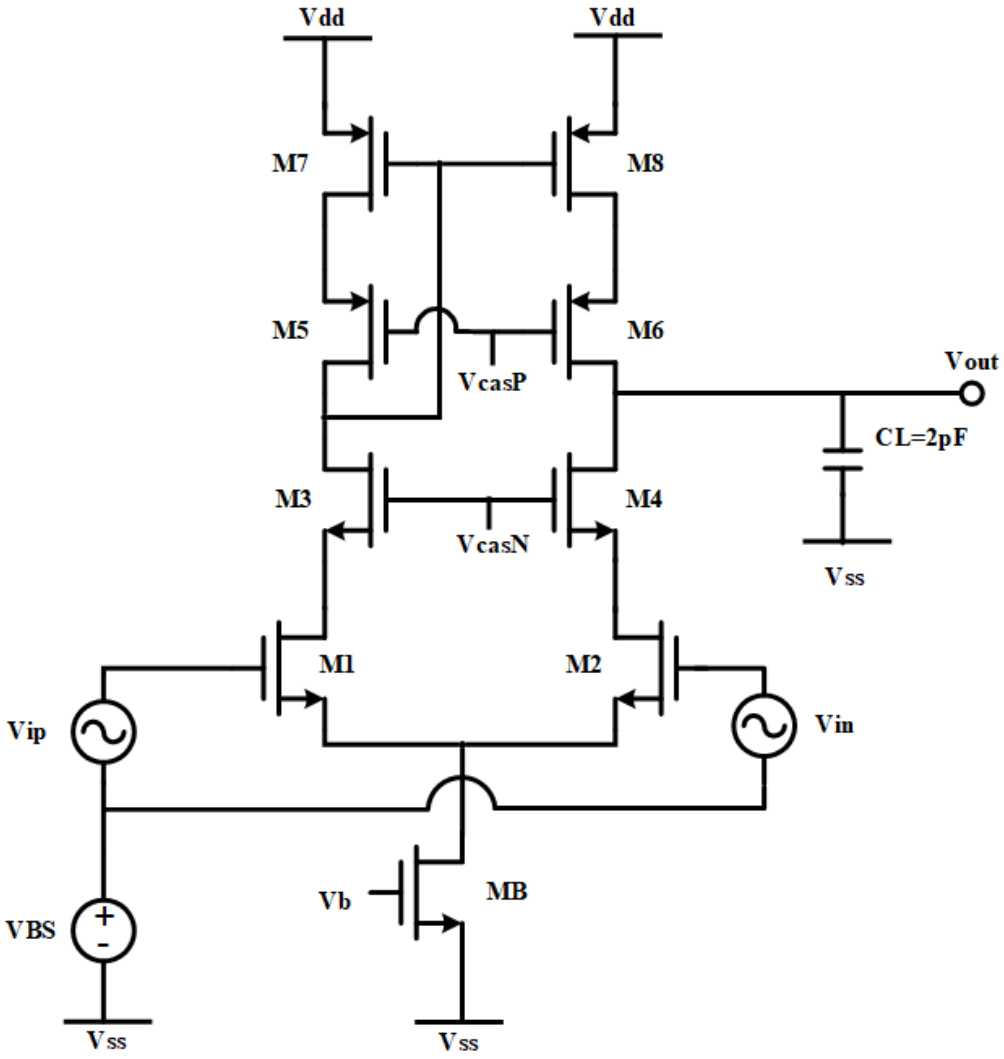

Fig. 2. Architecture of operational amplifier

PART1: open-loop simulation			
Working Item	Specification	Simulation	Calculation
Tail current	(uA)		
gain(Vout/(Vip-Vin))	Gain you need to derive(dB) (You need to fill this blank)		
Input common mode	V_{BS}(V)		
Tail current bias	V_b(V)		
-3dB Bandwidth	>7k Hz		
Power dissipation	(uW)		
PART2: closed-loop simulation as Fig. 1			
Working Item	Specification	Simulation	Calculation
Closed-loop gain (Vout/Vi)	$10 \pm 0.2\ (V/V)$		

Table. Summary table

PART1：Design the amplifier in Fig. 2

1. Ideal operational amplifier simulation

Before you diving into circuit design, please use the ideal opamp to do the simulation. The purpose of simulation is to find the gain, which makes you achieve the specification of gain error($\pm 0.2\ V/V$). Please attach the screenshot of your simulation to the report.

2. Circuit Design

Please design the device size of transistor M1-M8、MB, and the bias voltage VBS, Vb, VcasP and VcasN, to make the small differential signal voltage gain (Vout/(Vip-Vin)) larger than the gain you derive in the last step. Make sure all transistors operate in saturation region. Please print out the small-signal parameters of active devices from the list file. Please write down your design flow.

3. Differential Mode

Please run .tf. And compare the gain value with hand calculation using the small-signal parameters from question 1.

4. Frequency Response/Pole and zero

The small-signal -3dB bandwidth of differential-mode signal has to be larger than 7k Hz. Please simulate and plot the differential mode frequency response of this gain stage. And use .pz to simulate and mark the poles/zeros on this curve. Compare with hand calculation.

5. Specification

Remember to fill the table1 and the PART1 simulation result to summary table

Device Size			
M1 (W/L, m)		M5 (W/L, m)	
M2 (W/L, m)		M6 (W/L, m)	
M3 (W/L, m)		M7 (W/L, m)	
M4 (W/L, m)		M8 (W/L, m)	
MB (W/L, m)		----------	----------

Table1

Note：Please use .op to print out the power like Fig. 5 , filling the value into summary table and attach the screenshot to your report.

```
total voltage source power dissipation=   27.4399u       watts
```

Fig. 3 Power dissipation

Note：Please fill the summary table with the flat-band gain in frequency response, i.e. the gain in frequency=0Hz.

PART2：add resistive feedback as Fig. 1

Connect the feedback loop. Use R_1 and R_2 as feedback, and the ratio of $R_1$and R_2 (that is$\frac{R_1}{R_2}$) should be 10. Plot the frequency response of open-loop and closed loop and answering the following question.

1. Please discuss how you determine the value of $R_1$and R_2.

2. Observe the frequency response, you will see the gain change after we connect the feedback loop. Please mark the flat-band gain in both two curves and hand calculate the gain change($\frac{A.open\_loop}{A.closed\_loop}$), the flat-band gain after closed-loop as well as gain error.
   Hint: If your simulation is correct, you will see the two curves behave as Fig. 4.

3. Closed-loop gain is obviously lower than open-loop gain. Then, why we need the feedback loop? How it favors our needs ?

4. Observe the frequency response. How is the dominant pole change after connecting feedback loop? And hand calculate the dominant pole after connecting feedback loop.(The error is NOT important, just want you all to know how the pole changes.)

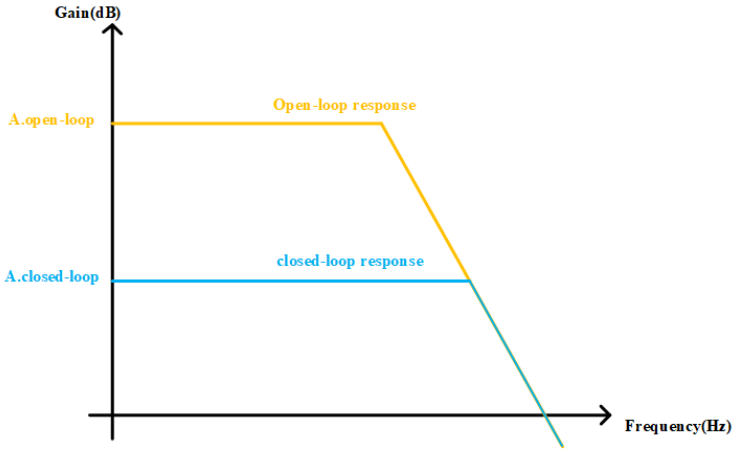

Fig. 4. Result of frequency response

Grading policy:

- PART1：
  1. Finish the ideal opamp simulation(5%)
  2. Finish simulation and attain specification.(5%)
  3. Report of PART1(50%)
- PART2：
  1. Finish simulation and attain specification(5%)
  2. Question1(5%)
  3. Question2(10%)
  4. Question3(5%)
  5. Question4(10%)
- Ranking： (5%)

  Please upload your performance in PART1 simulation to the following website, and the FoM will be calculate as

$$FoM(Figure\ of\ Merit) = \frac{gain(dB)}{Power(uW)}$$

Website：

https://docs.google.com/spreadsheets/d/18csLdedOZSiWoRc3yryum3do3FKd7mviunmTBMS4awg/edit#gid=0

Fill the Power dissipation(uW) and gain(dB) in the table as well as your student ID

Please round your power and gain to the nearest tenth(四捨五入至小數點後第一位)				
fill your name and performance below				
Name(Student ID)	Power(uW)	gain(dB)	FoM	Rank
TA1	27.4	62.6	2.3	1
TA2	30.7	60.8	2	2

Reference hspice code

Use in	Code reference
Differential input	Vcm vcm vss dc=0.9 Vdiff vdiff vss dc=0 ac=1 Ep vip vcm vdiff vss 0.5 En vin vcm vdiff vss -0.5
Gain measurement	.tf V(Vout) Vdiff
Pole / zero	.pz V(Vout) Vdiff
*AC response measurement	.AC DEC 10 1 1G .probe AC vdb(vout) vp(vout) .measure AC gain_db MAX Vdb(vout) .measure AC Bandwidth when Vdb(vout)='gain_db-3'

* Notice that：when you use the command of "AC response measurement", please make sure your frequency response is flat, not the case in Fig. 5. The frequency response in Fig. 5 **doesn't mean that you are wrong**.

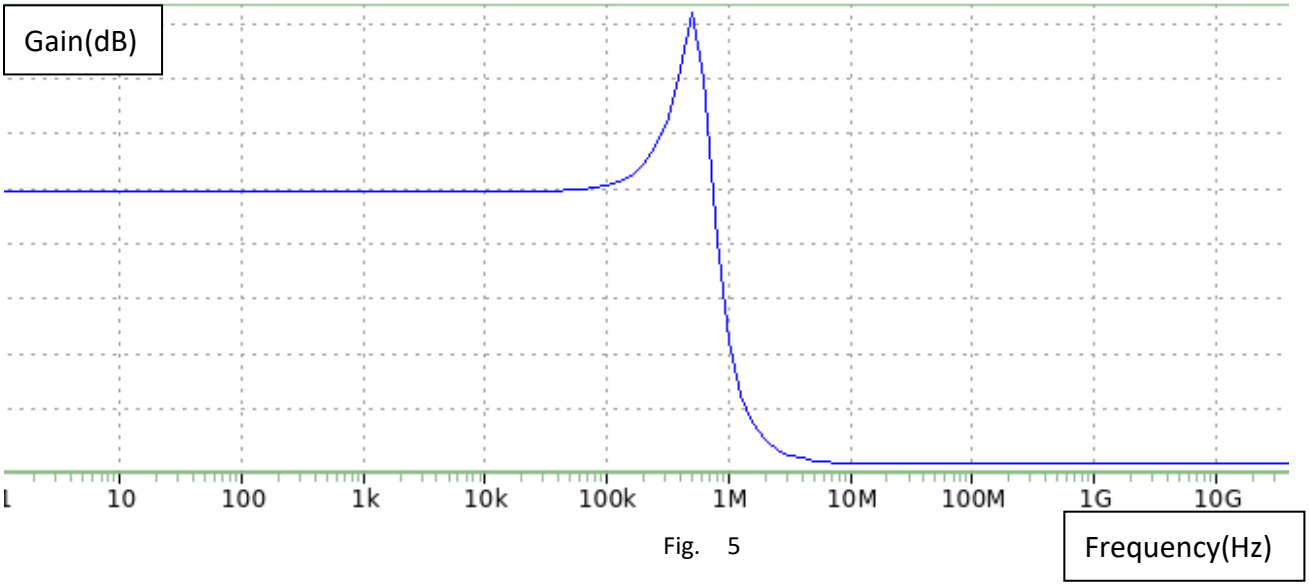

Fig. 5