Single Slope ADC

1. Introduction to analog to digital converter(ADC):

Analog to digital converter(ADC) is an essential block in the majority of chips nowadays, which plays a role as interface between real signal(analog) and digitized signal(digital). There are many types of ADC, such as Single Slope ADC, Dual Slope ADC, Pipelined ADC, Time Interleave ADC, Successive Approximation Register(SAR) ADC, Flash ADC and so on. Different types of ADC are of different advantages. Single Slope ADC is famous for its small area and simple design. And in this final project, we will use the Single Slope ADC to digitized the signal.

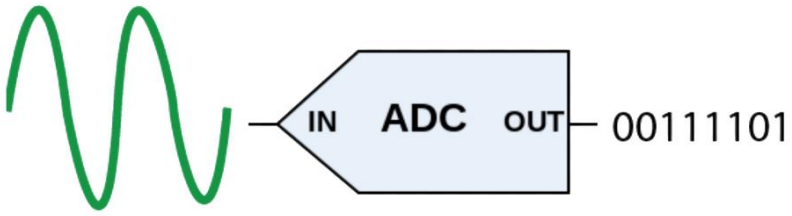

Fig. 1. ADC Concept Diagram

2. Introduction to Single Slope ADC(SSADC)

2-1 Block diagram of single slope ADC(SSADC)

The simplest block diagram of a SSADC is shown in Fig. 2. It consists of a sample&hold circuit, a comparator, a NAND3, a 6 bits digital counter and 6 latches.

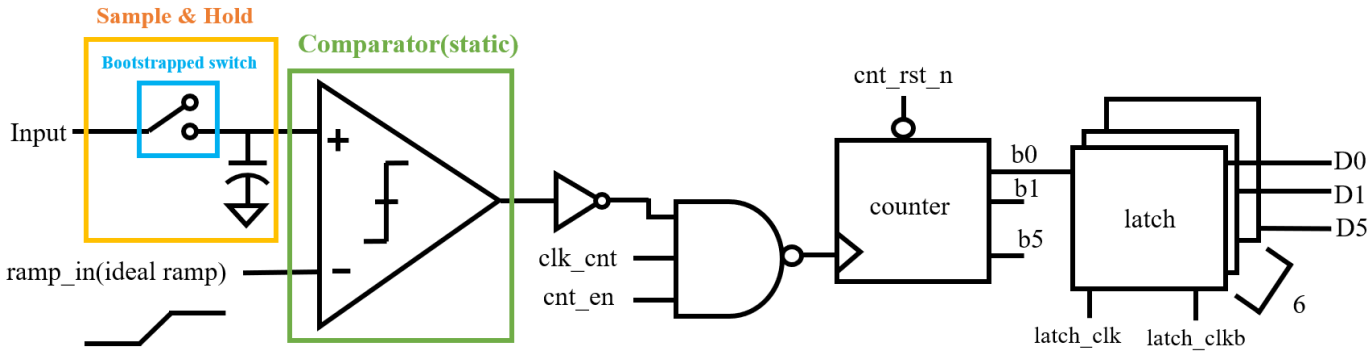

Fig. 2. Block diagram of Single Slope ADC(SSAD)

The following are the explanation of signal

(1) `Input : We will use sine wave to test the accuracy of the SSADC.`
(2) `clks : The sampling clock.`
(3) `ramp_in : An ideal ramp signal used in SSADC.`
(4) `clk_cnt : The clock for counter (counting frequency).`
(5) `cnt_en : The 'enable' signal for the counter.`
(6) `latch_clk, latch_clkb : The clock for latches to store the output of the counter.`

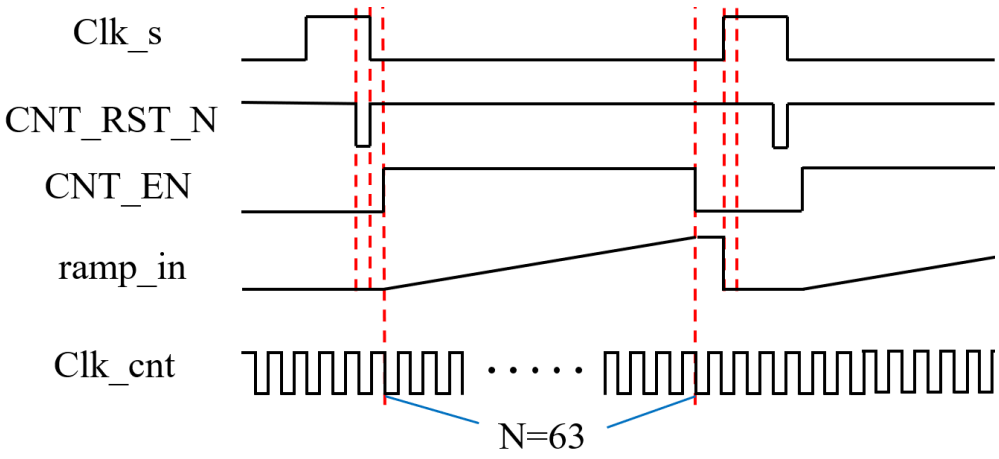

Fig. 3. Timing diagram of Single Slope ADC(SSADC)

2-2 Blocks of a SSADC

S/H:

The main function of a S/H circuit is to retain the input signal's value at the sampling moment until the subsequent sampling instance. As shown in Fig. 4, when the clock signal (clks) is high, the sample and hold circuit continuously samples the input signal; when the clock is low, it preserves the value obtained during the high clock phase. Its fundamental structure involves a bootstrapped switch, depicted in Figure 5.

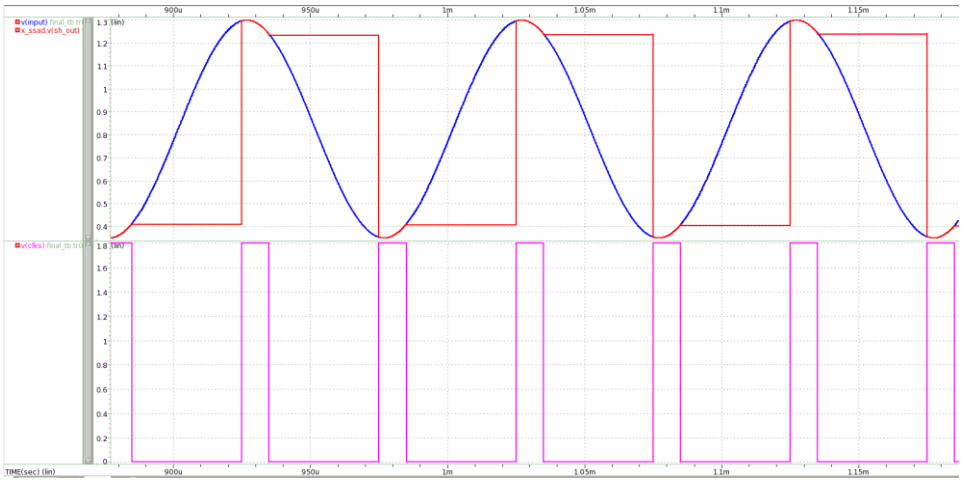

Fig. 4 waveform of sample and hold

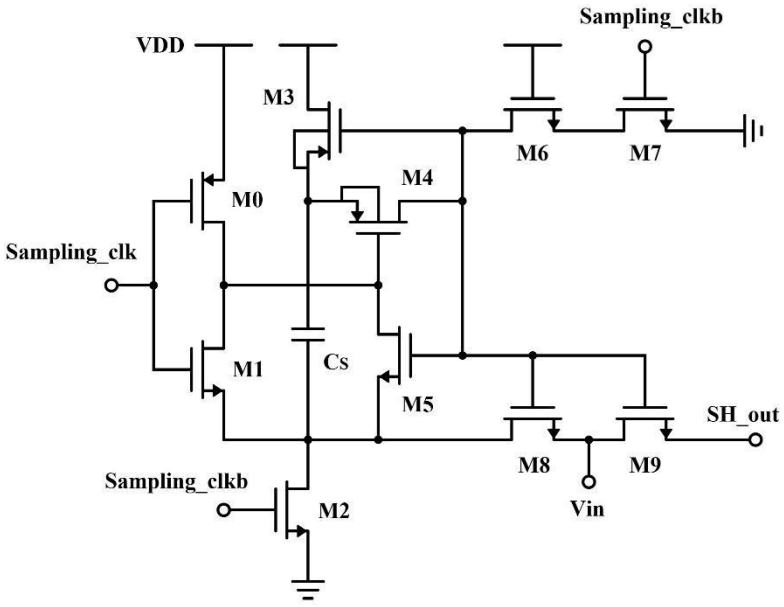

Fig. 5 architecture of bootstrapped switch

Ramp generator :

The ramp generator produces a signal that linearly increases with the increment of the counter, as illustrated in Figure 6.

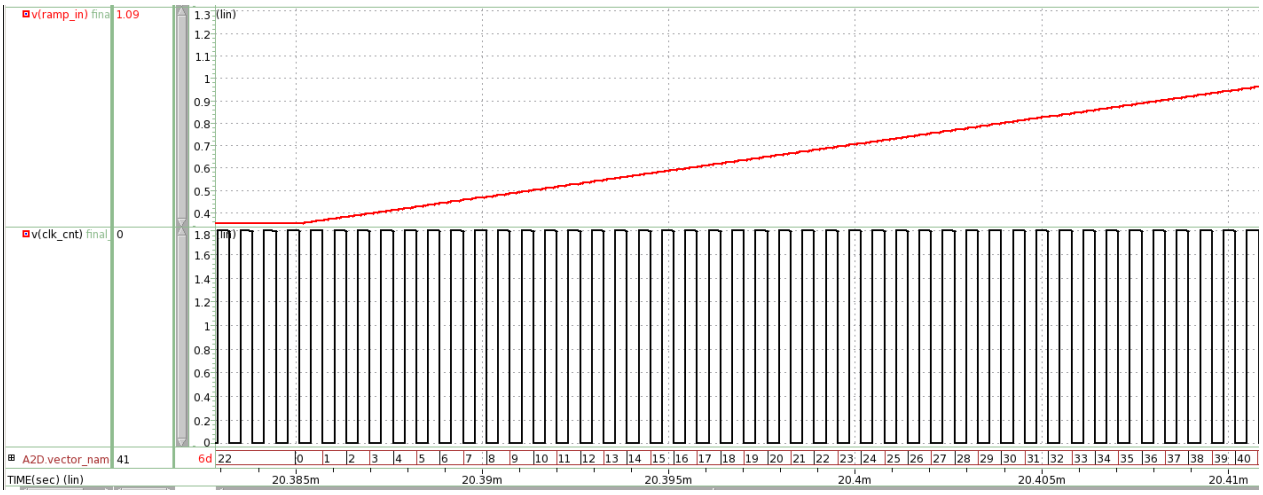

Fig. 6 waveform of ramp generator

Comparator :

A comparator is a circuit that compares two analog voltage signals and produces an output based on the relationship between these voltages. Its primary function is to determine which input voltage is greater and then provide a corresponding digital output based on that comparison.

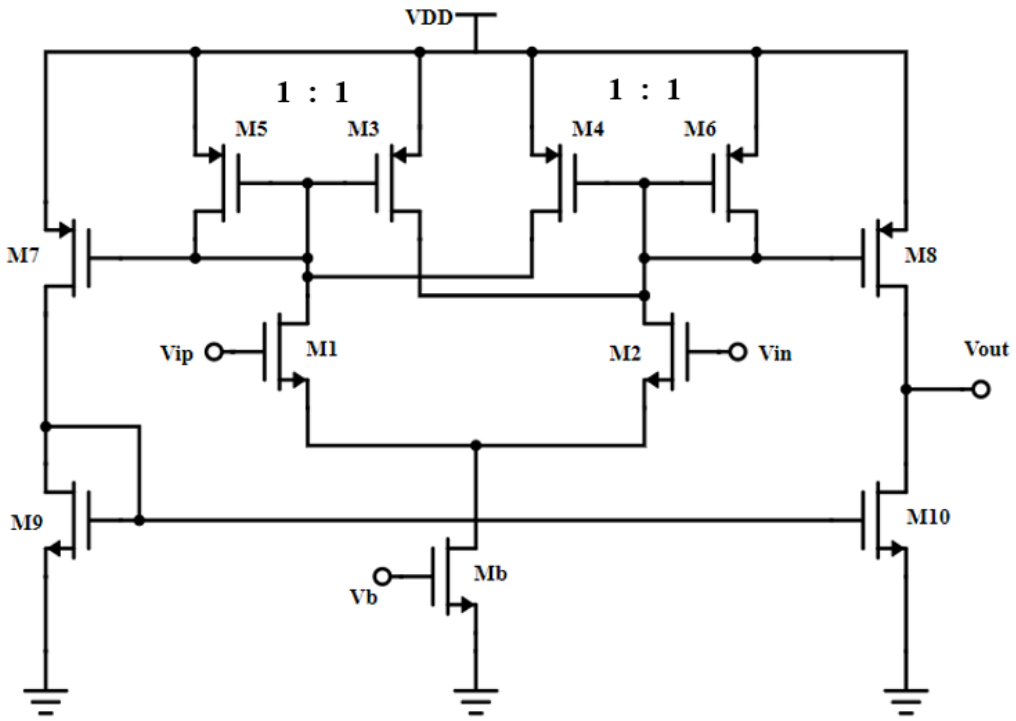

Fig. 7 architecture of comparator

Digital counter(6bits) :

The digital counter increments its value in response to specific trigger (counter_clk), and it resets to 0 when rst_n is logic “0”. The schematic is illustrated in Fig 8.

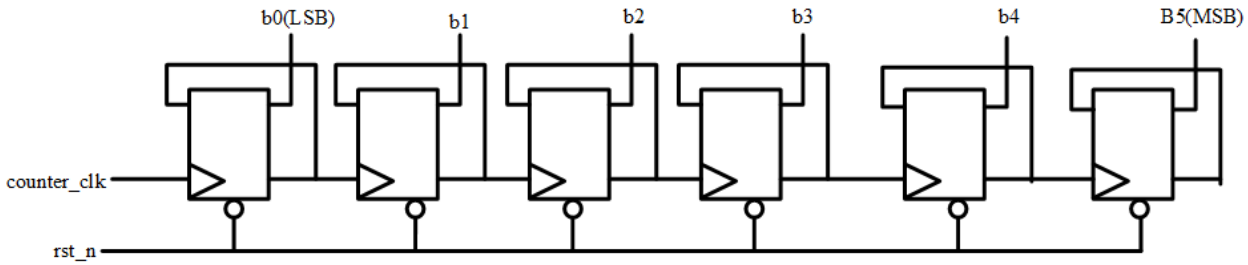

Fig 8. architecture of Digital counter

Latches(6bits) :

Latch is responsible for memorizing the final digital value obtained by the SSADC. Configured as illustrated in Fig 9.

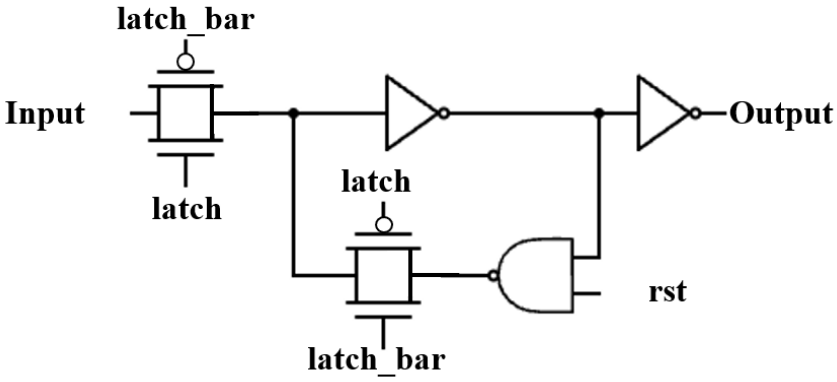

Fig 9. architecture of Latch

2-3 The operating mechanism of SSADC

When clks is logic “0”, the S/H will sample the input value. After the S/H records the input value, the digital counter's value increases with each clk_cnt cycle, as illustrated in Figure 10.

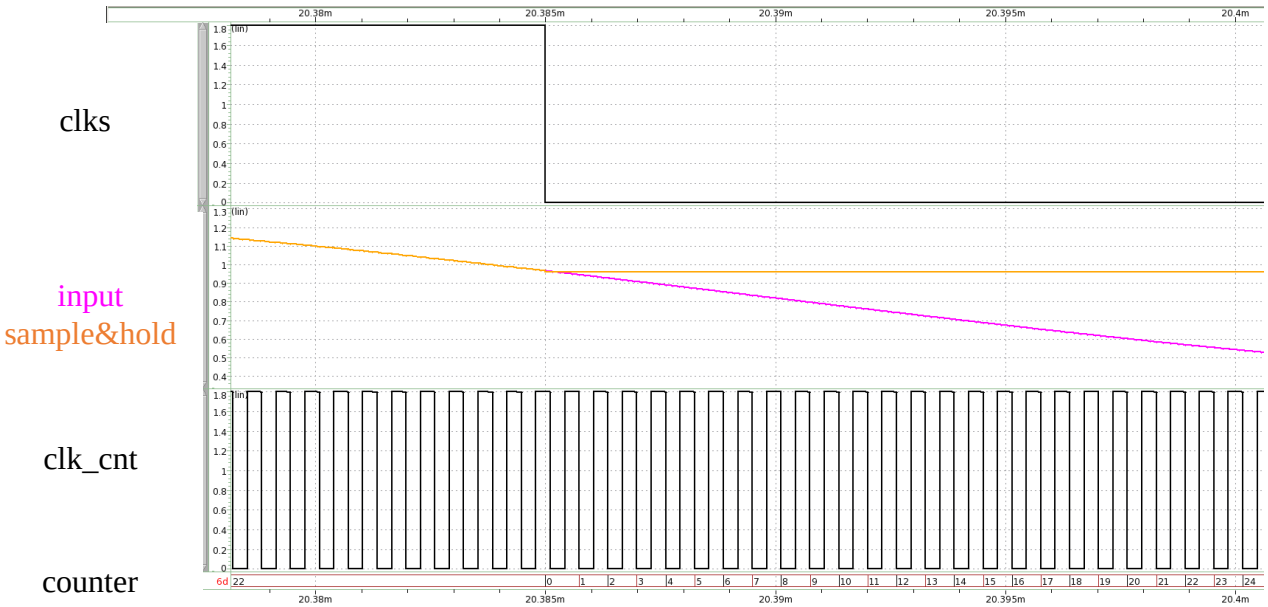

Fig 10. waveform of SSADC

The output signal of the digital counter is transmitted to the ramp generator, and the value of the ramp monotonically increases with the counter. The sampled input signal is then compared with the ramp voltage by the comparator. When ramp voltage exceeds the sampled input signal, the comparator's output switches from “0” to “1”, causing the counter to stop counting, as illustrated in Figure 11.

And at that moment, the value of the counter will be stored in memory and represented as the digital value output of the sampled input signal.

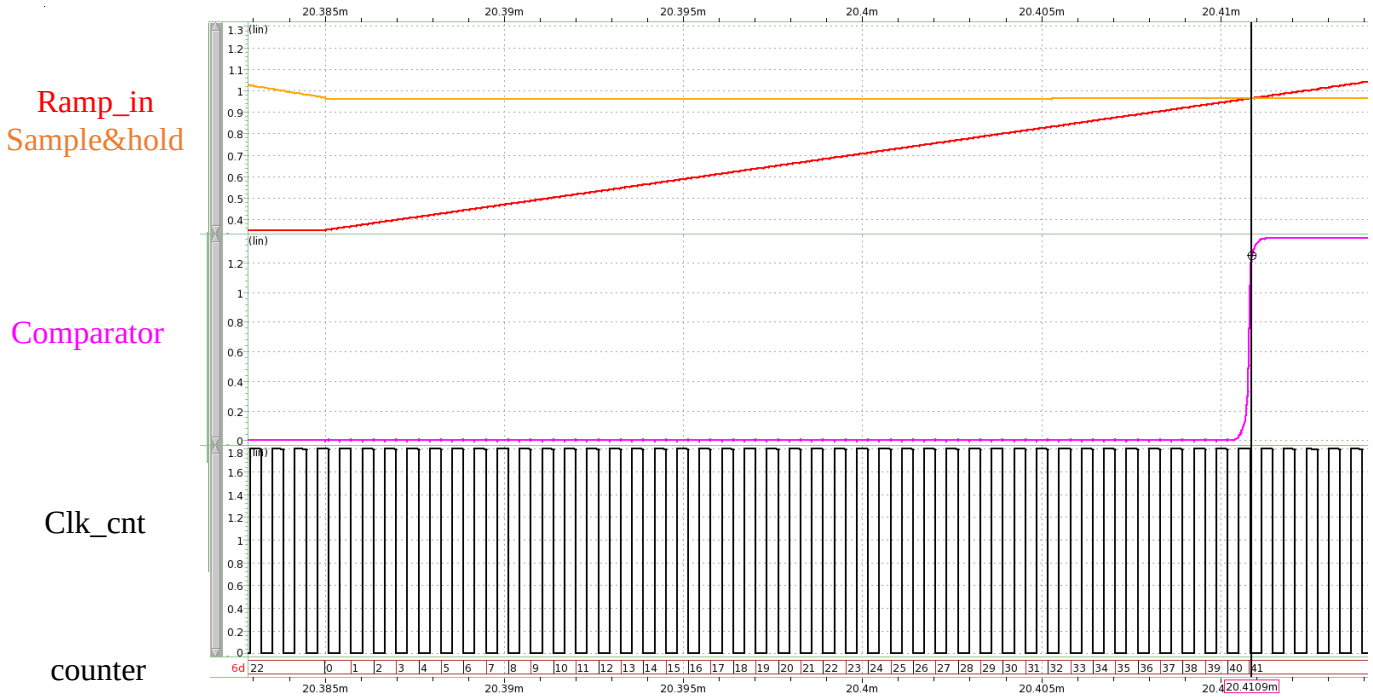

Fig 11. waveform of SSADC