EE3235 Analog Integrated Circuit Analysis and Design I

Homework 3

Cascade Amplifier

Due date: 2023.11.15 (Wed.) 13:20 (upload to eeclass system)

Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

Part I – Cascade Amplifier

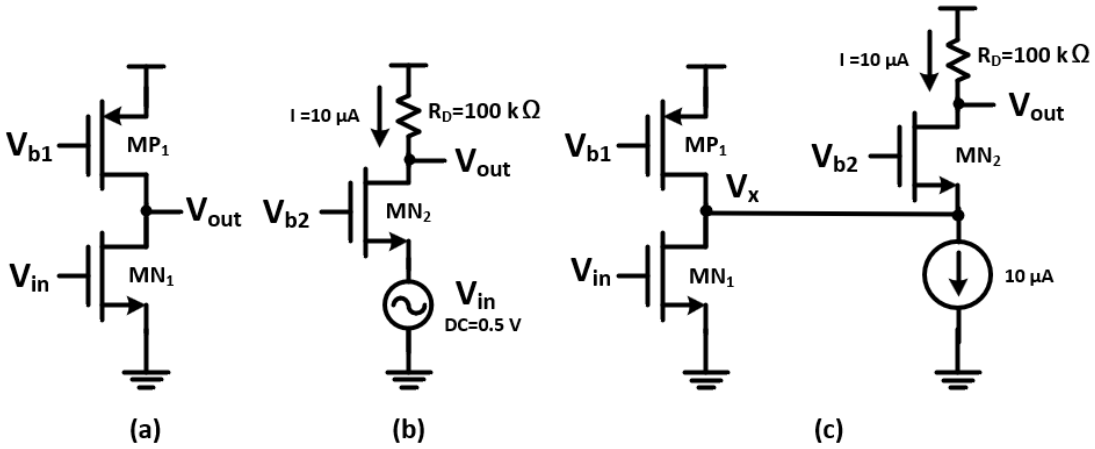

Fig. 1 (a) Common source amplifier. (b) Common gate amplifier (c) Cascade amplifier

All MOS should be operated in saturation region.

(a). Design a common source amplifier with gain $A_1 > 100$ (v/v) and output DC voltage = 0.5 V (only ±10mV V_{out} error is permitted) as shown in Fig. 1(a) . Describe how you design Vin, Vb1 and the size of MOS in detail.

(b). Please use .tf and .op command to print out the gain and small signal parameter. Please hand-calculate the gain value using SPICE parameters and compare it with the simulation result.

(c). Design a common gate amplifier with gain $A_2 > 15$ (v/v) and input DC voltage = 0.5 V (static current = 10μA, 5% error is permitted) as shown in Fig. 1(b).

(d). Please use .tf and .op command to print out the gain and small signal parameter. Please hand-calculate the gain value using SPICE parameters and compare it with the simulation result.

(e). Connect two stage and add additional 10μA current source as shown in Fig. 1(c).

i. Whether the DC bias (Vx) stay the same? Print out the operating point from .lis file.

ii. Please use .tf command to print out the gain. The over all gain equals to $A_1 \times A_2$ or not ? If not, why not ?

(f). Please use .pz command to plot the frequency response of the cascade amplifier. Based on the simulation result of .lis file (or .pz0), mark the **poles, zeros, unit-gain bandwidth** and **-3dB bandwidth** on the curve.

(g). Compare the **dominate pole** with hand-calculation.

(h). Finish the performance table.

Table I Perforamance Table

Work Item	Unit	Specification	Simulation	Calculation
Vdd	V	1.8		
	Common Source Amplifier			
Vin	V	-		
Vb1	V	-		
Vo	V	0.5		
Gain($\lvert A_1 \rvert$)	V/V	> 100		
	Common Gate Amplifier			
Vin	V	0.5		
Vo	V	-		
I	μA	10		
Gain($\lvert A_2 \rvert$)	V/V	> 15		
	Cascade Amplifier			
Vin	V	-		
Vx	V	0.5		
Vo	V	-		
Gain ($\lvert A_1 \times A_2 \rvert$)	V/V	> 1		
Dominate Pole	MHz	> 40		
Unit Gain Bandwidth	MHz	> 70		

(f) 題參考指令

```
.ac dec 10 1 100G
.pz v(vo) vi                                  $ find pole and zero
.probe vdb(vo) vp(vo)                         $ plot ac gain and phase response
.meas ac dcgain_in_db max Vdb(vo)             $ find max ac gain
.meas ac BW when Vdb(vo) = 'dcgain_in_db-3'   $ find bandwidth
.meas ac UGB when Vdb(vo)=0                   $ find UGB
```

(g) 題參考指令

```
.option captab                                $ list node capacitance
```