# **EE3235** Analog Integrated Circuit Analysis and Design I

# Homework 2 Elementary Gain Stages

Due date: 2023.10.25 (Wed.) 23:30 (upload to eeclass system)

Suppose V<sub>DD</sub>=1.8V, temperature=25°C, TT corner in this homework.

#### Please note that:

- 1. No delay allowed.
- 2. Please hand in your report using eeclass system.
- 3. Please generate your report with **pdf** format, name your report as HWX studentID name.pdf.
- 4. Please hand in the spice code file (.sp) for each work. Do not include output file.
- 5. Please print waveform with white background, and make sure the X, and Y labels are clear.
- 6. Please do not zip your report.

### Part I - Common Source Amplifier

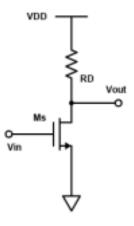


Fig. 1. Common source amplifier.

In part I, as shown in Fig. 1, you are to run HSPICE and design a common source amplifier with the SPEC shown in Tab. I. Note that  $V_{out}$  is required to be biased at 0.8V (only  $\pm 10$ mV  $V_{out}$  error is permitted).

TABLE I COMMON SOURCE PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
$V_{\mathrm{DD}}$	1.8V	1.8V	1.8V
$V_{in,DC}$	0.8V	0.8V	0.8V
$V_{\mathrm{out,DC}}$	0.8V		
Gain A <sub>V</sub>	> 3.2(V/V)		
$R_{D}$	< 90ΚΩ		-
$I_D$	$< 30 \mu A$		-
$M_S$ W/L	-		-

## (1) DC Swee

Please probe  $V_{out}$  v.s.  $V_{in}$  and measure the derivative of  $V_{out}$  when  $V_{in}$  is 0.8V.

## (2) TF Analysis

Please run the following command in HSPICE to measure the I/O impedance and DC gain  $A_v$ . Is  $A_v$  close to the result in (1)? Why?

## (3) Hand Calculation and Discussion

Show your operating point list in the report.

Calculate the DC gain,  $V_{out,DC}$ , and output impedance  $R_{out}$ , finish Tab. I and compare the simulation result with your hand calculation.

How do you design your common source amplifier to meet the SPEC? Describe your design considerations.

#### Part II - Common Gate

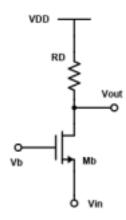


Fig. 2. Common gate.

In part II, as shown in Fig. 2, you are to run HSPICE and design a common gate stage with the SPEC shown in Tab. II. Note that  $V_{out}$  is required to be biased at 0.9V (only  $\pm 10 \text{mV}$   $V_{out}$  error is permitted).

TABLE II

COMMON GATE PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
$V_{\mathrm{DD}}$	1.8V	1.8V	1.8V
$V_{in,DC}$	0.16V	0.16V	0.16V
$V_{\mathrm{out,DC}}$	0.9V		
Gain A <sub>V</sub>	> 10(V/V)		
$R_D$	< 90ΚΩ		-
$I_D$	$< 30 \mu A$		-
$V_{\rm b}$	-		-
$M_b$ W/L	-		-

# (1) DC Sweep

Please probe  $V_{out}$  v.s.  $V_{in}$  and measure the derivative of  $V_{out}$  when  $V_{in}$  is 0.16V.

# (2) TF Analysis

Please run .tf analysis in HSPICE to measure the I/O impedance and DC gain  $A_v$ . Is  $A_v$  close to the result in (1)? Why?

### (3) Hand Calculation and Discussion

Show your operating point list in the report.

Calculate the DC gain,  $V_{out,DC}$ , and I/O impedance  $R_{in}$ ,  $R_{out}$ , finish Tab. II and compare the simulation result with your hand calculation.

How do you design your common gate stage to meet the SPEC? Describe your design considerations.

#### Part III - Source Follower

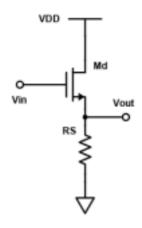


Fig. 3. Source follower.

In part III, as shown in Fig. 3, you are to run HSPICE and design a source follower with the SPEC shown in Tab. III. Note that  $V_{out}$  is required to be biased at 0.8V (only  $\pm 10$ mV  $V_{out}$  error is permitted).

TABLE III
SOURCE FOLLOWER PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
$V_{\mathrm{DD}}$	1.8V	1.8V	1.8V
$V_{in,DC}$	1.6V	1.6V	1.6V
$V_{\mathrm{out,DC}}$	0.8V		
Gain A <sub>V</sub>	>0.75(V/V)		
$R_{\mathcal{S}}$	< 90ΚΩ		-
$I_D$	$< 30 \mu A$		-
$M_d$ $W/L$	-		-

# (1) DC Sweep

Please probe  $\left.\partial V_{out}/\left.\partial V_{in}\right.\right.$  v.s.  $V_{in}$  and describe your observation.

# (2) TF Analysis

Please run .tf analysis in HSPICE to measure the I/O impedance and DC gain  $A_{\nu}$ .

### (3) Hand Calculation and Discussion

Show your operating point list in the report.

Calculate the DC gain,  $V_{out,DC}$ , and Output impedance  $R_{out}$ , finish Tab. III and compare the simulation result with your hand calculation.

How do you design your source follower to meet the SPEC? Describe your design considerations.