112 Fall EE3235 Analog Integrated Circuit Analysis and Design I

Final Project

Due date:2024.01.15 (Mon.) 23:59 pm (upload to eeclass System)

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report in **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the designated spice code file (.spi) for each work. Do not include the output file.
5. Please print waveform with white background, and make sure the X and Y labels are clear.
6. Please do not zip your report.

In this project, you are to design and analyze an 6-bit analog-to-digital converter(ADC) combined with a bandgap reference as the supply, the system architecture is shown in Fig. 1.

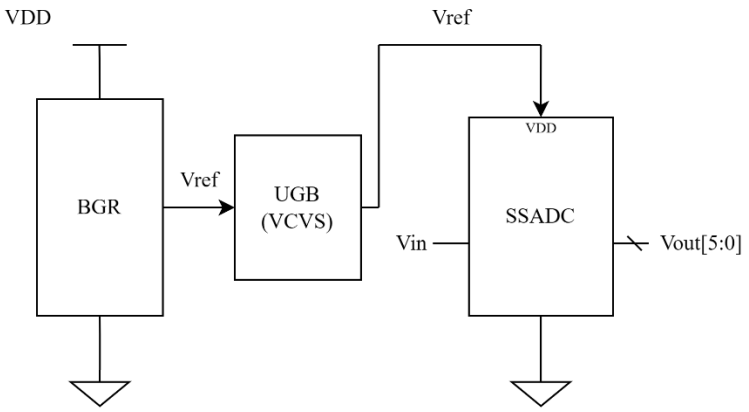

Fig. 1. ADC and bandgap reference.

PART I – Bandgap Reference

Bandgap reference circuits are widely used to generate a 'temperature-independent' voltage supply for power-sensitive circuits. For **PART I**, please design a bandgap reference circuit based on the schematic shown in Fig. 2, and finish the whole design step by step. Finally, fill out Tab. 1., and try to meet all specifications.

You'll need bipolar transistors to generate the temperature-independent reference voltage, please ues PNP_V50X50 or PNP_V100X100 in cic018.l, the command is:

Qname	Collector	Base	Emitter	Bulk	Model_Name	m=Multiplier

Note that only PNP is available in cic018.l, and the bulk should always be connected to GND.

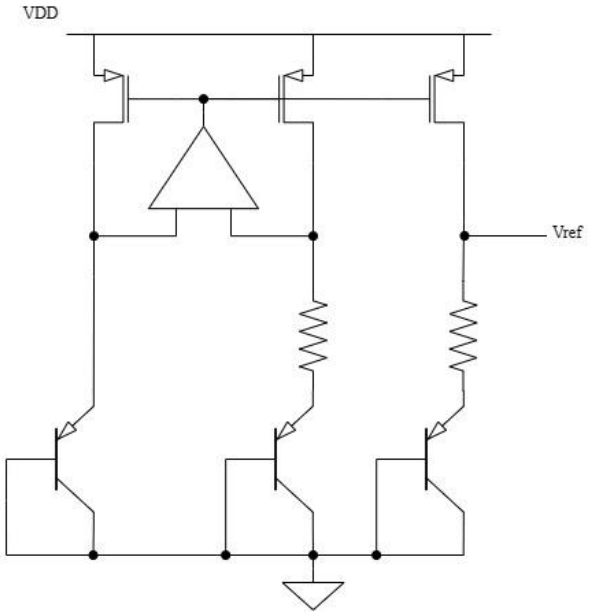

Fig. 2. Opamp-based BGR.

Bandgap Reference							
Working Item	SPEC			Your Work			
Supply Voltage V_{DD}	1.98V	1.8V	1.62V		1.98V	1.8V	1.62V
T.C. from -40~125°C	< 20ppm/°C			TT			
				SS			
				FF			
Bandgap Voltage (V)				TT			
V_{DD}	1.8V, -40~125°C						
PSR @ DC	< −40dB			TT			
				SS			
				FF			
PSR @ 10KHz	< −30dB			TT			
				SS			
				FF			
V_{DD}	1.8V, 27°C, TT						
Power Consumption (μW)	< 50μW						

Tab. 1. Bandgap reference SPECs

1. Design Consideration

In this part, you are asked to analyze the whole circuit based on the specifications given.

(a) Determine the ratio of the two resistors through calculation, and calculate the expected Vref.

(b) Given the power consumption limitation, arrange the total current you can use carefully; by doing so, you can determine the absolute value of the two resistors, and also be able to design the opamp based on the current budget you set.

(c) PSR (Power Supply Rejection) is an important indicator for evaluating the quality of a bandgap reference circuit. Please analyze the aspects through which PSR can be improved and how the gain of the opamp would affect PSR. Use proper calculation and analysis to establish the specifications for the opamp.

(d) Design the opamp based on the structure shown in Fig. 3. and Fig. 4. and also the analysis you did in the previous parts.

(e) Complete the whole bandgap reference circuit design.

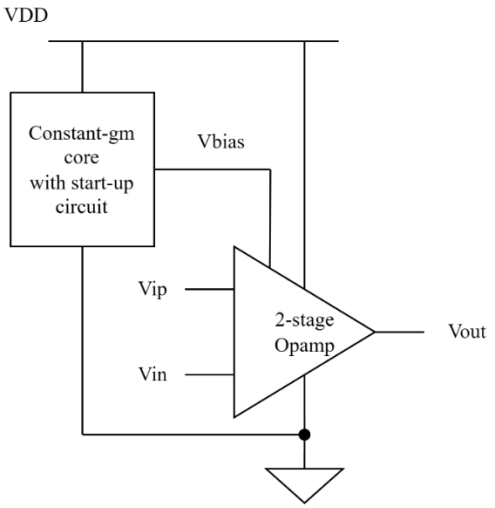

Fig. 3. Operational amplifier with constant-gm biasing

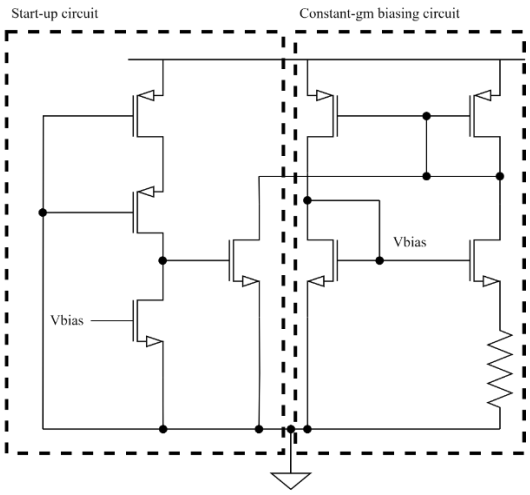

Fig. 4. Constant-gm core with start-up circuit

2. Simulation Result

In this part, please run simulation to check whether you meet all specs, compare the result with what you designed or what you expected, and also elaborate on what you observe from the simulation results . Please note that all of the simulation results must be accompanied with waveform plots.

(a) .DC

- Sweep VDD from 0V to 1.98V
- Sweep the temperature from -40°C to 125°C to derive the temperature coefficients.

$$\text{Temp. Coeff. (T. C.)} = \frac{1}{V_{ref}} \times \frac{V_{max} - V_{min}}{T_{max} - T_{min}}$$

(b) .Tran

- Use the following command to check the start-up condition and ensure that the reference voltage is indeed stable.

```
VDD VDD GND pwl(0 0    10u 0    100u 2)
.tran 0.01u 110u
```

(c) .AC

- Identify the main feedback loop and test the loop stability by the method in HW6.
- Measure the PSR under different corners and temperatures.

3. SPICE code submission

Netlist file of your circuit should look like:

```
.subckt bgr VDD VSS Vref
…
.ends
```

No additional pins are allowed, and also don't change the order of the pins. Otherwise, you will have zero score because we cannot run HSPICE with your netlist.

PART II – Single Slope ADC (SSADC)

Single Slope ADC is a type of ADC with a small area and simple design. For more information, please refer to Attachment 1. For **PART II**, please utilize the Vref generated by the bandgap reference designed in Part I as the power supply voltage to design the Single Slope ADC. The block diagram of the Single Slope ADC is illustrated in Fig. 5. Most of the blocks have already been provided to you; your task is to design the comparator and set the range for the ramp. Finally, use the provided Matlab code to measure the Effective Number of Bits (ENOB) and complete Table 2.

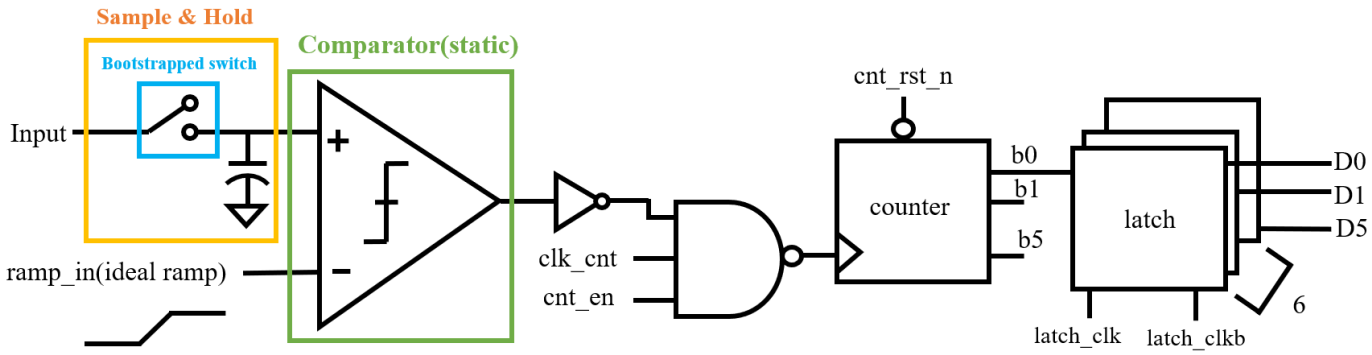

Fig. 5. The block diagram of the Single Slope ADC

Introduction to the system's signals

(1) Input：We will use sine wave to test the accuracy of the SSADC.

(2) clks：The sampling clock.

(3) ramp_in：An ideal ramp signal used in SSADC.

(4) clk_cnt：The clock for counter (counting frequency).

(5) cnt_en：The 'enable' signal for the counter.

(6) latch_clk, latch_clkb：The clock for latches to store the output of the counter.

Bandgap Reference + SSADC						
Working Item	SPEC			Your Work		
Single Slope ADC input range	$0.95V_{ref}$~$0.25V_{ref}$ (Round to the second decimal place.)					
Supply Voltage V_{DD}	1.8V	1.62V	1.98V	1.8V	1.62V	1.98V
Sampling rate	20kHz					
ENOB	> 5bits					

Tab. 2. Bandgap reference + SSADC SPECs

Note! Measuring the ENOB for both 1.98V and 1.62V does not require modifying the SSADC's input range.

1. Design Consideration

In this part, you are asked to analyze and design the comparator, as depicted in Figure 6.

(a) Please observe the operation of the SSADC and discuss the operational requirements that the comparator must meet (e.g. settling time, input range...).

(b) Complete the design of the comparator (An opamp connected with an inverter chain) and describe your design in detail, including the schematic, operation points of all the transistors (you should draw your schematic and mark the DC voltage and current on it), and how you run the simulations. For you reference, a basic implementation is shown in Fig. 6.

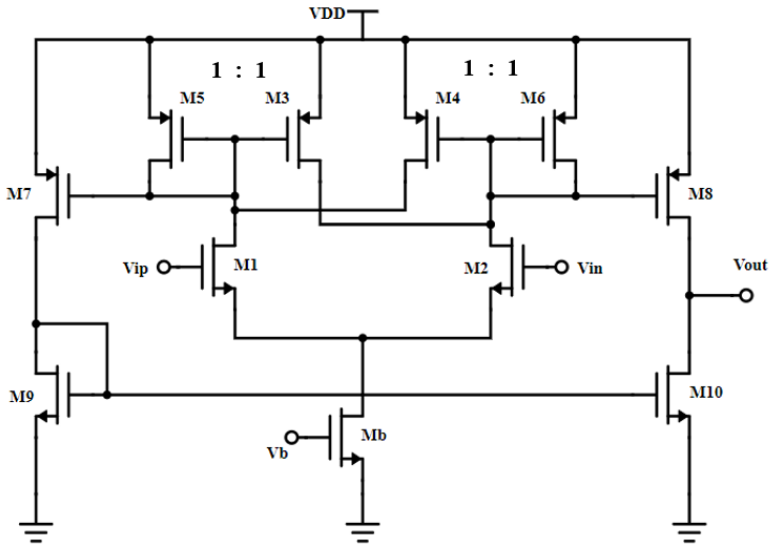

Fig. 6. architecture of Comparator

2. SPICE code submission

Netlist file of your circuit should look like:

```
.subckt cmp Vdd Vss Vb Vip Vin Vout
…
.ends
```

No additional pins are allowed, and also don't change the order of the pins. Otherwise, you will have zero score because we cannot run HSPICE with your netlist.

3. Measure the ENOB

In this part, you will utilize the provided 'final_tb.sp' file to run the .tran simulation and use WaveView to export waveform simulation data. Finally, use the MATLAB code we provided to calculate ENOB. Refer to Attachment 2 for detailed instructions.

PART III – Experience Sharing

Hello everyone, congratulations on completing this semester's course. We hope everyone has gained valuable knowledge throughout the semester.

For the final part, please share what you've learned from this course and provide suggestions for improvement. Wishing you all a happy winter break!