



112-1 SoC Design Laboratory

Lab1 submission guide

Teacher : Jiin Lai

TA : 陳揚哲



Lab1 Contents

- Xilinx tool installation on VM ubuntu (If you have install VMWare, skip it)
 - Install Oracle VM VirtualBox 6.1.42 and Extension pack
 - Refer to [Ubuntu_VM_on_Windows](#) Page.2
 - Install Xilinx suite tool (vitis, vitis_hls, vivado)
 - Refer to [Vitis_on_Ubuntu_VM](#)
- Complete course-lab_1
 - Export multip_2num IP
 - Deploy on PNYQ-Z2 / KV260
 - [OnlineFPGA manual](#)
- Report
- [course-lab_1 github](#)



Tool Installation

- The screenshot of Xilinx tools
 - Check your tool version

```
ubuntu@ubuntu2004: ~/Desktop
ubuntu@ubuntu2004:~/Desktop$ vitis
***** Xilinx Vitis Development Environment
***** Vitis v2022.1 (64-bit)
**** SW Build 3524922 on 2022-04-14-18:00:18
** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.

ubuntu@ubuntu2004:~/Desktop$ vitis_hls
***** Vitis HLS - High-Level Synthesis from C, C++ and OpenCL v2022.1 (64-bit)
**** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
**** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.

source /tools/Xilinx/Vitis_HLS/2022.1/scripts/vitis_hls/hls.tcl -notrace
INFO: [HLS 200-10] Running '/tools/Xilinx/Vitis_HLS/2022.1/bin/unwrapped/lnx64.o
/vitis_hls'
INFO: [HLS 200-10] For user 'ubuntu' on host 'ubuntu2004.linuxvmimages.local' (L
inux_x86_64 version 5.15.0-76-generic) on Wed Sep 06 11:55:03 EDT 2023
INFO: [HLS 200-10] On os Ubuntu 20.04.4 LTS
INFO: [HLS 200-10] In directory '/home/ubuntu/Desktop'
INFO: [HLS 200-10] Bringing up Vitis HLS GUI ...

ubuntu@ubuntu2004:~/Desktop$ vivado
***** Vivado v2022.1 (64-bit)
**** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
**** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.

start_gui
```



Co-Simulation Log

- Co-simulation log (TopFunctionName_csim.log)
 - Transcript of your testbench
- Usually located at VitisHLSProjectName/solution1/csim/report

```
INFO: [SIM 2] ***** CSIM start *****
INFO: [SIM 4] CSIM will launch GCC as the compiler.
Compiling ../../../../../../hls_Multiplication/MultiplierTester.cpp in debug mode
Compiling ../../../../../../hls_Multiplication/Multiplication.cpp in debug mode
Generating csim.exe
>> Start test!
-----
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
-----
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
-----
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
-----
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
```



Synthesis Report

- Synthesis Summary Report (csynth.rpt)
 - Summary report of your IP
- Synthesis Detail Report (TopFunctionName_csynth.rpt)
 - Detailed reports of your top function and sub-function
- Usually located at VitisHLSProjectName/solution1/syn/report

<pre>===== == Vitis HLS Report for 'multip_2num' ===== * Date: Wed Jun 28 20:35:44 2023 * Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022) * Project: hls_ip * Solution: solution1 (Vivado IP Flow Target) * Product Family: zynq * Target device: xc7z020-clg400-1 ===== == Performance Estimates ===== * Timing: * Summary: Clock Target Estimated Uncertainty ----- ----- ----- ----- ap_clk 10.00 ns 6.912 ns 2.70 ns * Latency: * Summary: Latency (cycles) Latency (absolute) Interval Pipeline min max min max min max Type ----- ----- ----- ----- ----- ----- ----- 3 3 30,000 ns 30,000 ns 4 4 no * Detail: * Instance: N/A * Loop: N/A ===== == Utilization Estimates ===== * Summary: Name BRAM 18K1 DSP FF LUT URAM ----- ----- ----- ----- ----- ----- ----- multip_2num 0 0 0 0 0 0 </pre>	<pre>===== == Synthesis Summary Report of 'multip_2num' ===== * General Information: * Date: Wed Jun 28 20:35:44 2023 * Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022) * Project: hls_ip * Solution: solution1 (Vivado IP Flow Target) * Product Family: zynq * Target device: xc7z020-clg400-1 ===== * Performance & Resource Estimates: ===== PS: '*' for module; 'o' for loop; '**' for dataflow Modules Issue Latency Latency Iteration Trip Pipeline BRAM DSP FF LUT URAM & Loops Type Slack (cycles) (ns) Latency Interval Count ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- * multip_2num - 0.39 3 30,000 - 4 - no 3 (1K) 409 (-0K) 307 (-0K) - ===== == HW Interfaces ===== * S_AXILITE Interfaces Interface Data Width Address Width Offset Register ----- ----- ----- ----- ----- s_axi_control 32 6 16 0 * S_AXILITE Registers Interface Register Offset Width Access Description Bit Fields ----- ----- ----- ----- ----- ----- ----- s_axi_control n32In1 0x10 32 W Data signal of n32In1 s_axi_control n32In2 0x18 32 W Data signal of n32In2 s_axi_control pn32ResOut 0x20 32 R Data signal of pn32ResOut s_axi_control pn32ResOut_ctrl 0x24 32 R Control signal of pn32ResOut 0=pn32ResOut_ap_vld ===== * TOP LEVEL CONTROL Interface Type Ports ----- ----- ----- s_axi_control IP 0 </pre>
---	--



Bitstream and Hardware Handoff

- Bitstream (.bit)

- Contains the programming information for FPGA device
- Usually located at :
 - VivadoProjectName/ VivadoProjectName.runs/impl_1/design_1_wrapper.bit

```
> vwd_Multip2Num > vwd_Multip2Num.runs > impl_1
```

```
design_1_wrapper.bit
```

- Hardware Handoff (.hwh)

- Contain block design information and is used by software tools to a targeted application
- Usually located at :
 - VivadoProjectName/VivadoProjectName.gen/sources_1/bd/design_1/hw_handoff/design_1.hwh

```
> vwd_Multip2Num > vwd_Multip2Num.gen > sources_1 > bd > design_1 > hw_handoff
```

```
design_1.hwh
```



Online FPGA Remote Login

- We have set up some PYNQ-Z2/KV260 boards in the lab. You can use them remotely
- Refer to OnlineFPGA使用者手冊_20230620.pdf
- IP : 140.112.207.200 : 1000
- Specify username : boledupynq
- password : boledupynq



Lab1 Submission File

- Folder Hierarchy:
 - StudentID_lab1/
 - Lab1/
 - screenshot of Xilinx tool installation (.jpg, .png)
 - .hwh, .bit (generated from vivado)
 - csynth.rpt, xxx_csynth.rpt, xxx_csim.log (generated from vitis_hls)
 - report.pdf
 - Compress all above files in a single zip file named **StudentID_lab1.zip**
 - Submit to NTHU eeclass
 - **Deadline : 9/21 (Thr.) 23:59**
 - 30% off for the late submission penalty



Report

- Brief introduction about the overall system
- What is observed & learned
- Screen dump
 - Performance
 - Utilization
 - Interface
 - Co-simulation transcript/waveform
 - Jupyter Notebook execution results



TA Information

- Yang-Che Chen / 陳揚哲 / bb890825@gmail.com
- TA session: Mon. 16:00 ~ 17:00
- Location: Delta 839