112-1 SoC Design Laboratory Lab1 submission guide
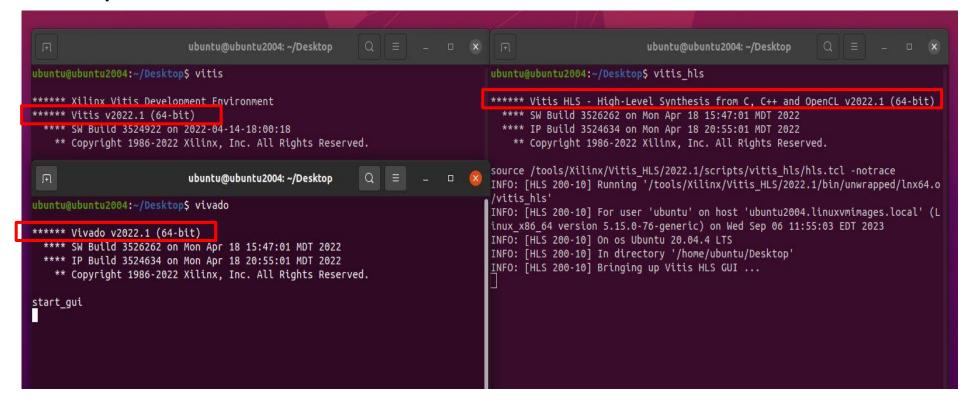
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TA：陳揚哲

Lab1 Contents

- Xilinx tool installation on VM ubuntu (If you have install VMWare, skip it)
  - Install Oracle VM VirtualBox 6.1.42 and Extension pack
    - Refer to Ubuntu_VM_on_Windows Page.2
  - Install Xilinx suite tool (vitis, vitis_hls, vivado)
    - Refer to Vitis_on_Ubuntu_VM

- Complete course-lab_1
  - Export multip_2num IP
  - Deploy on PNYQ-Z2 / KV260
    - OnlineFPGA_manual

- Report

- course-lab_1 github

Tool Installation

- The screenshot of Xilinx tools
  - Check your tool version

Co-Simulation Log

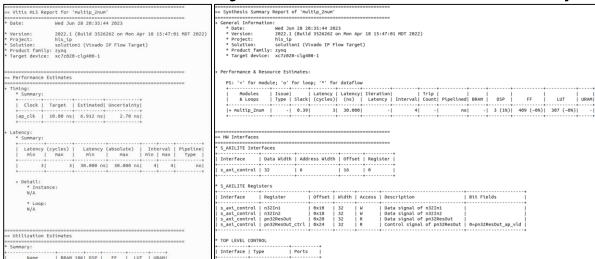- Co-simulation log (TopFunctionName_csim.log)
  - Transcript of your testbench
- Usually located at VitisHLSProjectName/solution1/csim/report

```
INFO: [SIM 2] ************** CSIM start **************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../hls_Multiplication/MultipTester.cpp in debug mode
   Compiling ../../../../hls_Multiplication/Multiplication.cpp in debug mode
   Generating csim.exe
>> Start test!
------------------------
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
------------------------
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
------------------------
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
------------------------
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
```

Synthesis Report

- ## Synthesis Summary Report (csynth.rpt)

  - ### Summary report of your IP

- ## Synthesis Detail Report (TopFunctionName_csynth.rpt)

  - ### Detailed reports of your top function and sub-function

- ## Usually located at VitisHLSProjectName/solution1/syn/report

Bitstream and Hardware Handoff

- Bitstream (.bit)
    - Contains the programming information for FPGA device
    - Usually located at：
        - VivadoProjectName/ VivadoProjectName.runs/impl_1/design_1_wrapper.bit

    > vvd_Multip2Num > vvd_Multip2Num.runs > impl_1
    ▢ design_1_wrapper.bit

- Hardware Handoff (.hwh)
    - Contain block design information and is used by software tools to a targeted application
    - Usually located at：
        - VivadoProjectName/VivadoProjectName.gen/sources_1/bd/design_1/ hw_handoff/design_1.hwh

    > vvd_Multip2Num > vvd_Multip2Num.gen > sources_1 > bd > design_1 > hw_handoff
    ▢ design_1.hwh

Online FPGA Remote Login

- We have set up some PYNQ-Z2/KV260 boards in the lab. You can use them remotely
- Refer to OnlineFPGA使用者手冊_20230620.pdf
- IP：140.112.207.200：1000
- Specify username：boledupynq
- password：boledupynq

Lab1 Submission File

- Folder Hierarchy:
  - StudentID_lab1/
    - Lab1/
      - screenshot of Xilinx tool installation (.jpg, .png)
      - .hwh, .bit (generated from vivado)
      - csynth.rpt, xxx_csynth.rpt, xxx_csim.log (generated from vitis_hls)
      - report.pdf
  - Compress all above files in a single zip file named **StudentID_lab1.zip**
  - Submit to NTHU eeclass
  - **Deadline：9/21 (Thr.) 23:59**
    - 30% off for the late submission penalty

Report

- Brief introduction about the overall system

- What is observed & learned

- Screen dump
  - Performance
  - Utilization
  - Interface
  - Co-simulation transcript/waveform
  - Jupyter Notebook execution results

TA Information

- Yang-Che Chen / 陳揚哲 / bb890825@gmail.com
- TA session: Mon. 16:00 ~ 17:00
- Location: Delta 839