112-1 SoC Design Laboratory
Lab2 submission guide

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Lab2 Contents

- Complete course-lab_2
  - FIR Design based on High-Level-Synthesis
  - Interface with Host by AXI Master, and Stream Interface
  - Deploy on PNYQ-Z2 / KV260
    - OnlineFPGA manual
- Report
- course-lab_2 github

Co-Simulation Log

- Co-simulation log (TopFunctionName_csim.log)
  - Transcript of your testbench
- Usually located at VitisHLSProjectName/solution1/csim/report

```
INFO: [SIM 2] ************** CSIM start **************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../hls_Multiplication/MultipTester.cpp in debug mode
   Compiling ../../../../hls_Multiplication/Multiplication.cpp in debug mode
   Generating csim.exe
>> Start test!
------------------------
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
------------------------
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
------------------------
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
------------------------
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
```

Synthesis Report

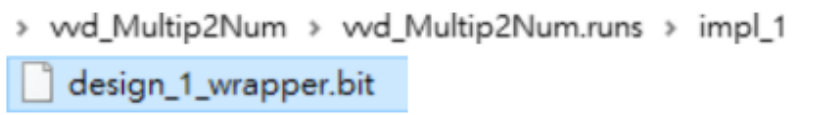
- Synthesis Summary Report (csynth.rpt)
  - Summary report of your IP
- Synthesis Detail Report (TopFunctionName_csynth.rpt)
  - Detailed reports of your top function and sub-function
- Usually located at VitisHLSProjectName/solution1/syn/report

```
================================================================
== Vitis HLS Report for 'multip_2num'
================================================================
* Date:           Wed Jun 28 20:35:44 2023

* Version:        2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
* Project:        hls_ip
* Solution:       solution1 (Vivado IP Flow Target)
* Product family: zynq
* Target device:  xc7z020-clg400-1


================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  6.912 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+-----------+-----------+-----+-----+---------+
    |  Latency (cycles) |   Latency (absolute)  |  Interval | Pipeline|
    |   min   |   max   |    min    |    max    | min | max |   Type  |
    +---------+---------+-----------+-----------+-----+-----+---------+
    |        3|        3|  30.000 ns|  30.000 ns|    4|    4|       no|
    +---------+---------+-----------+-----------+-----+-----+---------+

    + Detail:
        * Instance:
        N/A

        * Loop:
        N/A


================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-------+--------+-------+-----+
|       Name      | BRAM_18K| DSP   |   FF   |  LUT  | URAM|
```

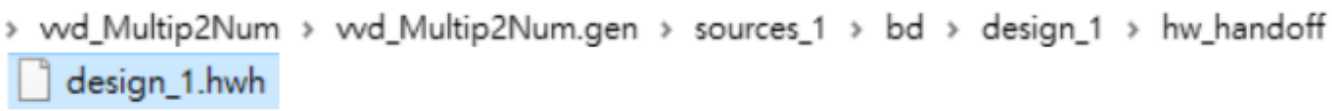
```
================================================================
== Synthesis Summary Report of 'multip_2num'
================================================================
+ General Information:
    * Date:           Wed Jun 28 20:35:44 2023
    * Version:        2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
    * Project:        hls_ip
    * Solution:       solution1 (Vivado IP Flow Target)
    * Product family: zynq
    * Target device:  xc7z020-clg400-1


+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +---------------+------+------+---------+---------+----------+---------+------+----------+-------+-------+---------+-----------+-----+
    |    Modules    | Issue|      | Latency | Latency | Iteration|         | Trip |          |       |       |         |           |     |
    |    & Loops    | Type | Slack| (cycles)|  (ns)   |  Latency | Interval| Count| Pipelined| BRAM  |  DSP  |    FF   |    LUT    | URAM|
    +---------------+------+------+---------+---------+----------+---------+------+----------+-------+-------+---------+-----------+-----+
    |+ multip_2num  |     -|  0.39|        3|  30.000 |         -|        4|     -|        no|     -|  3 (1%)|  409 (~0%)|  307 (~0%)|    -|
    +---------------+------+------+---------+---------+----------+---------+------+----------+-------+-------+---------+-----------+-----+


================================================================
== HW Interfaces
================================================================
* S_AXILITE Interfaces
+---------------+------------+---------------+--------+----------+
| Interface     | Data Width | Address Width | Offset | Register |
+---------------+------------+---------------+--------+----------+
| s_axi_control | 32         | 6             | 16     | 0        |
+---------------+------------+---------------+--------+----------+

* S_AXILITE Registers
+---------------+----------------+--------+-------+--------+-----------------------------------+-----------------------------+
| Interface     | Register       | Offset | Width | Access | Description                       | Bit Fields                  |
+---------------+----------------+--------+-------+--------+-----------------------------------+-----------------------------+
| s_axi_control | n32In1         | 0x10   | 32    | W      | Data signal of n32In1             |                             |
| s_axi_control | n32In2         | 0x18   | 32    | W      | Data signal of n32In2             |                             |
| s_axi_control | pn32ResOut     | 0x20   | 32    | R      | Data signal of pn32ResOut         |                             |
| s_axi_control | pn32ResOut_ctrl| 0x24   | 32    | R      | Control signal of pn32ResOut      | 0=pn32ResOut_ap_vld         |
+---------------+----------------+--------+-------+--------+-----------------------------------+-----------------------------+

* TOP LEVEL CONTROL
+-----------+--------------+---------+
| Interface | Type         | Ports   |
+-----------+--------------+---------+
```

Bitstream and Hardware Handoff

- Bitstream (.bit)
  - Contains the programming information for FPGA device
  - Usually located at：
    - VivadoProjectName/ VivadoProjectName.runs/impl_1/design_1_wrapper.bit



- Hardware Handoff (.hwh)
  - Contain block design information and is used by software tools to a targeted application
  - Usually located at：
    - VivadoProjectName/VivadoProjectName.gen/sources_1/bd/design_1/hw_handoff/design_1.hwh



Online FPGA Remote Login

- We have set up some PYNQ-Z2/KV260 boards in the lab. You can use them remotely
- Refer to OnlineFPGA使用者手冊_20230620.pdf
- IP：140.112.207.200：1000
- Specify username：boledupynq
- password：boledupynq

Lab2 Submission File

- Folder Hierarchy:
  - StudentID_lab2/
    - Lab2/
      - FIRN11MAXI/
        - .hwh, .bit (generated from vivado)
        - csynth.rpt, xxx_csynth.rpt, xxx_csim.log (generated from vitis_hls)
      - FIRN11Stream/
        - .hwh, .bit (generated from vivado)
        - csynth.rpt, xxx_csynth.rpt, xxx_csim.log (generated from vitis_hls)
      - report.pdf
  - Compress all above files in a single zip file named **StudentID_lab2.zip**
  - Submit to NTHU eeclass
  - **Deadline：9/28 (Thr.) 23:59**
    - 30% off for the late submission penalty

TA Information

- Yang-Che Chen / 陳揚哲/ bb890825@gmail.com
- TA session: Mon. 16:00 ~ 17:00
- Location: Delta 839